DDR5 SDRAM SODIMM Addendum

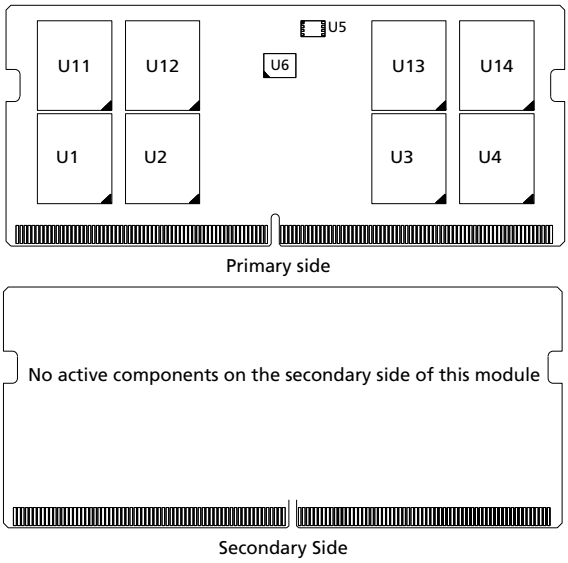
MTC8C1084S1SC – 16GB
16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 SODIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 SODIMM core data sheet
- 262-pin, DDR5 small outline dual in-line memory module (DDR5 SODIMM)
- Fast data transfer rate: PC5-4800
- 16GB (2Gig x 64)
- Single-rank
- 32 internal banks; 8 groups of 4 banks each

Figure 1: 262-Pin DDR5 SODIMM (R/C-D0)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	C
• Frequency/CAS latency	
– 0.416ns @ CL = 40 (DDR5-4800)	48B

Table 1: Addressing

Parameter	16GB
Row address[1]	64K (R0-R15)
Column address[1]	1K (C0-C9)
Device bank group address[1]	8 (BG0-BG2)
Device bank address per bank group[1]	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT60B2G8,[1] 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL\text{-}_nRCD\text{-}_nRP$)
MTC8C1084S1SC48BA1	16GB	2Gb x 64	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. The data sheet for the base device can be found on micron.com.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	0A	11	U2	0	16A	53
	1	1A	12		1	17A	54
	2	2A	15		2	18A	57
	3	3A	16		3	19A	58
	4	6A	27		4	22A	69
	5	5A	26		5	21A	68
	6	4A	23		6	20A	65
	7	7A	30		7	23A	72
U3	0	0B	179	U4	0	16B	221
	1	1B	180		1	17B	222
	2	2B	183		2	18B	225
	3	3B	184		3	19B	226
	4	6B	195		4	22B	237
	5	5B	194		5	21B	236
	6	4B	191		6	20B	233
	7	7B	198		7	23B	240
U11	0	9A	34	U12	0	25A	76
	1	8A	31		1	24A	73
	2	11A	38		2	27A	80
	3	10A	35		3	26A	77
	4	15A	50		4	31A	92
	5	12A	45		5	28A	87
	6	13A	46		6	29A	88
	7	14A	49		7	30A	91
U13	0	9B	202	U14	0	25B	244
	1	8B	199		1	24B	241
	2	11B	206		2	27B	248
	3	10B	203		3	26B	245
	4	15B	218		4	29B	256
	5	12B	213		5	28B	255
	6	13B	214		6	31B	260
	7	14B	217		7	30B	259

I_{DD} Specifications

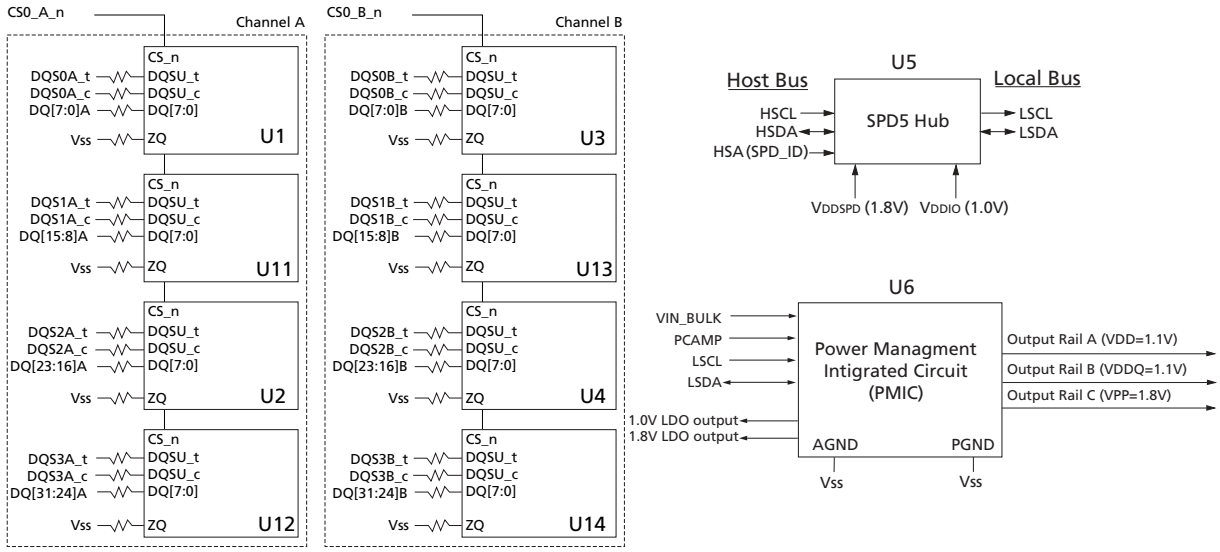
Table 4: DDR5 I_{DD} Specifications and Conditions – 16GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 5V input current and typical operating temperature. Each I_{DD} parameter includes PMIC efficiency and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}	127	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}	200	mA
Precharge standby current	I_{DD2N}	98	mA
Precharge standby non-target command	I_{DD2NT}	189	mA
Precharge power-down current	I_{DD2P}	86	mA
Active standby current	I_{DD3N}	116	mA
Active power-down current	I_{DD3P}	104	mA
Operating burst read current	I_{DD4R}	605	mA
Operating burst write current	I_{DD4W}	844	mA
Operating burst write with write CRC current	I_{DD4WC}	763	mA
Burst refresh (normal refresh mode) current	I_{DD5B}	445	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}	270	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}	185	mA
Self refresh current	I_{DD6N}	59	mA
Operating bank interleave read current	I_{DD7}	684	mA
Maximum power saving deep power down mode current	I_{DD8}	41	mA

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

Revision History

Rev. C – 08/2021

- Production Release

Rev. B – 02/2021

- Preliminary Release

Rev. A – 01/2021

- Preliminary Release

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