16nm 64Gb e-NAND Product Family

Revision History

Revision NO.	History	Draft Date	Remark
0.0	Preliminary	03, Sep, 2013	
0.1	Updated Bus timing in HS400 mode	24, Oct, 2014	
0.2	Updated Register value	12, Nov, 2014	
0.3	Updated eMMC5.0 Connection guide [P61_Connection guide]	10, Dec, 2014	
0.4	Updated tPre/tPost-Amble [p35_HS 400 Device out put timing]	12, Dec, 2014	
0.5	Revised HPI Time out -. Updated time out value [p28_Timings] -. Updated register value [54_Extended CSD_198]	20, Dec, 2014	

Table of Contents

1. Device summary

Density	NAND	Root Part Number	Package	PKG size (mm)
8GB	16nm 64Gb	H26M41103HPR	FBGA153	11.5x13x0.8
16GB	16nm 64Gb	H26M52103FMR	FBGA153	11.5x13x1.0
32GB	16nm 64Gb	H26M64103EMR	FBGA153	11.5x13x1.0
64GB	16nm 64Gb	H26M78103CCR	FBGA153	11.5x13x1.2

2. Features

- Packaged NAND flash memory with MultiMediaCard interface
- High capacity memory access
- e-NAND system specification, compliant with V5.0
- Full backward compatibility with previous e-NAND system specification (MMC 4.5)
- Bus mode
  - High-speed eMMC protocol.
  - Three different data bus widths: 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 400Mbyte/s (HS400)
  - DDR mode supported (Up to 400MB/s, 200MHz, DDR Mode)
- Operating voltage range
  VCC(NAND) : 2.7 - 3.6V
  VCCQ(Controller) : 1.7 - 1.95V / 2.7 - 3.6V
- Error free memory access
  - Error correction code (ECC)
  - Internal enhanced data management algorithm (Wear levelling, Bad block management, Garbage collection)
  - Possibility for the host to make sudden power failure safe-update operations for data content
- Hardware & Software reset supported
- Security
  - Secure Erase
  - Secure Trim
  - Write Protection
  - Sanitize
  - eDrive
  - RPMB
- Boot
  - Normal / Alternative boot sequence method
- Power saving
  - Enhanced power saving method by introducing sleep functionality
- Partition management with enhanced storage.
- Performance
  - HS400
  - Power off Notification
  - Context ID
  - Packed CMD
  - Discard
  - Cache
  - Data tag
- Maintenance
  - Health Report
  - Field Firmware Update
  - Product State Awareness
  - Power Off Notification Sleep Clarification
  - HPI
- Temperature
  Operation (-25℃ ~ +85℃), Storage without operation (-40℃ ~ 85℃)

*** This Product in compliance with the RoHS directive.**

3. Description

e-NAND is an embedded flash memory storage solution. e-NAND was developed for universal low cost data storage and communication media. e-NAND is fully compatible with MMC bus and host.

e-NAND communications are made through an advanced 13-pin bus, and it can be either 1-bit, 4-bit, or 8-bit in width. e-NAND operates in high-speed mode at clock frequencies equal or higher than 20MHz as defined in the MMC JEDEC standard. The communication protocol is defined in this MMC JEDEC standard.

e-NAND is designed to cover a wide area of applications such as smart phones, tablet PC, cameras, PDA, digital recorders, MP3 players, electronic toys, etc. Features are mainly high speed performance, low power consumption, low cost and high density.

To meet the requirements of embedded high density storage media and mobile applications, e-NAND supports 3.3V for VCC, and 3.3V or 1.8V for VCCQ. The address argument for e-NAND is consistent with 512-byte sector addressing rather than byte addressing. This means that e-NAND is not capable of supporting backward compatibility with devices using byte addressing(typically devices that have maximum capacity less that 2 Gigabytes). If the e-NAND receives byte addressing, then the e-NAND will change its state to inactive.

e-NAND has the built-in intelligent controller which manages interface protocols, Wear Leveling, Bad Block Management, Garbage Collection, and ECC. e-NAND protects the data contents from the host sudden power off failure by safe-update operations with reliable write features. The device supports a boot operation with enhance area and sleep/awake commands.
In particular, the host power regulator for VCC can minimize the power consumption during the sleep state.

3.1 e-NAND standard specification

e-NAND device is fully compatible with the JEDEC Standard Specification No. JESD84-B50. This data sheet describes the key and specific features of e-NAND. Any additional interface related information, the device to a host system, and all other practical methods for card detection/access can be found in the proper section of the JEDEC Standard Specification.

4. Device Physical Description

4.1 Package Connections

Figure 1: FBGA153 Package Connections (Top view through package)

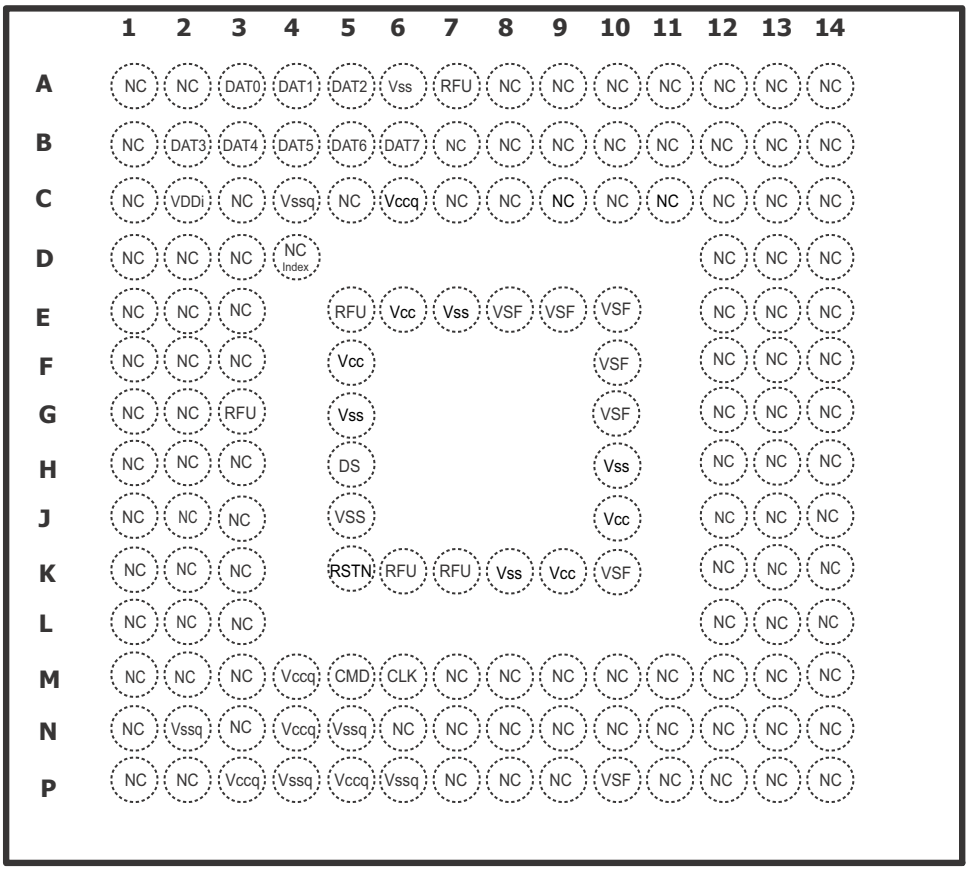


Table 1 : FBGA153 Ball Description

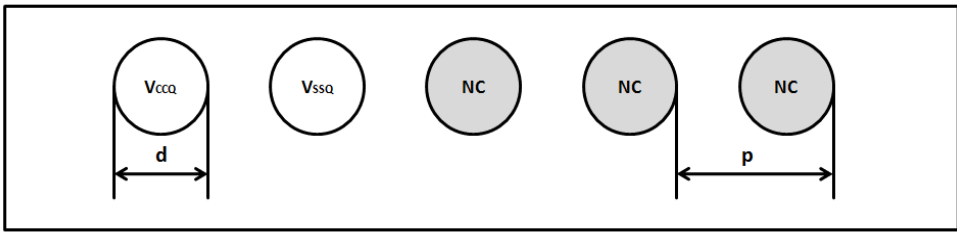
Ball NO	Symbol	Type	Ball Function
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
M5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open-Drain for initialization. 2) Push-Pull for fast command transfer.
A3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
A4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
A5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
B2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
B3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
B4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
B5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
B6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
K5	RST_n	Input	Reset signal pin
E6,F5,J10,K9	VCC	Supply	VCC: Flash memory I/F and Flash memory power supply.
C6, M4, N4, P3, P5	VCCQ	Supply	VCCQ: Memory controller core and MMC interface I/O power supply.
A6, E7, G5, H10, J5, K8	Vss	Supply	Vss: Flash memory I/F and Flash memory ground connection.
C4, N2, N5, P4, P6	Vssq	Supply	Vssq: Memory controller core and MMC I/F ground connection
C2	VDDi		VDDi: Connect 0.1uF capacitor from VDDi to ground.
H5	DS	Out put	DS : Data Strobe
E8, E9, E10, F10, G10, K10	VSF	Supply	**VSF : Vendor specific Function** SK hynix use E8, E9 Pin as VSF Pin
RFU	Reserved for future use		

4.2 Form Factor

The ball diameter, d, and the ball pitch, p, for the FBGA153 package are

- d = 0.30mm (solder ball diameter)
- p = 0.5mm (ball pitch)

Figure 2: e-NAND ball diameter and pitch



4.3 PKG mechanical drawing

4.3.1 11.5mm x13.0mm x0.8mm Package Dimension

Figure 3: 11.5x13.0x0.8 Top & Side View

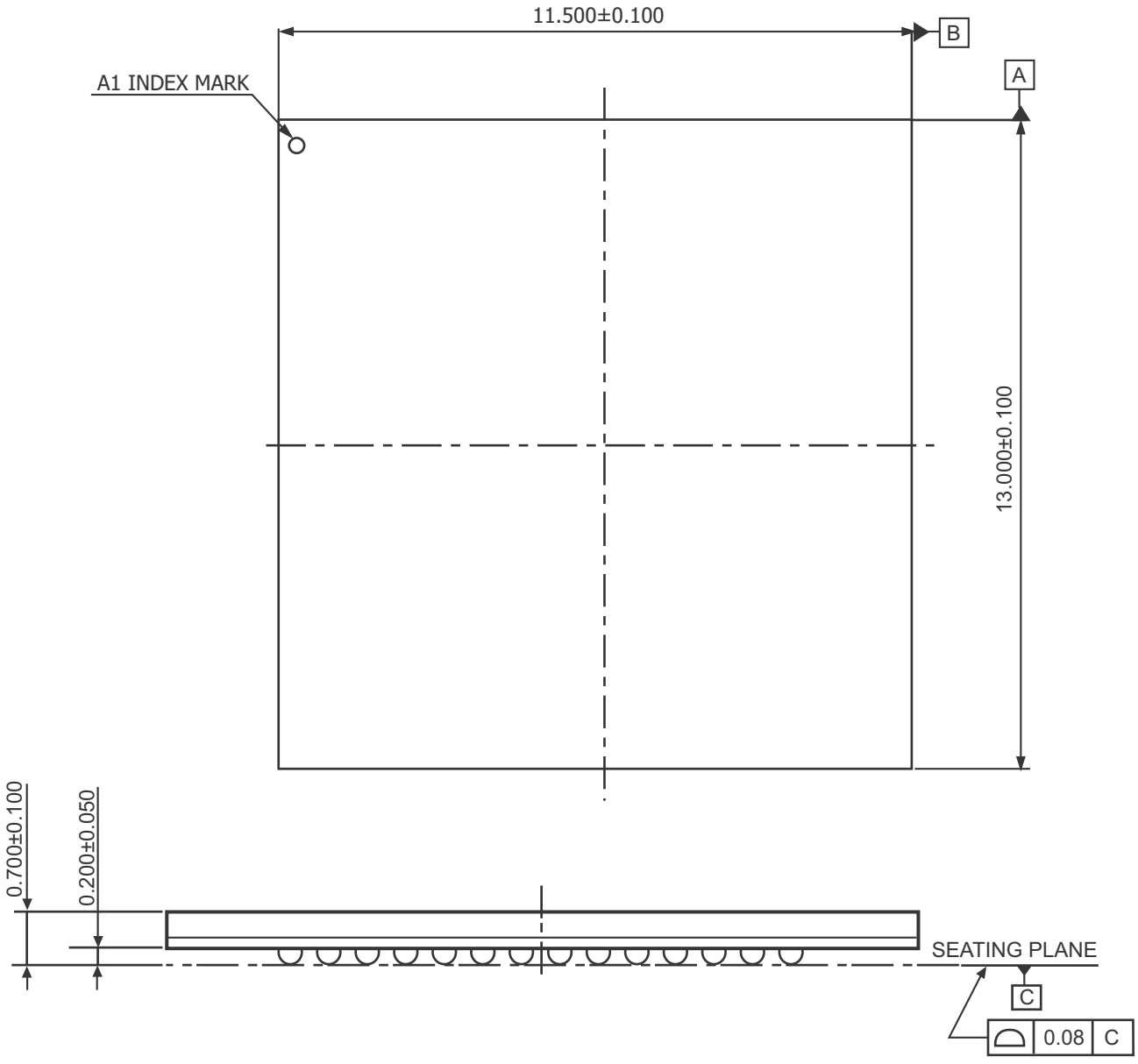
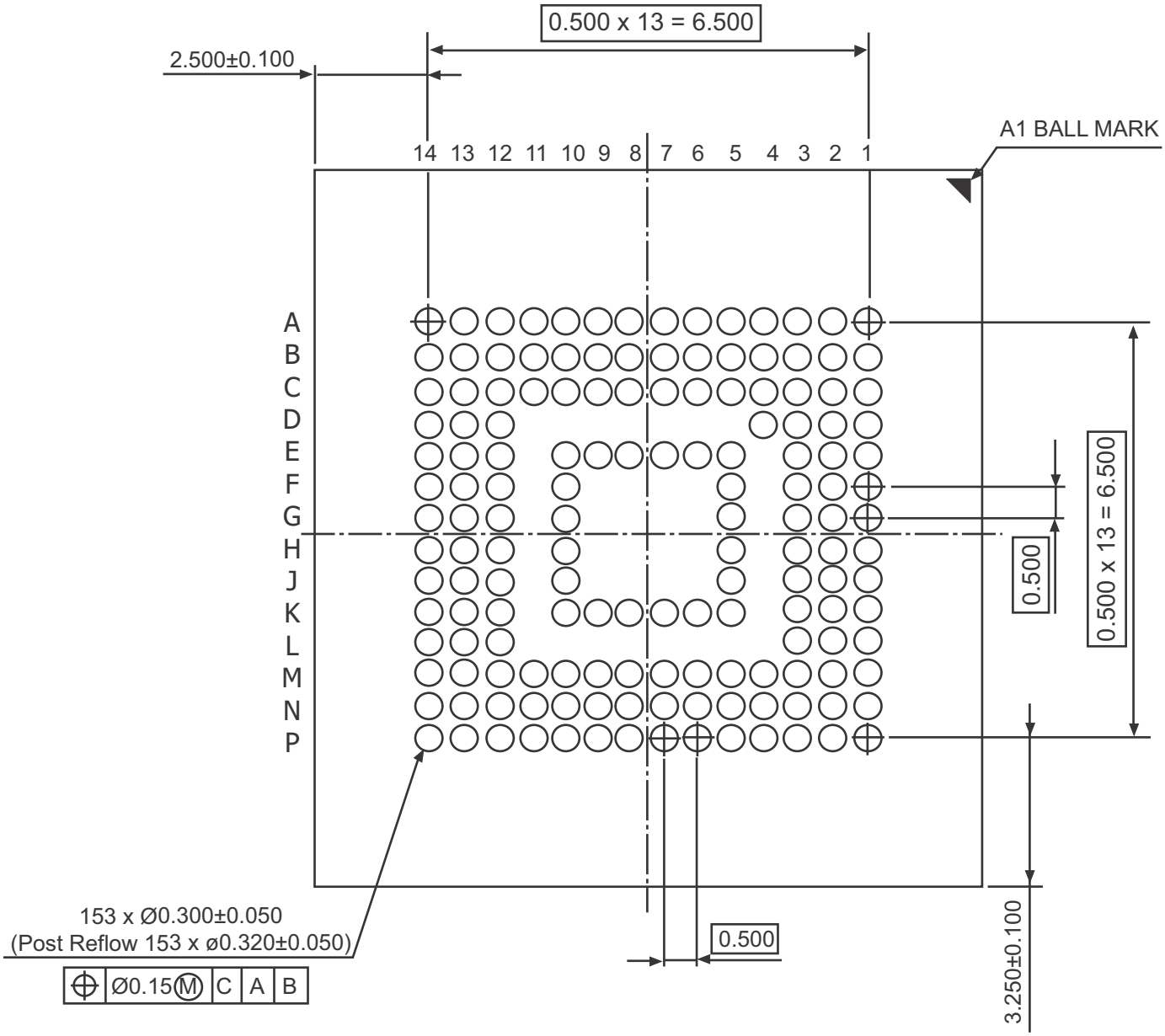


Figure 4: 11.5x13.0x0.8 Bottom View



4.3.2 11.5mm x13.0mm x1.0mm Package Dimension

Figure 5: 11.5x13.0x1.0 Top & Side View

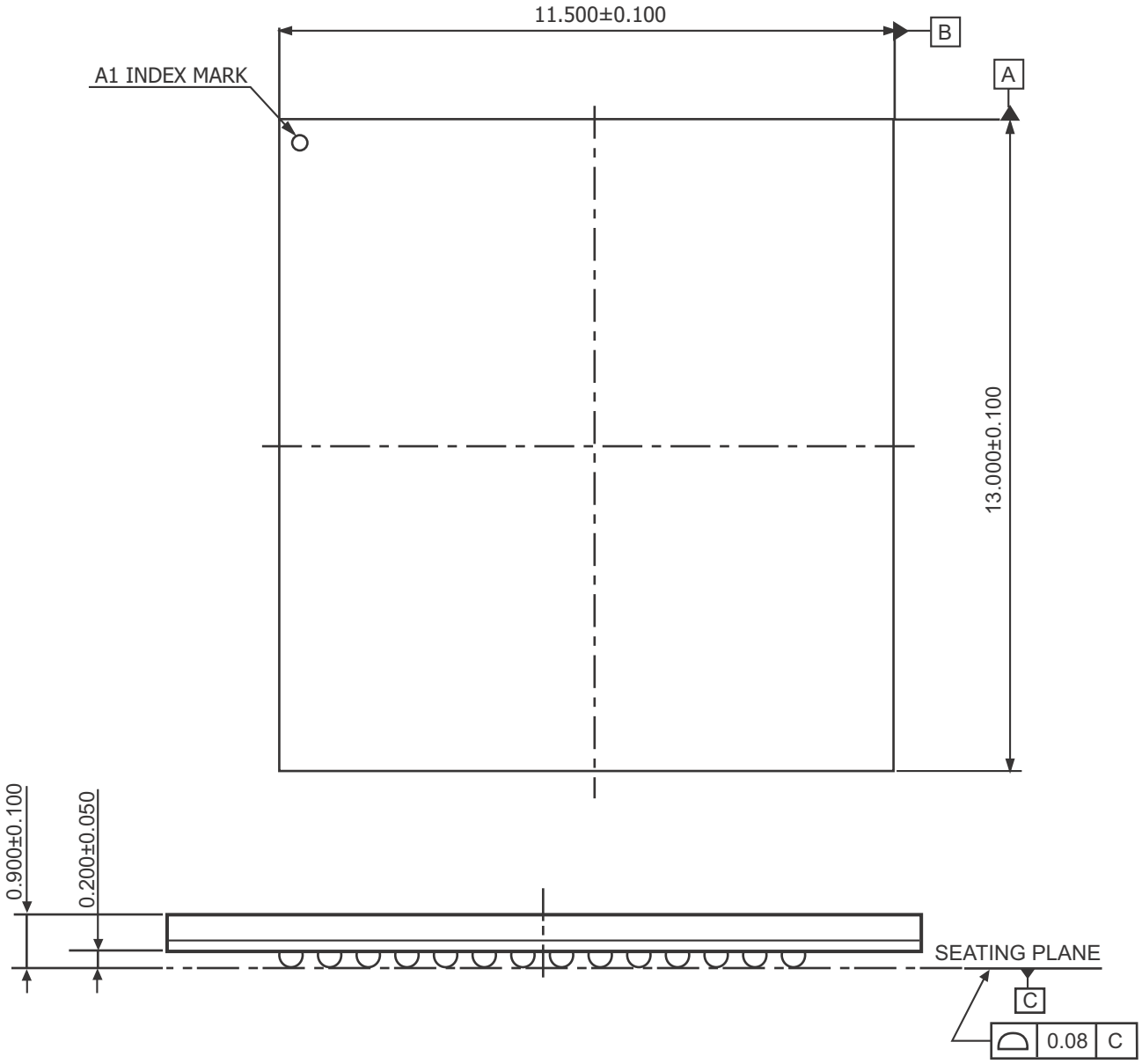
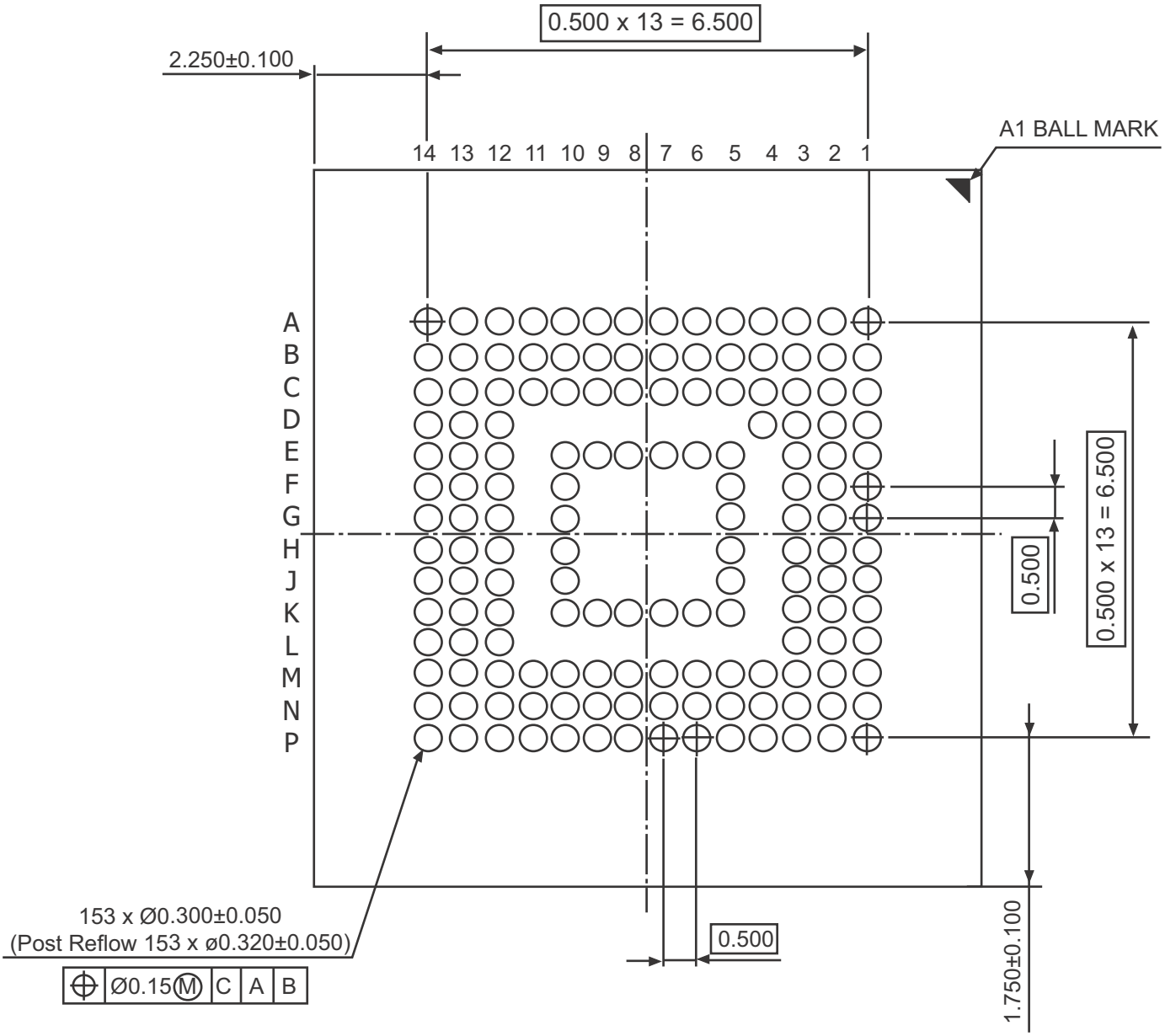


Figure 6: 11.5x13.0x1.0 Bottom View



4.3.3 11.5mm x13.0mm x1.2mm Package Dimension

Figure 7: 11.5x13.0x1.2 Top & Side View

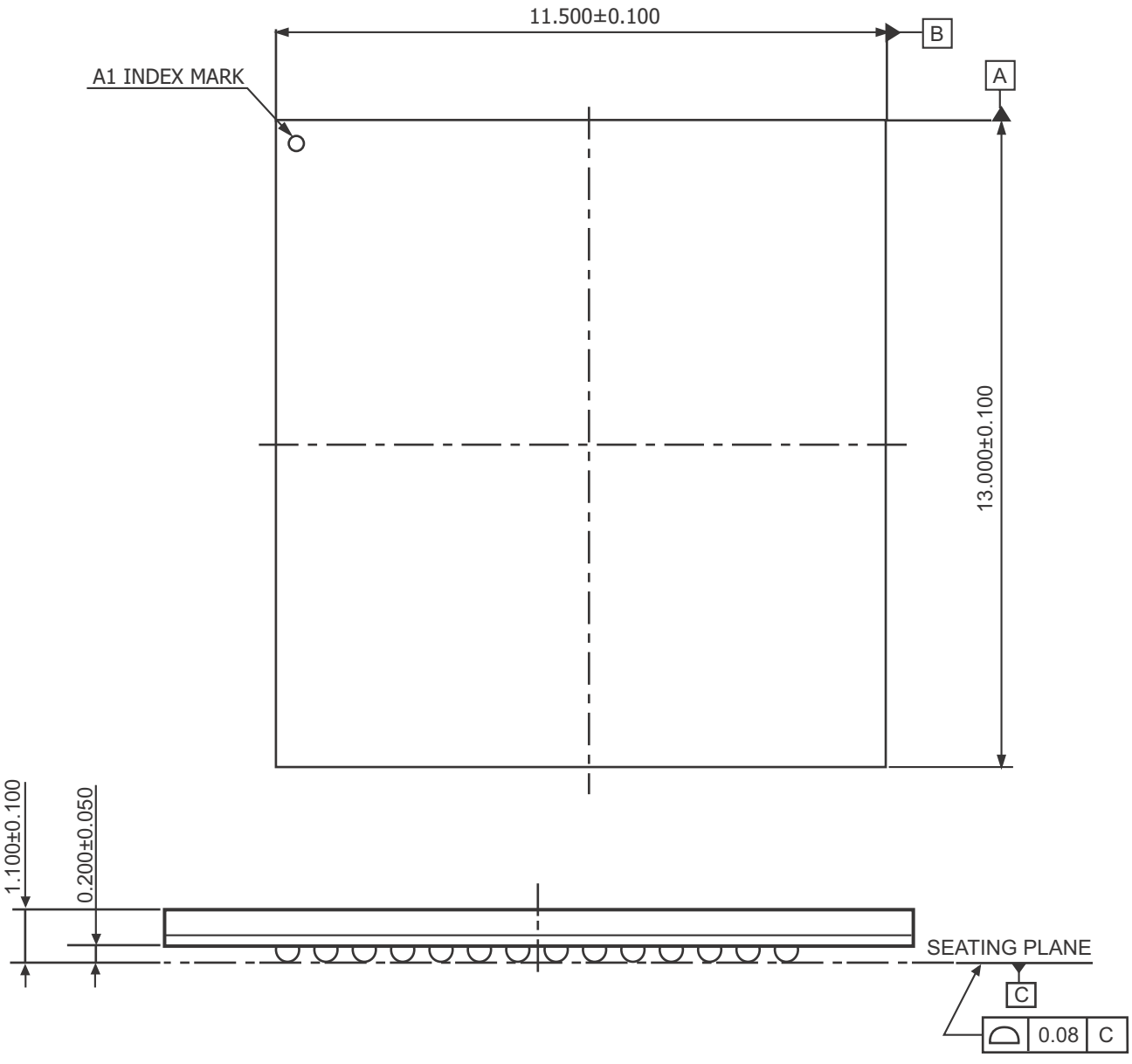
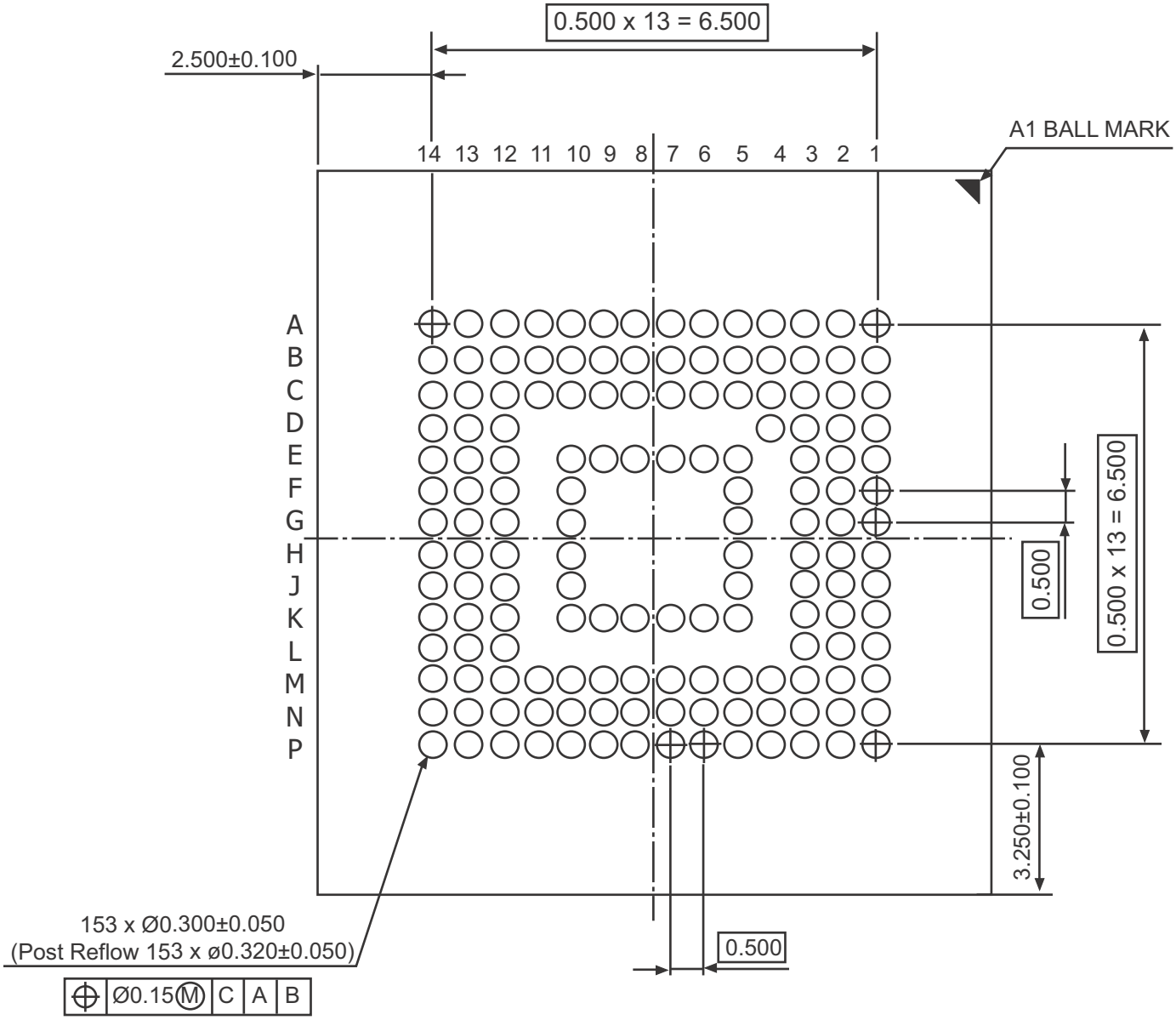


Figure 8: 11.5x13.0x1.2 Bottom View



5. e-NAND Features

5.1 Bus Modes

• **Boot mode**

e-NAND will be in boot mode after power cycle, reception of CMD0 with argument of 0xF0F0F0F0 or assertion of hardware reset signal.

• **Identification Mode**

e-NAND will be in identification mode when boot operation mode is finished or if host does not support a boot operation mode. e-NAND will be in this mode until the SET_RELATIVE_ADDR command (CMD3) is received.

• **Interrupt Mode**

e-NAND support Interrupt Mode. Host and device enter and exit interrupt mode simultaneously. In interrupt mode there is no data transfer. The only message allowed is an interrupt service request from the device or the host.

• **Data Transfer Mode**

e-NAND will enter Data Transfer Mode once RCA is assigned to it. The host will enter Data Transfer Mode after identifying e-NAND on the bus.

• **Inactive Mode**

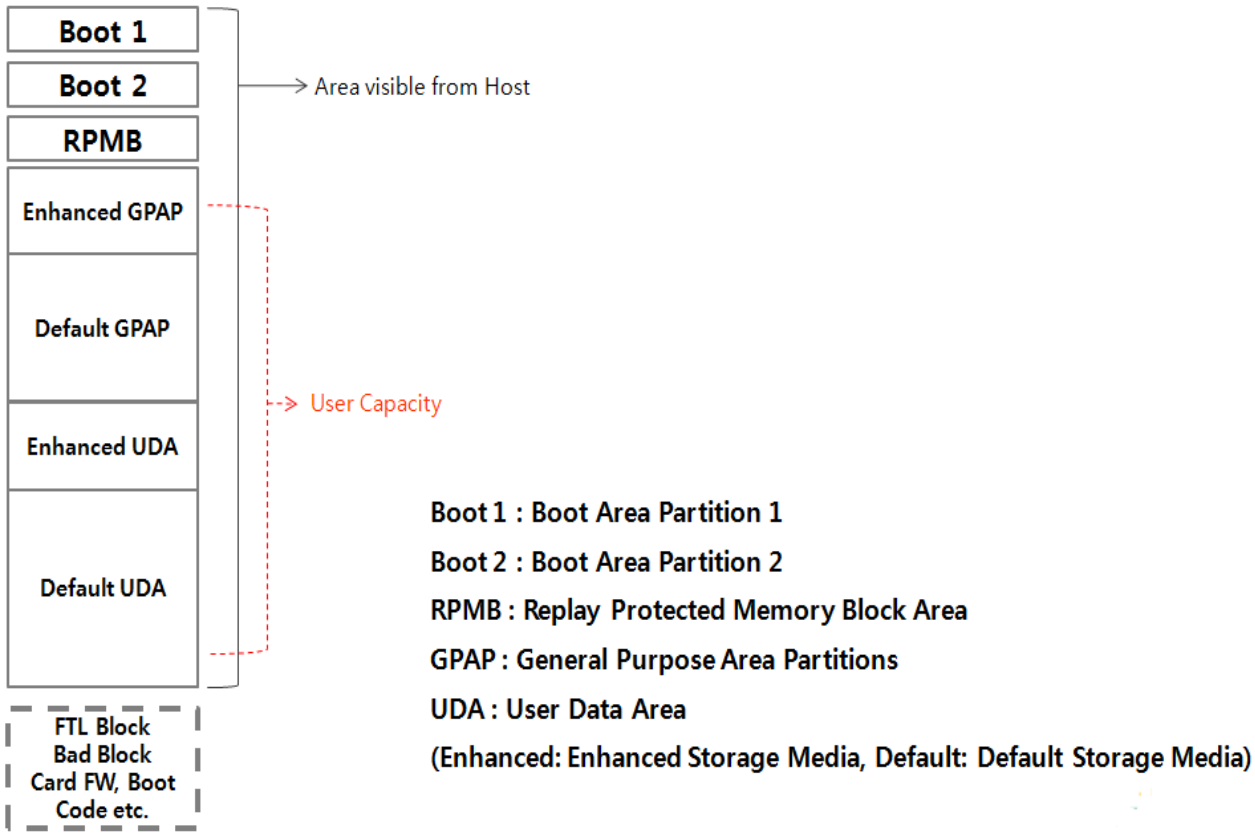
e-NAND will enter to inactive mode when e-NAND is operating invalid voltage range or access mode. Also e-NAND can be set to inactive mode by Go_INACTIVE_STATE command (CMD15). e-NAND can change from inactive mode to Pre-idle state by reset.

Table 2: Bus modes overview

e-NAND state	Operation mode	Bus mode
Inactive state	Inactive Mode	Open-Drain
Pre-Idle state	Boot Mode	
Pre-Boot state		
Idle state	Identification Mode	
Ready state		
Identification state		
Stand-by state	Data Transfer Mode	Push-Pull
Sleep state		
Transfer state		
Bus-Test state		
Sending-data state		
Receive-data state		
Programming state		
Disconnect state		
Boot state	Boot Mode	
Wait-IRQ State	Interrupt mode	Open-drain

5.2 User Density

Figure 9: Partition diagram



■ **Partition size (Boot , RPMB)**

Denisty	Boot Partition 1,2	RPMB		
		size	Performance	
8GB	4096KB	4096KB	Sequential. Read : 20MB/s Sequential. Write : 5MB/s	Data transfer unit : 8KB
16GB				
32 GB				
64 GB				

Note : RPMB is implemented oprating with sector unit. About RPMB data transfer unit, refer to the EXT_CSD REL_WR_SEC_C [222] value.
It is highly recommended to use 8KB data transfer unit to maximize access perfomance to RPMB area.

■ User Density Size

Capacity	LBA(Hex)	LBA(Dec)	Capacity(Bytes)
8GB	0xE90000	15,269,888	7,818,182,656
16GB	0x1D5C000	30,785,536	15,762,194,432
32 GB	0x3A40000	61,079,552	31,272,730,624
64 GB	0x7480000	122,159,104	62,545,461,248

Note : 1 sector = 512 bytes.
The total usable capacity of the e-NAND may be less than total physical capacity becuase a small portion of the capacity is used for NAND flash management and maintenance purpose.

■ Maximum Enhanced Partition Size

Enhanced User Data Area can be configured to store read-centric data such as sensitive data or for other host usage models.
SK hynix e-NAND support Enhanced User Data Area as SLC Mode. When customer adopts some portion as enhance user data area in User Data Area, that area occupies double the size of the orginal set-up size. Enhanced User Data Area of e-NAND guarantees 20K program and erase cycles

Capacity	Max ENH_SIZE_MULTI	HC_ERASE_GRP_SIZE	HC_WP_GRP_SIZE
8GB	1D2h	1h	10h
16GB	3ABh	1h	10h
32 GB	748h	1h	10h
64 GB	748h	1h	20h

Note : 1 sector = 512 bytes.
Max Enhanced Partition Size is defined as **MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512Byte.**
(refer to Table 32. Extended CSD)

Capacity	LBA(Hex)	LBA(Dec)	Capacity(Bytes)
8GB	1D2h	7,456	3,817,472
16GB	3AB0h	15,024	7,692,288
32 GB	7480h	29,824	15,269,888
64 GB	E900h	59,648	30,539,776

5.3 Write Endurance

This section provide "TBW(Total Bytes Written) refer to how much total data can be written to an e-NAND for a given workload before the device reaches its endurance limits."
The data is based on the SK hynix's data pattern, which is designed to be a good indication of endurance for mainstream application users.

Table 3: Write Endurance.

Density	TBW
8GB	TBD
16GB	6.2TB
32GB	22TB
64GB	TBD

5.4 Boot Operation

e-NAND supports Boot Mode and Alternative Boot Mode. e-NAND also, supports high speed timing and dual data rate during boot.

Figure 10: e-NAND state diagram (Boot Mode)

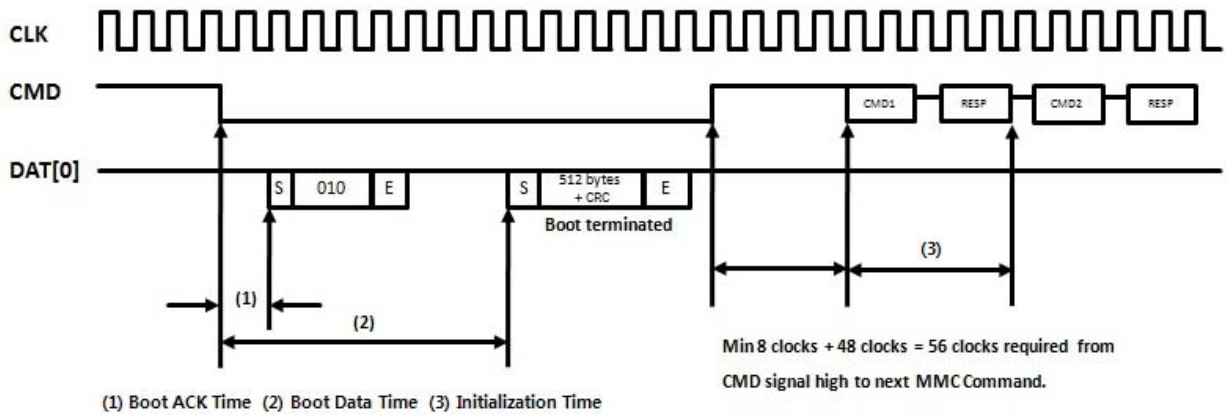
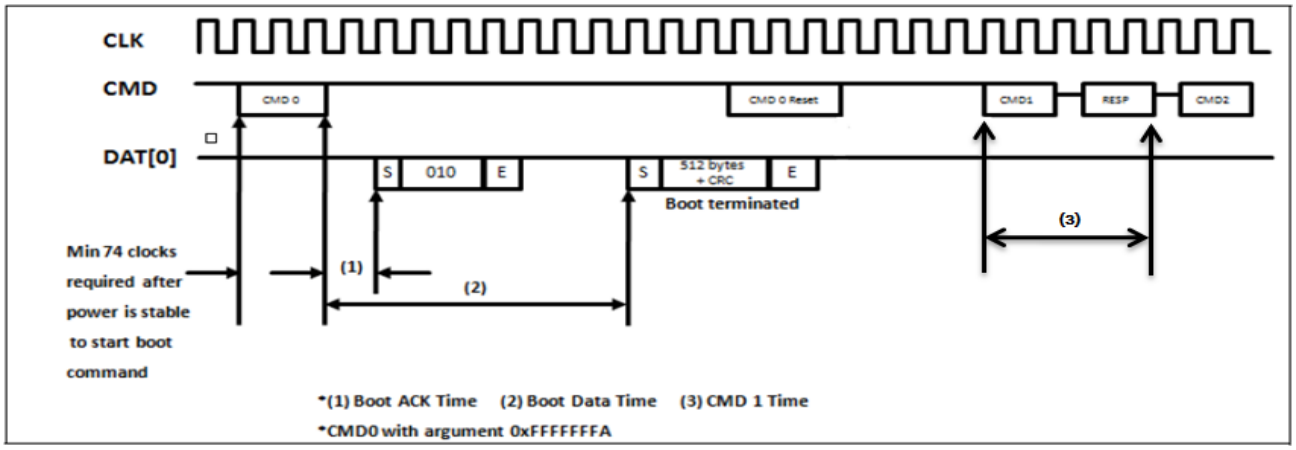


Figure 11: e-NAND state diagram (Alternative Boot Mode)



Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 1 sec
(3) Initialization Time	< 1 sec

1) Initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 7.4 Extended CSD Register.
Initailization time is completed within 1sec from issuning CMD1 until receving Respons.
2) The device has to send the acknowledge pattern "010" to the master within 50ms after the CMD0 with the argument of 0xFFFFFFFA is received.
3) Boot ACK Time can be over 50ms in worst case.

5.5 Power Modes

5.5.1 e-NAND power-up guidelines

e-NAND power-up must adhere to the following guidelines:

• When power-up is initiated, either VCC or VCCQ can be ramped up first, or both can be ramped up simultaneously.

• After power up, e-NAND enters the pre-idle state. The power up time of each supply voltage should be less than the specified tPRU (tPRUH, tPRUL or tPRUV) for the appropriate voltage range.

• If e-NAND does not support boot mode or its BOOT_PARTITION_ENABLE bit is cleared, e-NAND moves immediately to the idle state. While in the idle state, e-NAND ignores all bus transactions until receiving CMD1.
e-NAND begins boot operation with the argument of 0xFFFFFFFA. If a boot acknowledge is finished, e-NAND shall send acknowledge pattern "010" to the host within the specified time. After boot operation is terminated, e-NAND enters the idle state and shall be ready for CMD1 operation. If e-NAND receives CMD1 in the pre-boot state, it begins to respond to the command and moves to the card identification mode.

• When e-NAND is initiated by alternative boot command(CMD0 with arg=0xFFFFFFFA), all the data will be read from the boot partition and then e-NAND automatically goes to idle state. But hosts are still required to issue CMD0 with arg=0x0000000000 in order to complete a boot mode properly and move to the idle state. While in the idle state, e-NAND ignores all bus transactions until it receives CMD1.

• CMD1 is a special synchronization command which is used to negotiate the operating voltage range and poll the device until it is out of its power-up sequence. In addition to the operating voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready, and the host must wait until this bit is cleared. The device must complete its initialization within 1 second of the first CMD1 issued with a valid OCR range.

• If the e-NAND device was successfully partitioned during the previous power up session (bit 0 of EXT_CSD byte [155] PARTITION_SETTING_COMPLETE successfully set) then the initialization delay is (instead of 1s) calculated from INI_TIMEOUT_PA (EXT_CSD byte [241]). This timeout applies only for the very first initialization after successful paritioning. For all the consecutive initialization 1sec time out will be applied.

• The bus master moves the device out of the idle state. Because the power-up time and the supply ramp-up time depend on the application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.

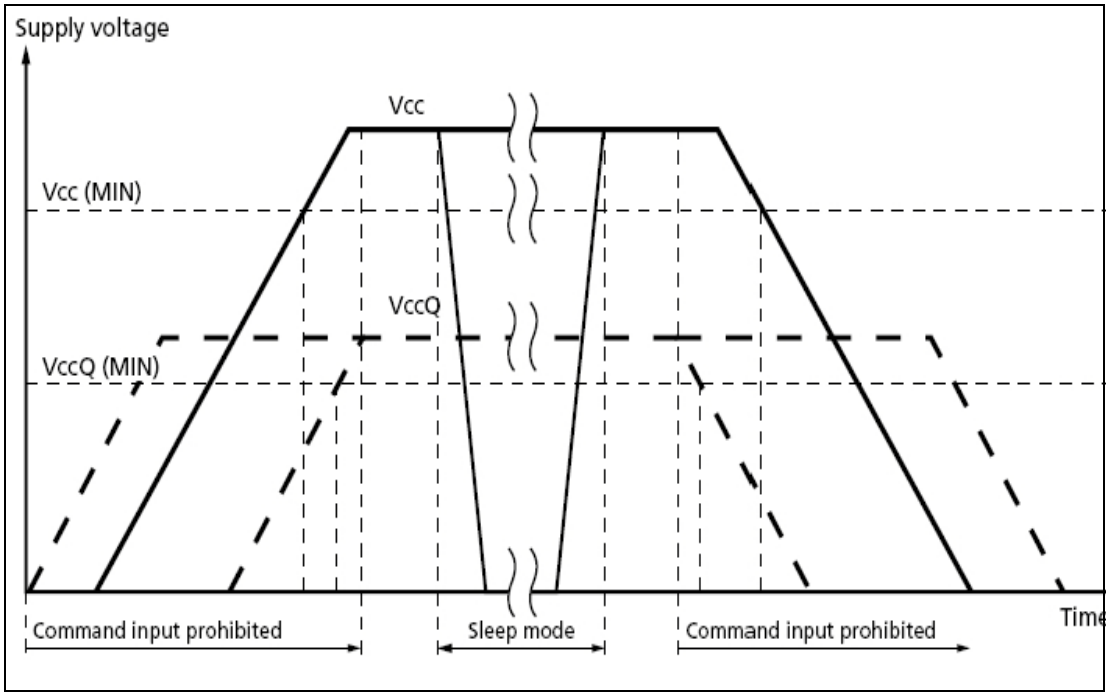
• After power-up, the host starts the clock and sends the initializing sequence on the CMD line. The sequence length is the longest of: 1ms, 74 clocks, the supply ramp-up time, or the boot operation period. An additional 10 clocks (beyond the 64 clocks of the power-up sequence) are provided to eliminate power-up synchronization problems.

• Every bus master must implement CMD1.

5.5.2 e-NAND Power Cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit.

Figure 12: e-NAND power cycle



If VCC or VCCQ are below 0.5 V for longer than 1 ms, the slave shall always return to the pre-idle state, and perform the appropriate boot behavior. The slave will behaves as in a standard power up condition once the voltages have returned to their functional ranges.
An exception to the this behavior is if the device is in sleep state, in which the voltage on VCC is not monitored.

5.5.3 Leakage

Table 4: General operation conditions

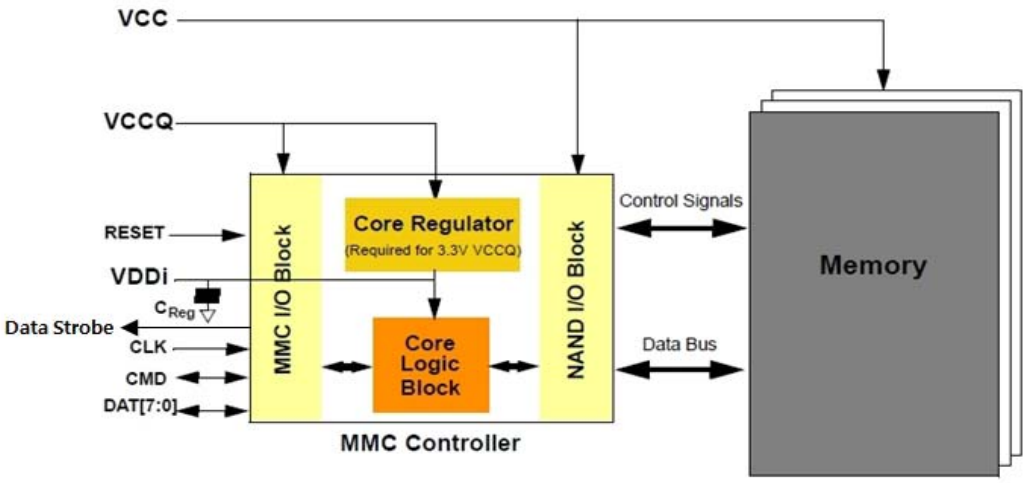
Parameter		Symbol	Min	Max.	Unit	Remark
	BGA		-0.5	VccQ+0.5	V	
All inputs						
Input leakage current (before initialization sequenceand/or the internalpull up resistors connected)			-100	100	μA	
Input leakage current (after initialization sequence and the internal pull up resistors disconnected)			-2	2	μA	
All outputs						
Output leakage current (before initialization sequence)			-100	100	μA	
Output leakage current (after initialization sequence)			-2	2	μA	

• NOTE 1. Initialization sequence is defined in JEDEC Section 10.1 on page 178

5.5.4 Power Supply

In e-NAND, VCC is used for the NAND core voltage and NAND interface; VCCQ is for the controller core and e-NAND interface voltage shown in **Figure 13**. The core regulator is optional and only required when internal core logic voltage is regulated from VCCQ. A Creg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

Figure 13: e-NAND internal power diagram



e-NAND supports one or more combinations of VCC and VCCQ as shown in **Table 5**.
The available voltage configuration is shown in **Table 6**.

Table 5: e-NAND power supply voltage

Parameter	Symbol	Min	Max.	Unit	Remark
Supply voltage (NAND)	VCC	2.7	3.6	V	
		1.7	1.95	V	**Not supported**
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.7	1.95	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 3.3V	tPRUL		25	ms	
Supply power-up for 3.3V	tPRUV		20	ms	

Table 6: e-NAND voltage combinations

		VCCQ	
		1.7V ~ 1.95V	**2.7V ~ 3.6V**
VCC	**2.7V–3.6V**	Valid	Valid
	1.7V–1.95V	NOT VALID	NOT VALID

5.5.5 Active Power Consumption during operation

Density	Max RMS current	
	Icc	**Iccq**
32GB(QDP)	TBD	180mA (HS200 Mode) 200mA (HS400 Mode)

Table 7: e-NAND Active Power Consumption during operation

Note 1 : Room temperature_25℃
Note 2 : RMS current consumption is over a period of 20ms

5.5.6 Low Power Mode

• Standby Power Mode

Density	NAND		CTRL	
	25℃	85℃	25℃	85℃
32GB(QDP)	TBD	TBD	TBD	TBD

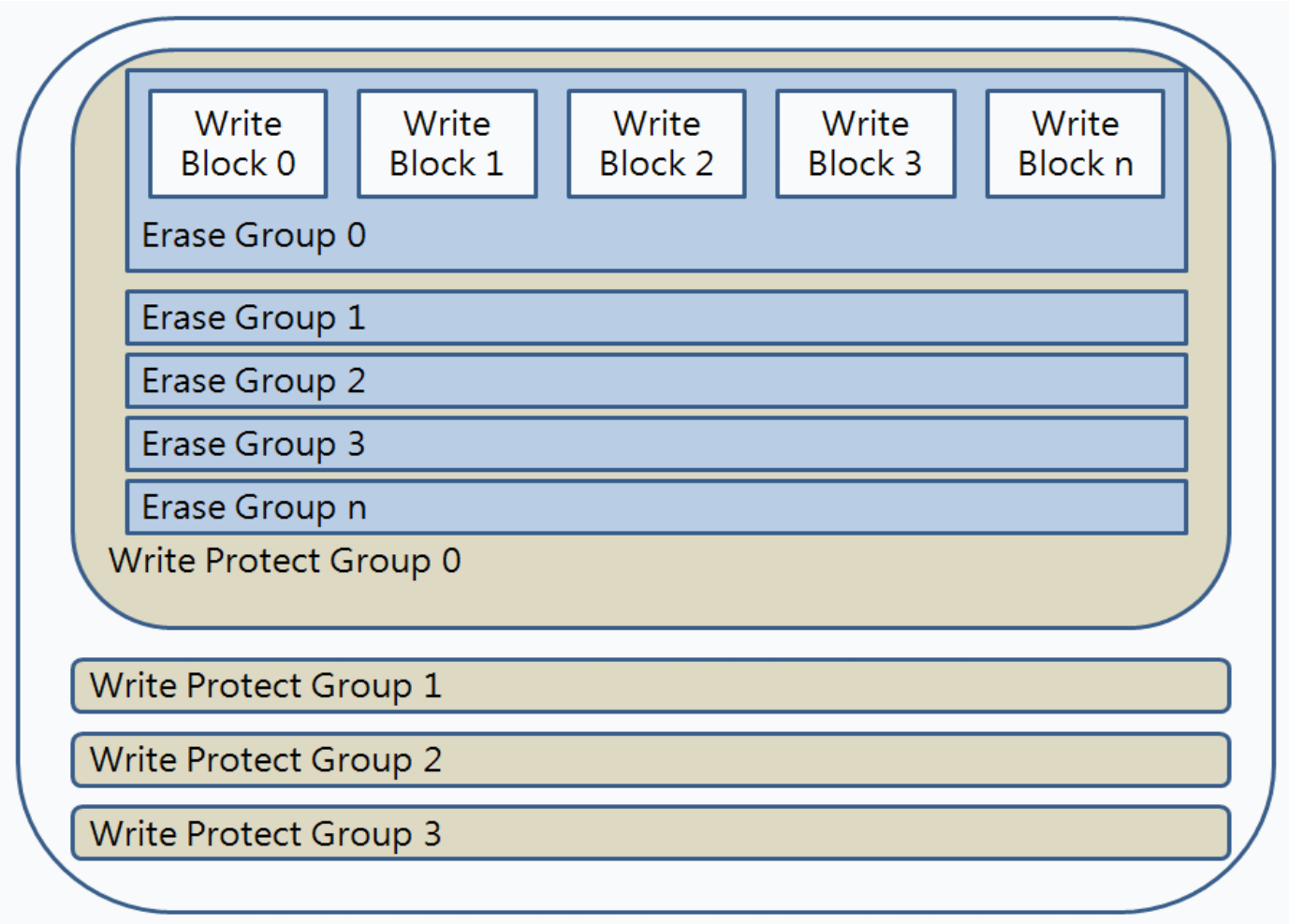
Note 1 : In Standby Power mode, CTRL Vccq & NAND Vcc power supply is swuched on.

• Sleep Power Mode

Density	NAND		CTRL	
	25℃	85℃	25℃	85℃
32GB(QDP)	0	0	TBD	TBD

Note 1 : In sleep state, triggered by CMD5, NAND Vcc power supply is swuched off (CTRL Vccq on)

5.6 Erase Write Protect Group Size



	Erase group size		Write protect group size
	ERASE_GROUP_DEF=0	ERASE_GROUP_DEF=1	
8GB	512KB	512KB	8MB
16GB	512KB	512KB	8MB
32 GB	512KB	512KB	8MB
64 GB	512KB	512KB	16MB

5.7 Timings

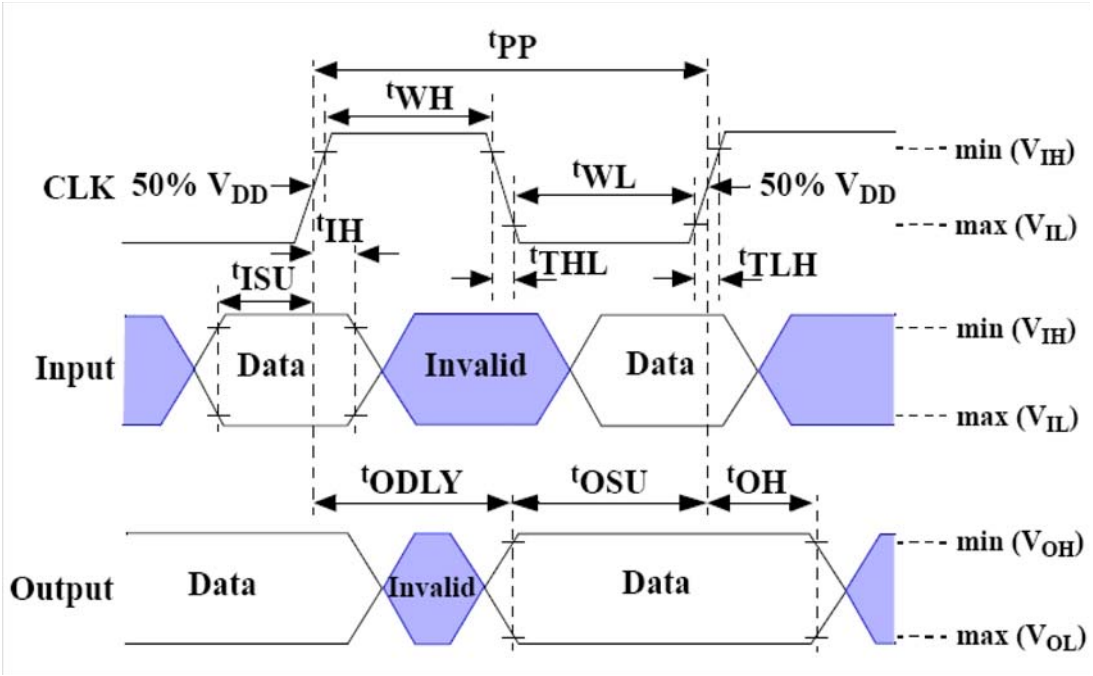
5.7.1 Time Out

Timing parameter	Value	Remark
Read Timeout	Max 100 ms	
Write Timeout (CMD to Write Done)	Max 500ms	
Write Timeout (Data to Data)	Max 300ms	
Erase Timeout	Max 300 ms	
Force erase Timeout	Max 3 min	
Trim Timeout	Max 300ms	
Secure Trim 1	Max 300ms	Only marking write block
Secure Trim 2	Max 300ms (Max 15 Min to Erase Physically)	Perform a secure purge operation
Secure Erase	Max 300ms (Max 15 Min to Erase Physically)	Map data invalid only
Discard	Max 300ms	
Partition switch Time	Max 1ms	Measured time after initialization
Initialization Timeout	Max 500ms	CMD to Response
PON Busy Time (Short / Long)	Max 50ms / 1000ms	PON Long busy time includes Garbage collection time.
PON Initialization Time (Short / Long)	Max 180ms	
BKOP Exit Time	Max 20ms	BKOP Off time after HPI
Auto-BKOP Exit Time	Max 100ms	BKOP Off time after any CMD from Host
HPI	Max 100ms	Response after HPI
Auto-standby Time-out	Max 50ms	
Auto-suspend Timeout	Max 40us	Fast wake up from Auto suspend at idle state
CMD5 Sleep In	3ms	
Sliding Window	Max 256ms	

-. NAND I/F : DDR 200Mhz, 16KB page size.
-. eMMC I/F : HS400, x16
-. Pre-conditioning states - Clean state / Test Range : Random Write - 1GB, Random Read - 1GB
-. Sequential Read / Write chunk size : 1MB
-. Current numbers are based on aligned 4KB
-. Maximum 4-way interleaving

5.7.2 Bus Timing

Figure 14: Timing diagram: data input / output



Data must always be sampled on the rising edge of the clock.

Table 8: High-speed e-NAND interface timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK(1)					
Clock frequency Data Transfer Mode (PP)(2)	f_{PP}	0	52(3)	MHz	C_L ≤30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	C_L ≤ 30 pF
Clock low time	tWL	6.5		ns	C_L ≤ 30 pF
Clock rise time(4)	tTLH		3	ns	C_L ≤ 30 pF
Clock fall time	tTHL		3	ns	C_L ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	C_L ≤ 30 pF
Input hold time	tIH	3		ns	C_L ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	C_L ≤ 30 pF
Output hold time	tOH	2.5		ns	C_L ≤ 30 pF
Signal rise time(5)	tRISE		3	ns	C_L ≤ 30 pF
Signal fall time	tFALL		3	ns	C_L ≤ 30 pF

- NOTE 1. CLK timing is measured at 50% of VDD.
- NOTE 2. e-NAND shall support the full frequency range from 0-26Mhz, or 0-52MHz
- NOTE 3. Card can operate as high-speed card interface timing at 26 MHz clock frequency.
- NOTE 4. CLK rising and falling times are measured by min (VIH) and max (VIL).
- NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

Table 9: Backward-compatible e-NAND interface timing

Parameter	Symbol	Min	Max	Unit	Remark(1)
Clock CLK(2)					
Clock frequency Data Transfer Mode (PP)(3)	fPP	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10		ns	CL ≤ 30 pF
Clock low time	tWL	10		ns	CL ≤ 30 pF
Clock rise time(4)	tTLH		10	ns	CL ≤ 30 pF
Clock fall time	t_{THL}		10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time(5)	tOSU	11.7		ns	CL ≤ 30 pF
Output hold time(5)	tOH	8.3		ns	CL ≤ 30 pF

- NOTE 1. e-NAND must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed timing by the host sending the SWITCH command (CMD6) with the argument for high speed interface select.
- NOTE 2. CLK timing is measured at 50% of VDD.
- NOTE 3. For compatibility with cards that support the v4.2 standard or earlier, host should not use > 20 MHz before switching to high-speed interface timing.
- NOTE 4. CLK rising and falling times are measured by min (VIH) and max (VIL).
- NOTE 5. tOSU and tOH are defined as values from clock rising edge. However, there may be cards or devices which utilize clock falling edge to output data in backward compatibility mode.

  Therefore, it is recommended for hosts either to set tWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices.

  In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its' application notes.

5.7.3 Bus Timing for DAT Signals During 2x Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operate synchronously with both the rising and falling edge of CLK and therefore complies with the bus timing specified in eMMC JEDEC spec. section 10.5, therefore there is no timing change for the CMD signal.

Figure 15: Timing diagram: data input/output in dual data rate mode

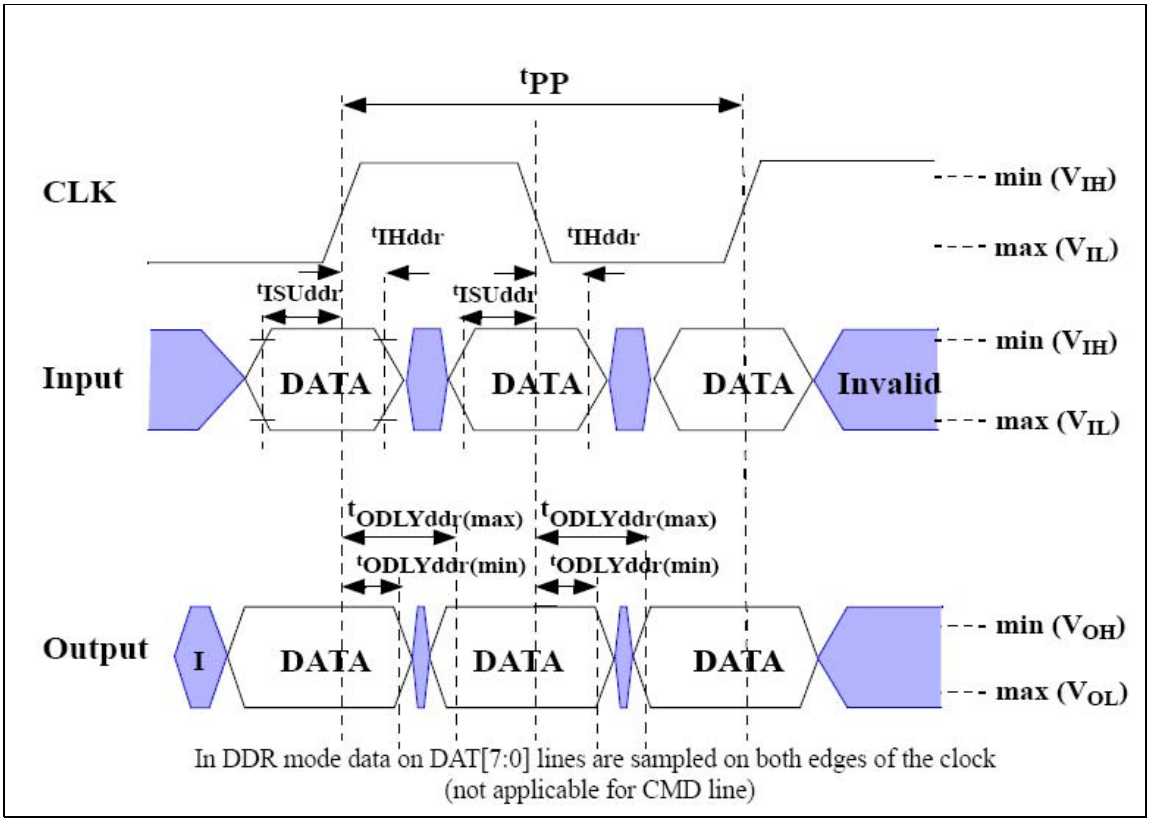


Table 10: Dual data rate interface timings

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK(1)					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Clock rise time	t_{TLH}		3	ns	CL≤30 pf
Clock fail time	t_{THL}		3	ns	CL≤30 pf
Input CMD (referenced to CLK-SDR mode)					
Input set-up time	tISUddr			ns	CL≤20 pf
Input hold time	tIHDDR			ns	CL≤20 pf
Output CMD (referenced to CLK-SDR mode)					
Output delay time during data transfer	tODLY		13.7	ns	CL≤20 pf
Output hold time	tOH	2.5		ns	CL≤20 pf
Signal rise time	tRISE		3	ns	CL≤20 pf
Signal fall time	tFALL		3	ns	CL≤20 pf
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL≤20 pf
Input hold time	tIHddr	2.5		ns	CL≤20 pf
Outputs DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL≤20 pf
Signal rise time(DAT0-7)(2)	tRISE		2	ns	CL≤20 pf
Signal fall time (DAT0-7)	tFALL		2	ns	CL≤20 pf

- NOTE 1. CLK timing is measured at 50% of VDD.
- NOTE 2. Inputs DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL)

5.7.4 Bus Timing Specification in HS 400 Mode

HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS 200 mode. (Previous bus timing parameter form DDR52 and HS200 mode are defined by JEDEC standard)

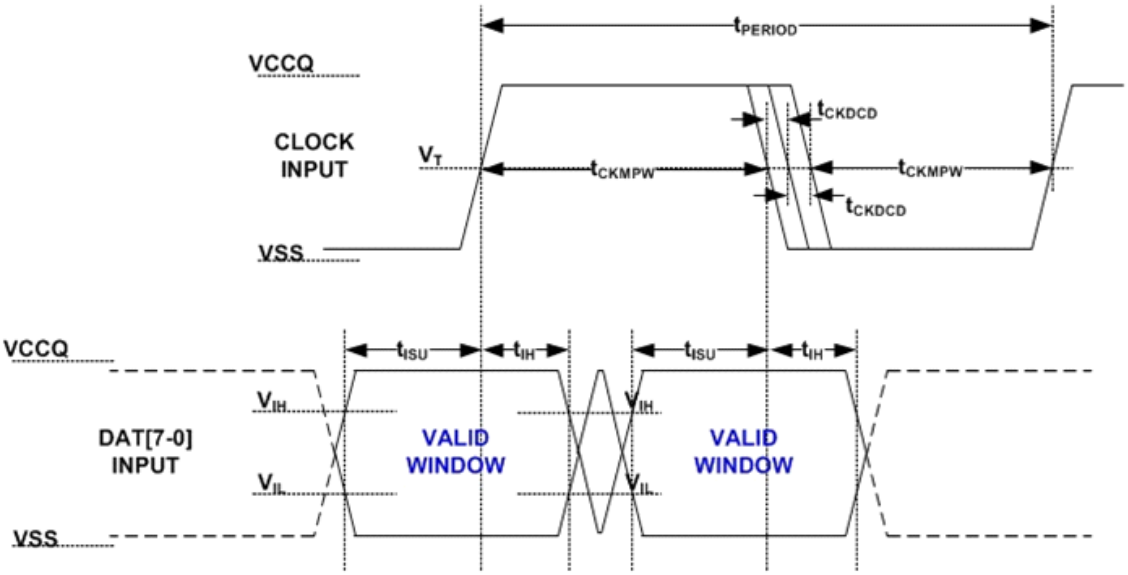


Figure 16. HS400 Device input timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges with respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	tCKDCD	0.0	0.4	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	tCKMPW	2.2		ns	With respect to V_T
Input DAT (referenced to CLK)					
Input set-up time	tISUddr	0.4		ns	$C_{DEVICE} \leq 6pF$ With respect to V_{IH}/V_{IL}
Input hold time	tIHddr	0.4		ns	$C_{DEVICE} \leq 6pF$ With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}

Table 12. HS400 Device input timing

5.7.4 Bus Timing Specification in HS 400 Mode

HS400 Device Output Timing

The Data Stobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

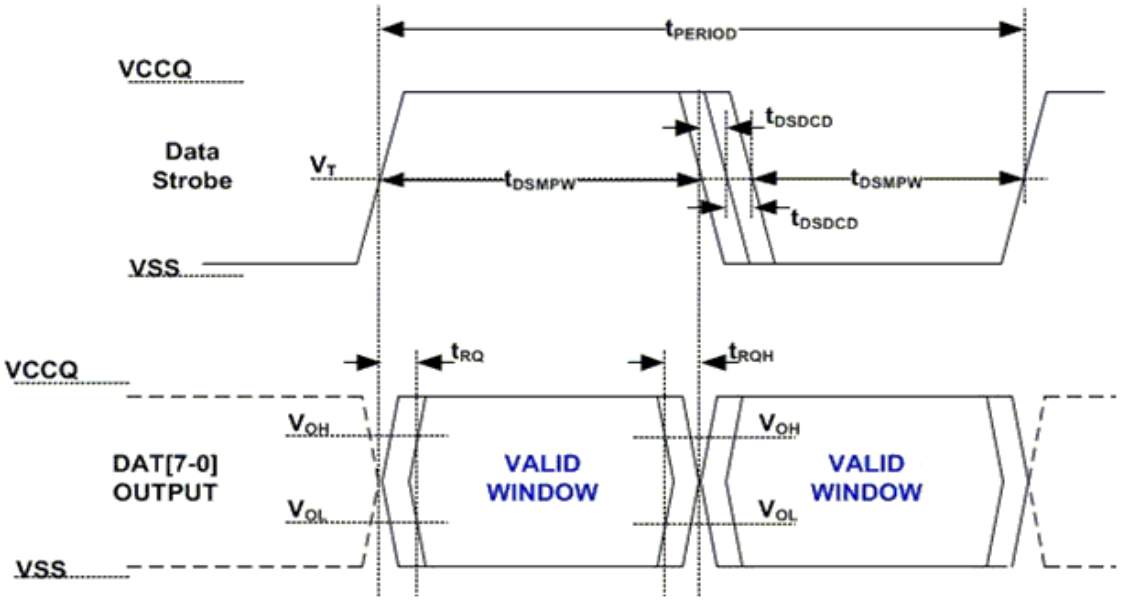


Figure 17. HS400 Device output timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5			200MHz(Max), between rising edges with respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL} and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion(tCKDCD) With respect to V_T Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0		ns	With respect to V_T
Read pre-amble	t_{RPRE}	0.4	5 (One Clock Cycle)	ns	
Read post-amble	t_{RPST}	0.4	2.5 (Half Clock Cycle)	ns	
Output DAT (referenced to Data Strobe)					
Input set-up time	tISUddr			ns	$C_{DEVICE} \leq 6pF$ With respect to V_{IH}/V_{IL}
Output Skew	tRQ		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	tRQH		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

Table 12. HS400 Device Output timing

Table 13. HS400 Capacitance

Parameter	Symbol	Min	Type	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	Kohm	
Pull-up resistance for DAT0-7	R_{DAT}	10		100	Kohm	
Pull-down resistance for Data strobe	R_{DS}	10		100	Kohm	
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	Kohm	
Bus signal line capacitance	CL			13	pF	
Single Device capacitance	C_{Device}			6	pF	

5.8 Bus Signal

5.8.1 Bus Signal Line Load

The total capacitance C_L of each line of e-MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself, and the capacitance C_{Device} of the eMMC connected to this line, and requiring the sum of the host and bus capacitances not to exceed 20 pF (see Table 14).

$$C_L = C_{HOST} + C_{BUS} + C_{Device}$$

Table 14 : e-NAND Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	Kohm	to prevent bus floating
Pull-up resistance for DAT0-7	R_{DAT}	10		100	Kohm	to prevent bus floating
Internal pull up resistance DAT1 - DAT7	R_{int}	10		150	Kohm	
Bus signal line capacitance	C_L			30	pF	Single Device
Single e-NAND capacitance	C_{DEVICE}			12	pF	
Maximum signal line inductance				16	nH	$f_{PP} \leq 52$ MHz
VDDi capacitor value	C_{REG}(2)	0.1			uF	To stablize regulator output when targt device bus speed mode is either backward-compatible, high speed SDR, high speed DDR, or HS200.
		1			uF	To stablize regulator output when target device bus speed mode is HS400
VCCQ decoupling capacitor	C_{H1}	1			uF	(3), (4), (5)

(1) Recommended maximum pull-up is 30 Kohm for 1.2 V and 50Kohm for 1.8V interface supply voltages. A 3V part, may use the whole range up to 100Kohms.

(2) Recommended value for C_{REG} might be different between *e*•MMC device vendors. Please confirm the maximum value and the accuracy of the capacitance with *e*•MMC vendor because the electrical characteristics of the regulator inside *e*•MMC is affected by the fluctuation of the capacitance.

(3) CH1 is VccQ-VssQ decoupling capacitor required for HS200&HS400 *e*•MMC device.

(4) CH1 should be placed adjacent to VccQ-VssQ balls (#K6 and #K4 accordingly, next to DAT[7..0] balls). It should be located as close as possible to the balls defined in order to minimize connection parasitics.

5.8.2 Overshoot / Undershoot Specification

		V_{CCQ}	Unit
		1.70V - 1.95V	
Maximum peak amplitude allowed for overshoot area.	Max	0.9	V
Maximum peak amplitude allowed for undershoot area.	Max	0.9	V
Maximum area above V_{CCQ}	Max	1.5	V-ns
Maximum area below V_{SSQ}	Max	1.5	V-ns

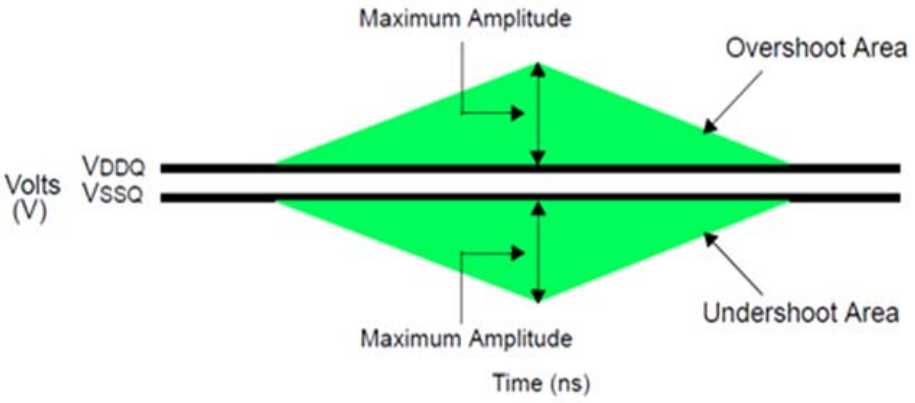
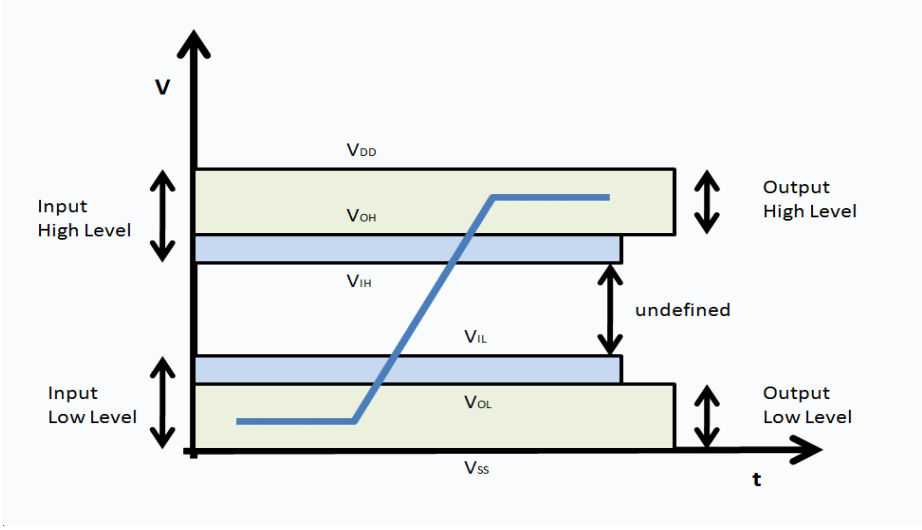


Figure 18. Overshoot / Undershoot definition

5.8.2 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 19: e-NAND bus signal level



- **Open-Drain mode bus signal level**

Table 15: Open-Drain signal level

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.2		V	Note[1)]
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2mA

(1) Because Voh depends on external resistance value (including outside the package), this value does not apply as device specifiaction.
Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min Value.

- **Push-Pull mode bus signal level**

The device input and output voltages shall be within the following specified ranges for any VDD of the allowed

Table 16: Push-Pull signal level 2.7V-3.6V VCCQ range

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75 * V_{DD}		V	I_{OH} = -100µA @ V_{CCQ}min
Output LOW voltage	V_{OL}		0.125 * V_{CCQ}	V	I_{OL} = -100µA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 * V_{DD}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25 * V_{CCQ}	V	

Table 17: Push-pull signal level 1.65V-1.95V VCCQ range

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	VDD - 0.45V		V	IOH = -2mA
Output LOW voltage	V_{OL}		0.45V	V	IOL = -2mA
Input HIGH voltage	V_{IH}	0.65 * V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35 * V_{DD}	V	

Note :
- 1) 0.7*VCCQ for eMMC 4.3 and older revisions.
- 2) 0.3*VCCQ for eMMC 4.3 and older revisions.

5.9 Performance

Performance measured using IOZone test with EXT4 file system.

Data transfer unit	512KB	1024KB
Sequential Read	170 MB/s	200 MB/s
Sequential Write	80 MB/s	80 MB/s
Data transfer unit	**4KB**	**8KB**
Random Read	4K IOPS	4K IOPS
Random Write	3K IOPS	3K IOPS

- **Note 1** : IOZone for Android based mobile platform.
- **Note 2** : Sequential performance measured using IOZone test with 512KB & 1024KB of data transfer unit size.
- **Note 3** : Random performance measured using IOZone test with 4KB & 8KB of data transfer unit size.
- **Note 4 :** Speed may vary due to host hardware, software and usage.
- **Density :** 32GB QDP
- 200MHz DDR, Cache operation

6. Commands

6.1 Command Classes

The command set of e-NAND is divided into several classes. Each class supports a subset of e-NAND functions.
The supported e-NAND command Classes are coded as a parameter in the eMMC specific data (CSD) register, providing the host with information on how to access the e-NAND.

Table 18: Supported eMMC command classes

e-NAND command class	Class description	Support commands																							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	23	24	25
Class 0	basic	+	+	+	+	+	+	+	+	+	+	+		+	+	+	+				+				
Class 1	obsolete																								
Class 2	block read																	+	+	+			+		
Class 3	obsolete																								
Class 4	block write																	+					+	+	+
Class 5	erase																								
Class 6	write protection																								
Class 7	lock eMMC																	+							
Class 8	Application specific																								
Class 9	I/O mode																								
Class 10	Security mode																								
Class 11	reserved																								

e-NAND command class	Class description	Support commands																		
		26	27	28	29	30	31	35	36	38	39	40	42	42	49	53	54	55	56	
Class 0	basic																			
Class 1	stream read																			
Class 2	block read																			
Class 3	stream write																			
Class 4	block write	+	+											+	+					
Class 5	erase							+	+	+										
Class 6	write protection			+	+	+	+													
Class 7	lock eMMC												+							
Class 8	Application specific																	+		
Class 9	I/O mode										+	+								
Class10	Security Protocols															+	+			
Class11	reserved																			

6.2 Command

The following tables define in detail all e-NAND commands.

Table 19: Basic command (class 0 and class 1)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD0	bc	[31:0] 00000000	-	GO_IDLE_STATE	Resets e-NAND to idle state
	bc	[31:0] F0F0F0F0	-	GO_PRE_IDLE_STATE	Resets e-NAND to pre-idle state
	-	[31:0] FFFFFFFA	-	BOOT_INITIATION	Inititiate alternative boot operation
CMD1	bcr	[31:0] OCR with-out busy	R3	SEND_OP_COND	Asks e-NAND, in idle state, to send its Operating Conditions Register contents in the response on the CMD line.
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	Asks e-NAND to send its CID number on the CMD line
CMD3	ac	[31:16] RCA [15:0] stuff bits	R1	SET_RELATIVE_ADDR	Assigns relative address to e-NAND
CMD4	bc	[31:16] DSR [15:0] stuff bits	-	SET_DSR	Programs the DSR of e-NAND
CMD5	ac	[31:16] RCA [15] Sleep/Awake [14:0] stuff bits	R1b	SLEEP_AWAKE	Toggles the card between Sleep state and Standby state.
CMD6	ac	[31:26] Set to 0 [25:24] Access [23:16] Index [15:8] Value [7:3] Set to 0 [2:0] Cmd Set	R1b	SWITCH	Switches the mode of operation of e-NAND the EXT_CSD registers.
CMD7	ac	[31:16] RCA [15:0] stuff bits	R1/ R1b(1)	SELECT/DESELECT_CARD	Command toggles e-NAND between the stand-by and transfer states or between the programming and disconnect states. In both cases e-NAND is selected by its own relative address and gets deselected by any other address; address 0 deselects e-NAND.
CMD8	adtc	[31:0] stuff bits	R1	SEND_EXT_CSD	e-NAND sends its EXT_CSD register as a block of data.
CMD9	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CSD	e-NAND sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CID	e-NAND sends its card identification (CID) on CMD the line.
CMD11				obsolete	The response to CMD11 will be undefined.
CMD12	ac	[31:16]RCA3 [15:1]stuff bits [0]HPI	R1/ R1b4	STOP_TRANSMISSION	Forces e-NAND to stop transmission.If HPI flag is set the device shall interrupt itsinternal operations in a well defined timing.

Table 19: Basic commands and read-stream command (class 0 and class 1) (continued)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD13	ac	[31:16] RCA [15:1] stuff bits [0] HPI	R1	SEND_STATUS	Addressed Device sends its status register. If HPI flag is set the device shall innterrupt its internal operations in a well defined timing
CMD14	adtc	[31:0] stuff bits	R1	BUSTEST_R	A host reads the reversed bus testing data pattern from e-NAND.
CMD15	ac	[31:16] RCA [15:0] stuff bits	-	GO_INACTIVE_STATE	Sets e-NAND to inactive state
CMD19	adtc	[31:0] stuff bits	R1	BUSTEST_W	A host sends the bus test data pattern to e-NAND.

- NOTE 1. R1 while selecting from Stand-By State to Transfer State; R1b while selecting from Disconnected State to Programming State.
- NOTE 2. RCA in CMD12 is used only if HPI bit is set. The argument does not imply any RCA check on the device side.
- NOTE 3. R1 for read cases and R1b for write cases.

Table 20: Block-oriented read commands (class 2)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	Sets the block length (in bytes) for all following block commands (read and write). Default block length is specified in the CSD.
CMD17	adtc	[31:0] data address(1)	R1	READ_SINGLE_BLOCK	Reads a block of the size selected by the SET_BLOCKLEN command.2
CMD18	adtc	[31:0] data address(1)	R1	READ_MULTIPLE_ BLOCK	Continuously transfers data blocks from e-NAND to host until interrupted by a stop command, or the requested number of data blocks is transmitted
CMD21	adtc	[31:0] stuff bits	R1	SEND_TUNING_ BLOCK	128 clocks of tuning pattern(64byte in 4bit mode or 128byte in 8 bit mode)is sent for HS200 optimal sampling point detection

• NOTE 1. Data address for media =<2GB is a 32bit byte address and data address for media > 2GB is a 32bit sector (512B) address.
• NOTE 2. The transferred data must not cross a physical block boundary, unless READ_BLK_MISALIGN is set in the CSD register.

Table 21: Stream write commands (class 3)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD20				Obsolete	The response to CMD20 will be undefined.
CMD22	reserved				

Table 22: Block-oriented write commands (class 4)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD23 (default)	ac	[31] Reliable Write Request [30] '0' non-packed [29] tag request [28:25] context ID [24]: forced programming [23:16] set to 0 [15:0] number of blocks	R1	SET_BLOCK_COUNT	**non-packed command version** Defines the number of blocks (read/write) and the reliable writer parameter(write)for a block read or write command (See section 6.6.10 and Section 6.6.11) Many contain a tag request or a context ID. Tag and Context cannot be used together in the same command, if one is used the other must be set to zero. The context ID is a identifier(0 to 15) that associates the read/write command with the specific context. When bit 24 is set to 1, forced programming enabled, data shall be forceably programmed to non-volatile storage instead of volatile cache while cache is turned ON.
CMD23 (packed)	ac	[31]set to 0 [30] '1' packed [29:16] set to 0 [15:0] number of blocks	R1	SET_BLOCK_COUNT	**packed command version** Defines the number of blocks (read/wirte) for the following packed write command or for the header of the following packed command. For packed write commands, the number of blocks should include the total number of blocks all packed commands plus one for the header block. For packed read commands, the number of blocks should equal one as only the header is sent inside the following CMD25. After that, a separate normal read command is sent to get the packed data.
CMD24	adtc	[31:0] data address(1)	R1	WRITE_BLOCK	Writes a block of the size selected by the SET_BLOCKLEN command(2).
CMD25	adtc	[31:0] data address(1)	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows or the requested number of block received. If sent as a packed command (either packed write, or the header of packed read) the argument shall contain the first read/write date address in the pack(address of first individual command inside the pack).
CMD26	adtc	[31:0] stuff bits	R1	PROGRAM_CID	Programming of the card identification register.This command shall be issued only once. e-NAND contains hardware to prevent this operation after the first programming. Normally this command is reserved for the manufacturer.
CMD27	adtc	[31:0] stuff bits	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.
CMD49	adtc	[31:0] stuff bits	R1	SET_TIME	Set the real time clock according to the RTC information in the 512B data block

- NOTE 1. Data address for media =<2GB is a 32bit byte address and data address for media > 2GB is a 32bit sector (512B) address.
- NOTE 2. The transferred data must not cross a physical block boundary unless WRITE_BLK_MISALIGN is set in the CSD.

Table 23: Block-oriented write protection commands (class 6)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD28	ac	[31:0] data address(1)	R1b	SET_BLOCK_COUNT	**IF Class_6_CTRL = 0x00:** If e-NAND has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE or HC_WP_GRP_SIZE). **IF Class_6_CTRL = 0x01:** This command releases the specifed addressed group.
CMD29	ac	[31:0] data address(1)	R1b	CLR_WRITE_PROT	**IF Class_6_CTRL = 0x00:** If e-NAND provides write protection features, this command clears the write protection bit of the addressed group. **IF Class_6_CTRL = 0x01:** This command releases the specified addressed group.
CMD30	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT	**IF Class_6_CTRL = 0x00:** If e-NAND provides write protection features, this command asks e-NAND to send the status of the write protection bits.(2) **IF Class_6_CTRL = 0x01:** This command asks the device to send the status of released groups. A bit '0' means the specific group is valid and assessible, a bit '1' means the specific group was released and it cannot be used.(3)
CMD31	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT_TYPE	**IF Class_6_CTRL = 0x00:** This command sends the type of write protection that is set for the different write protection group.(4) **IF Class_6_CTRL = 0x01:** This command returns a fixed pattern of 64bit zeros in its payload.

- NOTE 1. Data address for media =<2GB is a 32bit byte address and data address for media > 2GB is a 32bit sector (512B) address.
- NOTE 2. 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data lines. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to zero.
- NOTE 3. 32 released status bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data lines. The last (least significant) bit of the released bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding released bits shall be set to zero.
- NOTE 4. 64 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data lines. Each set of two protection bits shows the type of protection set for each of the write protection groups. The definition of the different bit settings are shown below. The last (least significant) two bits of the protection bits correspond to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to zero.
  "00" Write protection group not protected
  "01" Write protection group is protected bytemporary write protection
  "10" Write protection group is protected by power-on write protection
  "11" Write protection group is protected by permanent write protection

Table 24: Erase commands (class 5)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD32 … CMD34	Reserved. These command indexes cannot be used in order to maintain backwards compatibility with older versions of eMMCs				
CMD35	ac	[31:0] data address(1),(2)	R1	ERASE_GROUP_START	Sets the address of the first erase group within a range to be selected for erase
CMD36	ac	[31:0] data address(1),(2)	R1	ERASE_GROUP_END	Sets the address of the last erase group within a continuous range to be selected for erase
CMD37	Reserved. This command index cannot be used in order to maintain backwards compatibility with older versions of eMMCs				
CMD38	ac	[31] Secure request [30:16] set to 0 [15] Force garbage collect request(4) [14:2] set to 0 [1]Discard Enable [0]Identify Write block for Erase (or TRIM Enable)	R1b	ERASE	Erases all previously selected write blocks according to argument bits.(3) When all argument bits are zero CMD38 wil perform an erase on erase group(s). When Bit 0= 1 and Bit 1=0 then CMD38 will perform a TRIM on the sector(s) When Bit 0= 1 and Bit 1=1 then CMD38 will perform a Discard on the sector(s) To maintain backward compatibility the device must not report an error if bits 31 and 15 are set. The device behavior when these are set is undefined. All other argument setting should trigger an ERROR.

- NOTE 1. Data address for e-NAND is a 32bit sector (512B) address.
- NOTE 2. e-NAND will ignore all LSB's below the Erase Group size, effectively rounding the address down to the Erase Group boundary.
- NOTE 3. JEDEC Spec table 11 and 12 give a description of the argument bits and list of supported argument combinations.
- NOTE 4. Argument bit 15 is an optional feature that is only supported if SEC_GB_CL_EN (EXT_CSD[231] bit 0) is set. Argument bit 31 is an optional feature that is only supported if SEC_ER_EN (EXT_CSD[231] bit 0)is set

Table 25: Lock eMMC commands (class 7)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD42	adtc	[31:16] stuff bits	R1	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command.
CMD43 ... CMD48	reserved				

Table 26: Application-specific commands (class 8)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD55	ac	[31:16] RCA [15:0] stuff bits	R1	APP_CMD	Indicates to the Device that the next command is an application specific command rather than a standard command.
CMD56	adtc	[31:1] stuff bits. [0]: RD/WR(1)	R1	GEN_CMD	Used either to transfer a data block to the Device or to get a data block from the Device for general purpose / application specific commands. The size of the data block shall be set by the SET_BLOCK_LEN command.
CMD57 ... CMD59	reserved				
CMD60 ... CMD63	reserved for manufacturer				

• NOTE 1. RD/WR: "1" the host gets a block of data from e-NAND. "0" the host sends block of data to e-NAND.

Table 27: I/O mode commands (class 9)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD39	ac	[31:16] RCA [15:15] register write flag [14:8] register address [7:0] register dat	R4	FAST_IO	Used to write and read 8 bit (register) data fields. The command addresses a Device and a register and provides the data for sriting if the write flag is set. The R4 response contains data read from the addressed register if the write flag is cleared to 0. This command accesses application dependent registers which are not defined in th eMMC standard.
CMD40	bcr	[31:0] stuff bits	R5	GO_IRQ_STATE	Sets the system into interrupt mode
CMD41	reserved				

Table 28: Security Protocols (class 10)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD50-52	Reserved				
CMD53	adtc	[16:31] Security Protocol Specific [15:8] Security Protocol [7:0]reserved	R1	PROTOCOL_RD	Continuously transfers data blocks from device to host. Number of data blocks shall be defined by a preceding CMD23. Data Transfer may be interrupted by a STOP_TRANSMISSION command, This command is not supported if sent as a packed command. Block size is always 512byte.
CMD54	adtc	[16:31] Security Protocol Specific [15:8]Security Protocol [7:0]reserved	R1	PROTOCOL_WR	Continuously transfer data blocks from host to device. Number of data block shall be defined by a preceding CMD23. Data Transfer may be interrupted by a STOP_TRANSMISSION command. This command is not supported if sent as a packed command. Block size is always 512bytes.

7. Device Registers

There are six different registers within the device interface:

- •Operation Conditions Register (OCR)
- •Card Identification Register (CID)
- •Card Specific Data Register (CSD)
- •Relative Card Address Register (RCA)
- •DSR (Driver Stage Register)
- •Extended Card Specific Data Register (EXT_CSD).

These registers are used for the serial data communication and can be accessed only using the corresponding commands . e-NAND has a status register to provide information about the device current state and completion codes for the last host command.

7.1 Operation Conditions Register (OCR)

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of e-NAND and the access mode indication. In addition, this register includes a status information bit. This status bit is set if e-NAND power up procedure has been finished. The OCR register shall be implemented by e-NAND.

Table 29: OCR register definition

OCR bit	Description	High Voltage Multimedia Card	Dual voltage MultiMedia Card and eMMC
[6:0]	Reserved	000 0000b	00 00000b
[7]	1.70 - 1.95V	0b	1b
[14:8]	2.0 - 2.6	000 0000b	000 000b
[23:15]	2.7 - 3.6 (High VCCQ range)	1 1111 1111b	1 1111 1111b
[28:24]	Reserved	0 0000b	000 000b
[30:29]	Access mode	00b (byte mode) 10b (sector mode)	00b (byte mode) 10b (sector mode)
[31]	(card power up status bit (busy))(1)		

- NOTE 1. This bit is set to LOW if the card has not finished the power up routine

7.2 Card Identification (CID) Register

The Card IDentification (CID) register is 128 bits wide. It contains e-NAND identification information used during e-NAND identification phase (e-NAND protocol). Every individual flash or I/O e-NAND shall have a unique identification number. **Table 30** lists these identifiers. The structure of the CID register is defined in the following sections.

Table 30 : Card identification (CID) fields

Name	Field	Width	CID slice	CID value	Remark
Manufacturer ID	MID	8	[127:120]	90h	
Reserved		6	[119:114]		
Card/BGA	CBX	2	[113:112]	01h	BGA
OEM/application ID	OID	8	[111:104]	4ah	
Product name	PNM	48	[103:56]	8GB: 483847316506 16GB: 484147326505 32GB: 484247346505 64GB: 484347386505	
Product revision	PRV	8	[55:48]	01h	
Product serial number	PSN	32	[47:16]	-	Not Fixed
Manufacturing date	MDT	8	[15:8]	-	Not Fixed
CRC7 checksum	CRC	7	[7:1]	-	Not Fixed
Not used, always '1'	Reserved	1	[0:0]	1	

7.3 Card Specific Data Register (CSD)

The Card Specific Data (CSD) register provides information on how to access e-NAND contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the CSD Registry entries in the **Table 31** below is coded as follows:

- ***R:*** Read only. W: One time programmable and not readable. R/W: One time programmable and readable.
- ***W/E:*** Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- ***R/W/E:*** Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- ***R/W/C_P:*** Writable after value cleared by power failure and HW/rest assertion (the value not cleared by CMD0 reset) and readable.
- ***R/W/E_P:*** Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- ***W/E_P:*** Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Table 31: CSD fields

Name	Field	Width	Cell type	CSD slice	CSD value	Remark
CSD structure	CSD_STRUCTURE	2	R	[127:126]	4h	
System specification version	SPEC_VERS	4	R	[125:122]	4h	
Reserved		2	R	[121:120]		
Data read access-time 1	TAAC	8	R	[119:112]	27h	
Data read access-time 2in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h	
Card command classes	CCC	12	R	[95:84]	f5h	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h	
DSR implemented	DSR_IMP	1	R	[76:76]	0h	
Reserved		2	R	[75:74]		
Device size	C_SIZE	12	R	[73:62]	fffh	
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h	
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h	
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h	
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1fh	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1fh	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	fh	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h	
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h	

Table 31: CSD fields (continued)

Name	Field	Width	Cell type	CSD slice	CSD value	Remark
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h	
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h	
Reserved		4	R	[20:17]		
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h	
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h	
Copy flag (OTP)	COPY	1	R/W	[14:14]	1h	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h	
File format	FILE_FORMAT	2	R/W	[11:10]	0h	
ECC code	ECC	2	R/W/E	[9:8]	0h	
CRC	CRC	7	R/W/E	[7:1]	-	Not fixed
Reserved		1		[0:0]		

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

7.4 Extended CSD Register

The Extended CSD register defines e-NAND properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines e-NAND capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration e-NAND is working in. These modes can be changed by the host by means of the SWITCH command. For details.

Table 32. Extended CSD

Name	Field	CSD slice	Cell Type	EXT_CSD Value	Remark
Properties segment					
Reserved		[511:506]			
Extended Security Commands Error	EXT_SECURITY_ERR	[505]	R	0h	
Supported command sets	S_CMD_SET	[504]	R	1h	Allocated by MMCA
HPI features	HPI_FEATURES	[503]	R	1h	
Background operation support	BKOPS_SUPPORT	[502]	R	1h	Background operation are supported
Max packed read commands	MAX_PACKED_READS	[501]	R	8h	
Max packed write commands	MAX_PACKED_WRITES	[500]	R	8h	
Data Tag Support	DATA_TAG_SUPPORT	[499]	R	1h	
Tag Unit Size	TAG_UNIT_SIZE	[498]	R	0h	
Tag Resources Size	TAG_RES_SIZE	[497]	R	6h	
Context management capabilities	CONTEXT_CAPABILITIES	[496]	R	78h	
Large Unit size	LARGE_UNIT_SIZE_M1	[495]	R	1h	
Extended partitions attribute support	EXT_SUPPORT	[494]	R	3h	
Supported modes	SUPPORTED_MODES	[493]	R	1h	
FFU features	FFU_FEATURES	[492]	R	0h	
Operation codes timeout	OPERATION_CODE_TIME OUT	[491]	R	17h	
FFU Argument	FFU_ARG	[490:487]	R	6600h	
Reserved		[486:306]			
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS _CORECTLY_PROGRAMMED	[305:302]	R	0	
Vendor proprietary health report	VENDOR_PROPRIETARY_HE ALTH_REPORT	[301:270]	R	TBD	
Device life time estimation type B	DEVICE_LIFE_TIME_EST_T YP_B	[269]	R	1h	
Device life time estimation type A	DEVICE_LIFE_TIME_EST_T YP_A	[268]	R	1h	
Pre EOL information	PRE_EOL_INFO	[267]	R	1h	
Optimal read size	OPTIMAL_READ_SIZE	[266]	R	40h	
Optimal write size	OPTIMAL_WRITE_SIZE	[265]	R	40h	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	[264]	R	40h	
Device version	DEVICE_VERSION	[263:262]	R	4205h	
Firmware version	FIRMWARE_VERSION	[261:254]	R	1h	
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	[253]	R	0h	

Name	Field	CSD slice	Cell Type	EXT_CSD Value	Remark
Cache size	CACHE_SIZE	[252:249]	R	400h	
Generic CMD6 timeout	CENERIC_CMD6_TIME	[248]	R	5h	
Power off notification(long)timeout	POWER_OFF_LONG_TIME	[247]	R	64h	
Background operations status	BKOPS_STATUS	[246]	R	0h	Outstanding: No operations required
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	[245:242]	R	0h	Number of correctly programmed sectors = [245]*224+[244]*216+[243]*28+[242]
1st initialization time after partitioning	INI_TIMEOUT_AP	[241]	R	ah	100ms*10=1000ms
Reserved		[240]			
Power class for 52MHz, DDR at Vcc=3.6V	PWR_CL_DDR_52_360	[239]	R	0h	
Power class for 52MHz, DDR at Vcc=1.95V	PWR_CL_DDR_52_195	[238]	R	0h	
Power class for 200MHz at V_{CCQ}=1.95, Vcc=3.6V	PWR_CL_200_195	[237]	R	0h	
Power class for 200MHz at V_{CCQ}=1.3, Vcc=3.6V	PWR_CL_200_130	[236]	R	0h	
Minimum write performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	[235]	R	0h	
Minimum read performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	[234]	R	0h	
Reserved		[233]			
TRIM multiplier	TRIM_MULT	[232]	R	1h	TRIM Timeout = 300ms*1=300ms
Secure feature support	SEC_FEATURE_SUPPORT	[231]	R	55h	Bit[4]=1: Card supports the secure and insecure trim operations Bit[2]=1: Card supports the automatic secure purge operation on retired defective portions of the array Bit[0]=1: Secure purge operations are supported Bit[0,2,4]=0: Not support each feature Bit[1,3,5,6,7]=Reserved
Secure erase multiplier	SEC_ERASE_MULT	[230]	R	ah	
Secure TRIM multiplier	SEC_TRIM_MULT	[229]	R	ah	
Boot information	BOOT_INFO	[228]	R	7h	Bit[2]=1 : Device supports high speed timing duing boot Bit[1]=1 : Device supports dual data rate duing boot Bit[0]=1 : Device supports alternate boot method Bit[0,1,2]=0 : Not supports each feature Bit[7:3]=Reserved
Reserved		[227]			
Boot partition size	BOOT_SIZE_MULTI	[226]	R	20h	Boot partition size = 128Kbytes * BOOT_SIZE_MULTI
Access size	ACC_SIZE	[225]	R	6h	
High-capacity erase unit size	HC_ERASE_GRP_SIZE	[224]	R	1h	Erase Unit Size = 512KB*1=512KB
High_capacity erase timeout	ERASE_TIMEOUT_MULT	[223]	R	2h	Erase Timeout=300ms*2=600ms
Reliable write sector count	REL_WR_SEC_C	[222]	R	10h	1 sector supported for reliable write feature
High-capacity write protect group size	HC_WP_GRP_SIZE	[221]	R	8GB:10h 16GB:10h 32GB:10h 64GB:20h	8 high-capacity erase unit size

Name	Field	CSD slice	Cell Type	EXT_CSD Value	Remark
Sleep current(VCC)	S_C_VCC	[220]	R	7h	
Sleep current(VCCQ)	S_C_VCCQ	[219]	R	7h	
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	[218]	R	17h	
Sleep/awake timeout	S_A_TIMEOUT	[217]	R	11h	
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	[216]	R	ch	
Sector count	SEC_COUNT	[215:212]	R	8GB:E90000 16GB:1D5C000 32GB:3A40000h 64GB:7480000h	
Reserved		[211]			Reserved
Minimum write performance for 8bit at52MHz	MIN_PERF_W_8_52	[210]	R	8h	
Minimum read performance for 8bit at 52MHz	MIN_PERF_R_8_52	[209]	R		
Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	[208]	R		
Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	[207]	R		
Minimum write performance for 4bit at 26MHz	MIN_PERF_W_4_26	[206]	R		
Minimum read performance for 4bit at 26MHz	MIN_PERF_R_4_26	[205]	R		
Reserved		[204]			
Power class for 26MHz at 3.6V	PWR_CL_26_360	[203]	R	0h	
Power class for 52MHz at 3.6V	PWR_CL_52_360	[202]	R		
Power class for 26MHz at 1.95V	PWR_CL_26_195	[201]	R		
Power class for 52MHz at 1.95V	PWR_CL_52_195	[200]	R		
Partition switching timing	PARTITION_SWITCH_TIME	[199]	R	1h	Maximum partition switch timeout = 10ms*1=10ms
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	[198]	R	0Ah	Maximum out-of-interrupt timeout = 10ms*10=100ms
I/O Driver Strength	DRIVER_STRENGTH	[197]	R	1fh	
Device type	DEVICE_TYPE	[196]	R	57h	Bit[7]= HS400 Dual Data Rate eMMC @200MHz-1.2V I/O Bit[6]= HS400 Dual Data Rate eMMC @200MHz-1.8V I/O Bit[5]= HS200 Single Data Rate eMMC @ 200MHz-1.2V I/O Bit[4]= HS200 Single Data Rate eMMC @ 200MHz-1.8V I/O Bit[3]= High-Speed Dual Data Rate eMMC@52MHz-1.2V I/O Bit[2]= High-Speed Dual Data Rate eMMC@52MHz-1.8V or 3V I/O Bit[1]= High-Speed eMMC @ 52MHz - at rated device voltage(s) Bit[0]= High-Speed eMMC @ 26MHz - at rated device voltage(s)
Reserved		[195]			
CSD structure	CARD_STRUCTURE	[194]	R	2h	Version 4.1 - 4.2 - 4.3 - 4.41 - 4.5 - 4.51 - 5.0
Reserved		[193]			

Name	Field	CSD slice	Cell Type	EXT_CSD Value	Remark
Extended CSD revision	EXT_CSD_REV	[192]	R	7h	7 : Revision 1.7 (for MMC v5.0) 6 : Revision 1.6 (for MMC v4.5, v4.51) 5 : Revision 1.5 (for MMC v4.41) 4 : Revision 1.4 (Obsolete) 3 : Revision 1.3 (for MMC v4.3) 2 : Revision 1.2 (for MMC v4.2) 1 : Revision 1.1 (for MMC v4.1) 0 : Revision 1.0 (for MMC v4.0)
Modes Segment					
Command set	CMD_SET	[191]	R/W/ E_P	0h	Currently active command set. It can be 1 by host.
Reserved		[190]			
Command set revision	CMD_SET_REV	[189]	R	0h	See EXT_CSD in spec. It does not have a fixed rule.
Reserved		[188]			
Power class	POWER_CLASS	[187]	R/W/ E_P	0h	See EXT_CSD in spec.
Reserved		[186]			
High-speed interface timing	HS_TIMING	[185]	R/W/ E_P	1h	
Reserved		[184]			
Bus width mode	BUS_WIDTH	[183]	W/E_P	0h	Default = 0h Update in run time
Reserved		[182]			
Erased memory content	ERASED_MEM_CONT	[181]	R	0h	Erased memory range shall be '0'
Reserved		[180]			
Partition configuration	PARTITION_CONFIG	[179]	R/W/E & R/ WE_P	0h	
Boot config protection	BOOT_CONFIG_PROT	[178]	R/W & R/W/ C_P	0h	
Boot bus width	BOOT_BUS_WIDTH	[177]	R/W/E	0h	
Reserved		[176]	TBD		
High-density erase group definition	ERASE_GROUP_DEF	[175]	R/W/ E_P	0h	Use old erase group size and write protect group size definition (default)
Boot area write protection register	BOOT_WP	[173]	R/W & R/W/ C_P	0h	
Reserved		[172]	TBD		
User area write protection register	USER_WP	[171]	R/W,R/ W/C_P & R/W/ E_P	0h	
Reserved		[170]	TBD		
FW configuration	FW_CONFIG	[169]	R/W	0h	FW updates enabled
RPMB Size	RPMB_SIZE_MULT	[168]	R	20h	RPMB Partition Size= 128kB * RPMB_SIZE_MULT
Write reliability setting register	WR_REL_SET	[167]	R/W	1fh	Write Data Reliability Partition FALSE
Write reliability parameter register	WR_REL_PARAM	[166]	R	5h	

Name	Field	CSD Slice	Cell Type	EXT_CSD Value	Remark
Sanitize start	SANITIZE_START	[165]	W/E_P	0h	-
Manually start background operations	BKOPS_START	[164]	W/E_P	0h	Writing any value to this field shall manually start BKOPs.
Enable background operations handshake	BKOPS_EN	[163]	R/W	0h	Host does not support BKOPs handling and is not expected to write to BKOPS_START field
H/W reset function	RST_n_FUNCTION	[162]	R/W	0h	RST_n signal is temporarily disabled (default)
HPI management	HPI_MGMT	[161]	R/W/E_P	0h	HPI mechanism not activated by the host (default)
Partitioning support	PARTITIONING_ SUPPORT	[160]	R	7h	Bit[1]=1 : Device can have enhanced technological features in partitions and user data area Bit[1]=0 : Device can not have enhanced technological features in partitions and user data area Bit[0]=1 : Device supports partitioning features Bit[0]=0 : Device does not support partitioning features
Max enhanced area size	MAX_ENH_SIZE_ MULT	[159:157]	R	8GB:1d2h 16GB:3abh 32GB:748h 64GB:748h	
Partitions attribute	PARTITIONS_ ATTRIBUTE	[156]	R/W	0h	Bit[7:5] : Reserved Bit[4]=1 : Set Enhanced attribute in General Purpose partition 4 Bit[4]=1 : Set Enhanced attribute in General Purpose partition 4 Bit[3]=1 : Set Enhanced attribute in General Purpose partition 3 Bit[2]=1 : Set Enhanced attribute in General Purpose partition 2 Bit[1]=1 : Set Enhanced attribute in General Purpose partition 1
Paritioning setting	PARTITION_SETTING_COMPLETED	[155]	R/W	0h	NOT PARTITION_SETTING_COMPLETED
General purpose partition size	GP_SIZE_MULT	[154:143]	R/W	0h	
Enhanced user data area size	ENH_SIZE_MULT	[142:140]	R/W	0h	
Enhanced user data start address	ENH_START_ADDR	[139:136]	R/W	0h	
Reserved		[135]			
Bad Block management mode	SEC_BAD_BLK_ MGMNT	[134]	R/W	0	
Production state awareness	PRODUCTION_STATE_AWARENESS	[133]	R/W/E	TBD	
Package Case Temperature is controlled	TCASE_SUPPORT	[132]	W/E_P	0h	
Periodic Wake-up	PERIODIC_WAKEUP	[131]	R/W/E	0h	
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	[130]	R	0h	
Reserved		[129:128]			
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	[127:64]	Vendor Specific	-	
Native sector size	NATIVE_SECTOR_SIZE	[63]	R	1h	0x01 : Native sector size is 4KB
Sector size emulation	USE_NATIVE_SECTOR	[62]	R/W	0h	
Sector size	DATA_SECTOR_SIZE	[61]	R	0h	0x00 : Data sector size is 512KB
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	[60]	R	ah	
Class 6 commands control	Class6_CTRL	[59]	R/W/E_P	0h	
Number of addressed group to be Released	DYNCAP_NEEDED	[58]	R	0h	
Exception events control	EXCEPTION_EVENTS_CTRL	[57:56]	R/W/E_P	0h	

Name	Field	CSD Slice	Cell Type	EXT_CSD Value	Remark
Exception events status	EXCEPTION_EVENTS_STATUS	[55:54]	R	0h	
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	[53:52]	R/W	0h	
Context configuration	CONTEXT_CONF	[51:37]	R/W/E_P	0h	
Packed command status	PACKED_COMMAND_STATUS	[36]	R	0h	
Packed command failure index	PACKED_FAILURE_INDEX	[35]	R	0h	
Power Off Notification	POWER_OFF_NOTIFICATION	[34]	R/W/E_P	0h	Defualt = 0h, Updated in run time
Control to turn the Cache ON/OFF	CACHE_CTRL	[33]	R/W/E_P	0h	
Flushing of the cache	FLUSH_CACHE	[32]	W/E_P	0h	
Reserved		[31:0]	TBD		
Mode config	MODE_CONFIG	[30]	R/W/E_P	0h	
Mode operation codes	MODE_OPERATION_CODES	[29]	W/E_P	0h	
Reserved		[28:27]			
FFU status	FFU_STATUS	[26]	R	0h	
Pre loading data size	PRE_LOADING_DATA_SIZE	[25:22]	R/W/E_P	0h	
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	[21:18]	R	TBD	
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	[17]	R/W/E & R	1	
Secure Removal Type	SECURE_REMOVAL_TYPE	[16]	R/W & R	3bh	
Reserved		[15:0]			

- NOTE 1. Reserved bits should read as "0"
- NOTE 2. Obsolete values should be don't care

7.5 RCA (Relative Card Address)

The writable 16-bit relative card address (RCA) register carries the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

7.6 DSR (Driver Stage Register)

The 16-bit driver stage register (DSR) is described in detail in Section 10.2. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

8. Connection Guide

Figure 20: Connection Guide Drawing

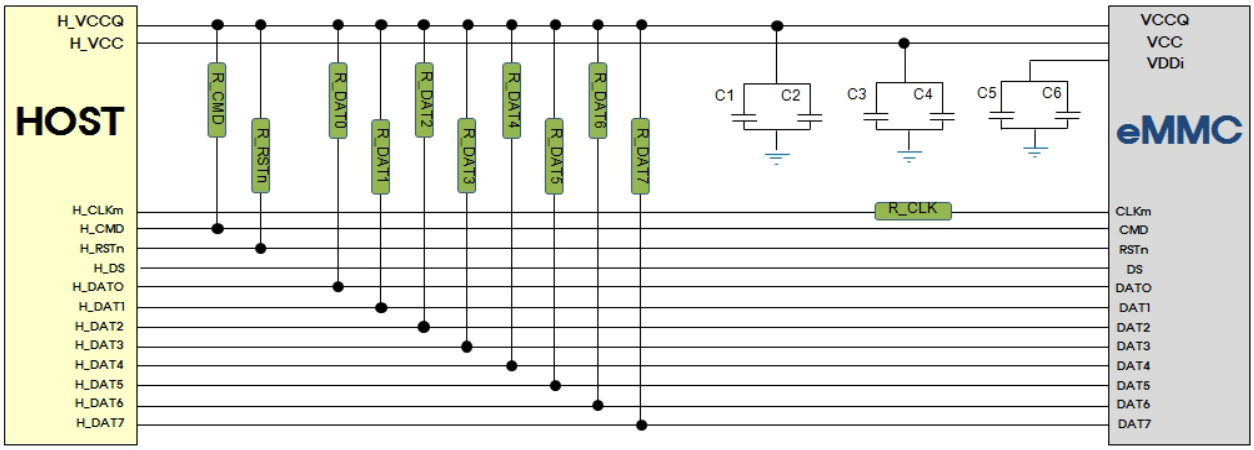


Table 33: Connection Guide Specification

Parameter	Symbol	Min	Max	Recommend	Unit	Remark
Pull-up resistance for CMD	R_CMD	4.7	100	10	kohm	Pull-up resistance should be put on CMD line to prevent bus floating.
Pull-up resistance for DAT0~7	R_DAT	10	100	50	kohm	Pull-up resistance should be put on DAT line to prevent bus floating.
Data strobe(DS)	R_DS	NC	NC	NC	-	It is not necessary to put pull-up/pull-down resistance on DS line since DS is internally pulled down. Direct connection to host is required and please float this pin if it is not used
Pull-up resistance for RSTn	R_RSTn	10	100	50	kohm	It is not necessary to put pull-up resistance on RSTn line if host does not use H/W reset. (Extended CSD register [162] = 0b)
Serial resistance on CLKm	R_RSTn	0	30	27	ohm	To reduce overshooting/undershooting and ringing. **Note: If the host uses HS200, we recommend to remove this resister for better CLK signal**
V_{CCQ} Capacitor value	C1 & C2	2±0.22	4.7	2.2±0.22	uF	Coupling cap should be connected with VCCQ and VssQm as closely possible.
V_{CC} Capacitor value(≤8GB)	C3 & C4	4.72±10%	10	4.7±10%	uF	Coupling cap should be connected with Vcc and Vssm as closely possible. Vcc / Vccq cap. value would be up to Host requirment and the application system characteristics.
V_{CC} Capacitor value(>8GB)						
VDDi capacitor value	C5 & C6	0	2.2	0.1	uF	Coupling cap should be connected with VDDi and Vssm as closely possible. (Internal Cap : 1uF)