DDR5 SDRAM SODIMM Addendum

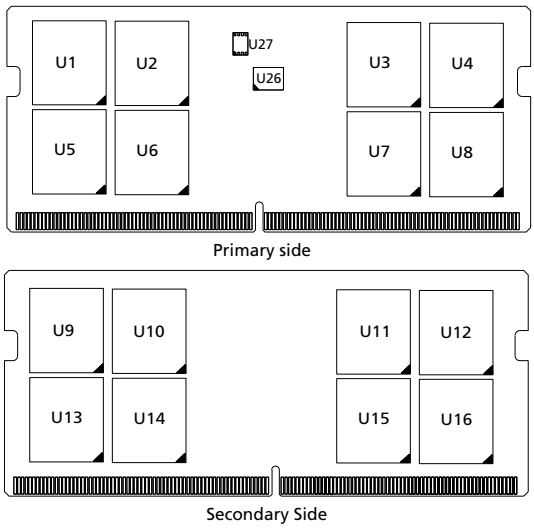
MTC16C2085S1SC – 32GB
16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 SODIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 SODIMM core data sheet
- 262-pin, DDR5 small outline dual in-line memory module (DDR5 SODIMM)
- Fast data transfer rate: PC5-4800
- 32GB (4Gig x 64)
- Dual-rank
- 32 internal banks; 8 groups of 4 banks each

Figure 1: 262-Pin DDR5 SODIMM (R/C-B0)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	C
• Frequency/CAS latency	
– 0.416ns @ CL = 40 (DDR5-4800)	48B

Table 1: Addressing

Parameter	32GB
Row address[1]	64K (R0-R15)
Column address[1]	1K (C0-C9)
Device bank group address[1]	8 (BG0-BG2)
Device bank address per bank group[1]	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	2 (CS0_n, CS1_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT60B2G8,[1] 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL\text{-}_nRCD\text{-}_nRP$)
MTC16C2085S1SC48BA1	32GB	4Gb x 64	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. The data sheet for the base device can be found on micron.com.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	11A	38	U2	0	27A	80
	1	8A	31		1	24A	73
	2	10A	35		2	26A	77
	3	9A	34		3	25A	76
	4	15A	50		4	31A	92
	5	12A	45		5	28A	87
	6	14A	49		6	30A	91
	7	13A	46		7	29A	88
U3	0	3B	184	U4	0	19B	226
	1	0B	179		1	16B	221
	2	2B	183		2	18B	225
	3	1B	180		3	17B	222
	4	7B	198		4	23B	240
	5	4B	191		5	20B	233
	6	6B	195		6	22B	237
	7	5B	194		7	21B	236
U5	0	3A	16	U6	0	19A	58
	1	0A	11		1	16A	53
	2	2A	15		2	18A	57
	3	1A	12		3	17A	54
	4	7A	30		4	23A	72
	5	4A	23		5	20A	65
	6	6A	27		6	22A	69
	7	5A	26		7	21A	68
U7	0	15B	218	U8	0	31B	260
	1	12B	213		1	28B	255
	2	14B	217		2	30B	259
	3	13B	214		3	29B	256
	4	11B	206		4	27B	248
	5	8B	199		5	24B	241
	6	10B	203		6	26B	245
	7	9B	202		7	25B	244

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U9	0	16B	221	U10	0	0B	179
	1	19B	226		1	3B	184
	2	17B	222		2	1B	180
	3	18B	225		3	2B	183
	4	20B	233		4	4B	191
	5	23B	240		5	7B	198
	6	21B	236		6	5B	194
	7	22B	237		7	6B	195
U11	0	24A	73	U12	0	8A	31
	1	27A	80		1	11A	38
	2	25A	76		2	9A	34
	3	26A	77		3	10A	35
	4	28A	87		4	12A	45
	5	31A	92		5	15A	50
	6	29A	88		6	13A	46
	7	30A	91		7	14A	49
U13	0	28B	255	U14	0	12B	213
	1	31B	260		1	15B	218
	2	29B	256		2	13B	214
	3	30B	259		3	14B	217
	4	24B	241		4	8B	199
	5	27B	248		5	11B	206
	6	25B	244		6	9B	202
	7	26B	245		7	10B	203
U15	0	16A	53	U16	0	0A	11
	1	19A	58		1	3A	16
	2	17A	54		2	1A	12
	3	18A	57		3	2A	15
	4	20A	65		4	4A	23
	5	23A	72		5	7A	30
	6	21A	68		6	5A	26
	7	22A	69		7	6A	27

I_{DD} Specifications

Table 4: DDR5 I_{DD} Specifications and Conditions – 32GB (Die Revision A)

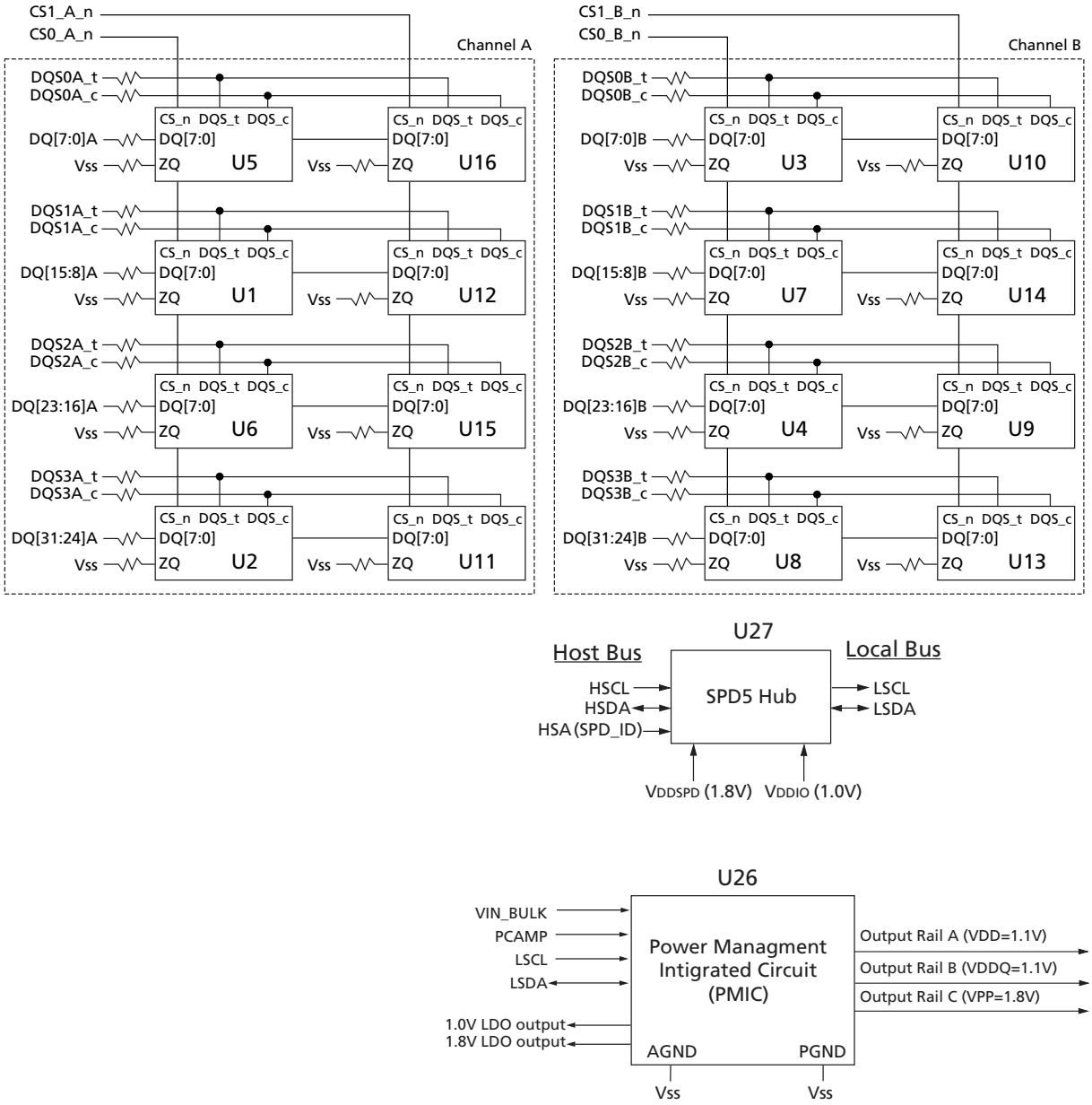
Module I_{DD} is based on PMIC VIN_BULK 5V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	247	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}[1]	328	mA
Precharge standby current	I_{DD2N}[2]	219	mA
Precharge standby non-target command	I_{DD2NT}[1]	370	mA
Precharge power-down current	I_{DD2P}[2]	187	mA
Active standby current	I_{DD3N}[2]	249	mA
Active power-down current	I_{DD3P}[2]	221	mA
Operating burst read current	I_{DD4R}[1]	757	mA
Operating burst write current	I_{DD4W}[1]	993	mA
Operating burst write with write CRC current	I_{DD4WC}[1]	907	mA
Burst refresh (normal refresh mode) current	I_{DD5B}[1]	550	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}[1]	373	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}[1]	290	mA
Self refresh current	I_{DD6N}[2]	119	mA
Operating bank interleave read current	I_{DD7}[1]	825	mA
Maximum power saving deep power down mode current	I_{DD8}[2]	86	mA

Notes: 1. One module rank in this I_{DD}/I_{DDQ}/I_{PP} condition, the other rank in I_{DD2N}/I_{DDQ2N}/I_{PP2N}.
2. Both ranks in this I_{DD}/I_{DDQ}/I_{PP} condition.

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

Revision History

Rev. C – 08/2021

- Production Release

Rev. B – 02/2021

- Preliminary Release

Rev. A – 01/2021

- Preliminary Release

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