16Gb DDR5 SDRAM

Lead-Free&Halogen-Free

(RoHS Compliant)

H5CG44AGBDX018N

H5CG48AGBDX018N

H5CG46AGBDX017N

H5CG44AGBJX018N

H5CG48AGBJX018N

H5CG46AGBJX017N

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Feb. 2022	
0.2	P/N decoder update	Feb. 2022	
0.3	P/N decoder update	May. 2022	
1.0	IDD Specification update	Jul. 2022	

Description

The H5CG44AGBDX018N, H5CG48AGBDX018N, H5CG46AGBDX017N, H5CG44AGBJX018N, H5CG48AGBJX018N, H5CG46AGBJX017N are a 16Gb DDR5 DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. SK hynix 16Gb DDR5 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 16bit prefetched to achieve very high bandwidth.

Device Features and Ordering Information

Features

- DRAM VDD/VDDQ = 1.1V (-33mV / +67mV)
- DRAM VPP = 1.8V (–54mV / +108mV)
- 32 Bank with x4/x8
- 16 Bank with x16
- 8 BG(Bank Group) for X4/X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Temperature Encoding
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Hard/Soft Post Package Repair
- Input Clock Frequency Change
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per Pin VREFDQ Training
- Write Leveling Training Mode
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- Loopback for multiple purposes - monitor data, BER(Bit Error Rate) analysis, etc.
- Package Output Driver Test Mode
- Training Modes:
    - VrefDQ / VrefCA / VrefCS Training
    - Read Training Mode
    - CA Training Mode
    - CS Training Mode
    - Per Pin VREFDQ Training
    - Write Leveling Training Mode
    - Duty Cycle Adjuster (DCA) for Read - Global
    - Per Pin DCA(Duty Cycle Adjuster) for Read - Per Pin(DQ)
- sPPR Do / Undo / Lock
- MBIST / mPPR
- 0.5*CK Write Levling Internal Cycle Alignment
- Partial Array Self Refresh (PASR)
- NOT supported Adaptive Refresh Management (ARFM)
- NOT supported Refresh Interval Rate Indicator
- NOT required RFM

Device Informatiom

1. DDR5 Component Product

1.1 Ordering Information

Part No.	Configuration	Package
H5CG44AGBDX018N	4Gb x 4	82ball FBGA
H5CG44AGBJX018N		
H5CG48AGBDX018N	2Gb x 8	
H5CG48AGBJX018N		
H5CG46AGBDX017N	1Gb x 16	106ball FBGA
H5CG46AGBJX017N		

Note: xxx indicates serial code.

* 16Gb A-die supports all the standard speed bins defined in this datasheet.

1.2 Operating Frequency

MT/s	Grade	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR5-5600	GB	0.357	16.00	16.00	16.00	32.00	48.00	46-45-45

DDR5 SDRAM Component Part Number Decoder

H5X XX X X XX X X XXX

1 2 3 4 5 6 7 8 9 10 11 12 3 4

1-3) Product Mode & Type

H5C	DDR5 Component

4-5) Product Density

G3	8Gb
G4	16Gb
GD	24Gb
G5	32Gb
G6	64Gb

6) Organization

4	X4
8	X8
6	X16

7) Generation

M	1st
A	2nd
B	3rd
C	4th
D	5th
E	6th
J	10th or Special gen.

8-9) Speed

GB	5600 46-45-45
GE	5600 52-45-45 (for 3DS)

10) emperature

D	CT (0~95℃)
J	IT (-40~95℃)

11) Reserved

X	(Reserved for future usage)

12-14) Serial Code

Code	Die Density	Number of Ball	Die Stack	Etc.
012	16Gb	82	2	TSV
013	16Gb	82	4	TSV
014	16Gb	82	1	-
015	16Gb	106	1	-
017	16Gb	106	1	
018	16Gb	82	1	
021	24Gb	82	1	-
022	24Gb	106	1	-
023	16Gb	82	4	TSV
024	16Gb	82	2	TSV

※ Codes can be added, deleted and changed by internal management.

※ This decoder can be used only for understanding SK hynix's part number. It doesn't mean supportability for all kinds of products.

1.3 IDD Specification

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

I_{DD} Specification

Symbol	5600			Unit	NOTE
	x4	x8	x16		
IDD0	62.8	62.8	72	mA	
IDD0F	97	97	133	mA	
IDD2N	51	51	51	mA	
IDD2NT	82.1	82.1	82.1	mA	
IDD2P	43.1	43.1	43.1	mA	
IDD3N	120	120	120	mA	
IDD3P	112	112	112	mA	
IDD4R	238	275.2	375	mA	
IDD4RC	231.8	268	363.4	mA	
IDD4W	270.7	313	406.8	mA	
IDD4WC	263.7	305	392.9	mA	
IDD5B	229	229	229	mA	
IDD5F	214.7	214.7	214.7	mA	
IDD5C	107	107	107	mA	
IDD6E	51.3	51.3	51.3	mA	
IDD7	292	312	450.1	mA	
IDD8	26	26	26	mA	
IDD9	188.4	188.4	188.4	mA	

I_{DDQ} Specification

Symbol	5600			Unit	NOTE
	x4	x8	x16		
IDDQ0	11.2	11.2	11.2	mA	
IDDQ0F	11.2	11.2	11.2	mA	
IDDQ2N	11.2	11.2	11.2	mA	
IDDQ2NT	11.2	11.2	11.2	mA	
IDDQ2P	7.2	7.2	7.2	mA	
IDDQ3N	11.2	11.2	11.2	mA	
IDDQ3P	7.2	7.2	7.2	mA	
IDDQ4R	54.9	77.4	140	mA	
IDDQ4W	49.4	77	137	mA	
IDDQ5B	10.8	10.8	10.8	mA	
IDDQ5F	10.8	10.8	10.8	mA	
IDDQ5C	10.8	10.8	10.8	mA	
IDDQ6E	7	7	7	mA	
IDDQ7	57	78	118	mA	
IDDQ8	7	7	7	mA	
IDDQ9	7	7	7	mA	

I_{PP} Specification

Symbol	5600			Unit	NOTE
	x4	x8	x16		
IPP0	6.9	6.9	9.4	mA	
IPP0F	14	14	26	mA	
IPP2N	4	4	4	mA	
IPP2NT	4	4	4	mA	
IPP2P	3.5	3.5	3.5	mA	
IPP3N	14.9	14.9	14.9	mA	
IPP3P	13.8	13.8	13.8	mA	
IPP4R	18	18	21.8	mA	
IPP4W	20.6	20.6	23.1	mA	
IPP5B	45	45	45	mA	
IPP5F	45	45	45	mA	
IPP5C	45	45	45	mA	
IPP6E	8.5	8.5	8.5	mA	
IPP7	52.8	52.8	73.5	mA	
IPP8	3.5	3.5	3.5	mA	
IPP9	30	30	30	mA	

Note(s):

1. Burst Length: BL16 fixed by MR0 OP[1:0]=00.

2. Output Buffer Enable
   - set MR5 OP[0] = 0] : Qoff = Output buffer enabled
   - set MR5 OP[2:1] = 00] : Pull-Up Output Driver Impedance Control = RZQ/7
   - set MR5 OP[7:6] = 00] : Pull-Down Output Driver Impedance Control = RZQ/7

   RTT_Nom enable
   - set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6
   RTT_WR enable
   - set MR34 OP[5:3] = 010 RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR34 OP[2:0] = 000

3. WRITE CRC enabled
   - set MR50 OP[2:1] = 11

DDR5 Specification

2 DDR5 SDRAM Package, Pinout Description and Addressing

2.1 DDR5 SDRAM Row for X4, X8

The DDR5 SDRAM x4/x8 component shall have 13 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. There may be additional rows of inactive balls for mechanical support.

2.2 DDR5 SDRAM Ball Pitch

The DDR5 SDRAM component shall use a ball pitch of 0.8mm by 0.8mm.
The number of fully depopulated columns is 3.

2.3 DDR5 SDRAM Columns for X4, X8

The DDR5 SDRAM x4/x8 component shall have 6 electrical columns of balls in 2 sets of 3 columns.
There shall be columns between the electrical columns where there are no balls populated. The number of these is 3.
Electrical is defined as columns that contain signal ball or power/ground balls. There may be additional columns of inactive balls for mechanical support.

2.4 DDR5 SDRAM X4/8 Ballout using MO-210

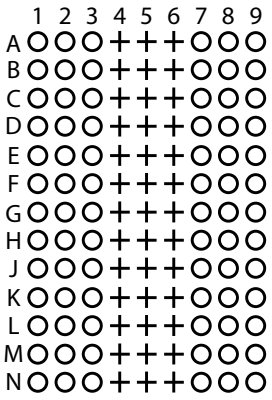
AN	1	2	3	4	5	6	7	8	9	10	11	
AL		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD		B
C		VSS	DQ0	DQS_t				DM_n, TDQS_t	DQ1	VSS		C
D		VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ		D
E		VDD	DQ4	DQ6				DQ7	DQ5	VDD		E
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS		F
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		G
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		H
J		VDDQ	CA4	CA0				CA1	CA5	VDDQ		J
K		VDD	CA6	CA2				CA3	CA7	VDD		K
L		VDDQ	VSS	CA8				CA9	VSS	VDDQ		L
M		CAI	CA10	CA12				CA13	CA11	RESET_n		M
N	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	N

Note(s):
1 - DQ4-DQ7 are higher order DQ pins and are not connected for the x4 configuration.
2 - TDQS_t is not valid for the x4 configuration

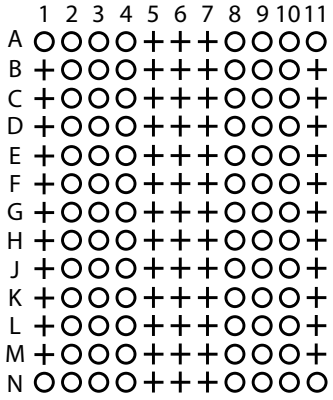
3 - TDQS_c is not available for the x4 configuration4 - DM_n not valid for the x4 configuration

Figure 1 — DDR5 Ball Assignments for the x4/8 component

MO-210-AL (x4/x8)



MO-210-AN (x4/x8) with support balls



○ **Populated ball**
＋ **Ball not populated**

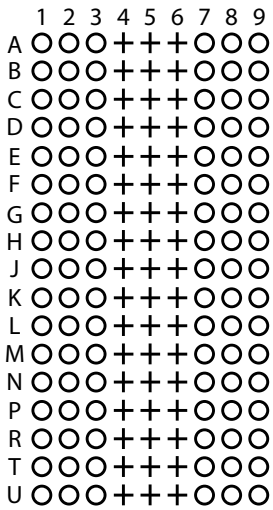
Note(s):
1. Additional columns and rows of inactive balls in MO-210 Terminal Pattern AN (x4/x8) with support balls are for mechanical support only, and should not be tied to either electrically high or low.
2. Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

2.5 DDR5 SDRAM X16 Ballout using MO-210

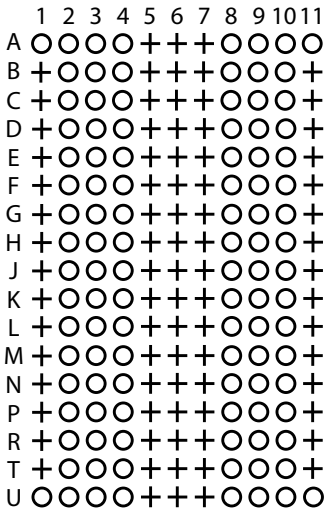
AU	1	2	3	4	5	6	7	8	9	10	11	
AT		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQU2				DQU3	VDDQ	VDD		B
C		VSS	DQU0	DQSU_t				DMU_n	DQU1	VSS		C
D		VDDQ	VSS	DQSU_c				RFU	VSS	VDDQ		D
E		VDD	DQU4	DQU6				DQU7	DQU5	VDD		E
F		VDD	VDDQ	DQL2				DQL3	VDDQ	VDD		F
G		VSS	DQL0	DQSL_t				DML_n	DQL1	VSS		G
H		VDDQ	VSS	DQSL_c				RFU	VSS	VDDQ		H
J		VDD	DQL4	DQL6				DQL7	DQL5	VDD		J
K		VSS	VDDQ	VSS				VSS	VDDQ	VSS		K
L		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		L
M		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		M
N		VDDQ	CA4	CA0				CA1	CA5	VDDQ		N
P		VDD	CA6	CA2				CA3	CA7	VDD		P
R		VDDQ	VSS	CA8				CA9	VSS	VDDQ		R
T		CAI	CA10	CA12				CA13	CA11	RESET_n		T
U	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	U

Figure 2 — DDR5 Ball Assignments for the x16 component

MO-210-AT (x16)



MO-210-AU (x16) with support balls



○ **Populated ball**
\+ **Ball not populated**

Note(s):
1. Additional columns and rows of inactive balls in MO-210 Terminal Pattern AU (x16) with support balls are for mechanical support only, and should not be tied to either electrically high or low.
2. Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DM_n, DMU_n, DML_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
CA [13:0]	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DDQ},
DQ	Input / Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via MR5:OP[4]=1, the DRAM shall enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t shall provide the data mask function depending on MR5:OP[5]; TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via MR5:OP[4]=0.
ALERT_n	Input/Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to V_{DDQ} on board.
TEN	Input	Connectivity Test Mode Enable: Required on x4, x8 & x16 devices. HIGH in this pin shall enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of V_{DDQ}. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
MIR	Input	Mirror: Used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected (strapped) to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSS if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note that the CA[13] function is only relevant for certain densities (including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected (Strapped) to VDDQ. No active signaling requirements defined.
CAI	Input	Command & Address Inversion: With the CAI pin connected (strapped) to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSS if no CA inversion is required. No active signaling requirements defined.
CA_ODT	Input	ODT for Command and Address. Apply Group A settings if the pin is connected (strapped) to VSS and apply Group B settings if the pin is connected (strapped) to V_{DDQ}. No active signalling requirements defined.
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].

Symbol	Type	Function
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V
VDD	Supply	Power Supply: 1.1 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8V
ZQ	Reference	Reference Pin for ZQ calibration. This ball is tied to an external 240 ohm resistor(RZQ), which is tied to V_{SS}.
NOTES:		

2.7 DDR5 SDRAM Addressing

Table 1 — 8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0	BA0	BA0
	# BG / # Banks per BG / # Banks	8 / 2 / 16	8 / 2 / 16	4 / 2 / 8
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 2 — 16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 3 — 24 Gb Addressing Table

Configuration		6 Gb x4	3 Gb x8	1.5 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R16	R0~ R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Note 1 For non-binary memory densities, a quarter of the row address space is invalid. When the MSB address bit is “HIGH”, the MSB-1 address bit shall be “LOW”.

Table 4 — 32 Gb Addressing Table

Configuration		8 Gb x4	4 Gb x8	2 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R16	R0~R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

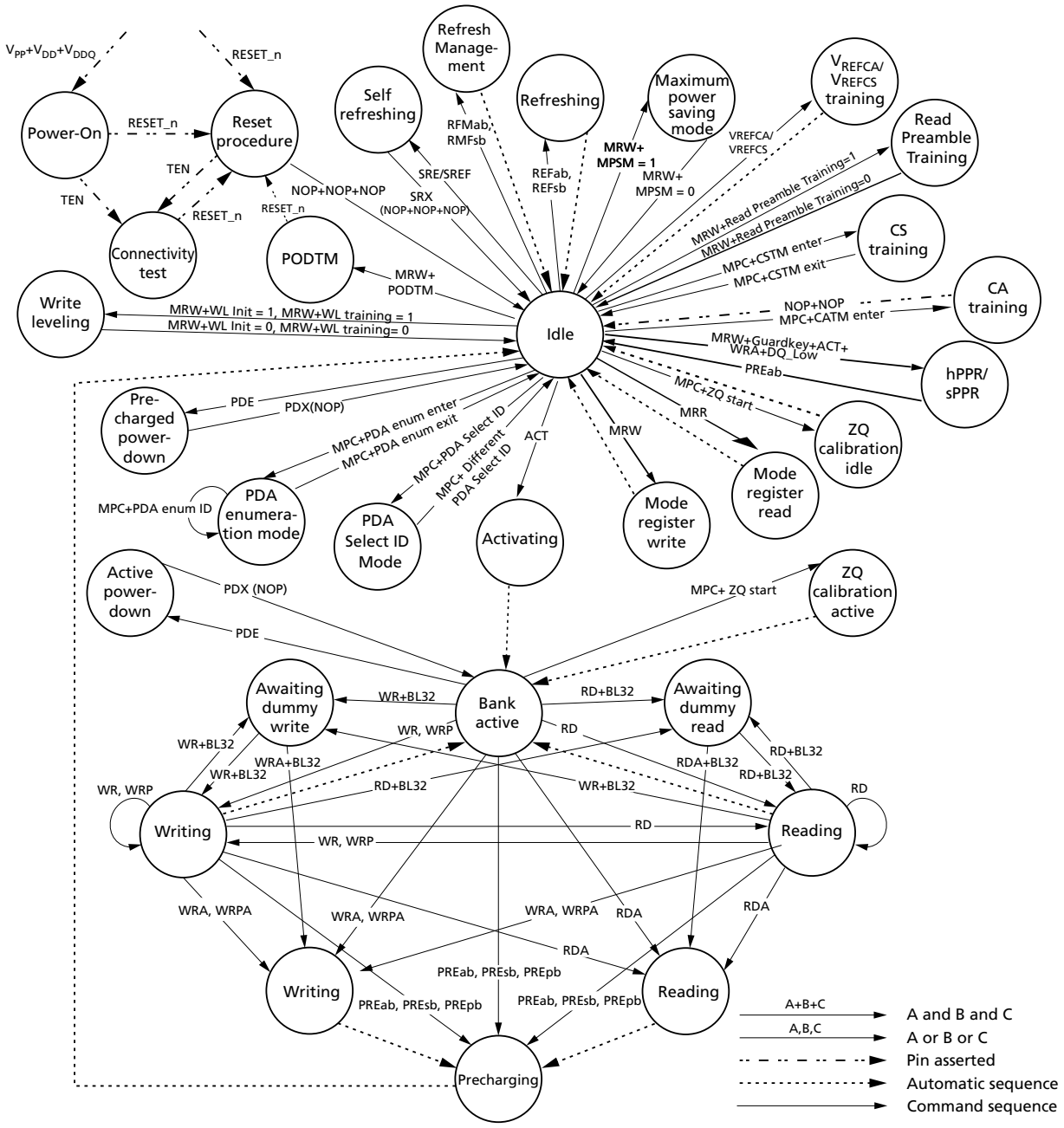
Table 5 — 64 Gb Addressing Table

Configuration		16 Gb x4	8 Gb x8	4 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R17	R0~R17	R0~R17
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~2 / 8H	CID0~2 / 8H	CID0~2 / 8H

3 Functional Description

3.1 Simplified State Diagram

This Simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.



3.2 Basic Functionality

The DDR5 SDRAM is a high-speed dynamic random-access memory. To ease transition from DDR4 to DDR5, the introductory density (8Gb) shall be internally configured as 16-bank, 8 bank group with 2 banks for each bank group for x4/x8 and 8-bank, 4 bank group with 2 banks for each bankgroup for x16 DRAM. When the industry transitions to higher densities (=>16Gb), it doubles the bank resources and internally be configured as 32-bank, 8 bank group with 4 banks for each bank group for x4/x8 and 16-bank, 4 bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR5 SDRAM uses a 16n prefetch architecture to achieve high-speed operation. The 16n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR5 SDRAM consists of a single 16n-bit wide, eight clock data transfer at the internal DRAM core and sixteen corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR5 SDRAM are burst oriented, start at a selected location, and continue for a burst length of sixteen or a 'chopped' burst of eight in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered with the ACTIVATE Command are used to select the bank and row to be activated (i.e. in a 16Gb part, BG0-BG2 in a x4/8 and BG0-BG1 in x16 select the bankgroup; BA0-BA1 select the bank; R0-R17 select the row; refer to "DDR5 SDRAM Addressing" for specific requirements). The address bits registered with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (CA10=L), and select BC8 on-the-fly (OTF), fixed BL16, fixed BL32 (optional), or BL32 OTF (optional) mode if enabled in the mode register.

Prior to normal operation, the DDR5 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

3.3 RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings need to be defined.

Table 6 — MR default settings

Item	Mode Register	Default Setting	Description
Burst Length	MR0 OP[1:0]	00_B	BL16
Read Latency	MR0 OP[6:2]	00010_B	RL(CL) = 26 @3200
Write Latency	n/a	WL=RL-2 (CWL=CL-2)	Fixed based on RL (CL)
Write Recovery (tWR)	MR6 OP[3:0]	0000_B	WR = 48nCK @3200 or 30ns
Read to Precharge Delay (tRTP)	MR6 OP[7:4]	0000_B	tRTP=12nCK @3200 or 7.5ns
VrefDQ Value	MR10	$0010\ 1101_B$	VREF(DQ) Range: 75% of V_{DDQ}
VrefCA Value	MR11	$0010\ 1101_B$	VREF(CA) Range: 75% of V_{DDQ}
VrefCS Value	MR12	0010 1101B	VREF(CS) Range: 75% of VDDQ
ECS Error Threshold Count (ETC)	MR15	011B	256
Post Package Repair	MR23 OP[1:0]	00B	hPPR & sPPR Disabled
CK ODT	MR32 OP[2:0]	CK ODT is based on strap value	Group A= RTT_OFF=000B Group B= 40 Ohms=111B
CS ODT	MR32 OP[5:3]	CS ODT is based on strap value	Group A= RTT_OFF=000B Group B= 40 Ohms=111B
CA ODT	MR33 OP[2:0]	CA ODT is based on strap value	Group A= RTT_OFF=000B Group B= 80 Ohms=100B
DQS_RTT_PARK	MR33 OP[5:3]	000B	RTT OFF
RTT_PARK	MR34 OP[2:0]	000B	RTT OFF
RTT_WR	MR34 OP[5:3]	001B	240 Ohm
RTT_NOM_WR	MR35 OP[2:0]	011B	80 Ohm
RTT_NOM_RD	MR35 OP[5:3]	011B	80 Ohm
RTT Loopback	MR36 OP[2:0]	000B	RTT OFF
RFM RAAIMT	MR58 OP[4:1]	vendor specific	vendor specific
RFM RAAMMT	MR58 OP[7:5]	vendor specific	vendor specific
RFM RAA Counter	MR59 OP[7:6]	vendor specific	vendor specific

3.3.1 Power-up Initialization Sequence

The following sequence shall be used to power up the DDR5 device. Unless specified otherwise, these steps are mandatory.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x VDDQ) and all other inputs may be undefined. The device outputs remain disabled while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 2. VPP must ramp at the same time or earlier than VDD.

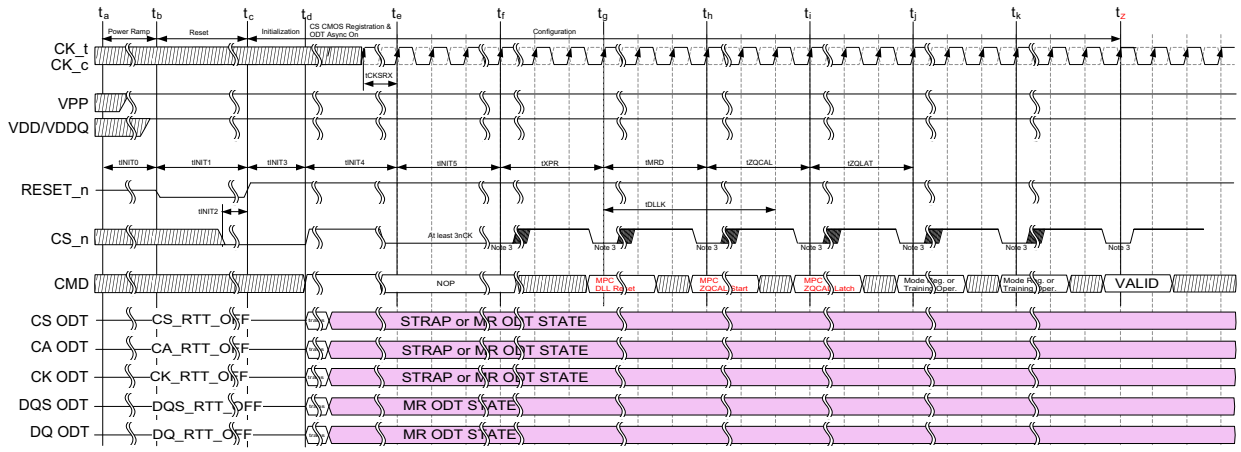
Table 7 — Voltage Ramp Conditions

After	Application Conditions
Ta is reached	VPP must be greater than VDD - TBD mV

Note:
1) Ta is the point when any power supply first reaches 300mV
2) Voltage ramp conditions in the table above apply between (Ta) and Power-off (controlled or uncontrolled).
3) Tb is the point at which all supply and reference voltages are within their defined ranges.
4) Power ramp duration (Tb-Ta) must not exceed tINIT0.

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DQS_t, DQS_c, voltage levels must be between VSS and VDDQ to avoid latch-up. CS_n, CK_t, CK_c and CA input levels must be between VSS and VDDQ to avoid latch-up.

3. Beginning at Tb, RESET_n must be maintained LOW for a minimum of tINIT1 (Tb to Tc), after which RESET_n may be deasserted to HIGH (Tc). At least tINIT2 before RESET_n de-assertion, CS_n is required to be set LOW. All other input signals are “Don’t Care”. The DRAM shall support the ability for RESET_n to be held indefinitely.



Note(s):
1. From time point (Td) until (Te), the command bus must be held high.
2. From time point (Te) until (Tf), NOP commands must be applied on the command bus.
3. From time point (Tf) until (Tz), DES commands must be applied between legal commands (MRR/MRW/MPC & VREFCA).
4. MRW Commands must be issued to all Mode Registers that require defined settings.
5. Default ODT tolerances are wider prior to ZQ calibration.
6. Prior to ZQcal completion (Tj), MPC commands shall be multi-cycle as described in the MPC command Timings section.

Figure 3 — RESET_n and Initialization Sequence at Power-on Ramping

4. After RESET_n is de-asserted (Tc), wait at least tINIT3 before driving CS_n high.

5. After setting CS_n high (Td), wait a minimum of tINIT4 to allow the DRAM CMOS based receiver to register the exit and allow the CS_n, CK, CA, DQ and DQS ODT to go to the defined strap or MRS state (Te). Clock (CK_t, CK_c) is required to be started and stabilized for tCKSRX before exit of tINIT4 (Te). Upon the completion of Te, all ODT states (CA, CS_n, CK, DQ and DQS ODT) should be valid and the DRAM's CS_n receiver should no longer be in its CMOS based mode. ODT termination states will be uncalibrated until completion of ZQcal at (Tj)

6. Upon Te, NOP commands must be issued for a minimum of tINIT5 to conclude exit of initialization process and start tXPR timer at (Tf). The system must wait at least tXPR before issuing any legal configuration commands (Tg). During configuration, only MRR, MRW, MPC and VREFCA commands are legal.

7. Between (Tg to Tj), the following initial configuration modes must be completed prior to other training modes:
   - MPC for setting MR13 (tCCD/tDLLK) must be issued before the MPC command to reset the DLL.
   - MPC to execute DLL RESET must be issued before ZQCal Start
   - MPC to execute ZQCal Start and ZQCal Latch must be issued before any other training modes such as CS Training

8. Between (Tj to Tz), any number of legal configuration commands are allowed. Training based commands are optional and may be done at the system architect's discretion and may vary depending on the systems, though proper setting of certain registers, such as those related to Write Leveling Training, is required.

9. After (Tz), and the completion of any training or calibration timing parameters (i.e. tZQLAT is satisfied), the DDR5 device is ready for normal operation and is able to accept any valid command. Any additional mode registers that have not previously been set up for normal operation should be written at this time. If host use writeback suppression mode, it should be set after the initial write process to prevent aliasing to 2-bit errors.

10. After all mode registers have been programmed for normal operation, optional MBIST mode can be entered by writing MR23:OP[4] to HIGH, followed by subsequent MR24 PPR guard keys, then DRAM will drive ALERT_N to LOW for a maximum of tSELFTEST time. DRAM will drive ALERT_N to HIGH to indicate that this operation is completed. After ALERT_N is driven high, the DRAM is immediately ready to receive valid commands. The MBIST/mPPR transparency status must subsequently be checked in MR22:OP[2:0] in order to determine whether mPPR should be performed. Please refer to Ch. 4.30 MBIST/mPPR for more detailed operation procedures.

Table 8 — Initialization Timing Parameters

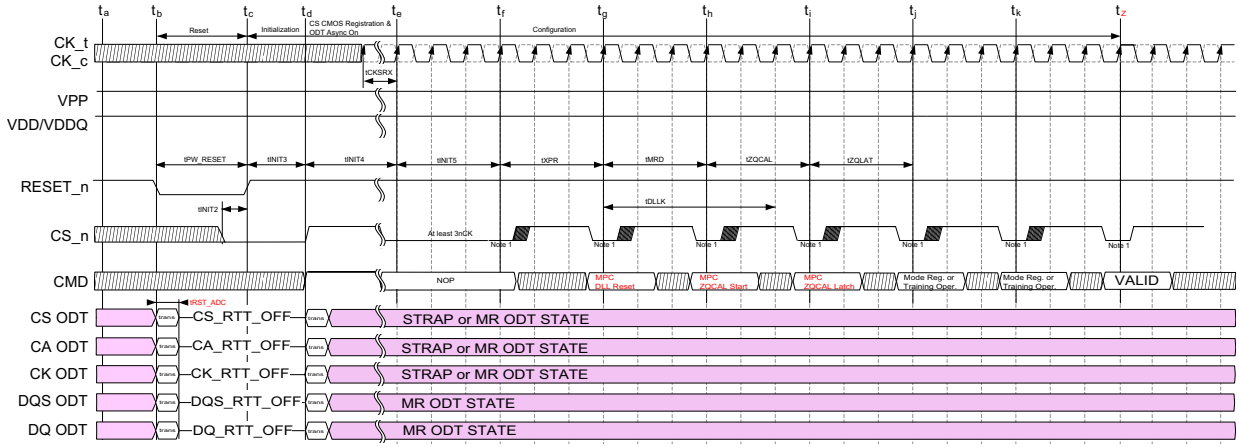
Parameter	Symbol	Value		Units	Note(s)
		MIN	MAX		
Maximum voltage-ramp time	tINIT0	-	20	ms	
Minimum RESET_n LOW time after completion of voltage ramp	tINIT1	200		us	
Minimum CS_n LOW time before RESET_n HIGH	tINIT2	10	-	ns	
Minimum CS_n LOW time after RESET_n HIGH	tINIT3	4	-	ms	
Minimum time for DRAM to register EXIT on CS_n with CMOS.	tINIT4	2	-	us	
Minimum cycles required after CS_n HIGH	tINIT5	3	-	*n*CK	1
Minimum time from Exit Reset to first valid Configuration Command	tXPR	tXS	-	ns	
Minimum stable clock time	tCKSRX	SEE Self Refresh Timing Table			

Note(s):
1 - Min number of NOP commands issued after CS_n High (tINIT4).

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization as shown in Figure 4.

1. Assert RESET_n below 0.2 x VDDQ anytime when reset is needed. RESET_n needs to be maintained for a minimum of tPW_RESET. CS_n must be pulled LOW at least tINIT2 before de-asserting RESET_n.
2. Repeat steps 4 to 9 in Section 3.3.1



Note(s):
1. From time point (Td) until (Te), the command bus must be held high.
2. From time point (Te) until (Tf), NOP commands must be applied on the command bus.
3. From time point (Tf) until (Tz), DES commands must be applied between legal commands (MRR/MRW/MPC & VREFCA).
4. MRW Commands must be issued to all Mode Registers that require defined settings.

Figure 4 — Reset Procedure at Power Stable

Table 9 — Reset Timing Parameters

Parameter	Symbol	Value		Units	Note(s)
		MIN	MAX		
Minimum RESET_n low time for Reset Initialization with stable power	tPW_RESET	1	-	uS	
Maximum time after RESET_n assertion to ODT off	tRST_ADC	-	50	nS	

Note(s):

3.3.3 Input Voltage Power-up and Power-Down Sequence

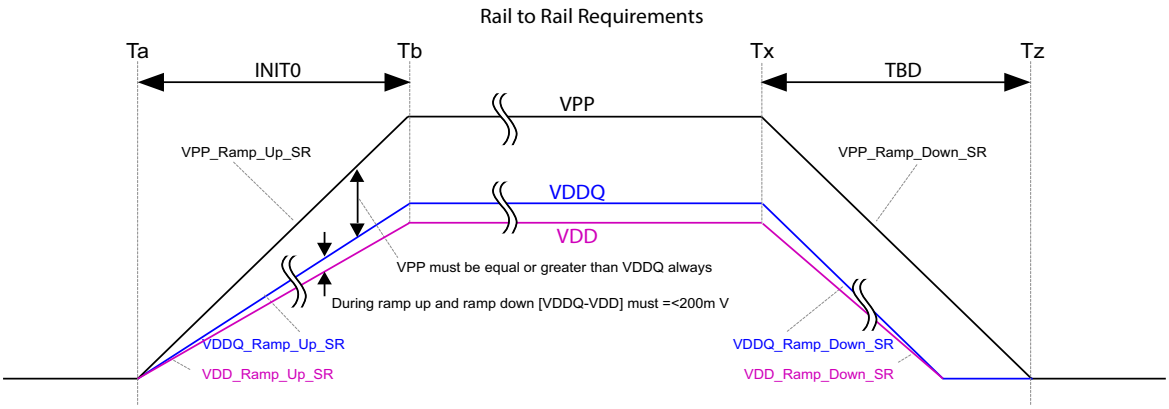


Figure 5 — Requirement for Voltage Ramp Control

Table 10 — Input Voltage Slew Rates

Description	Symbol	Min	Max	Units	Notes
VPP Rail	VPP_Ramp_Up_SR	0.2	5	V/ms	1,2,3,4,5
	VPP_Ramp_Down_SR	0.1	4.5	V/ms	
VDD Rail	VDD_Ramp_Up_SR	0.1	4.5	V/ms	
	VDD_Ramp_Down_SR	0.1	4.5	V/ms	
VDDQ Rail	VDDQ_Ramp_Up_SR	0.1	4.5	V/ms	
	VDDQ_Ramp_Down_SR	0.1	4.5	V/ms	

Note(s):
1. Both VDD and VPP supply measurements made between 10% & 90% nominal voltage
2. 1Mhz bandwidth limited measurement
3. VPP must be equal to or greater than VDD/VDDQ at all times.
4. During ramp up and ramp down [VDDQ-VDD] must be equal or less than 200mV.
5. After tINIT0, all supplies must be within their specified tolerance, as defined in the DC Operating Tables.

3.4 Mode Register Definition

3.4.1 Mode Register Read (MRR)

The Mode Register Read (MRR) command is used to read configuration and status data from the DDR5-SDRAM registers. The MRR command is initiated with CS_n and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[7:0]) allow the user to select one of 256 registers. The mode register contents are available on the second 8 UI's of the burst and are repeated across all DQ's after the RL following the MRR command. To avoid a potentially worst-case pattern, every odd DQ bit (represented with !) shall have its contents inverted. Data in the burst (BL0-7) shall be either "0" or "1", with "1" indicating that the content of the later UI's (BL8-15) are inverted.

DQS is toggled for the duration of the MRR burst. The MRR has a command burst length 16 regardless of the MR0 setting, the training mode or the mode register address. MRR termination control and ODT timings are the same as for the READ command. The MRR operation must not be interrupted. Non-Target ODT encoding is available for MRR, just like a normal READ. NT ODT MRR termination control and ODT timings are the same as for the READ NT command.

In the case that CRC is enabled, MRR's output will come with BL18 (BL16 plus 2 CRC-bit), but the host has the option to consider the 17th and 18th bits "don't care" for MRR handling. Regardless on if the host uses the 17th and 18th bits, while CRC is enabled, the strobe needs to toggle for BL18.

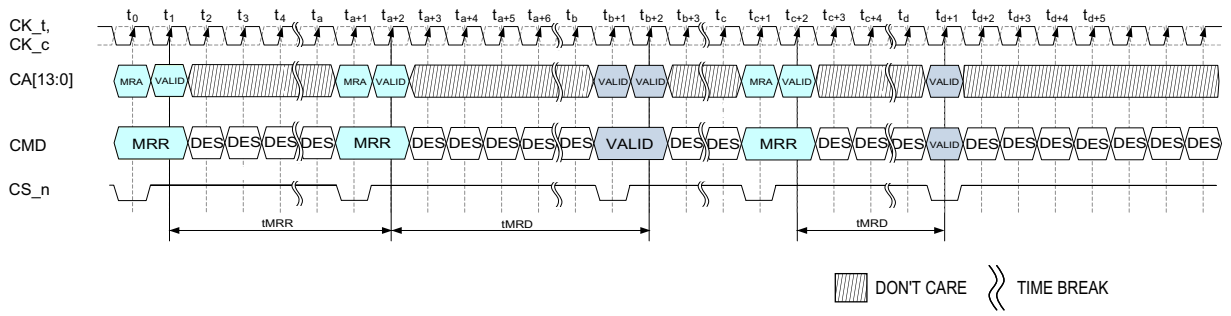


Figure 6 — Mode Register Read Timing

Table 11 — DQ output mapping for x4 device

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Notes:
1. The read pre-amble and post-amble of MRR are same as normal read.

Table 12 — DQ output mapping for x8 device

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Notes:
1. The read pre-amble and post-amble of MRR are same as normal read.

Table 13 — DQ output mapping for x16 device (OSC Count - MR46 & MR47 only)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Notes:
1. The read pre-amble and post-amble of MRR are same as normal read.
2. Output map excludes per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

Table 14 — DQ output mapping for x16 device (DFE REGISTERS EXCLUDED)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don’t Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									

Notes:
1. The read pre-amble and post-amble of MRR are same as normal read.
2. Output of mode register data is only duplicated and inverted across the first 8 bits of a x16 device.
3. Output map excludes per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

Table 15 — DQ output mapping for x16 device (DFE Lower Byte - DQ[0:7], DML)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don’t Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									

Notes:
1. The read pre-amble and post-amble of MRR are same as normal read.
2. Output of mode register data is only duplicated and inverted across the first 8 bits of a x16 device when reading from a DFE register associated with a lower byte DQ or DML.
3. Output map is ONLY for per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

Table 16 — DQ output mapping for x16 device (DFE Upper Byte - DQ[15:8], DMU)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	Don’t Care								
DQ1									
DQ2									
DQ3									
DQ4									
DQ5									
DQ6									
DQ7									
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Note(s):
1. The read pre-amble and post-amble of MRR are same as normal read.
2. Output of mode register data is only duplicated and inverted across the last 8 bits of a x16 device when reading from a DFE register associated with an upper byte DQ or DMU.
3. Output map is ONLY for per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

3.4.2 Mode Register WRITE (MRW)

The Mode Register Write (MRW) command is used to write configuration data to the mode registers.
The MRW command is initiated with CS_n and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address and the data written to the mode registers is contained in CA[13:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode register Writes to read-only registers have no impact on the functionality of the device.

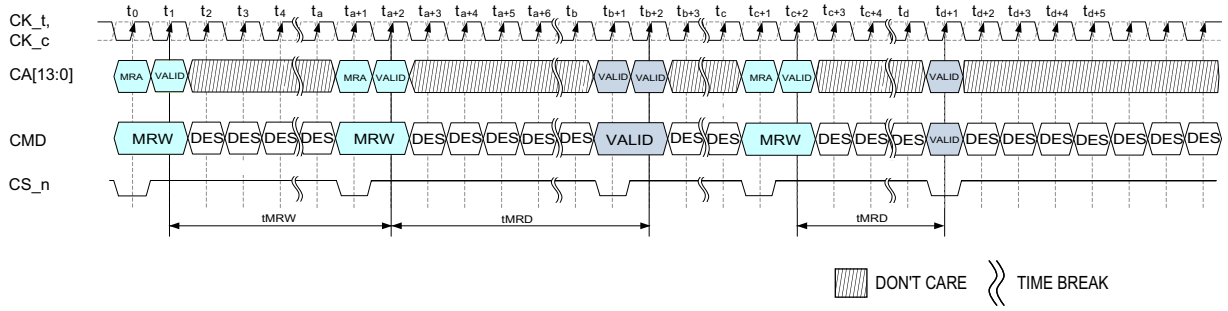


Figure 7 — Mode Register Write Timing

3.4.3 DFE Mode Register Write Update Timing

This Mode Register update timing parameter applies for MR112 (MA[7:0]=70H) thru MR248 (MA[7:0]=F8H) - Mode Registers for DFE including DFE Gain Bias, DFE Tap-1, DFE Tap-2, DFE Tap-3, DFE Tap-4 mode registers

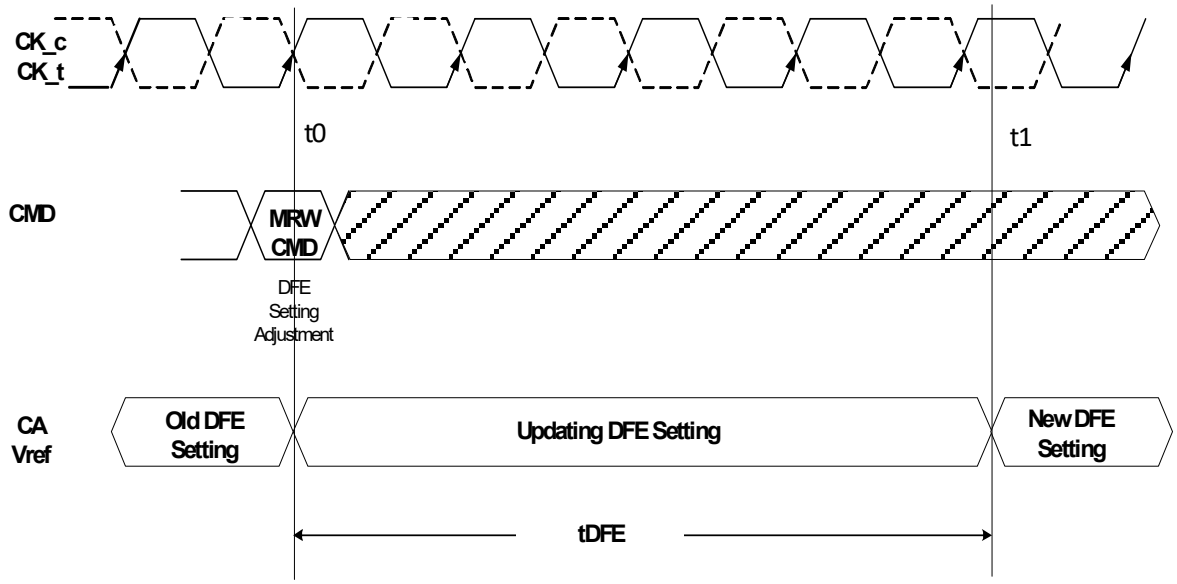


Figure 8 — DFE Update Setting

3.4.4 Mode Register Truth Tables and Timing Constraints

Table 17 — Mode Register Read/Write AC timing

Parameter	Symbol	Min/Max	Value	Unit	Note
Mode Register Read command period	tMRR	Min	max(14ns, 16nCK)	nCK	1
Mode Register Read Pattern to Mode Register Read Pattern Command spacing	tMRR_p	Min	8	nCK	
Mode Register Write command period	tMRW	Min	max(5ns, 8nCK)	nCK	1
Mode Register Set command delay	tMRD	Min	max(14ns, 16nCK)	nCK	
DFE Mode Register Write Update Delay Time	tDFE	Min	80	ns	2

Note(s):
1 - MRR and MRW commands are not allowed with pages open.
2 - This parameter applies only to MRW's to DFE registers and is defined as the settling time before a new DFE setting is active.

Table 18 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
SDRAM		SDRAM	SDRAM
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle

Table 19 — MRR/MRW Timing Constraints: DQ ODT is Disable

From Command	To Command	Minimum Delay between “From Command” and “To Command”	Unit	Note
MRR	MRR	tMRR	-	2
	MRW	CL+BL/2+1	tCK	2
	MPC	CL+BL/2+1	tCK	2
	VrefCA	CL+BL/2+1	tCK	2
	Any other valid command	tMRD	-	1,2
MRW	MRW	tMRW	-	
	Any other valid command	tMRD	-	
			-	
			-	
PRE	MRR	tRP	-	
	MRW	tRP	-	
REF	MRR	tRFC	-	
	MRW	tRFC	-	

Note(s):
1. All data should be completed before entry into self refresh or power down.
2. MRR can refer to both Target ODT MRR and Non-Target ODT MRR

Table 20 — MRR/MRW Timing Constraints: DQ ODT is Enable

From Command	To Command	Minimum Delay between “From Command” and “To Command”	Unit	Note
MRR	MRR	Same as ODT Disable Case	-	
	MRW		-	
	MPC		-	
	VrefCA		-	
	Any other valid command		-	
			-	
			-	
MRW	MRW		-	
	Any other valid command		-	
			-	
			-	
PRE	MRR		-	
	MRW		-	
REF	MRR		-	
	MRW		-	

3.5 Mode Registers

With DDR5, the utilization and programming method shall change from the traditional addressing scheme found in DDR3 and DDR4, and shall move to the method used by LPDDR, where the Mode Register Addresses (MRA) and Payload placed in Op Codes (OP) are all packeted in the command bus encoding method. Please refer to the Command Truth Table 27 for Mode Register Read (MRR) and Mode Register Write (MRW) command protocol.

For DDR5, the SDRAM shall support up to 8 MRA's, each with a byte-wide payload. Allowing for up to 256 byte-wide registers.

3.5.1 Mode Register Assignment and Definition in DDR5 SDRAM

Table 21 shows the mode registers for DDR5 SDRAM. Each bit in a register byte (MR#) is denoted as "R" if it can be read but not written, "W" if it can be written but reads shall always produce a ZERO for those specific bits, and "R/W" if it can be read and written. Additionally, a DRAM read-only bit combined with a Host write-only bit is denoted as a "SR/W" bit. This bit allows the DRAM to return a defined status during a read of that bit (SR = Status Read), independent of what the Host may have written to the bit.

A defined register byte (MR#), is any MR# that has at least one of the bits defined.

When the entire MR# is marked RFU, then it is considered undefined and all the bits from the DRAM shall be don't care for reads or writes. These undefined mode registers (completely empty bytes, not individual bits of an MR) may not be supported in the DRAM. When a defined register byte (MR#) contains an "RFU" bit, the host must write a ZERO for those specific bits and the DRAM does not guarantee any operation of those specific RFU bits. When the host issues an MRR to a defined register (MR#) that contains RFU bits in it, those specific bits shall always produce a ZERO.

For cases in which a mode register is specific to a particular device configuration (x16, x8, x4) and/or density (32Gb, 16Gb, 8Gb), the following rules shall be applied:

- When the DRAM is configured as a x4/x8, an entire MR# used only for a x16 shall be considered RFU. These bits are don't care for reads and writes, and they may be unsupported.
- When a bit field within a register is used by a different configuration or density than a given DRAM, the host may write/read programmed values to these fields, but DRAM operation will not be affected.

A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register

Table 21 — Mode Register Assignment in DDR5 SDRAM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	RFU	CAS Latency (RL)					Burst Length	
1	PDA Select ID				PDA Enumerate ID			
2	Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training
3	Write Leveling Internal Cycle Alignment - Upper Byte				Write Leveling Internal Cycle Alignment - Lower Byte			
4	TUF	RFU	Wide Range (Optional)	Refresh tRFC Mode	Refresh Interval Rate Indicator	Minimum Refresh Rate		
5	Pull-Down Output Driver Impedance		DM Enable	TDQS Enable	PODTM Support	Pull-up Output Driver Impedance		Data Output Disable
6	tRTP				Write Recovery Time			
7	RFU						(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Upper Byte	(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Lower Byte

Table 21 — Mode Register Assignment in DDR5 SDRAM

8	Write Postamble Settings	Read Postamble Settings	RFU	Write Preamble Settings		Read Preamble Settings		
9	TM	RFU					x4 Writes	ECS Write-back
10	VrefDQ Calibration Value							
11	VrefCA Calibration Value							
12	VrefCS Calibration Value							
13	RFU				tCCD_L / tDLLK			
14	ECS Mode	Reset ECS Counter	Row Mode/ Code Word Mode	RFU	CID3	CID2	CID1	CID0
15	x4 Writes	ECS Writeback	RFU		Automatic ECS in Self Refresh	ECS Error Threshold Count (ETC)		
16	Transparency - Row Address with Max Errors 1 - See MR for encoding details							
17	Transparency - Row Address with Max Errors 2 - See MR for encoding details							
18	Transparency - Row Address with Max Errors 3 - See MR for encoding details							
19	PASR	RFU	Transparency - Max Row Error Count - See MR for encoding details					
20	Transparency - Error Count (EC) - See MR for encoding details							
21	RFU							
22	RFU					MBIST/mPPR Transparency (Optional)		
23	RFU		RFU	MBIST (Optional)	mPPR (Optional)	sPPR		hPPR
24	PPR Guard Key							
25	RFU				Continuous Burst Mode	LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pattern Format
26	Read Training Pattern Data0 / LFSR0 Seed							
27	Read Training Pattern Data1 / LFSR1 Seed							
28	Read Training Pattern Invert DQL7:0 (DQ7:0)							
29	Read Training Pattern Invert DQU7:0 (DQ15:8)							
30	LFSR Assignment DQL7/ DQU7	LFSR Assignment DQL6/ DQU6	LFSR Assignment DQL5/ DQU5	LFSR Assignment DQL4/ DQU4	LFSR Assignment DQL3/ DQU3	LFSR Assignment DQL2/ DQU2	LFSR Assignment DQL1/ DQU1	LFSR Assignment DQL0/ DQU0
31	Read Training Pattern Address							
32	RFU	CA_ODT Strap Value	CS ODT			CK ODT		
33	RFU		DQS_RTT_PARK			CA ODT		
34	RFU		RTT_WR			RTT_PARK		
35	RFU		RTT_NOM_RD			RTT_NOM_WR		
36	RFU					RTT_Loopback		
37	RFU		ODTLoff_WR_offset			ODTLon_WR_offset		
38	RFU		ODTLoff_WR_NT_offset			ODTLon_WR_NT_offset		
39	RFU		ODTLoff_RD_NT_offset			ODTLon_RD_NT_offset		
40	RFU					Read DQS offset timing		
41	RFU							
42	RFU				DCA Training Assist Mode	DCA Types Supported		

Table 21 — Mode Register Assignment in DDR5 SDRAM

43	Sign Bit for OP[6:4]	DCA for IBCLK in 4-phase clocks			Sign Bit for OP[2:0]	DCA for single/two-phase clock(s) or QCLK in 4-phase clocks		
44	RFU				Sign Bit for QBCLK in 4-phase clocks	DCA for QBCLK in 4-phase clocks		
45	DQS Interval Timer Run Time							
46	DQS Oscillator Count - LSB							
47	DQS Oscillator Count - MSB							
48	Write Pattern Mode							
49	RFU							
50	RFU	RFU	Write CRC auto-disable status	Write CRC auto-disable enable	Write CRC error status	Write CRC enable upper nibble	Write CRC enable lower nibble	Read CRC enable
51	RFU	Write CRC Auto-Disable Threshold - See MR for encoding details						
52	RFU	Write CRC Auto-Disable Window - See MR for encoding details						
53	Loopback Output Mode	Loopback Select Phase		Loopback Output Select				
54	hPPR Resource BG1 Bank 3	hPPR Resource BG1 Bank 2	hPPR Resource BG1 Bank 1	hPPR Resource BG1 Bank 0	hPPR Resource BG0 Bank 3	hPPR Resource BG0 Bank 2	hPPR Resource BG0 Bank 1	hPPR Resource BG0 Bank 0
55	hPPR Resource BG3 Bank 3	hPPR Resource BG3 Bank 2	hPPR Resource BG3 Bank 1	hPPR Resource BG3 Bank 0	hPPR Resource BG2 Bank 3	hPPR Resource BG2 Bank 2	hPPR Resource BG2 Bank 1	hPPR Resource BG2 Bank 0
56	hPPR Resource BG5 Bank 3	hPPR Resource BG5 Bank 2	hPPR Resource BG5 Bank 1	hPPR Resource BG5 Bank 0	hPPR Resource BG4 Bank 3	hPPR Resource BG4 Bank 2	hPPR Resource BG4 Bank 1	hPPR Resource BG4 Bank 0
57	hPPR Resource BG7 Bank 3	hPPR Resource BG7 Bank 2	hPPR Resource BG7 Bank 1	hPPR Resource BG7 Bank 0	hPPR Resource BG6 Bank 3	hPPR Resource BG6 Bank 2	hPPR Resource BG6 Bank 1	hPPR Resource BG6 Bank 0
58	RAAMMT[2:0]			RAAIMT[3:0]				RFM Required
59	RFM RAA Counter		ARFM	RFU				
60	PASR Segment Mask							
61	RSVD			Package Output Driver Test Mode				
62	Vendor Specified							
63	DRAM Scratch Pad							
64	Reserved							
65	Serial Number 1							
66	Serial Number 2							
67	Serial Number 3							
68	Serial Number 4							
69	Serial Number 5							
70-102	RFU							
103	DQSL_t IBCLK Sign	RFU	DQSL_t DCA for IBCLK		DQSL_t QCLK Sign	RFU	DQSL_t DCA for QCLK	
104	RFU				DQSL_t QBCLK Sign	RFU	DQSL_t DCA for QBCLK	
105	DQSL_c IBCLK Sign	RFU	DQSL_c DCA for IBCLK		DQSL_c QCLK Sign	RFU	DQSL_c DCA for QCLK	
106	RFU				DQSL_c QBCLK Sign	RFU	DQSL_c DCA for QBCLK	
107	DQSU_t IBCLK Sign	RFU	DQSU_t DCA for IBCLK		DQSU_t QCLK Sign	RFU	DQSU_t DCA for QCLK	
108	RFU				DQSU_t QBCLK Sign	RFU	DQSU_t DCA for QBCLK	
109	DQSU_c IBCLK Sign	RFU	DQSU_c DCA for IBCLK		DQSU_c QCLK Sign	RFU	DQSU_c DCA for QCLK	

Table 21 — Mode Register Assignment in DDR5 SDRAM

110	RFU		DQSU_c QBCLK Sign	RFU	DQSU_c DCA for QBCLK	
111	RFU	Global DFE Tap-4 Enable	Global DFE Tap-3 Enable	Global DFE Tap-2 Enable	Global DFE Tap-1 Enable	Global DFE gain Enable
112	RFU		DML DFE Gain Bias - See MR for encoding details			
113	DML DFE Tap-1 Bias - See MR for encoding details					
114	DML DFE Tap-2 Bias - See MR for encoding details					
115	DML DFE Tap-3 Bias - See MR for encoding details					
116	DML DFE Tap-4 Bias - See MR for encoding details					
117	RFU					
118	DML VREFDQ sign	DML VREFDQ Offset	RFU			
119	RFU					
120	RFU		DMU DFE Gain Bias - See MR for encoding details			
121	DMU DFE Tap-1 Bias - See MR for encoding details					
122	DMU DFE Tap-2 Bias - See MR for encoding details					
123	DMU DFE Tap-3 Bias - See MR for encoding details					
124	DMU DFE Tap-4 Bias - See MR for encoding details					
125	RFU					
126	DMU VREFDQ sign	DMU VREFDQ Offset	RFU			
127	RFU					
128	RFU		DQL0 DFE Gain Bias - See MR for encoding details			
129	DQL0 DFE Tap-1 Bias - See MR for encoding details					
130	DQL0 DFE Tap-2 Bias - See MR for encoding details					
131	DQL0 DFE Tap-3 Bias - See MR for encoding details					
132	DQL0 DFE Tap-4 Bias - See MR for encoding details					
133	DQL0 IBCLK Sign	RFU	DQL0 DCA for IBCLK	DQL0 QCLK Sign	RFU	DQL0 DCA for QCLK
134	DQL0 VREFDQ Sign	DQL0 VREFDQ Offset		DQL0 QBCLK Sign	RFU	DQL0 DCA for QBCLK
135	RFU					
136	RFU		DQL1 DFE Gain Bias - See MR for encoding details			
137	DQL1 DFE Tap-1 Bias - See MR for encoding details					
138	DQL1 DFE Tap-2 Bias - See MR for encoding details					
139	DQL1 DFE Tap-3 Bias - See MR for encoding details					
140	DQL1 DFE Tap-4 Bias - See MR for encoding details					
141	DQL1 IBCLK Sign	RFU	DQL1 DCA for IBCLK	DQL1 QCLK Sign	RFU	DQL1 DCA for QCLK
142	DQL1 VREFDQ Sign	DQL1 VREFDQ Offset		DQL1 QBCLK Sign	RFU	DQL1 DCA for QBCLK
143	RFU					
144	RFU		DQL2 DFE Gain Bias - See MR for encoding details			
145	DQL2 DFE Tap-1 Bias - See MR for encoding details					
146	DQL2 DFE Tap-2 Bias - See MR for encoding details					
147	DQL2 DFE Tap-3 Bias - See MR for encoding details					
148	DQL2 DFE Tap-4 Bias - See MR for encoding details					
149	DQL2 IBCLK Sign	RFU	DQL2 DCA for IBCLK	DQL2 QCLK Sign	RFU	DQL2 DCA for QCLK
150	DQL2 VREFDQ Sign	DQL2 VREFDQ Offset		DQL2 QBCLK Sign	RFU	DQL2 DCA for QBCLK

Table 21 — Mode Register Assignment in DDR5 SDRAM

155	RFU					
152	RFU			DQL3 DFE Gain Bias - See MR for encoding details		
153	DQL3 DFE Tap-1 Bias - See MR for encoding details					
154	DQL3 DFE Tap-2 Bias - See MR for encoding details					
155	DQL3 DFE Tap-3 Bias - See MR for encoding details					
156	DQL3 DFE Tap-4 Bias - See MR for encoding details					
157	DQL3 IBCLK Sign	RFU	DQL3 DCA for IBCLK	DQL3 QCLK Sign	RFU	DQL3 DCA for QCLK
158	DQL3 VREFDQ Sign	DQL3 VREFDQ Offset		DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK
159	RFU					
160	RFU			DQL4 DFE Gain Bias - See MR for encoding details		
161	DQL4 DFE Tap-1 Bias - See MR for encoding details					
162	DQL4 DFE Tap-2 Bias - See MR for encoding details					
163	DQL4 DFE Tap-3 Bias - See MR for encoding details					
164	DQL4 DFE Tap-4 Bias - See MR for encoding details					
165	DQL4 IBCLK Sign	RFU	DQL4 DCA for IBCLK	DQL4 QCLK Sign	RFU	DQL4 DCA for QCLK
166	DQL4 VREFDQ Sign	DQL4 VREFDQ Offset		DQL4 QBCLK Sign	RFU	DQL4 DCA for QBCLK
167	RFU					
168	RFU			DQL5 DFE Gain Bias - See MR for encoding details		
169	DQL5 DFE Tap-1 Bias - See MR for encoding details					
170	DQL5 DFE Tap-2 Bias - See MR for encoding details					
171	DQL5 DFE Tap-3 Bias - See MR for encoding details					
172	DQL5 DFE Tap-4 Bias - See MR for encoding details					
173	DQL5 IBCLK Sign	RFU	DQL5 DCA for IBCLK	DQL5 QCLK Sign	RFU	DQL5 DCA for QCLK
174	DQL5 VREFDQ Sign	DQL5 VREFDQ Offset		DQL5 QBCLK Sign	RFU	DQL5 DCA for QBCLK
175	RFU					
176	RFU			DQL6 DFE Gain Bias - See MR for encoding details		
177	DQL6 DFE Tap-1 Bias - See MR for encoding details					
178	DQL6 DFE Tap-2 Bias - See MR for encoding details					
179	DQL6 DFE Tap-3 Bias - See MR for encoding details					
180	DQL6 DFE Tap-4 Bias - See MR for encoding details					
181	DQL6 IBCLK Sign	RFU	DQL6 DCA for IBCLK	DQL6 QCLK Sign	RFU	DQL6 DCA for QCLK
182	DQL6 VREFDQ Sign	DQL6 VREFDQ Offset		DQL6 QBCLK Sign	RFU	DQL6 DCA for QBCLK
183	RFU					
184	RFU			DQL7 DFE Gain Bias - See MR for encoding details		
185	DQL7 DFE Tap-1 Bias - See MR for encoding details					
186	DQL7 DFE Tap-2 Bias - See MR for encoding details					
187	DQL7 DFE Tap-3 Bias - See MR for encoding details					
188	DQL7 DFE Tap-4 Bias - See MR for encoding details					
189	DQL7 IBCLK Sign	RFU	DQL6 DCA for IBCLK	DQL7 QCLK Sign	RFU	DQL7 DCA for QCLK
190	DQL7 VREFDQ Sign	DQL7 VREFDQ Offset		DQL7 QBCLK Sign	RFU	DQL7 DCA for QBCLK
191	RFU					
192	RFU			DQU0 DFE Gain Bias - See MR for encoding details		
193	DQU0 DFE Tap-1 Bias - See MR for encoding details					

Table 21 — Mode Register Assignment in DDR5 SDRAM

194	DQU0 DFE Tap-2 Bias - See MR for encoding details					
195	DQU0 DFE Tap-3 Bias - See MR for encoding details					
196	DQU0 DFE Tap-4 Bias - See MR for encoding details					
197	DQU0 IBCLK Sign	RFU	DQU0 DCA for IBCLK	DQU0 QCLK Sign	RFU	DQU0 DCA for QCLK
198	DQU0 VREFDQ Sign	DQU0 VREFDQ Offset		DQU0 QBCLK Sign	RFU	DQU0 DCA for QBCLK
199	RFU					
200	RFU			DQU1 DFE Gain Bias - See MR for encoding details		
201	DQU1 DFE Tap-1 Bias - See MR for encoding details					
202	DQU1 DFE Tap-2 Bias - See MR for encoding details					
203	DQU1 DFE Tap-3 Bias - See MR for encoding details					
204	DQU1 DFE Tap-4 Bias - See MR for encoding details					
205	DQU1 IBCLK Sign	RFU	DQU1 DCA for IBCLK	DQU1 QCLK Sign	RFU	DQU1 DCA for QCLK
206	DQU1 VREFDQ Sign	DQU1 VREFDQ Offset		DQU1 QBCLK Sign	RFU	DQU1 DCA for QBCLK
207	RFU					
208	RFU			DQU2 DFE Gain Bias - See MR for encoding details		
209	DQU2 DFE Tap-1 Bias - See MR for encoding details					
210	DQU2 DFE Tap-2 Bias - See MR for encoding details					
211	DQU2 DFE Tap-3 Bias - See MR for encoding details					
212	DQU2 DFE Tap-4 Bias - See MR for encoding details					
213	DQU2 IBCLK Sign	RFU	DQU2 DCA for IBCLK	DQU2 QCLK Sign	RFU	DQU2 DCA for QCLK
214	DQU2 VREFDQ Sign	DQU2 VREFDQ Offset		DQU2 QBCLK Sign	RFU	DQU2 DCA for QBCLK
215	RFU					
216	RFU			DQU3 DFE Gain Bias - See MR for encoding details		
217	DQU3 DFE Tap-1 Bias - See MR for encoding details					
218	DQU3 DFE Tap-2 Bias - See MR for encoding details					
219	DQU3 DFE Tap-3 Bias - See MR for encoding details					
220	DQU3 DFE Tap-4 Bias - See MR for encoding details					
221	DQU3 IBCLK Sign	RFU	DQU3 DCA for IBCLK	DQU3 QCLK Sign	RFU	DQU3 DCA for QCLK
222	DQU3 VREFDQ Sign	DQU3 VREFDQ Offset		DQU3 QBCLK Sign	RFU	DQU3 DCA for QBCLK
223	RFU					
224	RFU			DQU4 DFE Gain Bias - See MR for encoding details		
225	DQU4 DFE Tap-1 Bias - See MR for encoding details					
226	DQU4 DFE Tap-2 Bias - See MR for encoding details					
227	DQU4 DFE Tap-3 Bias - See MR for encoding details					
228	DQU4 DFE Tap-4 Bias - See MR for encoding details					
229	DQU4 IBCLK Sign	RFU	DQU4 DCA for IBCLK	DQU4 QCLK Sign	RFU	DQU4 DCA for QCLK
230	DQU4 VREFDQ Sign	DQU4 VREFDQ Offset		DQU4 QBCLK Sign	RFU	DQU4 DCA for QBCLK
231	RFU					
232	RFU			DQU5 DFE Gain Bias - See MR for encoding details		
233	DQU5 DFE Tap-1 Bias - See MR for encoding details					
234	DQU5 DFE Tap-2 Bias - See MR for encoding details					
235	DQU5 DFE Tap-3 Bias - See MR for encoding details					
236	DQU5 DFE Tap-4 Bias - See MR for encoding details					

Table 21 — Mode Register Assignment in DDR5 SDRAM

237	DQU5 IBCLK Sign	RFU	DQU5 DCA for IBCLK	DQU5 QCLK Sign	RFU	DQU5 DCA for QCLK
238	DQU5 VREFDQ Sign	DQU5 VREFDQ Offset		DQU5 QBCLK Sign	RFU	DQU5 DCA for QBCLK
239	RFU					
240	RFU			DQU6 DFE Gain Bias - See MR for encoding details		
241	DQU6 DFE Tap-1 Bias - See MR for encoding details					
242	DQU6 DFE Tap-2 Bias - See MR for encoding details					
243	DQU6 DFE Tap-3 Bias - See MR for encoding details					
244	DQU6 DFE Tap-4 Bias - See MR for encoding details					
245	DQU6 IBCLK Sign	RFU	DQU6 DCA for IBCLK	DQU6 QCLK Sign	RFU	DQU6 DCA for QCLK
246	DQU6 VREFDQ Sign	DQU6 VREFDQ Offset		DQU6 QBCLK Sign	RFU	DQU6 DCA for QBCLK
247	RFU					
248	RFU			DQU7 DFE Gain Bias - See MR for encoding details		
249	DQU7 DFE Tap-1 Bias - See MR for encoding details					
250	DQU7 DFE Tap-2 Bias - See MR for encoding details					
251	DQU7 DFE Tap-3 Bias - See MR for encoding details					
252	DQU7 DFE Tap-4 Bias - See MR for encoding details					
253	DQU7 IBCLK Sign	RFU	DQU7 DCA for IBCLK	DQU7 QCLK Sign	RFU	DQU7 DCA for QCLK
254	DQU7 VREFDQ Sign	DQU7 VREFDQ Offset		DQU7 QBCLK Sign	RFU	DQU7 DCA for QBCLK
255	RFU					

3.5.2 MR0 (MA[7:0]=00H) Burst Length and CAS Latency

MR0 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CAS Latency (RL)					Burst Length	

Function	Register Type	Operand	Data	Notes
Burst Length	R/W	OP[1:0]	00_B: BL16 01_B: BC8 OTF 10_B: BL32 (Optional) 11_B: BL32 OTF (Optional)	
CAS Latency (RL)	R/W	OP[6:2]	00000_B: 22 00001_B: 24 00010_B: 26 00011_B: 28 ... 10011_B: 60 10100_B: 62 10101_B: 64 10110_B: 66 All other encodings reserved.	1, 2
RFU	RFU	OP[7]	RFU	

Notes

1 - Range covers both Monolithic DDR5 and 3DS-DDR5 devices up to 6400

2 - WL=RL-2, also known as CWL=CL-2

3.5.3 MR1 (MA [7:0] = 01_H) - PDA Mode Details

MR1 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PDA Select ID				PDA Enumerate ID			

Function	Register Type	Operand	Data	Notes
PDA Enumerate ID	**R**	**OP[3:0]**	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Enumerate ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Enumerate ID opcode. This can only be set when PDA Enumerate Programming Mode is enabled and the associated DRAM's DQ0 is asserted LOW. The PDA Enumerate ID opcode includes 4 bits for this encoding. Default setting is 1111_B	
PDA Select ID	**R**	**OP[7:4]**	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Select ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Select ID opcode. The PDA Select ID opcode includes 4 bits for this encoding. 1111_B = all DRAMs execute MRW, MPC, and VrefCA commands For all other encodings, DRAMs execute MRW, MPC, and VrefCA commands only if PDA Select ID[3:0] = PDA Enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA Select ID. Default setting is 1111_B	

Note(s):

3.5.4 MR2 (MA [7:0] = 02_H) - Functional Modes MR2 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training

Function	Register Type	Operand	Data	Notes
Read Preamble Training	R/W	OP[0]	0B: Normal Mode (Default) 1B: Read Preamble Training	
Write Leveling	R/W	OP[1]	0B: Normal Mode (Default) 1B: Write Leveling	1,2,3
2N Mode	R	OP[2]	0B: 2N Mode (Default) 1B: 1N Mode	4
Max Power Saving Mode	R/W	OP[3]	0B: Disable (Default) 1B: Enable	
CS Assertion Duration (MPC)	R/W	OP[4]	0B: Only Multiple cycles of CS assertion supported for MPC, VrefCA and VrefCS commands (Default) 1B: Only a single cycle of CS assertion supported for MPC, VrefCA and VrefCS commands	
Device 15 Maximum Power Savings Mode	R/W	OP[5]	0B: Disable (Default) 1B: Enable	
Reserved	Reserved	OP[6]	Reserved	
Internal Write Timing	R/W	OP[7]	0B: Disable 1B: Enable	5

Note(s):

1. To enter WL Training Mode the MR field must be programmed to 1. WL Training Mode is used when Internal Write Timing = 0 (External WL Training) and when Internal Write Timing = 1 (Internal WL Training).
2. To exit WL Training Mode the MR field must be programmed to 0.
3. MRR's are not supported during Write Leveling.
4. This mode register is programmed via an explicit MPC command only.
5. This is set during WL Training, after the host DQS has been aligned to the ideal External WL timings. The Internal Write Timing is enabled and the WL Internal Timing Alignment is set to ensure the internal Write Enable aligns within tDQS2CK of the external WL Trained location. When Internal Write Timing is Disabled, the WL Internal Cycle Alignment setting does not change the behavior of the write timings

3.5.5 MR3 (MA[7:0]=03_H) - DQS Training

MR3 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Write Leveling Internal Cycle Alignment - Upper Byte				Write Leveling Internal Cycle Alignment - Lower Byte			

Function	Register Type	Operand	Data	Notes
Write Leveling Internal Cycle Alignment - Lower Byte	**R/W**	**OP[3:0]**	0000_B: 0 tCK (Default) 0001_B: -1 tCK 0010_B: -2 tCK 0011_B: -3 tCK 0100_B: -4 tCK 0101_B: -5 tCK 0110_B: -6 tCK (Optional OPcode: 0111_B through 1111_B) 0111_B: -7 tCK 1000_B: -8 tCK ... 1110_B: -14 tCK 1111_B: -15 tCK	1,2,3, 5
Write Leveling Internal Cycle Alignment - Upper Byte	**R/W**	**OP[7:4]**	0000_B: 0 tCK (Default) 0001_B: -1 tCK 0010_B: -2 tCK 0011_B: -3 tCK 0100_B: -4 tCK 0101_B: -5 tCK 0110_B: -6 tCK (Optional OPcode: 0111_B through 1111_B) 0111_B: -7 tCK 1000_B: -8 tCK ... 1110_B: -14 tCK 1111_B: -15 tCK	1,2,4, 5

Note(s):

1. This is set during WL Training, after the host DQS has been aligned to the ideal External WL timings. The Internal Write Timing is enabled and the WL Internal Timing Alignment is set to ensure the internal Write Enable aligns within t_{DQS2CK} of the external WL Trained location. When Internal Write Timing is Disabled, the WL Internal Cycle Alignment setting does not change the behavior of the write timings.
2. The DRAM implementation may optionally have the same behavior when the Internal Write Timing is enabled vs disabled. This would mean that the CK and DQS timing paths remain matched internally. The WL Internal Cycle Alignment setting must still support pulling the Internal WL Pulse earlier so that the same WL Training Flow will produce the correct result.
3. Lower Byte WL Internal Cycle Alignment is intended for x4, x8, and x16 configurations.
4. Upper Byte WL Internal Cycle Alignment is intended for x16 configuration only. Although training of the Lower and Upper Bytes is independent, contact the DRAM vendor regarding recommendations for setting the WICA values to the same offset.
5. Optional OPcode may be needed for certain speed bins.

3.5.6 MR4 (MA[7:0]=04_H) - Refresh Settings

MR4 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	RFU	Wide Range (Optional)	Refresh tRFC Mode	Refresh Interval Rate Indicator	Minimum Refresh Rate		

Function	Register Type	Operand	Data	Notes
Minimum Refresh Rate	R	OP[2:0]	If Wide Range is not supported (OP[5]=0): 000_B: RFU 001_B: tREFI x1 (1x Refresh Rate), <80°C nominal 010_B: tREFI x1 (1x Refresh Rate), 80-85°C nominal 011_B: tREFI /2 (2x Refresh Rate), 85-90°C nominal 100_B: tREFI /2 (2x Refresh Rate), 90-95°C nominal 101_B: tREFI /2 (2x Refresh Rate), >95°C nominal 110_B: RFU 111_B: RFU If Wide Range is supported (OP[5]=1): 000_B: tREFI x1 (1x Refresh Rate), <75°C nominal 001_B: tREFI x1 (1x Refresh Rate), 75-80°C nominal 010_B: tREFI x1 (1x Refresh Rate), 80-85°C nominal 011_B: tREFI /2 (2x Refresh Rate), 85-90°C nominal 100_B: tREFI /2 (2x Refresh Rate), 90-95°C nominal 101_B: tREFI /2 (2x Refresh Rate), 95-100°C nominal 110_B: tREFI /2 (2x Refresh Rate), >100°C nominal 111_B: RFU	1,2,3,4,5, 6,7,8
Refresh Interval Rate Indicator	SR/W	OP[3]	DRAM Status Read (SR): 0_B: Not implemented (Default) 1_B: Implemented Host Write (W): 0_B: Disabled (Default) 1_B: Enabled	
Refresh tRFC Mode	R/W	OP[4]	0_B: Normal Refresh Mode (tRFC1) 1_B: Fine Granularity Refresh Mode (tRFC2)	
Wide Range (Optional)	R	OP[5]	0_B: Wide range is not supported (Default) 1_B: Wide range is supported (Optional)	
RFU	RFU	OP[6]	RFU	
TUF (Temperature Update Flag)	R	OP[7]	0_B: No change in OP[2:0] since last MR4 read (default) 1_B: Change in OP[2:0] since last MR4 read	

Note(s):

1. The minimum required refresh rate for each OP[2:0] setting applies to tREFI1 and tREFI2. Each OP[2:0] setting specifies a nominal temperature range. The ranges defined by OP[2:0] are determined by temperature thresholds used by the system for proper operation.
2. When OP[5]=0, the four temperature thresholds are nominally at 80°C, 85°C, 90°C and 95°C. The <80°C threshold has no minimum value specified and the >95°C threshold has no maximum temperature value specified. When OP[5]=1, the six temperature thresholds are nominally at 75°C, 80°C, 85°C, 90°C, 95°C, and 100°C. The <75°C threshold has no minimum value specified and the >100°C threshold has no maximum temperature value specified 3. DRAM vendors must report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range when the system refresh interval follows there guidelines:

Threshold £ 85°C: tREFI x1 (1x Refresh Rate) or faster may be used
Threshold > 85°C: tREFI /2 (2x Refresh Rate) or faster is required
Data integrity at thresholds >95°C is not assured regardless of refresh rate

4. The 2x Refresh Rate must be provided by the system before the DRAM Tj has gone up by more than 2°C (Temperature Margin) since the first report out of OP[2:0]=011B. This condition is reset when OP[2:0] is equal to 010B.
5. The device may not operate properly when OP[2:0]=101B, if the DRAM Tj has gone up by more than 2°C (Temperature Margin) since the first report out of OP[2:0]=101B. This condition is reset when OP[2:0] is equal to 100B. OP[2:0]=101B must be a temporary condition of the DRAM, to be addressed by immediately reducing the Tj of the DRAM by throttling its power, and/or the power of nearby devices.
6. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence (Te).
7. See the section on “Temperature Sensor” for information on the recommended frequency of reading MR4
8. Support for extended temperature sensor ranges does not indicate that the DDR5 DRAM device may operate properly at temperature ranges above 95°C – side effects may include loss of data integrity

3.5.7 MR5 (MA[7:0]=05_H) - IO Settings

MR5 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pull-Down Output Driver Impedance		DM Enable	TDQS Enable	PODTM Support	Pull-up Output Driver Impedance		Data Output Disable

Function	Register Type	Operand	Data	Notes
Data Output Disable	W	OP[0]	0_B: Normal Operation (Default) 1_B: Outputs Disabled	
Pull-up Output Driver Impedance	R/W	OP[2:1]	00_B: RZQ/7 (34) 01_B: RZQ/6 (40) 10_B: RZQ/5 (48) 11_B: RFU	
Package Output Driver Test Mode Supported	R	OP[3]	0B: Function Not Supported 1B: Function Supported	
TDQS Enable	R/W	OP[4]	0B: Disable (Default) 1B: Enable	
DM Enable	R/W	OP[5]	0B: Disable (Default) 1B: Enable	
Pull-Down Output Driver Impedance	R/W	OP[7:6]	00B: RZQ/7 (34) 01B: RZQ/6 (40) 10B: RZQ/5 (48) 11B: RFU	

NOTE:

3.5.8 MR6 (MA[7:0]=06_H) - Write Recovery Time & tRTP

MR6 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
tRTP				Write Recovery Time			

Function	Register Type	Operand	Data	Notes
Write Recovery Time	R/W	OP[3:0]	0000_B: 48nCK 0001_B: 54nCK 0010_B: 60nCK 0011_B: 66nCK 0100_B: 72nCK 0101_B: 78nCK 0110_B: 84nCK 0111_B: 90nCK 1000_B: 96nCK 1001_B: RFU 1010_B: RFU 1011_B: RFU All other encodings reserved	1
tRTP	R/W	OP[7:4]	0000_B: 12nCK 0001_B: 14nCK 0010_B: 15nCK 0011_B: 17nCK 0100_B: 18nCK 0101_B: 20nCK 0110_B: 21nCK 0111_B: 23nCK 1000_B: 24nCK 1001_B: RFU 1010_B: RFU 1011_B: RFU All other encodings reserved	2

Notes:

1. tWR,min is defined in the “Timing Parameters” tables (Table 300 - Table 302). Host must operate with MR settings resulting in tCK * MR6:OP[3:0] >= tWR,min.
2. tRTP, min is defined in the “Timing Parameters” tables (Table 300 - Table 302). Host must operate with MR settings resulting in tCK * MR6:OP[7:4]>= tRTP,min.
3. All nCK conversions require rounding algorithm consideration.

3.5.9 MR7 (MA[7:0]=07_H) - Write Leveling Internal +0.5tCK Alignment Offsest

MR7 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU						(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Upper Byte	(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Lower Byte

Function	Register Type	Operand	Data	Notes
(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Lower Byte	R/W	OP[0]	0_B: Disabled (Default) 1_B: 0.5tCK	1,2
(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Upper Byte	R/W	OP[1]	0_B: Disabled (Default) 1_B: 0.5tCK	1,3

Note(s)

1. The WICA 0.5 tCK offset is a positive adjustment to the target WICA value. (Ex. MR3:OP[3:0] = -3 tCK (0011_B) and MR7:OP[0] = 1, WICA + WICAhalfCycle = -3 tCK + 0.5 tCK = -2.5 tCK)
2. Lower Byte WL Internal Cycle Alignment is intended for x4, x8, and x16 configurations.
3. Upper Byte WL Internal Cycle Alignment is intended for x16 configuration only. Although training of the Lower and Upper Bytes is independent, contact the DRAM vendor regarding recommendations for setting the WICA values to the same offset.

3.5.10 MR8 (MA[7:0]=08_H) - Preamble / Postamble

MR8 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Write Postamble Settings	Read Postamble Settings	RFU	Write Preamble Settings		Read Preamble Settings		

Function	Register Type	Operand	Data	Notes
Read Preamble Settings	R/W	OP[2:0]	000B: 1 tCK - 10 Pattern 001B: 2 tCK - 0010 Pattern 010B: 2 tCK - 1110 Pattern (DDR4 Style) 011B: 3 tCK - 000010 Pattern 100B: 4 tCK - 00001010 Pattern 101B: Reserved 110B: Reserved 111B: Reserved	1
Write Preamble Settings	R/W	OP[4:3]	00B: Reserved 01B: 2 tCK - 0010 Pattern (Default) 10B: 3 tCK - 000010 Pattern 11B: 4 tCK - 00001010 Pattern	
RFU	RFU	OP[5]	RFU	
Read Postamble Settings	R/W	OP[6]	0B: 0.5 tCK - 0 Pattern 1B: 1.5 tCK - 010 Pattern	
Write Postamble Settings	R/W	OP[7]	0B: 0.5 tCK - 0 Pattern 1B: 1.5 tCK - 000 Pattern	

Notes:

1 - Please refer to the Preamble Specification for details on the Read Preamble modes and patterns.

3.5.11 MR9 (MA[7:0]=09H) - Writeback Suppression and TM

MR9 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TM	RFU					x4 Write	ECS Write-back

Function	Register Type	Operand	Data	Notes
ECS Writeback	R/W	OP[0]	0B: Do not suppress writeback of Data and ECC Check Bits (Default) 1B: Suppress writeback of Data and ECC Check Bits (Optional)	
x4 Writes	R/W	OP[1]	0B: Do not suppress writeback of Data during RMW (Default) 1B: Suppress writeback of Data during RMW (Optional)	
RFU	RFU	OP[6:2]	RFU	
TM	W	OP[7]	0B: Normal (Default) 1B: Test Mode	

Note(s):

3.5.12 MR10 (MA[7:0]=$0A_H$) - VrefDQ Calibration Value

MR10 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VrefDQ Calibration Value							

Function	Register Type	Operand	Data	Notes
VrefDQ Cal Value	R/W	OP[7:0]	$0000:0000_B$: --Thru-- $1111:1111_B$: See Table Below	

Table 22 — VrefDQ Setting Range

Function	Operand						Notes
VrefDQ Cal Value for MR10	OP	$0000\ 0000_B$: 97.5%	$0001\ 1011_B$: 84.0%	$0011\ 0110_B$: 70.5%	$0101\ 0001_B$: 57.0%	$0110\ 1100_B$: 43.5%	
		$0000\ 0001_B$: 97.0%	$0001\ 1100_B$: 83.5%	$0011\ 0111_B$: 70.0%	$0101\ 0010_B$: 56.5%	$0110\ 1101_B$: 43.0%	
		$0000\ 0010_B$: 96.5%	$0001\ 1101_B$: 83.0%	$0011\ 1000_B$: 69.5%	$0101\ 0011_B$: 56.0%	$0110\ 1110_B$: 42.5%	
		$0000\ 0011_B$: 96.0%	$0001\ 1110_B$: 82.5%	$0011\ 1001_B$: 69.0%	$0101\ 0100_B$: 55.5%	$0110\ 1111_B$: 42.0%	
		$0000\ 0100_B$: 95.5%	$0001\ 1111_B$: 82.0%	$0011\ 1010_B$: 68.5%	$0101\ 0101_B$: 55.0%	$0111\ 0000_B$: 41.5%	
		$0000\ 0101_B$: 95.0%	$0010\ 0000_B$: 81.5%	$0011\ 1011_B$: 68.0%	$0101\ 0110_B$: 54.5%	$0111\ 0001_B$: 41.0%	
		$0000\ 0110_B$: 94.5%	$0010\ 0001_B$: 81.0%	$0011\ 1100_B$: 67.5%	$0101\ 0111_B$: 54.0%	$0111\ 0010_B$: 40.5%	
		$0000\ 0111_B$: 94.0%	$0010\ 0010_B$: 80.5%	$0011\ 1101_B$: 67.0%	$0101\ 1000_B$: 53.5%	$0111\ 0011_B$: 40.0%	
		$0000\ 1000_B$: 93.5%	$0010\ 0011_B$: 80.0%	$0011\ 1110_B$: 66.5%	$0101\ 1001_B$: 53.0%	$0111\ 0100_B$: 39.5%	
		$0000\ 1001_B$: 93.0%	$0010\ 0100_B$: 79.5%	$0011\ 1111_B$: 66.0%	$0101\ 1010_B$: 52.5%	$0111\ 0101_B$: 39.0%	
		$0000\ 1010_B$: 92.5%	$0010\ 0101_B$: 79.0%	$0100\ 0000_B$: 65.5%	$0101\ 1011_B$: 52.0%	$0111\ 0110_B$: 38.5%	
		$0000\ 1011_B$: 92.0%	$0010\ 0110_B$: 78.5%	$0100\ 0001_B$: 65.0%	$0101\ 1100_B$: 51.5%	$0111\ 0111_B$: 38.0%	
		$0000\ 1100_B$: 91.5%	$0010\ 0111_B$: 78.0%	$0100\ 0010_B$: 64.5%	$0101\ 1101_B$: 51.0%	$0111\ 1000_B$: 37.5%	
		$0000\ 1101_B$: 91.0%	$0010\ 1000_B$: 77.5%	$0100\ 0011_B$: 64.0%	$0101\ 1110_B$: 50.5%	$0111\ 1001_B$: 37.0%	
		$0000\ 1110_B$: 90.5%	$0010\ 1001_B$: 77.0%	$0100\ 0100_B$: 63.5%	$0101\ 1111_B$: 50.0%	$0111\ 1010_B$: 36.5%	
		$0000\ 1111_B$: 90.0%	$0010\ 1010_B$: 76.5%	$0100\ 0101_B$: 63.0%	$0110\ 0000_B$: 49.5%	$0111\ 1011_B$: 36.0%	
		$0001\ 0000_B$: 89.5%	$0010\ 1011_B$: 76.0%	$0100\ 0110_B$: 62.5%	$0110\ 0001_B$: 49.0%	$0111\ 1100_B$: 35.5%	
		$0001\ 0001_B$: 89.0%	$0010\ 1100_B$: 75.5%	$0100\ 0111_B$: 62.0%	$0110\ 0010_B$: 48.5%	$0111\ 1101_B$: 35.0%	
		$0001\ 0010_B$: 88.5%	$0010\ 1101_B$: 75.0%	$0100\ 1000_B$: 61.5%	$0110\ 0011_B$: 48.0%	All Others: Reserved	
		$0001\ 0011_B$: 88.0%	$0010\ 1110_B$: 74.5%	$0100\ 1001_B$: 61.0%	$0110\ 0100_B$: 47.5%		
		$0001\ 0100_B$: 87.5%	$0010\ 1111_B$: 74.0%	$0100\ 1010_B$: 60.5%	$0110\ 0101_B$: 47.0%		
		$0001\ 0101_B$: 87.0%	$0011\ 0000_B$: 73.5%	$0100\ 1011_B$: 60.0%	$0110\ 0110_B$: 46.5%		
		$0001\ 0110_B$: 86.5%	$0011\ 0001_B$: 73.0%	$0100\ 1100_B$: 59.5%	$0110\ 0111_B$: 46.0%		
		$0001\ 0111_B$: 86.0%	$0011\ 0010_B$: 72.5%	$0100\ 1101_B$: 59.0%	$0110\ 1000_B$: 45.5%		
		$0001\ 1000_B$: 85.5%	$0011\ 0011_B$: 72.0%	$0100\ 1110_B$: 58.5%	$0110\ 1001_B$: 45.0%		
		$0001\ 1001_B$: 85.0%	$0011\ 0100_B$: 71.5%	$0100\ 1111_B$: 58.0%	$0110\ 1010_B$: 44.5%		
		$0001\ 1010_B$: 84.5%	$0011\ 0101_B$: 71.0%	$0101\ 0000_B$: 57.5%	$0110\ 1011_B$: 44.0%		

3.5.13 MR11 (MA[6:0]=$0B_H$) - Vref CA Calibration Value

MR11 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VrefCA Calibration Value							

Function	Register Type	Operand	Data	Notes
VrefCA Cal Value	R	OP[6:0]	000:0000_B: --Thru-- 111:1111_B: See Table Below	1, 2
	R	OP[7]	V: Valid	

1 - Since VREF CA Calibration setting has an explicit command (VrefCA COMMAND), it can only be programmed via that command and its mode register is therefore read only.

2 - Since the state of CA12 is used to differentiate the VrefCA vs VrefCS command, the MR11/12 OP[7] value is defined as valid.

Table 23 — VrefCA Setting Range

Function	Operand						Notes
VrefCA Cal Value for MR11	OP	V000 0000_B: 97.5%	V001 1011_B: 84.0%	V011 0110_B: 70.5%	V101 0001_B: 57.0%	V110 1100_B: 43.5%	
		V000 0001_B: 97.0%	V001 1100_B: 83.5%	V011 0111_B: 70.0%	V101 0010_B: 56.5%	V110 1101_B: 43.0%	
		V000 0010_B: 96.5%	V001 1101_B: 83.0%	V011 1000_B: 69.5%	V101 0011_B: 56.0%	V110 1110_B: 42.5%	
		V000 0011_B: 96.0%	V001 1110_B: 82.5%	V011 1001_B: 69.0%	V101 0100_B: 55.5%	V110 1111_B: 42.0%	
		V000 0100_B: 95.5%	V001 1111_B: 82.0%	V011 1010_B: 68.5%	V101 0101_B: 55.0%	V111 0000_B: 41.5%	
		V000 0101_B: 95.0%	V010 0000_B: 81.5%	V011 1011_B: 68.0%	V101 0110_B: 54.5%	V111 0001_B: 41.0%	
		V000 0110_B: 94.5%	V010 0001_B: 81.0%	V011 1100_B: 67.5%	V101 0111_B: 54.0%	V111 0010_B: 40.5%	
		V000 0111_B: 94.0%	V010 0010_B: 80.5%	V011 1101_B: 67.0%	V101 1000_B: 53.5%	V111 0011_B: 40.0%	
		V000 1000_B: 93.5%	V010 0011_B: 80.0%	V011 1110_B: 66.5%	V101 1001_B: 53.0%	V111 0100_B: 39.5%	
		V000 1001_B: 93.0%	V010 0100_B: 79.5%	V011 1111_B: 66.0%	V101 1010_B: 52.5%	V111 0101_B: 39.0%	
		V000 1010_B: 92.5%	V010 0101_B: 79.0%	V100 0000_B: 65.5%	V101 1011_B: 52.0%	V111 0110_B: 38.5%	
		V000 1011_B: 92.0%	V010 0110_B: 78.5%	V100 0001_B: 65.0%	V101 1100_B: 51.5%	V111 0111_B: 38.0%	
		V000 1100_B: 91.5%	V010 0111_B: 78.0%	V100 0010_B: 64.5%	V101 1101_B: 51.0%	V111 1000_B: 37.5%	
		V000 1101_B: 91.0%	V010 1000_B: 77.5%	V100 0011_B: 64.0%	V101 1110_B: 50.5%	V111 1001_B: 37.0%	
		V000 1110_B: 90.5%	V010 1001_B: 77.0%	V100 0100_B: 63.5%	V101 1111_B: 50.0%	V111 1010_B: 36.5%	
		V000 1111_B: 90.0%	V010 1010_B: 76.5%	V100 0101_B: 63.0%	V110 0000_B: 49.5%	V111 1011_B: 36.0%	
		V001 0000_B: 89.5%	V010 1011_B: 76.0%	V100 0110_B: 62.5%	V110 0001_B: 49.0%	V111 1100_B: 35.5%	
		V001 0001_B: 89.0%	V010 1100_B: 75.5%	V100 0111_B: 62.0%	V110 0010_B: 48.5%	V111 1101_B: 35.0%	
		V001 0010_B: 88.5%	V010 1101_B: 75.0%	V100 1000_B: 61.5%	V110 0011_B: 48.0%	All Others: Reserved	
		V001 0011_B: 88.0%	V010 1110_B: 74.5%	V100 1001_B: 61.0%	V110 0100_B: 47.5%		
		V001 0100_B: 87.5%	V010 1111_B: 74.0%	V100 1010_B: 60.5%	V110 0101_B: 47.0%		
		V001 0101_B: 87.0%	V011 0000_B: 73.5%	V100 1011_B: 60.0%	V110 0110_B: 46.5%		
		V001 0110_B: 86.5%	V011 0001_B: 73.0%	V100 1100_B: 59.5%	V110 0111_B: 46.0%		
		V001 0111_B: 86.0%	V011 0010_B: 72.5%	V100 1101_B: 59.0%	V110 1000_B: 45.5%		
		V001 1000_B: 85.5%	V011 0011_B: 72.0%	V100 1110_B: 58.5%	V110 1001_B: 45.0%		
		V001 1001_B: 85.0%	V011 0100_B: 71.5%	V100 1111_B: 58.0%	V110 1010_B: 44.5%		
		V001 1010_B: 84.5%	V011 0101_B: 71.0%	V101 0000_B: 57.5%	V110 1011_B: 44.0%		

Note: “V” = Valid.

3.5.14 MR12 (MA[7:0]=$0C_H$) - Vref CS Calibration Value

MR12 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VrefCS Calibration Value							

Function	Register Type	Operand	Data	Notes
VrefCS Cal Value	R	OP[6:0]	$000:0000_B$: --Thru-- $111:1111_B$: See Table Below	1, 2
	R	OP[7]	V: Valid	

1 - Since VREF CS Calibration setting has an explicit command (VrefCS COMMAND), it can only be programmed via that command and its mode register is therefore read only.

2 - Since the state of CA12 is used to differentiate the VrefCA vs VrefCS command, the MR11/12 OP[7] value is defined as valid.

Table 24 — VrefCS Setting Range

Function	Operand						Notes
VrefCS Cal Value for MR12	OP	V000 0000B: 97.5%	V001 1011B: 84.0%	V011 0110B: 70.5%	V101 0001B: 57.0%	V110 1100B: 43.5%	
		V000 0001B: 97.0%	V001 1100B: 83.5%	V011 0111B: 70.0%	V101 0010B: 56.5%	V110 1101B: 43.0%	
		V000 0010B: 96.5%	V001 1101B: 83.0%	V011 1000B: 69.5%	V101 0011B: 56.0%	V110 1110B: 42.5%	
		V000 0011B: 96.0%	V001 1110B: 82.5%	V011 1001B: 69.0%	V101 0100B: 55.5%	V110 1111B: 42.0%	
		V000 0100B: 95.5%	V001 1111B: 82.0%	V011 1010B: 68.5%	V101 0101B: 55.0%	V111 0000B: 41.5%	
		V000 0101B: 95.0%	V010 0000B: 81.5%	V011 1011B: 68.0%	V101 0110B: 54.5%	V111 0001B: 41.0%	
		V000 0110B: 94.5%	V010 0001B: 81.0%	V011 1100B: 67.5%	V101 0111B: 54.0%	V111 0010B: 40.5%	
		V000 0111B: 94.0%	V010 0010B: 80.5%	V011 1101B: 67.0%	V101 1000B: 53.5%	V111 0011B: 40.0%	
		V000 1000B: 93.5%	V010 0011B: 80.0%	V011 1110B: 66.5%	V101 1001B: 53.0%	V111 0100B: 39.5%	
		V000 1001B: 93.0%	V010 0100B: 79.5%	V011 1111B: 66.0%	V101 1010B: 52.5%	V111 0101B: 39.0%	
		V000 1010B: 92.5%	V010 0101B: 79.0%	V100 0000B: 65.5%	V101 1011B: 52.0%	V111 0110B: 38.5%	
		V000 1011B: 92.0%	V010 0110B: 78.5%	V100 0001B: 65.0%	V101 1100B: 51.5%	V111 0111B: 38.0%	
		V000 1100B: 91.5%	V010 0111B: 78.0%	V100 0010B: 64.5%	V101 1101B: 51.0%	V111 1000B: 37.5%	
		V000 1101B: 91.0%	V010 1000B: 77.5%	V100 0011B: 64.0%	V101 1110B: 50.5%	V111 1001B: 37.0%	
		V000 1110B: 90.5%	V010 1001B: 77.0%	V100 0100B: 63.5%	V101 1111B: 50.0%	V111 1010B: 36.5%	
		V000 1111B: 90.0%	V010 1010B: 76.5%	V100 0101B: 63.0%	V110 0000B: 49.5%	V111 1011B: 36.0%	
		V001 0000B: 89.5%	V010 1011B: 76.0%	V100 0110B: 62.5%	V110 0001B: 49.0%	V111 1100B: 35.5%	
		V001 0001B: 89.0%	V010 1100B: 75.5%	V100 0111B: 62.0%	V110 0010B: 48.5%	V111 1101B: 35.0%	
		V001 0010B: 88.5%	V010 1101B: 75.0%	V100 1000B: 61.5%	V110 0011B: 48.0%	All Others: Reserved	
		V001 0011B: 88.0%	V010 1110B: 74.5%	V100 1001B: 61.0%	V110 0100B: 47.5%		
		V001 0100B: 87.5%	V010 1111B: 74.0%	V100 1010B: 60.5%	V110 0101B: 47.0%		
		V001 0101B: 87.0%	V011 0000B: 73.5%	V100 1011B: 60.0%	V110 0110B: 46.5%		
		V001 0110B: 86.5%	V011 0001B: 73.0%	V100 1100B: 59.5%	V110 0111B: 46.0%		
		V001 0111B: 86.0%	V011 0010B: 72.5%	V100 1101B: 59.0%	V110 1000B: 45.5%		
		V001 1000B: 85.5%	V011 0011B: 72.0%	V100 1110B: 58.5%	V110 1001B: 45.0%		
		V001 1001B: 85.0%	V011 0100B: 71.5%	V100 1111B: 58.0%	V110 1010B: 44.5%		
		V001 1010B: 84.5%	V011 0101B: 71.0%	V101 0000B: 57.5%	V110 1011B: 44.0%		

Note: “V” = Valid.

3.5.15 MR13 (MA [7:0] = 0DH) - tCCD_L / tCCD_L_WR / tCCD_L_WR2 / tDLLK

MR13 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				tCCD_L / tCCD_L_WR / tCCD_L_WR2 / tDLLK			

Function	Register Type	Operand	Data	Notes
tCCD_L / tCCD_L_WR / tCCD_L_WR2 / tDLLK	R	OP[3:0]	0000_B: --Thru-- 1111_B: See Table Below	
RFU	RFU	OP[7:4]	RFU	

Table 25 — tCCD_L/tCCD_L_WR/tCCD_L_WR2/tDLLK Encoding Details

Function	OP[3:0]	tCCD_L.min (nCK)	tCCD_L_WR2. min (nCK)	tCCD_L_WR. min (nCK)	tDLLK.min (nCK)	Details	Notes
tCCD_L / tCCD_L_WR / tCCD_L_WR2/ tDLLK	0000	8	16	32	1024	1980MT/s≤ Data Rate ≤ 2100MT/s & 2933MT/s≤ Data Rate =< 3200MT/s	1,2,3
	0001	9	18	36	1024	3200MT/s< Data Rate ≤ 3600MT/s	
	0010	10	20	40	1280	3600MT/s< Data Rate ≤ 4000MT/s	
	0011	11	22	44	1280	4000MT/s< Data Rate ≤ 4400MT/s	
	0100	12	24	48	1536	4400MT/s< Data Rate ≤ 4800MT/s	
	0101	13	26	52	1536	4800MT/s< Data Rate ≤ 5200MT/s	
	0110	14	28	56	1792	5200MT/s< Data Rate ≤ 5600MT/s	
	0111	15	30	60	1792	5600MT/s< Data Rate ≤ 6000MT/s	
	1000	16	32	64	2048	6000MT/s< Data Rate ≤ 6400MT/s	
	1001 ... 1111	All other encodings Reserved					

Note(s)

1 - tCCD_L /tCCD_L_WR/tCCD_L_WR2/tDLLK are programmed according to the value defined in the AC parametric table per operating frequency.

2. The register type is “R” (read only) since MR13 is set by the “Configure tDLLK/tCCD_L/tCCD_L_WR/tCCD_L_WR2” MPC command.

3. Data rate ranges align with Speed Bin Table definitions.

3.5.16 MR14 (MA[7:0]=0EH) - Transparency ECC Configuration

MR14 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECS Mode	Reset ECS Counter	Row Mode/ Code Word Mode	RFU	CID3	CID2	CID1	CID0

Function	Register Type	Operand	Data	Notes
ECS Error Register Index/ MBIST Rank Select	R/W	OP[3:0]	CID[3:0]	1,2,3,4,5
RFU	RFU	OP[4]	RFU	
Code Word/Row Count	R/W	OP[5]	0B: ECS counts Rows with errors 1B: ECS counts Code words with errors	1
ECS Reset Counter	W	OP[6]	0B: Normal (Default) 1B: Reset ECC Counter	1,4
ECS Mode	R/W	OP[7]	0B: Manual ECS Mode Disabled (Default) 1B: Manual ECS Mode Enabled	1

Notes:

1 - MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data and MR22 MBIST transparency data. On 3DS devices that support optional MBIST/mPPR, prior to MBIST initialization via MR23:OP[4] followed by guard keys, MR14:OP[3:0] must be programmed according to the logical rank that is desired to perform MBIST.

2 - CID[3:0] encoding is based on the stack height of the device and varies depending on the number of dies in the stack.

3 - For Monolithic DDR5, CID[3:0] should be set to 0.

4 - ECS stands for Error Check Scrub operation.

5- On 3DS devices that support optional MBIST/mPPR, prior to MBIST initialization via MR23:OP[4] followed by guard keys, MR14:OP[3:0] must be programmed according to the logical rank that is desired to perform MBIST. Once MBIST completes, the transparency status reflected in MR22:OP[2:0] will apply to the logical rank that was programmed in MR14:OP[3:0] prior to the last MBIST run.

3.5.17 MR15 (MA[7:0]=0F$_H$) - Transparency ECC Threshold per Gb of Memory Cells and Automatic ECS in Self Refresh

MR15 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
x4 Writes	ECS Writeback	RFU		Automatic ECS in Self Refresh	ECS Error Threshold Count (ETC)		

Function	Register Type	Operand	Data	Notes
ECS Error Threshold Count (ETC)	R/W	OP[2:0]	000_B: 4 001_B: 16 010_B: 64 011_B: 256 (Default) 100_B: 1024 101_B: 4096 110_B: RFU 111_B: RFU	
Automatic ECS in Self Refresh	W	OP[3]	0_B: Automatic ECS disabled in Self-Refresh in Manual ECS mode (default) 1_B: Automatic ECS enabled in Self-Refresh in Manual ECS mode	
RFU	R/W	OP[5:4]	RFU	
ECS Writeback	R/W	OP[6]	0B: Do not suppress writeback of Data and ECC Check Bits (Default) 1B: Suppress writeback of Data and ECC Check Bits (Optional)	
x4 Writes	R/W	OP[7]	0B: Do not suppress writeback of Data during RMW (Default) 1B: Suppress writeback of Data during RMW (Optional)	

Notes:

1 - MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data.

2 - DDR5 performs Automatic ECS operation while in Self-Refresh mode either by enabling MR15:OP[3]=1_B (Automatic ECS in Self-Refresh enable) or disabling MR14:OP[7]=0_B (Automatic ECS mode enable).

3 - If the Automatic ECS in Self-Refresh is enabled, transparency mode-registers updated cannot be controlled by the number of Manual ECS operation MPC command since the ECS counter is increased by both manual ECS command and the Automatic ECS Operation in Self-Refresh mode.

3.5.18 MR16 (MA [7:0] = 10_H) - Row Address with Max Errors 1

MR16 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
R7	R6	R5	R4	R3	R2	R1	R0

Function	Register Type	Operand	Data	Notes
Max Row Error Address R[7:0]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count	1

Notes:

1 - MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data

3.5.19 MR17 (MA [7:0] = 11_H) - Row Address with Max Errors 2

MR17 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
R15	R14	R13	R12	R11	R10	R9	R8

Function	Register Type	Operand	Data	Notes
Max Row Error Address R[15:8]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count	1

Notes:

1 - MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data

3.5.20 MR18 (MA [7:0] = 12_H) - Row Address with Max Errors 3

MR18 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	BG2	BG1	BG0	BA1	BA0	R17	R16

Function	Register Type	Operand	Data	Notes
Max Row Error Address BG[2:0],BA[1,0], R[17,16]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count	1
RFU	RFU	OP[7]	RFU	

Notes:

1 - MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data

3.5.21 MR19 (MA [7:0] = 13_H) - Max Row Error Count

MR19 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR	RFU	REC5	REC4	REC3	REC2	REC1	REC0

Function	Register Type	Operand	Data	Notes
Max Row Error Count REC[5:0]	R	OP[5:0]	Contains number of errors within the row with the most errors	1
RFU	RFU	OP[6]	RFU	
PASR	R	OP[7]	0 = PASR not supported 1 = PASR supported	

Notes:

1 - MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data.

3.5.22 MR20 (MA [7:0] = 14_H) - Error Count (EC)

MR20 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Function	Register Type	Operand	Data	Notes
Error Count EC[7:0]	R	OP[7:0]	Contains the error count range data	1

Notes:

1 - MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data.

3.5.23 MR21 (MA [7:0] = 15_H) - RFU

MR21 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

Function	Register Type	Operand	Data	Notes
RFU	RFU	OP[7:0]	RFU	1

Notes:

3.5.24 MR22 (MA [7:0] = 16_H) - MBIST/mPPR Transparency

MR22 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					MBIST/mPPR Transparency (Optional)		

Note 2 applies to the entire table

Function	Register Type	Operand	Data	Notes
MBIST/mPPR Transparency (Optional)	R	OP[2:0]	000_B: MBIST hasn't run since INIT OR no fails remain after most recent run (Default)	1
			001_B: Fails remain	
			010_B: Unrepairable fails remain	
			011_B: MBIST should be run again	
			100B-111_B: Reserved	
RFU	RFU	OP[7:3]	RFU	

Notes:

1. The host should track whether MBIST has run since INIT. If MBIST is run and finds no fails, this transparency state will remain set to 000_B.
2. On 3DS devices, transparency status is applicable only to the logical rank selected by MR14:OP[3:0] prior to previous MBIST run.

3.5.25 MR23 (MA [7:0] = 17_H) - MBIST/PPR Settings

MR23 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		RFU	MBIST (Optional)	mPPR (Optional)	sPPR		hPPR

Function	Register Type	Operand	Data	Notes
hPPR	R/W	OP[0]	0_B: Disable 1_B: Enable	1
sPPR	R/W	OP[1]	0_B: Disable 1_B: Enable See OP[2] for definition with sPPR Undo/Lock Implemented	1
	SR/W	OP[2]	DRAM Status Read (SR): 0_B: Not Implemented (Default) 1_B: sPPR Undo/Lock Implemented Host Write (W) for OP[2:1] 00_B: Disabled (Normal Operation) 01_B: sPPR Enabled 10_B: sPPR Undo Enabled 11_B: sPPR Lock Enabled	
mPPR	W	OP[3]	0_B: Disable 1_B: Enable (Optional)	1
MBIST	SR/W	OP[4]	DRAM Status Read (SR): 0_B: No MBIST/mPPR Support 1_B: Supports MBIST/mPPR (Optional) Host Write (W): 0_B: MBIST Disabled 1_B: MBIST Enable	1,2
RFU	RFU	OP[7:5]	RFU	

Note:

1. Only one of these opcode bits may be programmed by the host to 1 at any given time. If any one of these opcode bits are enabled, the remaining bits must be programmed to 0.
2. DRAM will automatically write to 0 when MBIST completes. Therefore, the host is not required to program to zero before performing MBIST again.

3.5.26 MR24 (MA [7:0] = 18_H) - PPR Guard Key

MR24 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PPR Guard Key							

Function	Register Type	Operand	Data	Notes
PPR Guard Key	W	OP[7:0]	See PPR Section for Sequence	

3.5.27 MR25 (MA[7:0]=19_H) - Read Training Mode Settings

MR25 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				Continu-ous Burst Mode	LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pattern Format

Function	Register Type	Operand	Data	Notes
Read Training Pattern Format	R/W	OP[0]	0B: Serial 1B: LFSR	
LFSR0 Pattern Option	R/W	OP[1]	0B: LFSR 1B: Clock	
LFSR1 Pattern Option	R/W	OP[2]	0B: LFSR 1B: Clock	
Continuous Burst Mode	R/W	OP[3]	0B: MRR command based (Default) 1B: Continuous Burst Output	
RFU	RFU	OP[7:4]	RFU	

3.5.28 MR26 (MA[7:0]=1A$_H$) - Read Pattern Data0 / LFSR0

MR26 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Data0 / LFSR0 Seed							

Function	Register Type	Operand	Data	Notes
Read Pattern / LFSR Seed UI 0	R/W	OP[0]	UI<7:0> data for serial mode, LFSR0 seed for LFSR mode	1
Read Pattern / LFSR Seed UI 1	R/W	OP[1]		
Read Pattern / LFSR Seed UI 2	R/W	OP[2]		
Read Pattern / LFSR Seed UI 3	R/W	OP[3]		
Read Pattern / LFSR Seed UI 4	R/W	OP[4]		
Read Pattern / LFSR Seed UI 5	R/W	OP[5]		
Read Pattern / LFSR Seed UI 6	R/W	OP[6]		
Read Pattern / LFSR Seed UI 7	R/W	OP[7]		

Note:

1 - The default value for the **Read Training Pattern Data0/LFSR0** register setting is: 0x5A.

3.5.29 MR27 (MA[7:0]=1B$_H$) - Read Pattern Data1 / LFSR1

MR27 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Data1 / LFSR1 Seed							

Function	Register Type	Operand	Data	Notes
Read Pattern / LFSR Seed UI 8	R/W	OP[0]	UI<15:8> data for serial mode, LFSR1 seed for LFSR mode	1
Read Pattern / LFSR Seed UI 9	R/W	OP[1]		
Read Pattern / LFSR Seed UI 10	R/W	OP[2]		
Read Pattern / LFSR Seed UI 11	R/W	OP[3]		
Read Pattern / LFSR Seed UI 12	R/W	OP[4]		
Read Pattern / LFSR Seed UI 13	R/W	OP[5]		
Read Pattern / LFSR Seed UI 14	R/W	OP[6]		
Read Pattern / LFSR Seed UI 15	R/W	OP[7]		

Note:

1 - The default value for the Read Training Pattern Data1/LFSR1 register setting is: 0x3C.

3.5.30 MR28 (MA[7:0]=1C$_H$) - Read Pattern Invert DQL7:0 (DQ7:0)

MR28 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Invert DQL7:0 (DQ7:0)							

Function	Register Type	Operand	Data	Notes
DQ Invert (Lower DQ Bits)	R/W	OP[0]	DQL0 (DQ0) 0_B: Normal 1_B: Invert	1
	R/W	OP[1]	DQL1 (DQ1) 0_B: Normal 1_B: Invert	
	R/W	OP[2]	DQL2 (DQ2) 0_B: Normal 1_B: Invert	
	R/W	OP[3]	DQL3 (DQ3) 0_B: Normal 1_B: Invert	
	R/W	OP[4]	DQL4 (DQ4) 0_B: Normal 1_B: Invert	
	R/W	OP[5]	DQL5 (DQ5) 0_B: Normal 1_B: Invert	
	R/W	OP[6]	DQL6 (DQ6) 0_B: Normal 1_B: Invert	
	R/W	OP[7]	DQL7 (DQ7) 0_B: Normal 1_B: Invert	

Note:

1 - The default value for the **Read Training Pattern Invert DQL7:0 (DQ7:0)** register setting is: 0x00.

3.5.31 MR29 (MA[7:0]= D_H) - Read Pattern Invert DQU7:0 (DQ15:8)

MR29 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Invert DQU7:0 (DQ15:8)							

Function	Register Type	Operand	Data	Notes
DQ Invert (Upper DQ Bits)	R/W	OP[0]	DQU0 (DQ8) 0_B: Normal 1_B: Invert	1
	R/W	OP[1]	DQU1 (DQ9) 0_B: Normal 1_B: Invert	
	R/W	OP[2]	DQU2 (DQ10) 0_B: Normal 1_B: Invert	
	R/W	OP[3]	DQU3 (DQ11) 0_B: Normal 1_B: Invert	
	R/W	OP[4]	DQU4 (DQ12) 0_B: Normal 1_B: Invert	
	R/W	OP[5]	DQLU5 (DQ13) 0_B: Normal 1_B: Invert	
	R/W	OP[6]	DQU6 (DQ14) 0_B: Normal 1_B: Invert	
	R/W	OP[7]	DQU7 (DQ15) 0_B: Normal 1_B: Invert	

Note:

1 - The default value for the **Read Training Pattern Invert DQU7:0 (DQ15:8)** register setting is: 0x00.

3.5.32 MR30 (MA[7:0]=1E$_H$) - Read LFSR Assignments

MR30 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LFSR Assignment DQL7/ DQU7	LFSR Assignment DQL6/ DQU6	LFSR Assignment DQL5/ DQU5	LFSR Assignment DQL4/ DQU4	LFSR Assignment DQL3/ DQU3	LFSR Assignment DQL2/ DQU2	LFSR Assignment DQL1/ DQU1	LFSR Assignment DQL0/ DQU0

Function	Register Type	Operand	Data	Notes
LFSR Assignment DQL0/DQU0	R/W	OP[0]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	1
LFSR Assignment DQL1/DQU1	R/W	OP[1]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL2/DQU2	R/W	OP[2]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL3/DQU3	R/W	OP[3]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL4/DQU4	R/W	OP[4]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL5/DQU5	R/W	OP[5]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL6/DQU6	R/W	OP[6]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL7/DQU7	R/W	OP[7]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	

Note:

1 - The default value for the **Read LFSR Assignments** register setting is: 0xFE.

3.5.33 MR31 (MA[7:0]=1F$_H$) - Read Training Pattern Address

MR31 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Address							

Function	Register Type	Operand	Data	Notes
Read Training Pattern Address	R	OP[7:0]	This MR address is reserved. There are no specific register fields associated with this address. In response to the MRR to this address the DRAM shall send the BL16 read training pattern. All 8 bits associated with this MR address are reserved.	

3.5.34 MR32 (MA[7:0]=20H) - CK & CS ODT

MR32 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA_ODT Strap Value	CS ODT			CK ODT		

Function	Register Type	Operand	Data	Notes
CK ODT	R	OP[2:0]	000_B: RTT_OFF (Disable) Group A default 001_B: RZQ/0.5 (480) 010_B: RZQ/1 (240) 011_B: RZQ/2 (120) 100_B: RZQ/3 (80) 101_B: RZQ/4 (60) 110_B: RFU 111_B: RZQ/6 (40) Group B default	1
CS ODT	R	OP[5:3]	000_B: RTT_OFF (Disable) Group A default 001_B: RZQ/0.5 (480) 010_B: RZQ/1 (240) 011_B: RZQ/2 (120) 100_B: RZQ/3 (80) 101_B: RZQ/4 (60) 110_B: RFU 111_B: RZQ/6 (40) Group B default	1
CA_ODT Strap Value	R	OP[6]	0_B: Strap Configured to Group A 1_B: Strap Configured to Group B	2
RFU	RFU	OP[7]	RFU	

Notes:

1 - This mode register is programmed via an explicit MPC command only.

2 - Strapping for ODT on Command and Address. The DRAM applies to Group A settings if the CA_ODT pin is connected to VSS and applies Group B settings if the pin is connected to VDD. This MR is used to confirm the DRAM's setting for that config.

3.5.35 MR33 (MA[7:0]=21H) - CA & DQS_PARK ODT MR33 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		DQS_RTT_PARK			CA ODT		

Function	Register Type	Operand	Data	Notes
CA ODT	R	OP[2:0]	000_B: RTT_OFF (Disable) Group A default 001_B: RZQ/0.5 (480) 010_B: RZQ/1 (240) 011_B: RZQ/2 (120) 100_B: RZQ/3 (80) Group B default 101_B: RZQ/4 (60) 110_B: RFU 111_B: RZQ/6 (40)	1
DQS_RTT_PARK	R	OP[5:3]	000_B: RTT_OFF default 001_B: RZQ (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) 111_B: RZQ/7 (34)	1
RFU	RFU	OP[7:6]	RFU	

Notes:

1 - This mode register is programmed via an explicit MPC command only.

3.5.36 MR34 (MA[7:0]=22_H) - RTT_PARK & RTT_WRMR34 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		RTT_WR			RTT_PARK		

Function	Register Type	Operand	Data	Notes
RTT_PARK	R	OP[2:0]	000_B: RTT_OFF default 001_B: RZQ (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) 111_B: RZQ/7 (34)	1
RTT_WR	R/W	OP[5:3]	000_B: RTT_OFF 001_B: RZQ (240) default 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) 111_B: RZQ/7 (34)	
RFU	RFU	OP[7:6]	RFU	

Notes:

1 - This mode register is programmed via an explicit MPC command only.

3.5.37 MR35 (MA[7:0]=23_H) - RTT_NOM_WR & RTT_NOM_RD

MR35 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		RTT_NOM_RD			RTT_NOM_WR		

Function	Register Type	Operand	Data	Notes
RTT_NOM_WR	R/W	OP[2:0]	000_B: RTT_OFF 001_B: RZQ (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) default 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) 111_B: RZQ/7 (34)	
RTT_NOM_RD	R/W	OP[5:3]	000_B: RTT_OFF 001_B: RZQ (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) default 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) 111_B: RZQ/7 (34)	
RFU	RFU	OP[7:6]	RFU	

3.5.38 MR36 (MA[7:0]=24_H) - RTT Loopback

MR36 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					RTT Loopback		

Function	Register Type	Operand	Data	Notes
RTT Loopback	R/W	OP[2:0]	000_B: RTT_OFF Default 001_B: RFU 010_B: RFU 011_B: RFU 100_B: RFU 101_B: RZQ/5 (48) 110_B: RFU 111_B: RFU	1, 2
RFU	RFU	OP[7:3]	RFU	

1. When Loopback is disabled, both LBDQS and LBDQ pins are either at HiZ or Termination Mode this configuration. When Loopback is enabled, it is in driver mode.

3.5.39 MR37 (MA[7:0]= 25_H) - ODTL Write Control Offset

MR37 Register Information

This byte is setup to allow the host controller to push out or pull in the Write RTT enable time (tODTLon_WR) or the Write RTT disable time (tODTLoff_WR) outside of the default setting. The default state is based on internal DRAM design and is defined in Table 167 in the ODT Configuration section. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_WR_Offset			ODTLon_WR_Offset		

Function	Register Type	Operand	Data	Notes
ODTLon_WR_Offset	R/W	OP[2:0]	000_B: RFU 001_B: -4 Clocks 010_B: -3 Clocks 011_B: -2 Clocks 100_B: -1 Clock - Default 101_B: 0 Clock 110_B: +1 Clock 111_B: +2 Clocks	
ODTLoff_WR_Offset	R/W	OP[5:3]	000_B: RFU 001_B: +4 Clocks 010_B: +3 Clocks 011_B: +2 Clocks 100_B: +1 Clock 101_B: 0 Clock - Default 110_B: -1 Clock 111_B: -2 Clocks	
RFU	RFU	OP[7:6]	RFU	

3.5.40 MR38 (MA[7:0]=26_H) - ODTL NT Write Control Offset

MR38 Register Information

This byte is setup to allow the host controller to push out or pull in the Non-Target Write RTT enable time (tODTLon_WR_NT) or the Non-Target Write RTT disable time (tODTLoff_WR_NT) outside of the default setting. The default state is based on internal DRAM design and is defined in Table 167 in the ODT Configuration section. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_WR_NT_Offset			ODTLon_WR_NT_Offset		

Function	Register Type	Operand	Data	Notes
ODTLon_WR_NT_Offset	R/W	OP[2:0]	000_B: RFU 001_B: -4 Clocks 010_B: -3 Clocks 011_B: -2 Clocks 100_B: -1 Clock - Default 101_B: 0 Clock 110_B: +1 Clock 111_B: +2 Clocks	
ODTLoff_WR_NT_Offset	R/W	OP[5:3]	000_B: RFU 001_B: +4 Clocks 010_B: +3 Clocks 011_B: +2 Clocks 100_B: +1 Clock 101_B: 0 Clock - Default 110_B: -1 Clock 111_B: -2 Clocks	
RFU	RFU	OP[7:6]	RFU	

3.5.41 MR39 (MA[7:0]=27_H) - ODTL NT Read Control Offset

MR39 Register Information

This byte is setup to allow the host controller to push out or pull in the Non-Target Read RTT enable time (tODTLon_RD_NT) or the Non-Target Read RTT disable time (tODTLoff_RD_NT) outside of the default setting. The default state is based on internal DRAM design and is defined in Table 167 in the ODT Configuration section. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_RD_NT_Offset			ODTLon_RD_NT_Offset		

Function	Register Type	Operand	Data	Notes
ODTLon_RD_NT_Offset	**R/W**	**OP[2:0]**	000_B: RFU 001_B: RFU 010_B: -3 Clocks 011_B: -2 Clocks 100_B: -1 Clock - Default 101_B: 0 Clock 110_B: +1 Clock 111_B: RFU	
ODTLoff_RD_NT_Offset	**R/W**	**OP[5:3]**	000_B: RFU 001_B: RFU 010_B: +3 Clocks 011_B: +2 Clocks 100_B: +1 Clock 101_B: 0 Clock - Default 110_B: -1 Clock 111_B: RFU	
RFU	**RFU**	**OP[7:6]**	RFU	

3.5.42 MR40 (MA[7:0]=28_H) - Read DQS Offset Timing

MR40 Register Information

This byte is used for configuring the DRAM to support different HOST receiver designs.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					Read DQS offset timing		

Function	Register Type	Operand	Data	Notes
Read DQS offset timing	**R/W**	**OP[2:0]**	000_B: 0 Clock (DEFAULT) 001_B: 1 Clock 010_B: 2 Clocks 011_B: 3 Clocks 100_B: RFU 101_B: RFU 110_B: RFU 111_B: RFU	
RFU	**RFU**	**OP[7:3]**	RFU	

Note(s):

1. When operating at low speed(CL <= 30), tRPRE + Read DQS Offset >= 5 Clocks cannot be supported.

	tRPRE \ DQS Offset	0	1	2	3
When CL <= 30	1	O	O	O	O
	2	O	O	O	X
	3	O	O	X	X
	4	O	X	X	X

3.5.43 MR41 (MA[7:0]=29_H) - RFU -

MR41 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							

Function	Register Type	Operand	Data	Notes

3.5.44 MR42 (MA[7:0]=$2A_H$) - DCA Types Supported

MR42 Register Information

This byte is used for configuring DCA

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DCA Training Assist Mode		DCA Types Supported	

Function	Register Type	Operand	Data	Notes
DCA Types Supported	R	OP[1:0]	00B: Device does not support DCA 01B: Device supports DCA for single/two-phase internal clock(s) 10B: Device supports DCA for 4-phase internal clocks 11B: RFU	
DCA Training Assist Mode	R/W	OP[3:2]	00B: Disable (default) 01B: MRR (or Read) synchronized with IBCLK is blocked 10B: MRR (or Read) synchronized with ICLK is blocked 11B: RFU	1,2,3,4,5,6
RFU	RFU	OP[7:4]	RFU	

Note(s):
1. When “MRR (or Read) synchronized with IBCLK is blocked” is set by MR42 OP[3:2]=01b, DQs caused by MRR (or Read) synchronized with IBCLK are driven HIGH.
2. When “MRR (or Read) synchronized with ICLK is blocked” is set by MR42 OP[3:2]=10b, DQs caused by MRR (or Read) synchronized with ICLK are driven HIGH.
3. DQS_t/DQS_c output normal toggling waveforms meaning that DQS_t/DQS_c are not affected by the settings of DCA Assist Mode MR42 OP[3:2].
4. The CRC function is not supported during DCA Training Assist Mode.
5. DCA Training Assist Mode is only supported by DRAMs with DCAs that have 4-phase internal clocks
6. If MR42:OP[3:2] is set to either 01B or 10B, odd-gap READ or odd-gap Mode Register Read Pattern commands should follow the tMRR timing spec.

3.5.45 MR43 (MA[7:0]=2B$_H$) - DCA Settings 1

MR43 Register Information

This byte is used for configuring TRR

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Sign Bit for OP[6:4]	DCA for IBCLK in 4-phase clocks			Sign Bit for OP[2:0]	DCA for single/two-phase clock(s) or QCLK in 4-phase clocks		

Function	Register Type	Operand	Data	Notes
DCA for single/two-phase clock(s) or QCLK in 4-phase clocks	W	OP[2:0]	000_B: DCA step +0 (default) 001_B: DCA step +1 010_B: DCA step +2 011_B: DCA step +3 100_B: DCA step +4 101_B: DCA step +5 110_B: DCA step +6 111_B: DCA step +7	1
Sign Bit for OP[2:0]	W	OP[3]	0_B: Positive Offset (default) 1_B: Negative Offset	1
DCA for IBCLK in 4-phase clocks	W	OP[6:4]	000_B: DCA step +0 (default) 001_B: DCA step +1 010_B: DCA step +2 011_B: DCA step +3 100_B: DCA step +4 101_B: DCA step +5 110_B: DCA step +6 111_B: DCA step +7	2
Sign Bit for OP[6:4]	W	OP[7]	0_B: Positive Offset (default) 1_B: Negative Offset	2

Note(s):
1. These settings can only be applied if MR42:OP[1:0] =**01_B** or 1**0_B**.
2. These settings can only be applied if MR42:OP[1:0] =1**0_B**.

3.5.46 MR44 (MA[7:0]=$2C_H$) - DCA Settings 2

MR44 Register Information

This byte is used for configuring TRR

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				Sign Bit for QBCLK in 4-phase clocks	DCA for QBCLK in 4-phase clocks		

Function	Register Type	Operand	Data	Notes
DCA for QBCLK in 4-phase clocks	W	OP[2:0]	000_B: DCA step +0 (default) 001_B: DCA step +1 010_B: DCA step +2 011_B: DCA step +3 100_B: DCA step +4 101_B: DCA step +5 110_B: DCA step +6 111_B: DCA step +7	1
Sign Bit for QBCLK in 4-phase clocks	W	OP[3]	0_B: Positive Offset (default) 1_B: Negative Offset	1
RFU	RFU	OP[7:4]	RFU	

Note(s):
1. These settings can only be applied if MR42 OP[1:0]=10_B.

3.5.47 MR45 (MA[7:0]=2D$_H$) - DQS Interval Control

MR45 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Interval Timer Run Time							

Function	Register Type	Operand	Data	Notes
DQS Interval Timer Run Time	W	OP[7:0]	0000 0000$_B$: DQS interval timer stop via MPC Command (Default) 0000 0001$_B$: DQS timer stops automatically at 16th clocks after timer start 0000 0010$_B$: DQS timer stops automatically at 32nd clocks after timer start 0000 0011$_B$: DQS timer stops automatically at 48th clocks after timer start 0000 0100$_B$: DQS timer stops automatically at 64th clocks after timer start ---------- Thru ---------- 0011 1111$_B$: DQS timer stops automatically at (63X16)th clocks after timer start 01XX XXXX$_B$: DQS timer stops automatically at 2048th clocks after timer start 10XX XXXX$_B$: DQS timer stops automatically at 4096th clocks after timer start 11XX XXXX$_B$: DQS timer stops automatically at 8192nd clocks after timer start	1, 2

Note(s)
1. MPC command with OP[7:0]=0000 0110$_B$ (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR45:OP[7:0] = 00000000$_B$.
2. MPC command with OP[7:0]=0000 0110$_B$ (Stop DQS Interval Oscillator) is illegal with non-zero values in MR45:OP[7:0].

3.5.48 MR46 (MA[7:0]=2E$_H$) - DQS Osc Count - LSB

MR46 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count - LSB	R	OP[7:0]	0 - 255 LSB DRAM DQS Oscillator Count	

NOTE:
1. MR46 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR46 and MR47 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR46/MR47.

3.5.49 MR47 (MA[7:0]=2F$_H$) - DQS Osc Count - MSB

MR47 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count - MSB	R	OP[7:0]	0 - 255 MSB DRAM DQS Oscillator Count	

NOTE:
1. MR47 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR46 and MR47 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR46/MR47.

3.5.50 MR48 (MA[7:0]=30_H) - Write Pattern Mode

MR48 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Write Pattern Mode							

Function	Register Type	Operand	Data	Notes
DQL0/DQU0	R/W	OP[0]	Valid	1,2
DQL1/DQU1	R/W	OP[1]		
DQL2/DQU2	R/W	OP[2]		
DQL3/DQU3	R/W	OP[3]		
DQL4/DQU4	R/W	OP[4]		
DQL5/DQU5	R/W	OP[5]		
DQL6/DQU6	R/W	OP[6]		
DQL7/DQU7	R/W	OP[7]		

NOTES:

1. OP[7:0] can be independently programmed with either “0” or “1”.
2. Default is all zeros for OP[7:0]

3.5.51 MR50 (MA[7:0]=32_H) - Write CRC Settings

MR50 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	Write CRC auto-dis-able status	Write CRC auto-dis-able enable	Write CRC error status	Write CRC enable upper nibble	Write CRC enable lower nibble	Read CRC enable

Function	Register Type	Operand	Data	Notes
Read CRC enable	R/W	OP[0]	0_B: Disable (Default) 1_B: Enable	
Write CRC enable lower nibble	R/W	OP[1]	0_B: Disable (Default) 1_B: Enable	1
Write CRC enable upper nibble	R/W	OP[2]	0_B: Disable (Default) 1_B: Enable	1
Write CRC error status	R/W	OP[3]	0_B: Clear 1_B: Error	2
Write CRC auto-disable enable	R/W	OP[4]	0_B: Disable (Default) 1_B: Enable	
Write CRC auto-disable status	R/W	OP[5]	0_B: Not triggered 1_B: Triggered	
RFU	RFU	OP[6]	RFU	
RFU	RFU	OP[7]	RFU	

Note(s):

1 - When at least one of the two write CRC enable bits is set to '1' in x8, the timing of write CRC enable mode is applied to the entire device (i.e. both nibbles). When write CRC is enabled in one nibble and disabled in the other nibble in x8, then the DRAM does not check CRC errors on the disabled nibble, and hence the ALERT_n signal and any internal status bit related to CRC error is not impacted by the disable nibble.

2. The host shall disable Write CRC, if it was enabled, prior to entering Write Leveling Training mode.

3.5.52 MR51 (MA[7:0]=33_H) - Write CRC Auto-Disable Threshold

MR51 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]

Function	Register Type	Operand	Data	Notes
Write CRC auto-disable threshold	R/W	OP[6:0]	0000000_B: 0 ... 1111111_B: 127	
RFU	RFU	OP[7]	RFU	

3.5.53 MR52 (MA[7:0]=34_H) - Write CRC Auto-Disable Window

MR52 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]

Function	Register Type	Operand	Data	Notes
Write CRC auto-disable window	R/W	OP[6:0]	0000000_B: 0 ... 1111111_B: 127	
RFU	RFU	OP[7]	RFU	

3.5.54 MR53 (MA[7:0]=35_H) - Loopback

MR53 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Loopback Output Mode	Loopback Select Phase		Loopback Output Select				

Function	Register Type	Operand	Data	Notes
Loopback Output Select	R/W	OP[4:0]	00000_B: Loopback Disabled (Default) 00001_B: Loopback DML (X8 and X16 only) 00010_B: Loopback DMU (X16 only) 00011_B: Vendor Specific 00100_B: Vendor Specific 00101_B: RFU ...thru 01111_B: RFU 10000_B: Loopback DQL0 10001_B: Loopback DQL1 10010_B: Loopback DQL2 10011_B: Loopback DQL3 10100_B: Loopback DQL4 (X8 and X16 only) 10101_B: Loopback DQL5 (X8 and X16 only) 10110_B: Loopback DQL6 (X8 and X16 only) 10111_B: Loopback DQL7 (X8 and X16 only) 11000_B: Loopback DQU0 (X16 only) 11001_B: Loopback DQU1 (X16 only) 11010_B: Loopback DQU2 (X16 only) 11011_B: Loopback DQU3 (X16 only) 11100_B: Loopback DQU4 (X16 only) 11101_B: Loopback DQU5 (X16 only) 11110_B: Loopback DQU6 (X16 only) 11111_B: Loopback DQU7 (X16 only)	1, 2
Loopback Select Phase	R/W	OP[6:5]	00_B: Loopback Select Phase A 01_B: Loopback Select Phase B (4-way and 2-way interleave only) 10_B: Loopback Select Phase C (4-way interleave only) 11_B: Loopback Select Phase D (4-way interleave only)	3
Loopback Output Mode	R/W	OP[7]	0B: Normal Output (Default) 1B: Write Burst Output	4

Note(s):

1. When Loopback is disabled, both LBDQS and LBDQ pins are either at HiZ or Termination Mode per MR36:OP[2:0]. Loopback Termination default value is 48-ohms
2. When Loopback is enabled, both LBDQS and LBDQ pins are in driver mode using default RON of 34-ohms
3. Phase A through D selects which bit in the multiplexer is being selected for Loopback output
4. This configures the DRAM Loopback output to either send data out every time the DQS toggles in Normal Output Mode, or to only send data out when enabled by the Write command, so that only write burst data is send out via Loopback.

3.5.55 MR54 (MA[7:0]=36_H) - hPPR Resources

With hPPR, DDR5 can correct one Row address per Bank Group and the Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the hPPR mode entry and repair. (i.e. During the Command/ Address training period). Entry into hPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. After tRCD time, a WR command is used to select the individual DRAM through the DQ bits and to transfer the repair address to the DRAM. After program time, and PRE, the hPPR mode can be exited and normal operation can resume.

MR54 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
hPPR Resource BG1 Bank 3	hPPR Resource BG1 Bank 2	hPPR Resource BG1 Bank 1	hPPR Resource BG1 Bank 0	hPPR Resource BG0 Bank 3	hPPR Resource BG0 Bank 2	hPPR Resource BG0 Bank 1	hPPR Resource BG0 Bank 0

Function	Register Type	Operand	Data	Notes
hPPR Resource BG0 Bank 0	R	OP[0]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	3
hPPR Resource BG0 Bank 1		OP[1]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	3
hPPR Resource BG0 Bank 2		OP[2]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,3
hPPR Resource BG0 Bank 3		OP[3]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,3
hPPR Resource BG1 Bank 0		OP[4]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	3
hPPR Resource BG1 Bank 1		OP[5]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	3
hPPR Resource BG1 Bank 2		OP[6]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,3
hPPR Resource BG1 Bank 3		OP[7]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,3

Note(s):

1. Not valid for 8Gb
2. Not valid for x16
3. MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS DDR5 Stack is referenced in the MR54 through MR57 hPPR resource information.

3.5.56 MR55 (MA[7:0]=37_H) - hPPR Resources

MR55 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
hPPR Resource BG3 Bank 3	hPPR Resource BG3 Bank 2	hPPR Resource BG3 Bank 1	hPPR Resource BG3 Bank 0	hPPR Resource BG2 Bank 3	hPPR Resource BG2 Bank 2	hPPR Resource BG2 Bank 1	hPPR Resource BG2 Bank 0

Function	Register Type	Operand	Data	Notes
hPPR Resource BG2 Bank 0	R	OP[0]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	3
hPPR Resource BG2 Bank 1		OP[1]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	3
hPPR Resource BG2 Bank 2		OP[2]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,3
hPPR Resource BG2 Bank 3		OP[3]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,3
hPPR Resource BG3 Bank 0		OP[4]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	3
hPPR Resource BG3 Bank 1		OP[5]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	3
hPPR Resource BG3 Bank 2		OP[6]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,3
hPPR Resource BG3 Bank 3		OP[7]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,3

Note(s):

1. Not valid for 8Gb
2. Not valid for x16
3. MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS DDR5 Stack is referenced in the MR54 through MR57 hPPR resource information.

3.5.57 MR56 (MA[7:0]=38_H) - hPPR Resources

MR56 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
hPPR Resource BG5 Bank 3	hPPR Resource BG5 Bank 2	hPPR Resource BG5 Bank 1	hPPR Resource BG5 Bank 0	hPPR Resource BG4 Bank 3	hPPR Resource BG4 Bank 2	hPPR Resource BG4 Bank 1	hPPR Resource BG4 Bank 0

Function	Register Type	Operand	Data	Notes
hPPR Resource BG4 Bank 0	R	OP[0]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	2,3
hPPR Resource BG4 Bank 1		OP[1]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	2,3
hPPR Resource BG4 Bank 2		OP[2]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,2,3
hPPR Resource BG4 Bank 3		OP[3]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,2,3
hPPR Resource BG5 Bank 0		OP[4]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	2,3
hPPR Resource BG5 Bank 1		OP[5]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	2,3
hPPR Resource BG5 Bank 2		OP[6]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,2,3
hPPR Resource BG5 Bank 3		OP[7]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,2,3

Note(s):

1. Not valid for 8Gb
2. Not valid for x16
3. MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS DDR5 Stack is referenced in the MR54 through MR57 hPPR resource information.

3.5.58 MR57 (MA[7:0]=39_H) - hPPR Resources

MR57 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
hPPR Resource BG7 Bank 3	hPPR Resource BG7 Bank 2	hPPR Resource BG7 Bank 1	hPPR Resource BG7 Bank 0	hPPR Resource BG6 Bank 3	hPPR Resource BG6 Bank 2	hPPR Resource BG6 Bank 1	hPPR Resource BG6 Bank 0

Function	Register Type	Operand	Data	Notes
hPPR Resource BG6 Bank 0	R	OP[0]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	2,3
hPPR Resource BG6 Bank 1		OP[1]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	2,3
hPPR Resource BG6 Bank 2		OP[2]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,2,3
hPPR Resource BG6 Bank 3		OP[3]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,2,3
hPPR Resource BG7 Bank 0		OP[4]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	2,3
hPPR Resource BG7 Bank 1		OP[5]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	2,3
hPPR Resource BG7 Bank 2		OP[6]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,2,3
hPPR Resource BG7 Bank 3		OP[7]	0_B: hPPR Resource is not available 1_B: hPPR Resource is available	1,2,3

Note(s):

1. Not valid for 8Gb
2. Not valid for x16
3. MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS DDR5 Stack is referenced in the MR54 through MR57 hPPR resource information.

3.5.59 MR58 (MA[7:0]=$3A_H$) - Refresh Management

MR58 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RAAMMT[2:0]			RAAIMT[3:0]				RFM Required

Function	Register Type	Operand	Data	Notes
RFM Required	R	OP[0]	0_B: Refresh Management not required 1_B: Refresh Management required	1
Rolling Accumulated ACT Initial Management Threshold (RAAIMT)	R	OP[4:1]	0000_B- 0011_B: RFU 0100_B: 32 (Normal), 16 (FGR) 0101_B: 40 (Normal), 20 (FGR) ... 1001_B: 72 (Normal), 36 (FGR) 1010_B: 80 (Normal), 40 (FGR) 1011_B-1111_B: RFU	1, 2
Rolling Accumulated ACT Maximum Management Threshold (RAAMMT)	R	OP[7:5]	000_B-010_B: RFU 011_B: 3x (Normal), 6x (FGR) 100_B: 4x (Normal), 8x (FGR) 101_B: 5x (Normal), 10x (FGR) 110_B: 6x (Normal), 12x (FGR) 111_B: RFU	1, 2

Note(s):

1. Refresh Management settings are vendor specific by the MR settings.
2. Only applicable if the Refresh Management Required bit is set to “1” (MR58 OP[0]=1)

3.5.60 MR59 (MA[7:0]=$3B_H$) - RFM RAA Counter

MR59 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFM RAA Counter		ARFM		RFU			

Function	Register Type	Operand	Data	Notes
RFU	RFU	OP[3:0]	RFU	
Adaptive RFM (ARFM)	RW	OP[5:4]	00_B: Default - RAAIMT, RAAMMT, RAADEC 01_B: Level A - RAAIMT-A, RAAMMT-A, RAADEC-A 10_B: Level B - RAAIMT-B, RAAMMT-B, RAADEC-B 11_B: Level C - RAAIMT-C, RAAMMT-C, RAADEC-C	1
RAA Counter Decrement per REF Command	R	OP[7:6]	00_B: RAAIMT 01_B: RAAIMT * 0.5 10_B: RFU 11_B: RFU	1, 2

Note(s):
1. Refresh Management settings are vendor specific by the MR settings.
2. Only applicable if the Refresh Management Required bit is set to “1” (MR58 OP[0]=1).

3.5.61 MR60 Partial Array Self Refresh

MR60 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

Function	Register Type	Operand	Data	Notes
Segment 0 (000)	**W**	**OP0**	0=Normal, 1=Masked	
Segment 1 (001)	**W**	**OP1**	0=Normal, 1=Masked	
Segment 2 (010)	**W**	**OP2**	0=Normal, 1=Masked	
Segment 3 (011)	**W**	**OP3**	0=Normal, 1=Masked	
Segment 4 (100)	**W**	**OP4**	0=Normal, 1=Masked	
Segment 5 (101)	**W**	**OP5**	0=Normal, 1=Masked	
Segment 6 (110)	**W**	**OP6**	0=Normal, 1=Masked	Must be 0 for 24Gbit and 48Gbit devices.
Segment 7 (111)	**W**	**OP7**	0=Normal, 1=Masked	Must be 0 for 24Gbit and 48Gbit devices.

3.5.62 MR61 (MA[7:0]=$3D_H$) - Package Output Driver Test Mode

MR61 Register Information

This MR is used for the characterization of the DRAM package. Refer to the Package Output Driver Test Mode function for more details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RSVD			Package Output Driver Test Mode				

Function	Register Type	Operand	Data	Notes
Package Output Driver Test Mode	W	OP[4:0]	00000_B: Package Test Disabled (Default) 00001_B: Package Test DML 00010_B: Package Test DMU (X16 only) 00011_B: RFU 00100_B: RFU 00101_B: RFU ...thru 01111_B: RFU 10000_B: Package Test DQL0 10001_B: Package Test DQL1 10010_B: Package Test DQL2 10011_B: Package Test DQL3 10100_B: Package Test DQL4 (X8 and X16 only) 10101_B: Package Test DQL5 (X8 and X16 only) 10110_B: Package Test DQL6 (X8 and X16 only) 10111_B: Package Test DQL7 (X8 and X16 only) 11000_B: Package Test DQU0 (X16 only) 11001_B: Package Test DQU1 (X16 only) 11010_B: Package Test DQU2 (X16 only) 11011_B: Package Test DQU3 (X16 only) 11100_B: Package Test DQU4 (X16 only) 11101_B: Package Test DQU5 (X16 only) 11110_B: Package Test DQU6 (X16 only) 11111_B: Package Test DQU7 (X16 only)	1
RSVD	W	OP[7:5]	Must be programmed to 000	

Note(s):
1. TBD

3.5.63 MR62 (MA[7:0]=$3E_H$) - Vendor Specified

MR62 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specified							

Function	Register Type	Operand	Data	Notes

3.5.64 MR63 (MA[7:0]=3F$_H$) - DRAM Scratch Pad

MR63 Register Information

This MR is used by the host controller to read back Control Words from the RCD. Control Words are the RCD equivalent of the DRAM MR registers. The DRAM implements MR63 as a simple read/write register, writable via an MRW to address 3Fh, and readable via an MRR to address 3Fh.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DRAM Scratch Pad							

Function	Register Type	Operand	Data	Notes
DRAM Scratch Pad	R/W	OP[7:0]	Any value is valid	1

NOTE: The contents of this register have no function in the DRAM. Details for this function can be found in the DDR5 RCD01 Specification.

The following data is just for reference and is not part of the DRAM specification.

3.5.64.1 RCD Control Word Usage Example

The method to read an RCD Control Word is as follows:

- *The host controller writes to the RCD's CW Read Pointer, which selects the RCD control word to be read.*
- *The host controller then does an MRW to DRAM MR63. This MRW passes through the RCD to the DRAMs, but is modified by the RCD. The RCD will detect this write to MR63 and replace the data from the host controller with the contents of the RCD register pointed to by the CW Read Pointer.*
- *The host controller will then read the DRAM's MR63, which now contains the value from the desired RCD control word. All DRAMs in the rank will return this same value to the host controller*

3.5.65 MR64 (MA[7:0]=40_H) - NVRAM Paging (RFU)

MR64 Register Information

This MR is reserved for NVRAM paging.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							

Function	Register Type	Operand	Data	Notes

3.5.66 MR65 (MA[7:0]=41_H) - Serial Number 1

MR65 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 1							

Function	Register Type	Operand	Data	Notes
Serial Number 1	R	OP[7:0]	Serial Number 1	1,2

Note(s):
1. The serial number of 0x00 in all bytes is not allowed
2. This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.

3.5.67 MR66 (MA[7:0]=42_H) - Serial Number 2

MR66 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 2							

Function	Register Type	Operand	Data	Notes
Serial Number 2	R	OP[7:0]	Serial Number 2	1,2

Note(s):
1. The serial number of 0x00 in all bytes is not allowed
2. This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.

3.5.68 MR67 (MA[7:0]=43_H) - Serial Number 3

MR67 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 3							

Function	Register Type	Operand	Data	Notes
Serial Number 3	R	OP[7:0]	Serial Number 3	1,2

Note(s):
1. The serial number of 0x00 in all bytes is not allowed
2. This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.

3.5.69 MR68 (MA[7:0]=44_H) - Serial Number 4

MR68 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 4							

Function	Register Type	Operand	Data	Notes
Serial Number 4	R	OP[7:0]	Serial Number 4	1,2

Note(s):
1. The serial number of 0x00 in all bytes is not allowed
2. This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.

3.5.70 MR69 (MA[7:0]=45_H) - Serial Number 5

MR69 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 5							

Function	Register Type	Operand	Data	Notes
Serial Number 5	R	OP[7:0]	Serial Number 5	1,2

Note(s):
1. The serial number of 0x00 in all bytes is not allowed
2. This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.

3.5.71 Mode Register Definitions for DFE

The following mode registers are used to configure the Decision Feedback Equalization (DFE), Per Bit Duty Cycle Adjuster and Per Bit VrefDQ features of the DRAM. The Mode Registers MA[7:0]=70-FF_H are organized in a way such that mode registers for programming of DFE, DCA & VrefDQ configuration per DQ or DM are grouped together. For example:

DQL0 starts at MA[7:0]=80_H, MR128
DQL1 starts at MA[7:0]=88_H, MR136
:
DQU6 starts at MA[7:0]=$F0_H$, MR240
DQU7 starts at MA[7:0]=$F8_H$, MR248

Looking further into the 8-bit binary encoding, MA[6:3] is defined as a direct mapping for DQL0 to DQU7, i.e.,
MA[7:0]=1000:0XXXb for DQ0,
MA[7:0]=1000:1XXXb for DQ1,
:
MA[7:0]=1111:0XXXb for DQU6
MA[7:0]=1111:1XXXb for DQU7.

Table 26 — Visual Representation of DFE, per bit DCA & per bit VrefDQ Mode Register Mapping

MRW Address, Binary	Function	MRW address bits [2:0]							
		000b	001b	010b	011b	100b	101b	110b	111b
0111-0XXX	DML	Gain	Tap1	Tap2	Tap3	Tap4	MR Address Space not currently used		
0111-1XXX	DMU								
1000-0XXX	DQL0								
1000-1XXX	DQL1								
1001-0XXX	DQL2								
1001-1XXX	DQL3								
1010-0XXX	DQL4								
1010-1XXX	DQL5								
1011-0XXX	DQL6								
1011-1XXX	DQL7								
1100-0XXX	DQU0								
1100-1XXX	DQU1								
1101-0XXX	DQU2								
1101-1XXX	DQU3								
1110-0XXX	DQU4								
1110-1XXX	DQU5								
1111-0XXX	DQU6								
1111-1XXX	DQU7								

3.5.62 MR103 (MA[7:0]=67_H) - DQSL_t DCA for IBCLK and QCLK

MR103 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQSL_t IBCLK Sign	RFU	DQSL_t DCA for IBCLK		DQSL_t QCLK sign	RFU	DQSL_t DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQSL_t DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSL_t QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQSL_t DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQSL_t IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.63 MR104 (MA[7:0]=68_H) - DQSL_t DCA for QBCLK

MR104 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DQSL_t QBCLK Sign	RFU	DQSL_t DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQSL_t DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSL_t QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
RFU		OP[7:4]		

3.5.64 MR105 (MA[7:0]=69_H) - DQSL_c DCA for IBCLK and QCLK

MR105 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQSL_c IBCLK Sign	RFU	DQSL_c DCA for IBCLK		DQSL_c QCLK sign	RFU	DQSL_c DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQSL_c DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSL_c QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQSL_c DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQSL_c IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.65 MR106 (MA[7:0]=$6A_H$) - DQSL_c DCA for QBCLK

MR106 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DQSL_c QBCLK Sign	RFU	DQSL_c DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQSL_c DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSL_c QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
RFU		OP[7:4]		

3.5.66 MR107 (MA[7:0]=$6B_H$) - DQSU_t DCA for IBCLK and QCLK

MR107 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQSU_t IBCLK Sign	RFU	DQSU_t DCA for IBCLK		DQSU_t QCLK sign	RFU	DQSU_t DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQSU_t DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSU_t QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQSU_t DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQSU_t IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.67 MR108 (MA[7:0]=$6C_H$) - DQSU_t DCA for QBCLK

MR108 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DQSU_t QBCLK Sign	RFU	DQSU_t DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQSU_t DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSU_t QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
RFU		OP[7:4]		

3.5.68 MR109 (MA[7:0]=6D$_H$) - DQSU_c DCA for IBCLK and QCLK

MR109 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQSU_c IBCLK Sign	RFU	DQSU_c DCA for IBCLK		DQSU_c QCLK sign	RFU	DQSU_c DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQSU_c DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSU_c QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQSU_c DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQSU_c IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.69 MR110 (MA[7:0]=6E$_H$) - DQSU_c DCA for QBCLK

MR110 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DQSU_c QBCLK Sign	RFU	DQSU_c DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQSU_c DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSU_c QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
RFU		OP[7:4]		

3.5.70 MR111 (MA[7:0]=6F$_H$) - DFE Global Settings

MR111 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU			Global DFE Tap-4 Enable	Global DFE Tap-3 Enable	Global DFE Tap-2 Enable	Global DFE Tap-1 Enable	Global DFE Gain Enable

Function	Register Type	Operand	Data	Notes
Global DFE Gain Enable	R/W	OP[0]	0_B: DFE Gain Enabled (DEFAULT) 1_B: DFE Gain Disabled	1, 2
Global DFE Tap-1 Enable	R/W	OP[1]	0_B: DFE Tap-1 Enabled (DEFAULT) 1_B: DFE Tap-1 Disabled	1, 2
Global DFE Tap-2 Enable	R/W	OP[2]	0_B: DFE Tap-2 Enabled (DEFAULT) 1_B: DFE Tap-2 Disabled	1, 2
Global DFE Tap-3 Enable	R/W	OP[3]	0_B: DFE Tap-3 Enabled (DEFAULT) 1_B: DFE Tap-3 Disabled	1, 2
Global DFE Tap-4 Enable	R/W	OP[4]	0_B: DFE Tap-4 Enabled (DEFAULT) 1_B: DFE Tap-4 Disabled	1, 2
RFU	RFU	OP[7:5]	RFU	

Note(s):
1. This bit applies to all DM and DQ pins.
2. Setting MR111:OP[4:0] = 11111_B disables the DFE.

3.5.71 MR112 (MA[7:0]=70_H) thru MR248 (MA[7:0]=$F8_H$) - DFE Gain Bias

MR112 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Gain Bias. The MRs are positioned every 8 MRs (MR112, MR120, MR128, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				Sign Bit Gain Bias	DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DFE Gain Bias	R/W	OP[2:0]	000_B: DFE Gain Bias Step 0 (Default) 001_B: DFE Gain Bias Step 1 010_B: DFE Gain Bias Step 2 011_B: DFE Gain Bias Step 3 100_B: RFU 101_B: RFU 111_B: RFU	1,2,3,4
Sign Bit Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	4
RFU	RFU	OP[7:4]	RFU	

Note(s):

1. Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
3. The number of step size, step values and range are speed dependent
4. Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.72 MR113 (MA[7:0]=71_H) thru MR249 (MA[7:0]=$F9_H$) - DFE Tap-1

MR113 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-1. The MRs are positioned every 8 MRs (MR113, MR121, MR129, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/Disable DFE Tap-1	Sign Bit DFE Tap-1 Bias	DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DFE Tap-1 Bias	R/W	OP[5:0]	000000_B: DFE Tap-1 Bias Step 0 (Default) 000001_B: DFE Tap-1 Bias Step 1 000010_B: DFE Tap-1 Bias Step 2 000011_B: DFE Tap-1 Bias Step 3 000100_B: DFE Tap-1 Bias Step 4 000101_B: DFE Tap-1 Bias Step 5 : 100110_B: DFE Tap-1 Bias Step 38 100111_B: DFE Tap-1 Bias Step 39 101000_B: DFE Tap-1 Bias Step 40 101001_B: RFU : 111111_B: RFU	1,2,3,4
Sign Bit DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	4
Enable/Disable DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	4

Note(s):

1. Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
3. The number of step size, step values and range are speed dependent
4. Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.73 MR114 (MA[7:0]=72_H) thru MR250 (MA[7:0]=FA_H) - DFE Tap-2

MR114 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-2. The MRs are positioned every 8 MRs (MR114, MR122, MR130, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/Disable DFE Tap-2	Sign Bit DFE Tap-2 Bias	DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DFE Tap-2 Bias	R/W	OP[5:0]	000000_B: DFE Tap-2 Bias Step 0 (Default) 000001_B: DFE Tap-2 Bias Step 1 000010_B: DFE Tap-2 Bias Step 2 000011_B: DFE Tap-2 Bias Step 3 000100_B: DFE Tap-2 Bias Step 4 000101_B: DFE Tap-2 Bias Step 5 : 001101_B: DFE Tap-2 Bias Step 13 001110_B: DFE Tap-2 Bias Step 14 001111_B: DFE Tap-2 Bias Step 15 010000_B: RFU : 111111_B: RFU	1,2,3,4
Sign Bit DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	4
Enable/Disable DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	4

Note(s):

1. Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
3. The number of step size, step values and range are speed dependent
4. Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.74 MR115 (MA[7:0]=73_H) thru MR251 (MA[7:0]=FB_H) - DFE Tap-3

MR115 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Gain Bias. The MRs are positioned every 8 MRs (MR115, MR123, MR131, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/Disable DFE Tap-3	**Sign Bit DFE Tap-3 Bias**	**DFE Tap-3 Bias Programming**					

Function	Register Type	Operand	Data	Notes
DFE Tap-3 Bias	**R/W**	**OP[5:0]**	000000_B: DFE Tap-3 Bias Step 0 (Default) 000001_B: DFE Tap-3 Bias Step 1 000010_B: DFE Tap-3 Bias Step 2 000011_B: DFE Tap-3 Bias Step 3 000100_B: DFE Tap-3 Bias Step 4 000101_B: DFE Tap-3 Bias Step 5 : 001010_B: DFE Tap-3 Bias Step 10 001011_B: DFE Tap-3 Bias Step 11 001100_B: DFE Tap-3 Bias Step 12 001101_B: RFU : 111111_B: RFU	1,2,3,4
Sign Bit DFE Tap-3 Bias	**R/W**	**OP[6]**	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	4
Enable/Disable DFE Tap-3	**R/W**	**OP[7]**	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	4

Note(s):

1. Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
3. The number of step size, step values and range are speed dependent
4. Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.75 MR116 (MA[7:0]=74_H) thru MR252 (MA[7:0]=FC_H) - DFE Tap-4

MR116 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-4. The MRs are positioned every 8 MRs (MR116, MR124, MR132, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/Disable DFE Tap-4	Sign Bit DFE Tap-4 Bias	DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DFE Tap-4 Bias	R/W	OP[5:0]	000000_B: DFE Tap-4 Bias Step 0 (Default) 000001_B: DFE Tap-4 Bias Step 1 000010_B: DFE Tap-4 Bias Step 2 000011_B: DFE Tap-4 Bias Step 3 000100_B: DFE Tap-4 Bias Step 4 000101_B: DFE Tap-4 Bias Step 5 000110_B: DFE Tap-4 Bias Step 6 000111_B: DFE Tap-4 Bias Step 7 001000_B: DFE Tap-4 Bias Step 8 001001_B: DFE Tap-4 Bias Step 9 001010_B: RFU : 111111_B: RFU	1,2,3,4
Sign Bit DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	4
Enable/Disable DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	4

Note(s):

1. Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
3. The number of step size, step values and range are speed dependent
4. Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.76 MR117 (MA[7:0]=75_H) - RFU

3.5.77 MR118 (MA[7:0]=76_H) - DML VrefDQ Offset

MR118 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DML VREFDQ sign	DML VREFDQ Offset			RFU			

Function	Register Type	Operand	Data	Notes
RFU		OP[3:0]		
DML VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DML VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.78 MR126 (MA[7:0]=$7E_H$) - DMU VrefDQ Offset

MR126 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DMU VREFDQ sign	DMU VREFDQ Offset			RFU			

Function	Register Type	Operand	Data	Notes
RFU		OP[3:0]		
DMU VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DMU VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.79 MR133 (MA[7:0]=85_H) - DQL0 DCA for IBCLK and QCLK

MR133 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL0 IBCLK Sign	RFU	DQL0 DCA for IBCLK		DQL0 QCLK sign	RFU	DQL0 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL0 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL0 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL0 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL0 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.80 MR134 (MA[7:0]=86_H) - DQL0 DCA for QBCLK and DQL0 VrefDQ Offset

MR134 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL0 VREFDQ sign	DQL0 VREFDQ Offset			DQL0 QBCLK Sign	RFU	DQL0 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL0 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL0 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL0 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL0 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.81 MR141 (MA[7:0]=8D$_H$) - DQL1 DCA for IBCLK and QCLK

MR141 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL1 IBCLK Sign	RFU	DQL1 DCA for IBCLK		DQL1 QCLK sign	RFU	DQL1 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL1 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL1 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL1 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL1 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.82 MR142 (MA[7:0]=8E$_H$) - DQL1 DCA for QBCLK and DQL1 VrefDQ Offset

MR142 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL1 VREFDQ sign	DQL1 VREFDQ Offset			DQL1 QBCLK Sign	RFU	DQL1 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL1 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL1 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL1 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL1 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.83 MR149 (MA[7:0]=95_H) - DQL2 DCA for IBCLK and QCLK

MR149 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL2 IBCLK Sign	RFU	DQL2 DCA for IBCLK		DQL2 QCLK sign	RFU	DQL2 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL2 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL2 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL2 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL2 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.84 MR150 (MA[7:0]=96_H) - DQL2 DCA for QBCLK and DQL2 VrefDQ Offset

MR150 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL2 VREFDQ sign	DQL2 VREFDQ Offset			DQL2 QBCLK Sign	RFU	DQL2 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL2 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL2 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL2 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL2 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.85 MR157 (MA[7:0]=9D$_H$) - DQL3 DCA for IBCLK and QCLK

MR157 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL3 IBCLK Sign	RFU	DQL3 DCA for IBCLK		DQL3 QCLK sign	RFU	DQL3 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL3 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL3 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL3 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL3 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.86 MR158 (MA[7:0]=9E$_H$) - DQL3 DCA for QBCLK and DQL3 VrefDQ Offset

MR158 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL3 VREFDQ sign	DQL3 VREFDQ Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL3 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL3 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL3 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL3 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.87 MR165 (MA[7:0]=A5$_H$) - DQL4 DCA for IBCLK and QCLK

MR165 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL4 IBCLK Sign	RFU	DQL4 DCA for IBCLK		DQL4 QCLK sign	RFU	DQL4 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL4 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL4 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL4 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL4 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.88 MR166 (MA[7:0]=A6$_H$) - DQL4 DCA for QBCLK and DQL4 VrefDQ Offset

MR166 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL4 VREFDQ sign	DQL3 VREFDQ Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL4 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL4 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL4 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL4 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.89 MR173 (MA[7:0]=AD_H) - DQL5 DCA for IBCLK and QCLK

MR173 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL5 IBCLK Sign	RFU	DQL5 DCA for IBCLK		DQL5 QCLK sign	RFU	DQL5 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL5 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL5 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL5 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL5 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.90 MR174 (MA[7:0]=AE_H) - DQL5 DCA for QBCLK and DQL5 VrefDQ Offset

MR174 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL5 VREFDQ sign	DQL5 VREFDQ Offset			DQL5 QBCLK Sign	RFU	DQL5 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL5 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL5 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL5 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL5 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.91 MR181 (MA[7:0]=B5$_H$) - DQL6 DCA for IBCLK and QCLK

MR181 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL6 IBCLK Sign	RFU	DQL6 DCA for IBCLK		DQL6 QCLK sign	RFU	DQL6 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL6 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL6 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL6 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL6 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.92 MR182 (MA[7:0]=B6$_H$) - DQL6 DCA for QBCLK and DQL6 VrefDQ Offset

MR182 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL6 VREFDQ sign	DQL6 VREFDQ Offset			DQL6 QBCLK Sign	RFU	DQL6 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL6 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL6 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL6 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL6 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.93 MR189 (MA[7:0]=BD_H) - DQL7 DCA for IBCLK and QCLK

MR189 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL7 IBCLK Sign	RFU	DQL7 DCA for IBCLK		DQL7 QCLK sign	RFU	DQL7 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL7 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL7 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL7 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL7 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.94 MR190 (MA[7:0]=BE_H) - DQL7 DCA for QBCLK and DQL7 VrefDQ Offset

MR190 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL7 VREFDQ sign	DQL7 VREFDQ Offset			DQL7 QBCLK Sign	RFU	DQL7 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL7 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL7 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQL7 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL7 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.95 MR197 (MA[7:0]=$C5_H$) - DQU0 DCA for IBCLK and QCLK

MR197 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU0 IBCLK Sign	RFU	DQU0 DCA for IBCLK		DQU0 QCLK sign	RFU	DQU0 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU0 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU0 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU0 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU0 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.96 MR198 (MA[7:0]=$C6_H$) - DQU0 DCA for QBCLK and DQU0 VrefDQ Offset

MR198 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU0 VREFDQ sign	DQU0 VREFDQ Offset			DQU0 QBCLK Sign	RFU	DQU0 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU0 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU0 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU0 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU0 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.97 MR205 (MA[7:0]=CD_H) - DQU1 DCA for IBCLK and QCLK

MR205 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU1 IBCLK Sign	RFU	DQU1 DCA for IBCLK		DQU1 QCLK sign	RFU	DQU1 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU1 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU1 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU1 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU1 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.98 MR206 (MA[7:0]=CE_H) - DQU1 DCA for QBCLK and DQU1 VrefDQ Offset

MR206 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU1 VREFDQ sign	DQU1 VREFDQ Offset			DQU1 QBCLK Sign	RFU	DQU1 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU1 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU1 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU1 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU1 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.99 MR213 (MA[7:0]=$D5_H$) - DQU2 DCA for IBCLK and QCLK

MR213 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU2 IBCLK Sign	RFU	DQU2 DCA for IBCLK		DQU2 QCLK sign	RFU	DQU2 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU2 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU2 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU2 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU2 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.100 MR214 (MA[7:0]=$D6_H$) - DQU2 DCA for QBCLK and DQU2 VrefDQ Offset

MR214 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU2 VREFDQ sign	DQU2 VREFDQ Offset			DQU2 QBCLK Sign	RFU	DQU2 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU2 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU2 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU2 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU2 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.101 MR221 (MA[7:0]=DD_H) - DQU3 DCA for IBCLK and QCLK

MR221 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU3 IBCLK Sign	RFU	DQU3 DCA for IBCLK		DQU3 QCLK sign	RFU	DQU3 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU3 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU3 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU3 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU3 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.102 MR222 (MA[7:0]=DE_H) - DQU3 DCA for QBCLK and DQU3 VrefDQ Offset

MR222 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU3 VREFDQ sign	DQU3 VREFDQ Offset			DQU3 QBCLK Sign	RFU	DQU3 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU3 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU3 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU3 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU3 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.103 MR229 (MA[7:0]=$E5_H$) - DQU4 DCA for IBCLK and QCLK

MR229 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU4 IBCLK Sign	RFU	DQU4 DCA for IBCLK		DQU4 QCLK sign	RFU	DQU4 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU4 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU4 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU4 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU4 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.104 MR230 (MA[7:0]=$E6_H$) - DQU4 DCA for QBCLK and DQU4 VrefDQ Offset

MR230 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU4 VREFDQ sign	DQU4 VREFDQ Offset			DQU4 QBCLK Sign	RFU	DQU4 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU4 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU4 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU4 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU4 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.105 MR237 (MA[7:0]=ED_H) - DQU5 DCA for IBCLK and QCLK

MR237 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU5 IBCLK Sign	RFU	DQU5 DCA for IBCLK		DQU5 QCLK sign	RFU	DQU5 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU5 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU5 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU5 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU5 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.106 MR238 (MA[7:0]=EE_H) - DQU5 DCA for QBCLK and DQU5 VrefDQ Offset

MR238 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU5 VREFDQ sign	DQU5 VREFDQ Offset			DQU5 QBCLK Sign	RFU	DQU5 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU5 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU5 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU5 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU5 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.107 MR245 (MA[7:0]=$F5_H$) - DQU6 DCA for IBCLK and QCLK

MR245 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU6 IBCLK Sign	RFU	DQU6 DCA for IBCLK		DQU6 QCLK sign	RFU	DQU6 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU6 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU6 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU6 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU6 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.108 MR246 (MA[7:0]=$F6_H$) - DQU6 DCA for QBCLK and DQU6 VrefDQ Offset

MR246 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU6 VREFDQ sign	DQU6 VREFDQ Offset			DQU6 QBCLK Sign	RFU	DQU6 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU6 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU6 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU6 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU6 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.109 MR253 (MA[7:0]=FD_H) - DQU7 DCA for IBCLK and QCLK

MR253 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU7 IBCLK Sign	RFU	DQU7 DCA for IBCLK		DQU7 QCLK sign	RFU	DQU7 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU7 DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU7 QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU7 DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU7 IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.110 MR254 (MA[7:0]=FE_H) - DQU7 DCA for QBCLK and DQU7 VrefDQ Offset

MR254 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU7 VREFDQ sign	DQU7 VREFDQ Offset			DQU7 QBCLK Sign	RFU	DQU7 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU7 DCA for QBCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU7 QBCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQU7 VREFDQ Offset	W	OP[6:4]	000_B: disable (Default) 001_B: step +1 010_B: step +2 011_B: step +3 100_B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU7 VREFDQ sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.111 Undefined Mode Registers spaced in DFE, per bit DCA & per bit VrefDQ section

MR117
MR119
MR125
MR127
MR135
MR143
MR155
MR159
MR167
MR175
MR183
MR191
MR199
MR207
MR215
MR223
MR231
MR239
MR247
MR255

There are currently no plans to utilize these MR addresses.

4 DDR5 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Notes 1, 2 & 14 apply to the entire Command truth table
(b) To improve command decode time, the table has been optimized to orient all 1-cycle commands together and all 2-cycle commands together; allowing CA1 to be used to identify the difference between a 1-cycle and a 2-cycle command.

[BG=Bank Group Address, BA=Bank Address, R=Row Address, C=Column Address, MRA=Mode Register Address, OP=Op Code, CID=Chip ID, CW=Control Word, X=Don't Care, V=Valid].

Table 27 — Command Truth Table

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11,17,20
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/ R17	
RFU	RFU	L	H	L	L	L	L	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
RFU	RFU	L	H	L	L	L	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Write Pattern	WRP	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11,15,18,19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	H	H	V	CID3	
Write Pattern w/ Auto Precharge	WRPA	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11,15,18,19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	H	V	CID3	
RFU	RFU	L	H	L	L	H	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Mode Register Write	MRW	L	H	L	H	L	L	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8,11,13,20
		H	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	V	CW	V	V	V	
Mode Register Read	MRR	L	H	L	H	L	H	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8,13,21,20
		H	L	L	V	V	V	V	V	V	V	V	CW	V	V	V	
Write	WR	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,12,15,19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	H	WR Partial=L	V	CID3	
Write w/Auto Precharge	WRA	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,12,15,19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	WR Partial=L	V	CID3	
Read	RD	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,15,19,20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	V	V	CID3	
Read w/Auto Precharge	RDA	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,15,19,20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	V	V	CID3	
VrefCA Command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	L	V	
VrefCS Command	VrefCS	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	H	V	
Refresh All	REFab	L	H	H	L	L	H	CID3	V	V	V or RIR	V or H	L	CID0	CID1	CID2	3,23,24
Refresh Management All	RFMab	L	H	H	L	L	H	CID3	V	V	V	L	L	CID0	CID1	CID2	3,20
Refresh Same Bank	REFsb	L	H	H	L	L	H	CID3	BA0	BA1	V or RIR	V or H	H	CID0	CID1	CID2	4,20,23, 24
Refresh Management Same Bank	RFMsb	L	H	H	L	L	H	CID3	BA0	BA1	V	L	H	CID0	CID1	CID2	4,20
Precharge All	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2	5,20
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	6,20
Precharge	PREpb	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	7,20
RFU	RFU	L	H	H	H	L	L	V	V	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	L	H	H	H	L	H	V	V	V	V	H	L	V	V	V	9
Self Refresh Entry w/ Frequency Change	SREF	L	H	H	H	L	H	V	V	V	V	L	L	V	V	V	9
Power Down Entry	PDE	L	H	H	H	L	H	V	V	V	V	V	H	ODT=L	V	V	10,16
MPC	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	20
NOP	NOP	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	26
Power Down Exit	PDX	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	
Deselect	DES	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Reserved		L	L	H	Reserved												

1. V means H or L (a defined logic level). X means don't care in which case the signal may be floated.
2. Bank group addresses BG[2:0] and Bank addresses BA[1:0] determine which bank is to be operated upon in a specific bank group.
3. The Refresh All and Refresh Management All commands are applied to all banks in all bank groups. CA6 and CA7 are required to be valid (“V”)
4. The Refresh Same Bank and Refresh Management Same Bank commands refresh the same bank in all bank group bits. The bank bits, BA0 and BA1 on CA6 and CA7, respectively, specify the bank within each bank group.
5. The Precharge All command applies to all open banks in all bank groups.
6. The Precharge Same Bank command applies to the same bank in all bank groups. The bank bits specify the bank within each bank group.
7. The Precharge command applies to a single bank as specified by bank address and bank group bits.
8. CS_n=LOW during the 2nd cycle of a two cycle command controls ODT in non-target ranks for WR, RD and MRR commands.
9. The SRE command places the DRAM in self refresh state
10. The PDE command places the DRAM in power down state
11. Two cycle commands with no ODT control (ACT, MRW, WRP). DRAM does not execute the command if it receives CS as LOW on 2nd cycle.
12. WR command with WR_partial = Low indicates a partial write command. This is to help DRAM start an internal read for 'read modify write'.
13. If CW=Low during the MRW command then DRAM should execute the command, Mode Register will be written. If CW=HIGH then DRAM ignores the MRW command, and the Mode Register is not changed. If CW=Low, DRAM should execute the MRR command. If CW=High, DRAM may or may not execute MRR command.
14. CID[3:0] bits are used for 3DS stacking support. When CID[3:0] bits are not used, they are required to be Valid (“V”).
15. If CA5:BL*=L, the command places the DRAM into the alternate Burst mode described by MR0[1:0] instead of the default Burst Length 16 mode.
16. ODT=L is defined to allow On Die Termination (ODT) to persist when the device is in Power Down Mode.
17. CID3/R17 is a multi-mode pin allowing for either 16H 3DS stacking with the CID3 bit usage or R17 for high bit density monolithic usage. These usages are mutually exclusive.
18. Write Pattern only supports BL16 and BL32.
19. When CID3 is not used, its required to be Valid (“V”).
20. In the case of a DRAM where the density or stacking doesn't require CA[13] the ball location for that function (considering the state of MIR) shall be connected to VDDQ, and the DRAM shall decode CA[13]=L so that the proper selection of die and RA is provided.
21. CA[0:1] =[L:L] on the second cycle for burst ordering.
22. When host issue MRR with CRC enabled, data comes out with CRC bit.
23. If the Refresh Management Required bit is “0” (MR58 OP[0]=0), CA9 is only required to be valid (“V”) for a REF command, and the DRAM will treat a RFM command as a REF command. If MR58 OP[0]=1, a REF command requires CA9=H.
24. If the Refresh Interval Rate indicator bit is disabled (MR4:OP[3]=0) by the host, CA8 is only required to be valid (“V”). If the Refresh Interval Rate indicator bit is enabled (MR4:OP[3]=1) by the host, the host is required to set CA8=H for REF commands issued at the 1x refresh interval rate and CA8=L for REF commands issued at the 2x refresh interval rate. If the host issues 2x REF commands with CA8=L while MR4:OP[3]=1, but the Refresh rate requirement is 1x as determined internally by the DRAM, the DRAM may internally align to the 1x refresh rate.
25. Command Truth Table bits such as BG2, BA1, R16, R17, C10, and CID[3:0] which are unused based on a device’s density, configuration width, and stacking options, the CA decode is defined as VALID when in these unused states.
26. Unlike DES, NOP is considered a *valid command*, and timing from a preceding valid command must satisfy any associated command timings.

4.1.1 2-Cycle Command Cancel

DDR5 DRAM commands ACT, WRP, WRPA and MRW are 2-cycle commands without associated ODT control requirements. The DRAMwill not execute these2-cycle commands if the CS_n is LOW on the 2nd cycle (command cancel).

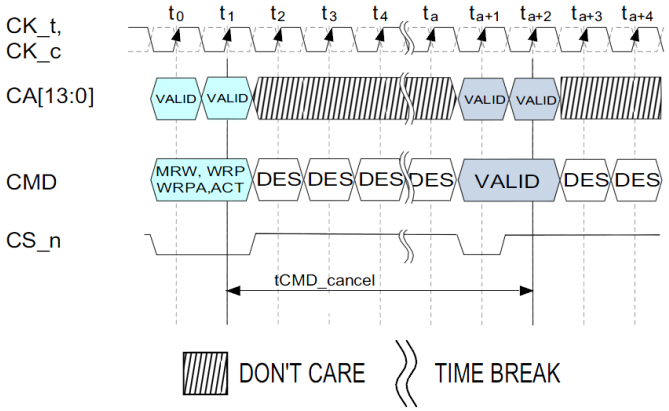


Figure 9 — Command Cancel Timing

Table 28 — Command Cancel Timing

Parameter	Symbol	DDR5 3200 ~ 6400		DDR5 6800 ~ 8400		unit
		min	max	min	max	
Command cancel timing for ACT, WRP, WRPA, MRW when CS_n is low on 2nd cycle	tCMD_cancel	8	-	8	-	nCK

4.2 Burst Length, Type and Order

Accesses within a given burst is currently limited to only sequential, interleaved is not supported. The ordering of accesses within a burst is determined by the burst length and the starting column address as shown in Table 29. The burst length is defined by bits OP[1:0] of Mode Register MR0. Burst length options include BC8 OTF, BL16, BL32 (optional) and BL32 OTF.

Table 29 — Burst Type and Burst Order for READ

Burst Length	Burst Type	C3	C2	C1	C0	Read Burst Cycle and Burst Address Sequence															
						1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
BC8	SEQ	0	0	V	V	0	1	2	3	4	5	6	7	T	T	T	T	T	T	T	T
		0	1	V	V	4	5	6	7	0	1	2	3	T	T	T	T	T	T	T	T
		1	0	V	V	8	9	A	B	C	D	E	F	T	T	T	T	T	T	T	T
		1	1	V	V	C	D	E	F	8	9	A	B	T	T	T	T	T	T	T	T
BL16	SEQ	0	0	V	V	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0	1	V	V	4	5	6	7	0	1	2	3	C	D	E	F	8	9	A	B
		1	0	V	V	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	V	V	C	D	E	F	8	9	A	B	4	5	6	7	0	1	2	3

Table 30 — Burst Type and Burst Order for WRITE

Burst Length	Burst Type	C3	C2	C1	C0	Write Burst Cycle and Burst Address Sequence															
						1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
BC8	SEQ	0	V	V	V	0	1	2	3	4	5	6	7	X	X	X	X	X	X	X	X
		1	V	V	V	8	9	A	B	C	D	E	F	X	X	X	X	X	X	X	X
BL16	SEQ	V	V	V	V	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Note(s):
1. T: Output driver for data and strobes are in RTT_PARK.
2. V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.
3. X: Don't Care.

4.2.1 Burst Type and Burst Order for Optional BL32 Mode

DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Table 31 — Burst Type and Burst Order for READ BL32

Burst Length	Burst Type	C10	C3	C2	C1	C0	Read Burst Cycle and Burst Address Sequence							
							1-4	5-8	9-12	13-16	17-20	21-24	25-28	29-32
BL32	SEQ	0	0	0	V	V	0-3	4-7	8-B	C-F	10-13	14-17	18-1B	1C-1F
		0	0	1	V	V	4-7	0-3	C-F	8-B	14-17	10-13	1C-1F	18-1B
		0	1	0	V	V	8-B	C-F	0-3	4-7	18-1B	1C-1F	10-13	14-17
		0	1	1	V	V	C-F	8-B	4-7	0-3	1C-1F	18-1B	14-17	10-13
		1	0	0	V	V	10-13	14-17	18-1B	1C-1F	0-3	4-7	8-B	C-F
		1	0	1	V	V	14-17	10-13	1C-1F	18-1B	4-7	0-3	C-F	8-B
		1	1	0	V	V	18-1B	1C-1F	10-13	14-17	8-B	C-F	0-3	4-7
		1	1	1	V	V	1C-1F	18-1B	14-17	10-13	C-F	8-B	4-7	0-3
BL16 in BL32 OTF		0	0	0	V	V	0-3	4-7	8-B	C-F	X	X	X	X
		0	0	1	V	V	4-7	0-3	C-F	8-B	X	X	X	X
		0	1	0	V	V	8-B	C-F	0-3	4-7	X	X	X	X
		0	1	1	V	V	C-F	8-B	4-7	0-3	X	X	X	X
		1	0	0	V	V	10-13	14-17	18-1B	1C-1F	X	X	X	X
		1	0	1	V	V	14-17	10-13	1C-1F	18-1B	X	X	X	X
		1	1	0	V	V	18-1B	1C-1F	10-13	14-17	X	X	X	X
		1	1	1	V	V	1C-1F	18-1B	14-17	10-13	X	X	X	X

Table 32 — Burst Type and Burst Order for WRITE BL32

Burst Length	Burst Type	C10	C3	C2	C1	C0	Write Burst Cycle and Burst Address Sequence			
							1-8	9-16	17-24	25-32
BL32	SEQ	0	V	V	V	V	0-7	8-F	17-24	25-32
BL16 in BL32 OTF		0	V	V	V	V	0-7	8-F	X	X
		1	V	V	V	V	10-17	18-1F	X	X

Note(s):
1. In case of BL16 in BL32 OTF mode by setting MR0[OP1:0=11], the internal write operation starts eight cycles earlier than for BL32 mode. This means that the starting point for tWR and tWTR shall be pulled in by eight clocks.
2. T: Output driver for data and strobes are in high impedance.
3. V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.
4. X: Don't Care.

4.3 Precharge Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) shall be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period shall be determined by the last PRECHARGE command issued to the bank.

If CA10 on the 2nd pulse of a Read or Write command is LOW, (shown as AP=L in the command truth table) then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read. Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command shall not begin until the last data of the burst write sequence is properly stored in the memory array. The bank shall be available for a subsequent row activation a specified time (tRP) after hidden PRECHARGE command (AutoPrecharge) is issued to that bank.

The precharge to precharge delay is defined by tPPD in the core timing tables. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

4.3.1 Precharge Command Modes

DDR5 supports three different types of precharge commands: Precharge, Precharge All and Precharge Same Bank

The Precharge Command (PREpb) applies precharge to a specific bank defined by BA[1:0] {if applicable} in a specific bank group defined by BG[2:0], while a Precharge All (PREab) applies precharge to all banks in all bank groups and a Precharge Same Bank (PREsb) applies precharge to a specific bank defined by BA[1:0] in all bank groups. In the case of a 3DS DDR5 SDRAM device, CID[3:0] shall also be selected to identify the target die.

Table 33 below shows the different encodes for PREpb, PREab and PREsb.

Table 33 — Precharge Encodings

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Precharge All	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2	
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	
Precharge	PREpb	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	

Note - See Command Truth Table for details

4.4 Programmable Preamble & Postamble

DDR5 shall support programmable preambles and postambles.

4.4.1 Read Preamble & Postamble

DDR5 supports a programmable read preamble & postamble.
Read Preamble is configured as 1tCK, 2tCK (two unique modes), 3tCK and 4tCK via MR8:OP[2:0].

Function	Register Type	Operand	Data
Read Preamble Settings	**R/W**	**OP[2:0]**	000_B: 1 tCK - 10 Pattern 001_B: 2 tCK - 0010 Pattern 010_B: 2 tCK - 1110 Pattern (DDR4 Style) 011_B: 3 tCK - 000010 Pattern 100_B: 4 tCK - 00001010 Pattern 101_B: Reserved 110_B: Reserved 111_B: Reserved

Read Postamble is configured as 0.5tCK or 1.5tCK via MR8:OP[6]

NOTE: DQS shall have an option to drive early by x-tCK to accommodate different HOST receiver designs as controlled by the Read DQS Offset in MR40:OP[2:0].

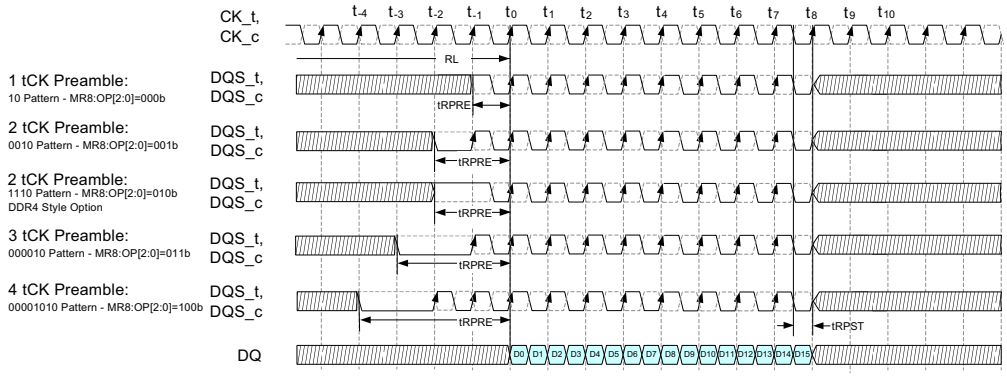


Figure 10 — Example of Read Preamble Modes (default) w/0.5 tCK Postamble

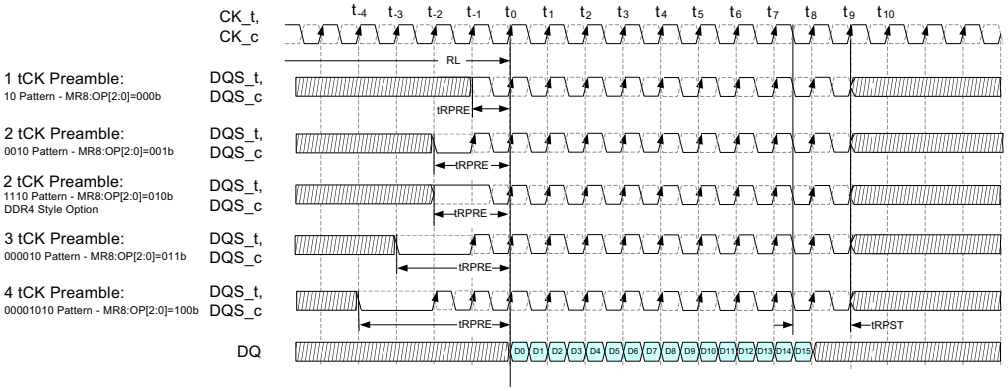


Figure 11 — Example of Read Preamble Modes (default) & w/1.5 tCK Postamble

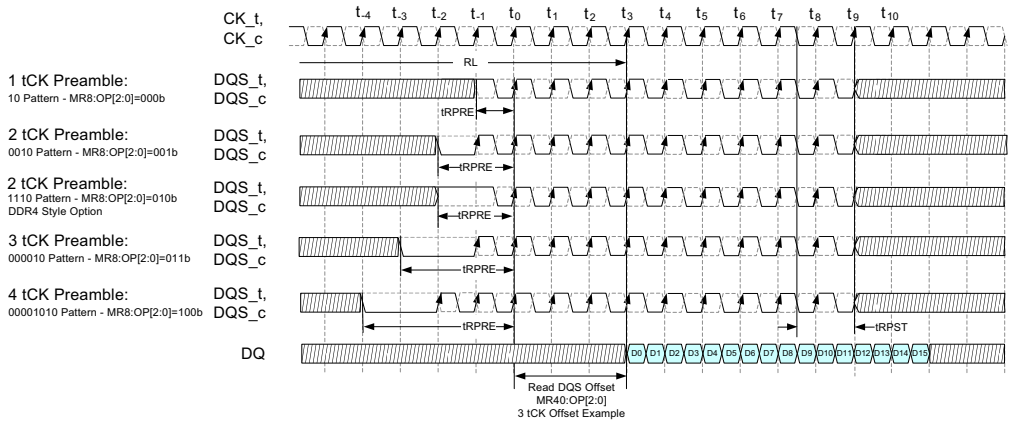


Figure 12 — Example of Read Preamble Modes w/ 3tCK DQS offset & w/1.5 tCK Postamble

4.4.2 Write Preamble & Postamble

DDR5 supports a programmable write preamble & postamble.
Write Preamble is configured as 2tCK, 3tCK and 4tCK via MR8:OP[4:3]
Write Postamble is configured as 0.5tCK or 1.5tCK via MR8:OP[7]

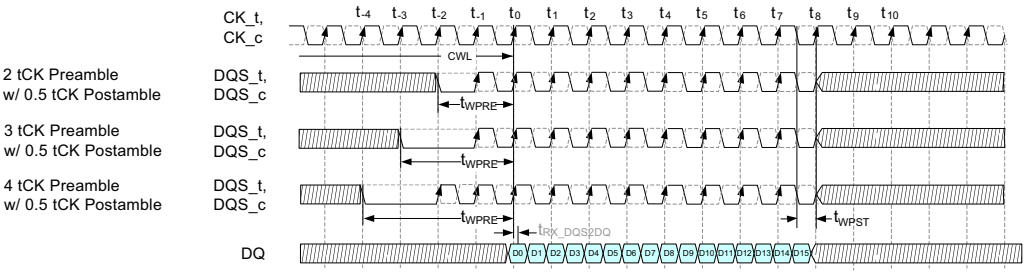


Figure 13 — Example of Write Preamble Modes (default) w/0.5tCK Postamble

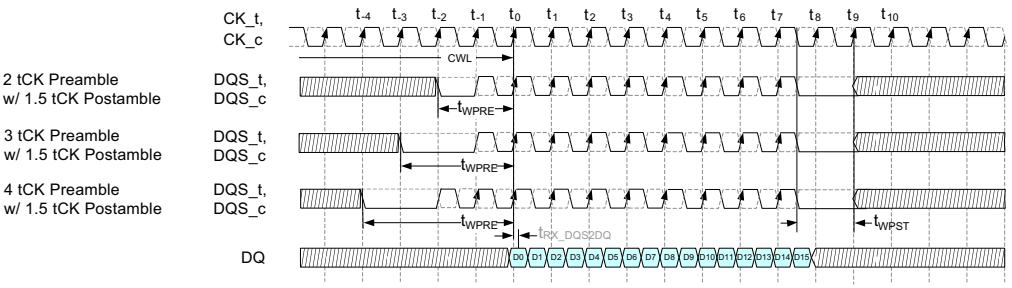


Figure 14 — Example of Write Preamble Modes (default) w/1.5tCK Postamble

4.4.3 Write Preamble Timings

During Write operations, the input receiver strobe shall be aligned with the DQ according to the preamble settings, and the strobe shall meet the timing requirements (tDQSH_pre, tDQSL_pre) to guarantee enough timing margin by setting the window for the strobe during the Write preamble time frame. This timing requirement is applied to all configurations of the Write preamble set by MR8 OP[4:3], which is 2tCK, 3tCK, and 4tCK Write preamble, for Write to Write operations as well as for normal Write operations.

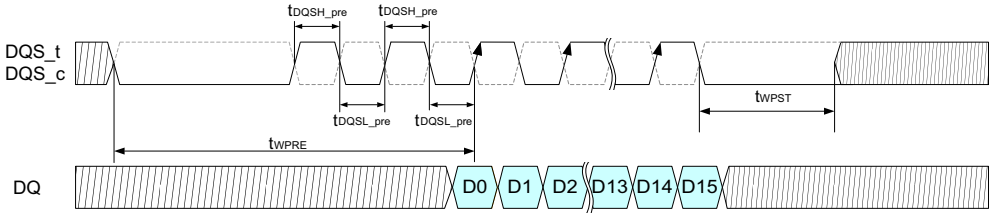


Figure 15 — DQS Timing While Write Preamble

Note(s):
1. BL=16, 4tCK Preamble
2. tDQSH_pre and tDQSL_pre are shown, and apply to all toggles during the preamble.
3. 2nd preamble during Write to Write operation shall follow the same requirement.

Table 34 — Strobe preamble timing parameters for DDR5 3200 to 8400

Parameter	Symbol	DDR5 3200 ~ 4400		DDR5 4800 ~ 6400		DDR5 6800 ~ 8400		Unit
		min	max	min	max	min	max	
Strobe's window of differentially high during Write preamble	tDQSH_pre	0.395	0.605	0.430	0.57	TBD	TBD	nCK
Strobe's window of differentially low during Write preamble	tDQSL_pre	0.395	0.395	0.430	0.570	TBD	TBD	nCK

4.5 Interamble

The DQS strobe for the device requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid), and it requires a postamble after the last latching edge. The preamble and postamble options are set via Mode Register Write commands. Additionally, the postamble and preamble configured size shall NOT force the HOST to add command gaps in the command interval just to satisfy postamble or preamble settings. (i.e. Preamble=4tCK + Postamble=1.5tCK shall not force tCCD+5).

4.5.1 Read Interamble Timing Diagrams

In Read to Read operations with tCCD=BL/2, postamble for 1st command and preamble for 2nd command shall disappear to create consecutive DQS latching edge for seamless burst operations.

In the case of Read to Read operations with command interval of tCCD+1, tCCD+2, etc., if the postamble and preambles overlap, the toggles take precedence over static preambles.

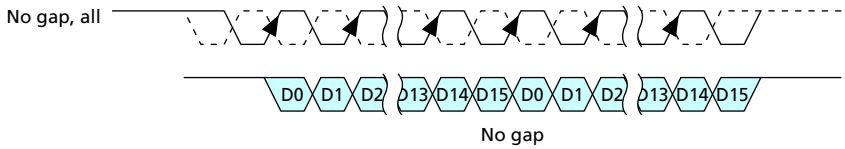


Figure 16 — Example of Seamless Reads Operation: tCCD=Min

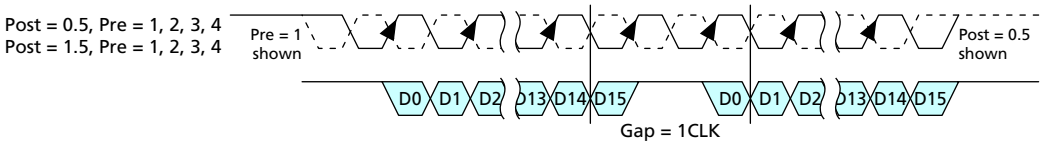


Figure 17 — Example of Consecutive Reads Operation: tCCD=Min+1

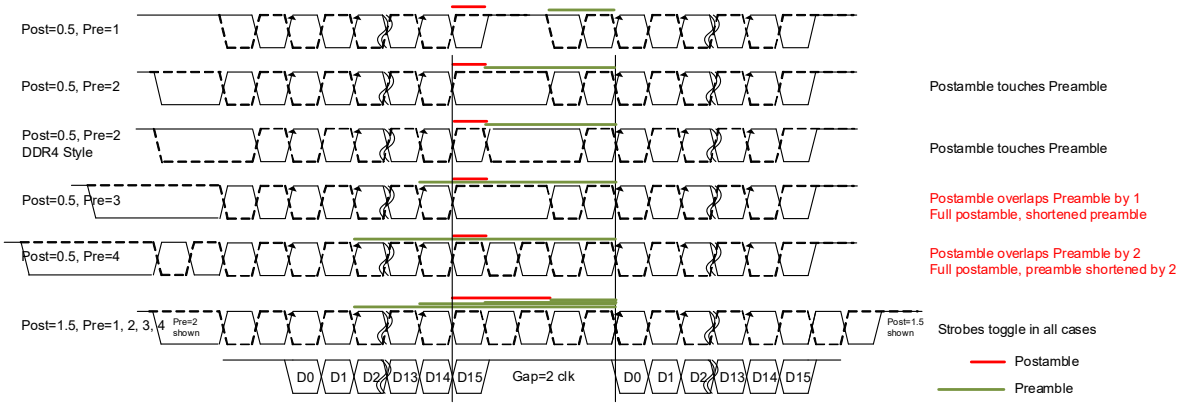


Figure 18 — Example of Consecutive Reads Operation: tCCD=Min+2

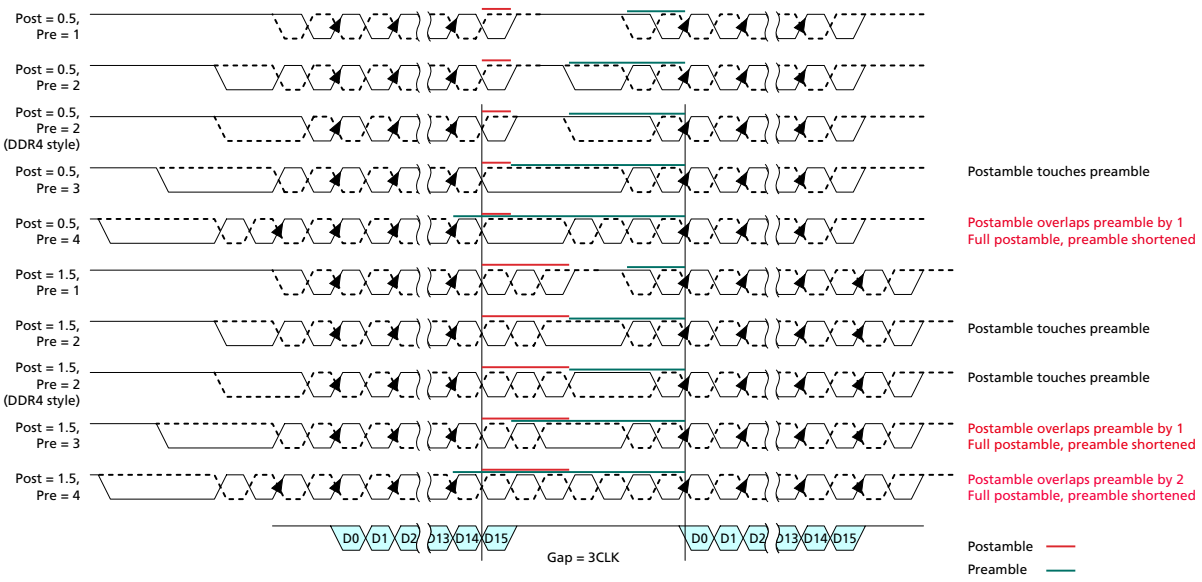


Figure 19 — Example of Consecutive Reads Operation: tCCD=Min+3

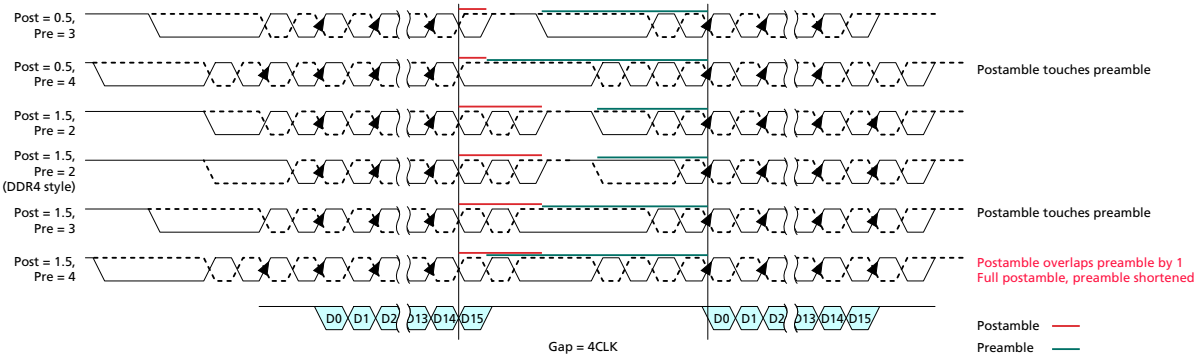


Figure 20 — Example of Consecutive Reads Operation: tCCD=Min+4

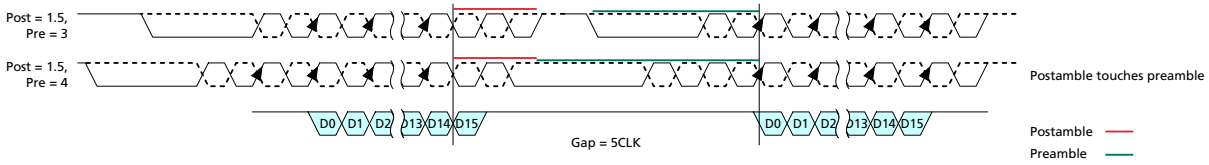


Figure 21 — Example of Consecutive Reads Operation: tCCD=Min+5

4.5.2 Write Interamble Timing Diagrams

In Write to Write operations with tCCD=BL/2, postamble for 1st command and preamble for 2nd command shall disappear to create consecutive DQS latching edge for seamless burst operations.

In the case of Write to Write operations with command interval of tCCD+1, tCCD+2, etc., if the postamble and preambles overlap, the toggles take precedence over static preambles.

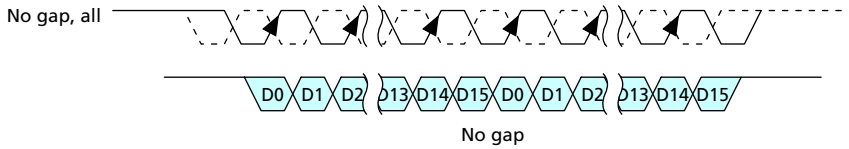


Figure 22 — Example of Seamless Writes Operation: tCCD=Min

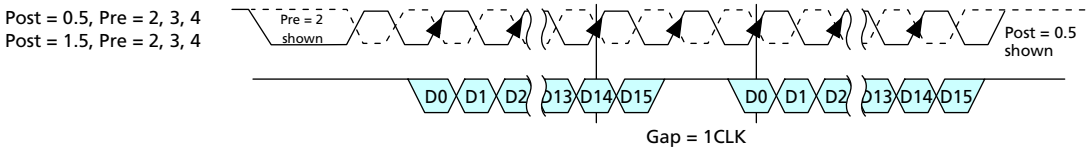


Figure 23 — Example of Consecutive Writes Operation: tCCD=Min+1

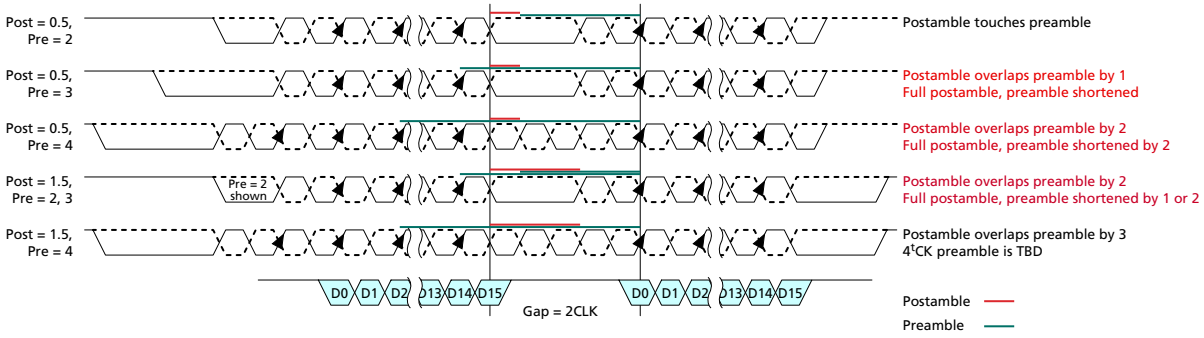


Figure 24 — Example of Consecutive Writes Operation: tCCD=Min+2

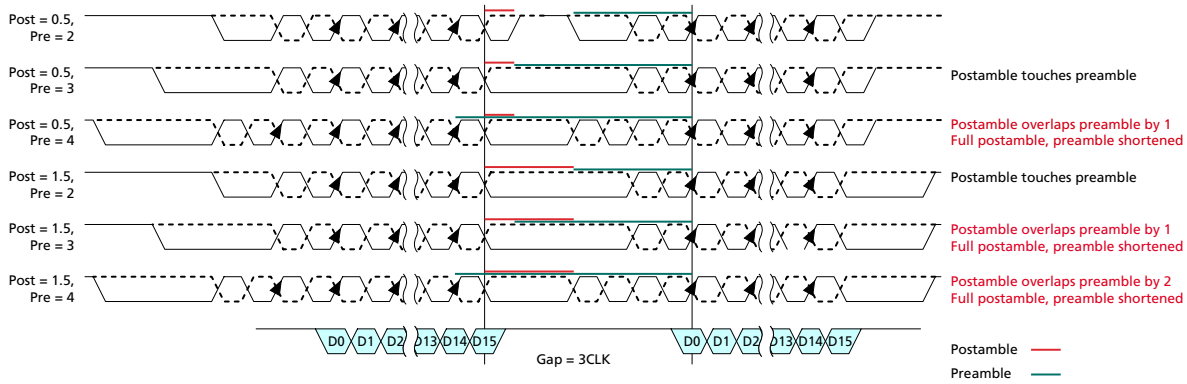


Figure 25 — Example of Consecutive Writes Operation: tCCD=Min+3

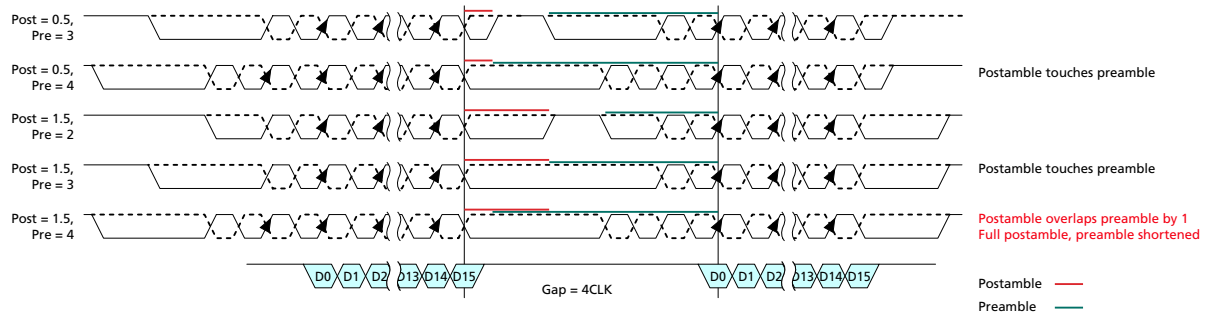


Figure 26 — Example of Consecutive Writes Operation: tCCD=Min+4

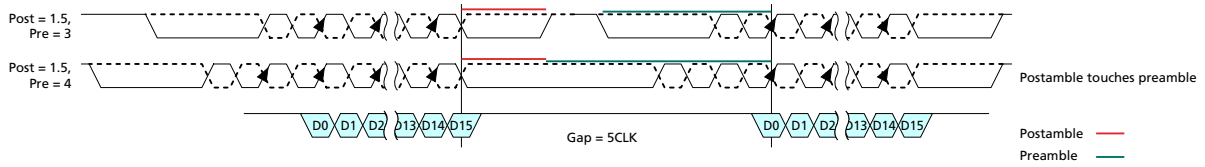


Figure 27 — Example of Consecutive Writes Operation: tCCD=Min+5

4.6 Activate Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG[2:0] in X4/8 and BG[1:0] in X16 select the bankgroup; BA[1:0] inputs selects the bank within the bankgroup, and the address provided on the appropriate CA pins for R[17:0] to select the row (see table 1 below). In the case of a 3DS DDR5 SDRAM device, the CID[3:0] shall also be selected to identify the correct die in the stack. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

Bank-to-bank command timing for ACTIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. tRRD_S (short) is used for timing between banks located in different bank groups. tRRD_L (long) is used for timing between banks located in the same bank group. Consecutive ACTIVATE commands, allowed to be issued at tRRDmin, are restricted to a maximum of four within the time period tFAW (four activate window).

Table 35 — Activate Command (for reference)

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/ R17	

Note - See Command Truth Table for details

4.6.1 Non-Binary Density Considerations

An ACT command with row address inputs which violate the 'MSB address bit “HIGH”, MSB-1 address bit “LOW”' non-binary density address restriction shall follow all timing and protocol rules as though the ACT were valid.

Any RD or RDA command following an ACT to the invalid address space within the same bank shall drive the DQS strobes with normaltiming but shall not output data on the DQs that can be used to learn about data stored in cells with valid addresses. DQ data that coincidentally matches cell array data is permissible (for example: always sending the all 1s and cell data sometimes being all 1s). Consistently exposing data from a previous read or previous activate is not permissible.

Any WR, WRA, WRP or WRPA command following an ACT to the invalid address space within the same bank shall not result in new databeing written anywhere within the DRAM.

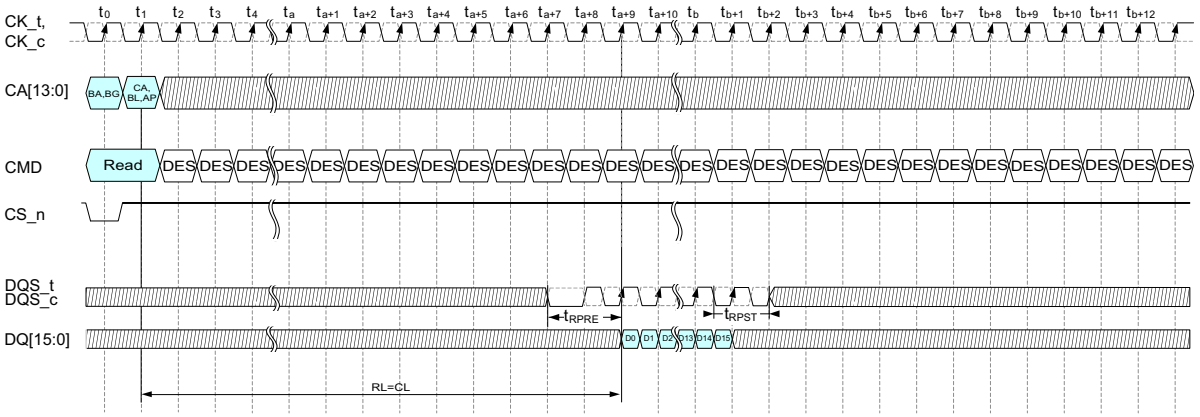
The DRAM will operate normally for Read and Write commands to banks which have pages open for valid rows.

4.7 Read Operation

The Read Operation causes the DRAM to retrieve and output data stored in its array. The Read Operation is initiated by the Read Command during which the beginning column address and bank/group address for the data to be retrieved from the array is provided. The data is driven by the DRAM on its DQ pins RL (CL) cycles after the Read Command along with the proper waveform on the DQS inputs. Read Latency (RL or CL) is defined from the Read command to data and is not affected by the Read DQS offset timing (MR40 OP[2:0]).

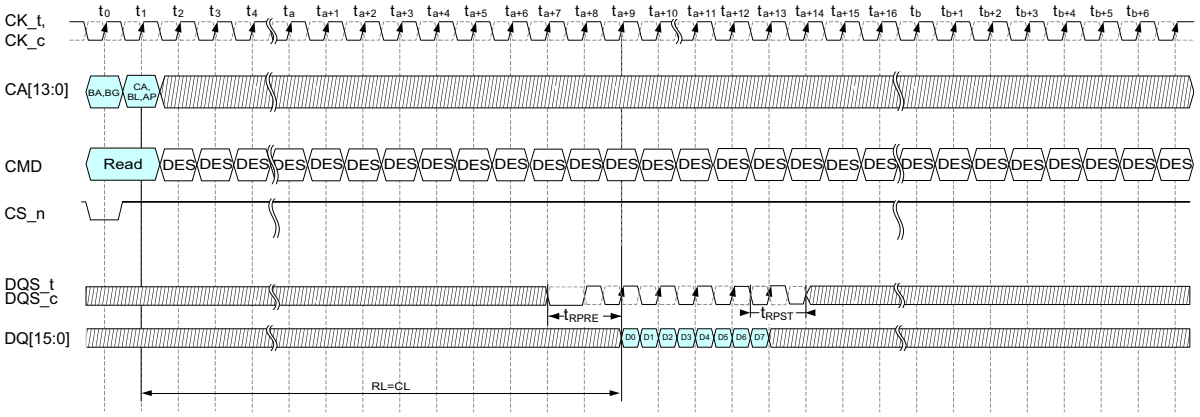
4.7.1 READ Burst Operation

During a READ or WRITE command, DDR5 shall support BC8, BL16, BL32 (optional) and BL32 OTF (optional) during the READ or WRITE. MR0[1:0] is used to select burst operation mode.



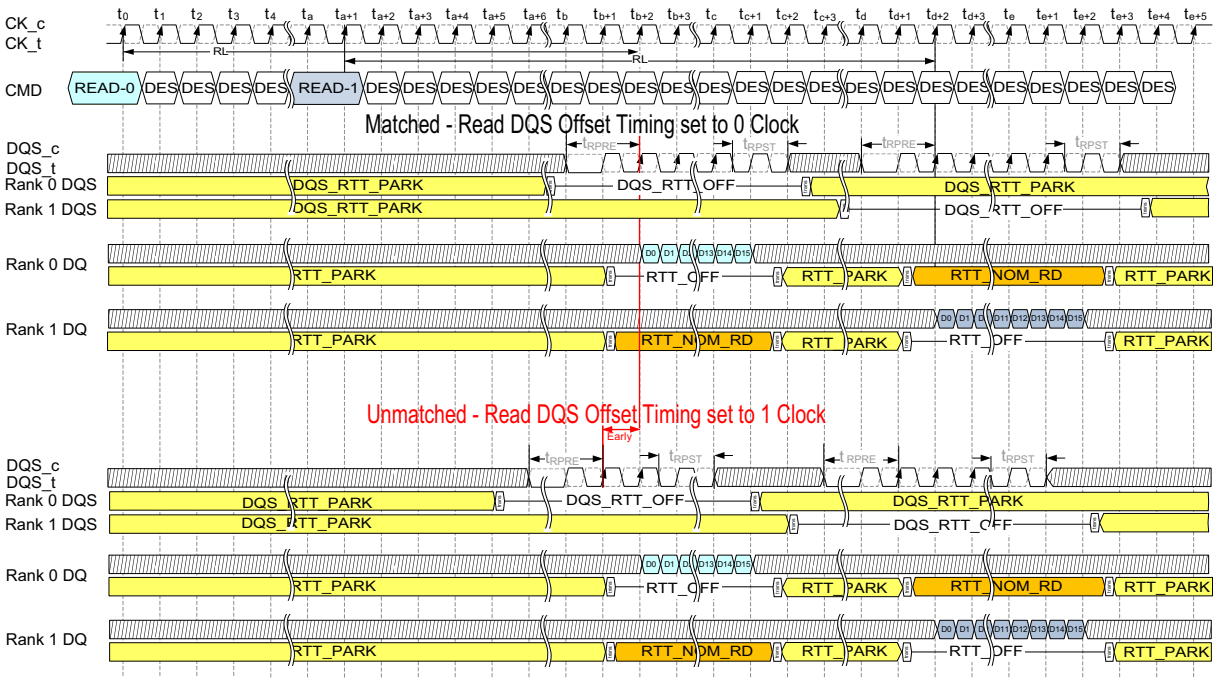
Note(s):
1. BL=16, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. In this example, Read DQS Offset Timing is set to 0 Clocks.

Figure 28 — READ Burst Operation (BL16)



Note(s):
1. BC=8, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. In this example, Read DQS Offset Timing is set to 0 Clocks
4. In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.

Figure 29 — Read Burst Operation (BC8)



Note(s):
1. BL=16, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Two different examples are shown side by side, the top with the default setting for Read DQS Offset = 0 Clock, the lower with a 1 Clock setting. In the lower case, the DQS is started 1 clock earlier than normal with respect to RL (CL).
4. In both cases, the Data does not move

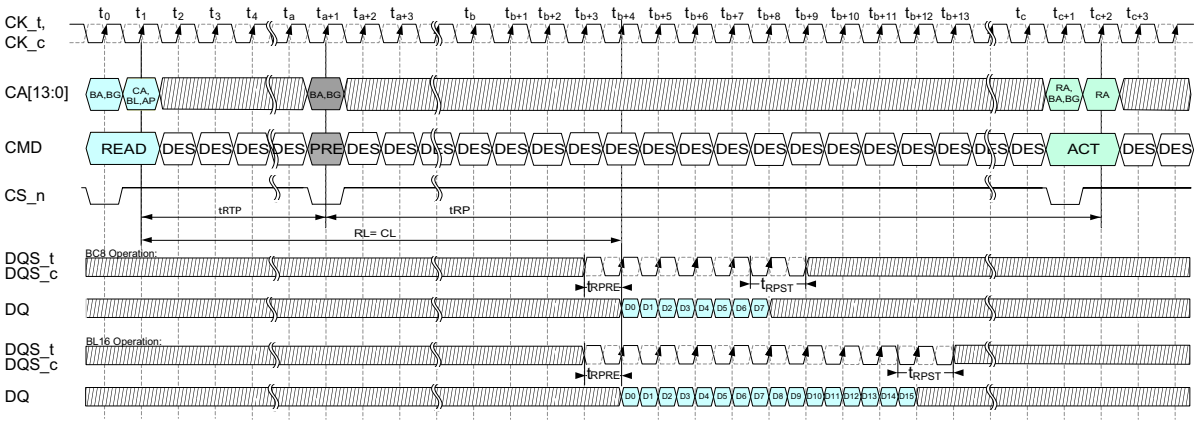
Figure 30 — READ to READ, Different Ranks Operation with Read DQS Offset usage (BL16)

4.7.2 Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.min. A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

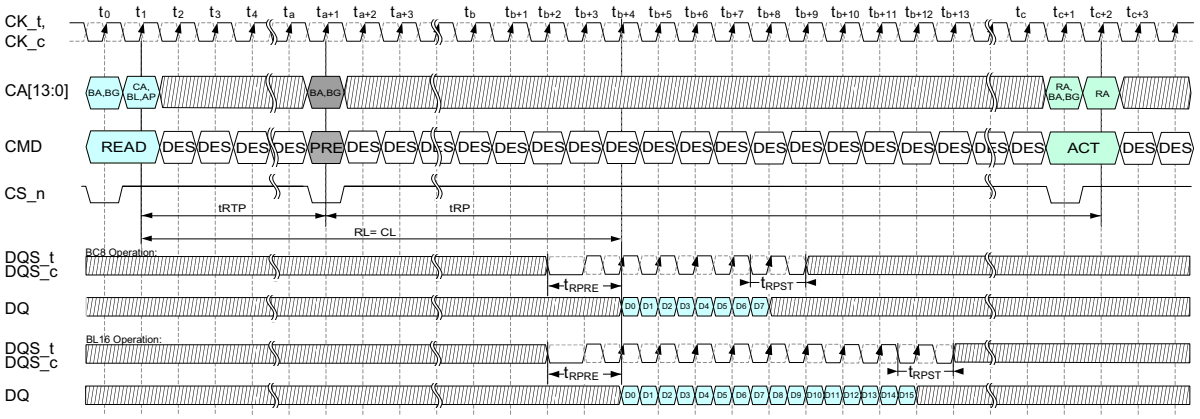
1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are shown in Figure 31 & Figure 32.



Note(s):
1. BL = 16, 1tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The example assumes tRAS. MIN is satisfied at Precharge command time(ta+1) and that tRC. MIN is satisfied at the next Active command time(tc+2).

Figure 31 — READ to PRECHARGE with 1tCK Preamble



Note(s):
1. BL = 16, 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble,
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The example assumes tRAS. MIN is satisfied at Precharge command time(ta+1) and that tRC. MIN is satisfied at the next Active command time(tc+2).

Figure 32 — READ to PRECHARGE with 2tCK Preamble

4.7.2.1 CLK to Read DQS timing parameters

Following parameters shall be defined for CK to read DQS timings.

Table 36 — CLK to Read DQS Timing Parameters DDR5-4400 to DDR5-4800

Speed		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max		
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK	-0.286	0.286	-0.300	0.300	tCK	1,4,5
DQS_t, DQS_c rising edge output variance window	tDQSCKi	-	0.475	-	0.490	tCK	2,3,4,5,6

Note(s):

1 - Measured over full VDD and Temperature spec ranges.
2 - Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
3 - These parameters are verified by design and characterization, and may not be subject to production test.
4 - Assume no jitter on input clock signals to the DRAM.
5 - Refer to Section 4.7.1 READ Timing Definitions.
6 - Measured at a fixed and constant VDD and Temperature condition.

Table 37 — CLK to Read DQS Timing Parameters DDR5-5200 to DDR5-5600

Speed		DDR5-5200		DDR5-5600		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max		
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK	-0.313	0.313	-0.325	0.325	tCK	1,4,5
DQS_t, DQS_c rising edge output variance window	tDQSCKi	-	0.510	-	0.530	tCK	2,3,4,5,6

Note(s):

1 - Measured over full VDD and Temperature spec ranges.
2 - Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
3 - These parameters are verified by design and characterization, and may not be subject to production test.
4 - Assume no jitter on input clock signals to the DRAM.
5 - Refer to Section 4.7.1 READ Timing Definitions.
6 - Measured at a fixed and constant VDD and Temperature condition.

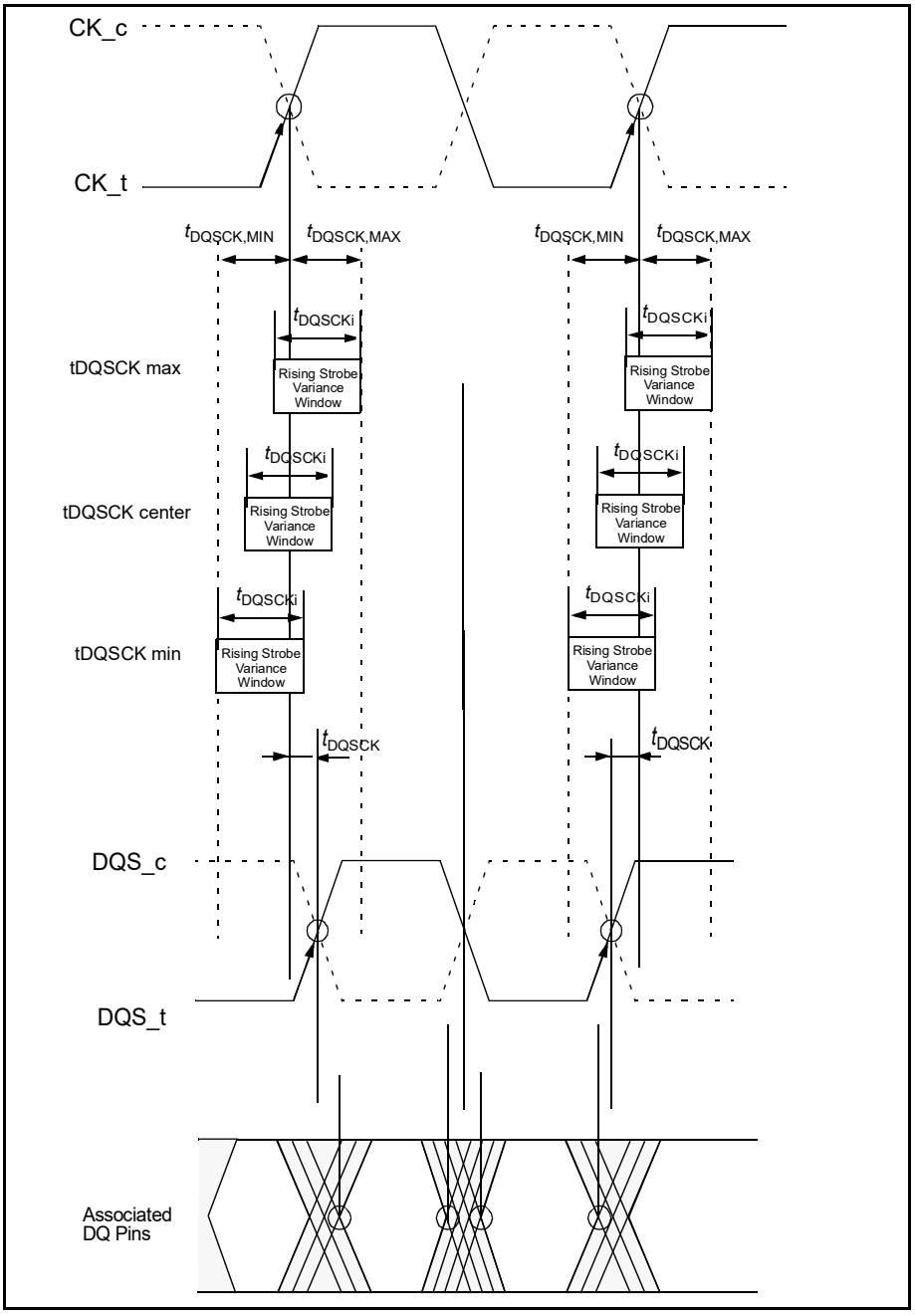


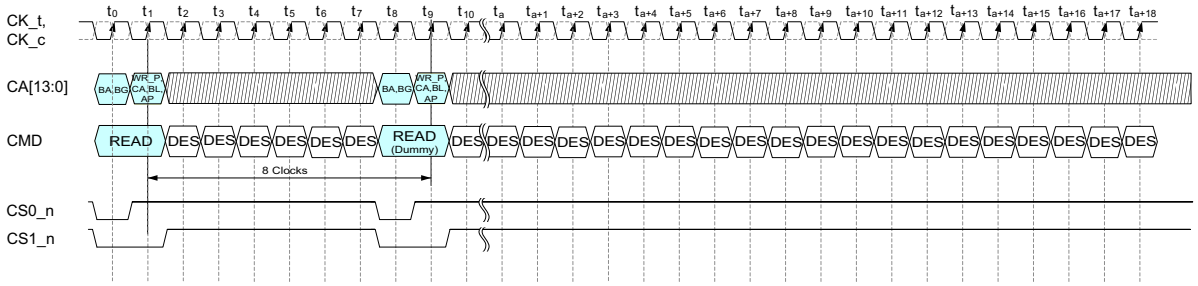
Figure 33 — TDQSCK Timing Definition

4.7.3 Read Burst Operation for Optional BL32 Mode

The following read timing diagrams cover write timings for fixed BL32 BL32 in BL32 OTF mode and BL16 in BL32 OTF mode for x4 devices only.

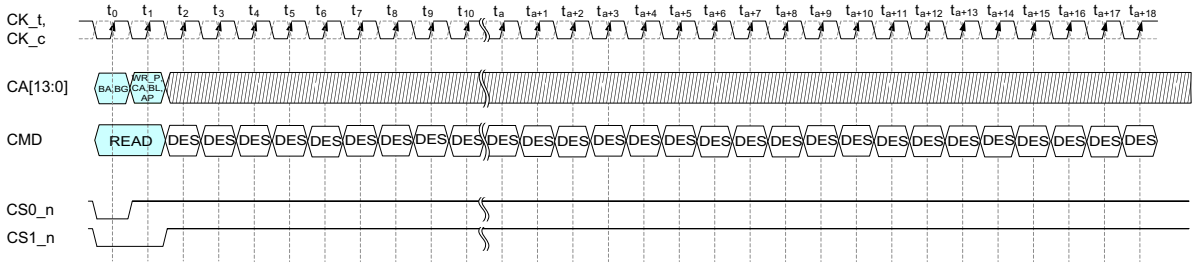
In these read timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be appropriate.

A dummy CAS command is required for second half of the transfer of BL32. If non-target ODT is needed in the system then a dummy ODT command must be issued to the non-target rank for second half of the transfer of BL32



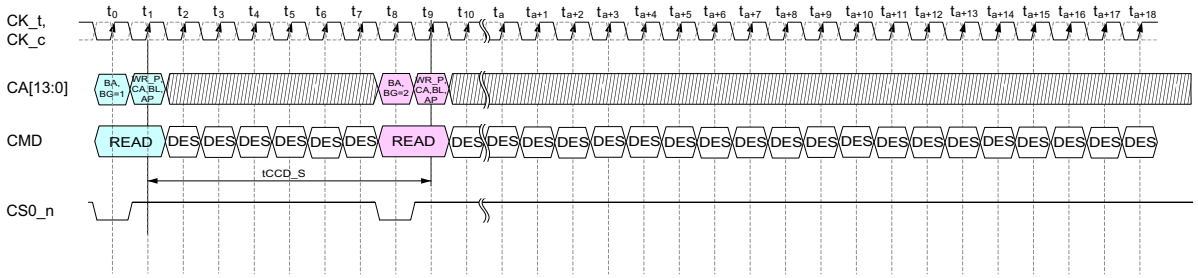
Note(s):
1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. A dummy RD command is required for the second half of the transfer with a delay of 8 clocks from the first RD command.
3. The figure also shows a dummy ODT command being issued to non-target rank 1 for the second half of the transfer.
4. C10 is used for burst ordering and can be LOW or HIGH for the first RD command. C10 for the dummy RD command must be the opposite value from the first RD command.
5. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.
6. CA bits other than C10 and AP in dummy CAS command are the same as the first CAS command.

Figure 34 — Read Timing for fixed BL32 and BL32 in BL32 OTF mode



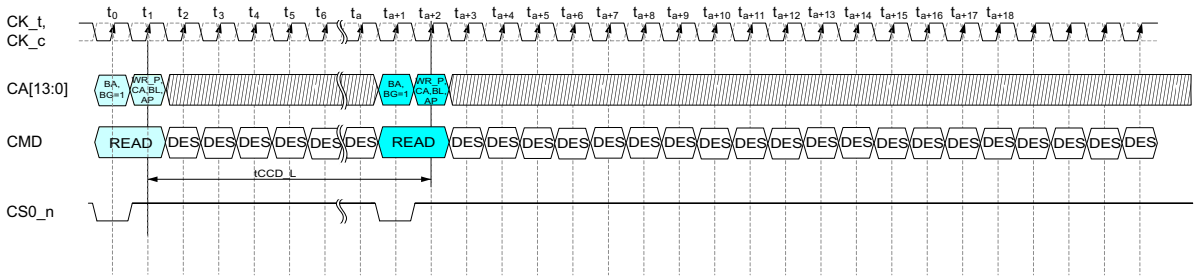
Note(s):
1. Figure shows BL16 read operation when MR0 is programmed to use BL32 OTF mode. In this case, no dummy RD command is required as transfer size is BL16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times including commands to allow data transfer from the same die after transfer of BL16.
3. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 35 — Read Timings for BL16 in BL32 OTF mode



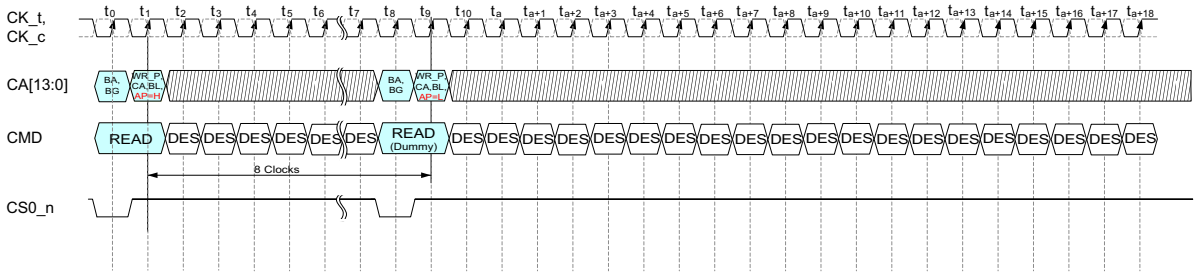
Note(s):
1. Figure shows back to back BL16 writes to different bank groups.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 36 — Read to Read to Different Bank Group for BL16 in BL32 OTF



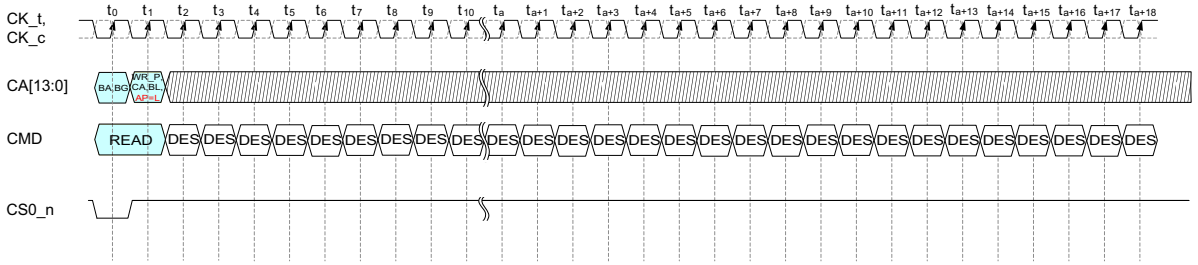
Note(s):
1. Figure shows back to back BL16 reads to same bank group using a timing of tCCD_L_WR.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 37 — Read to Read to Same Bank Group for BL16 in BL32 OTF



Note(s):
1. AP bit must be set HIGH for first CAS and LOW for dummy CAS command.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.
3. CA bits other than C10 and AP in dummy CAS command are the same as the first CAS command.

Figure 38 — Read with Auto-Precharge for Fixed BL32 and BL32 in BL32 OTF Mode



Note(s):
1. AP bit must be set to LOW with the CAS command.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 39 — Read with Auto-Precharge for BL16 in BL32 OTF Mode

4.7.4 Read and Write Command Interval

Table 38 — Minimum Read and Write Command Timings

Bank Group	Timing Parameter	DDR5-4400/4800/5200/5600	Units	Notes
same	Minimum Read to Write	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		1,3,4
	Minimum Write to Read	CWL + WBL/2 + tWTR_L		2,4,5
	Minimum Write to Read AP, same bank	CWL + WBL/2 + tWTRA		2,4,6
different	Minimum Read to Write	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		1,3,4
	Minimum Write to Read	CWL + WBL/2 + tWTR_S		2,4

Note(s):

1 - RBL: Read burst length associated with Read command
RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode
RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

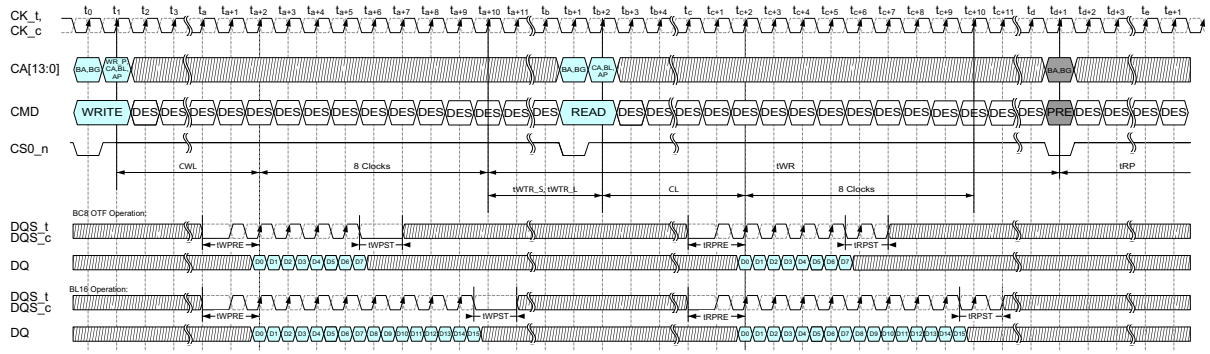
2 - WBL: Write burst length associated with Write command
WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

3. The following is considered for tRTW equation
1tCK needs to be added due to tDQS2CK
Read DQS offset timing can pull in the tRTW timing
1tCK needs to be added when 1.5tCK postamble

4. CWL=CL-2

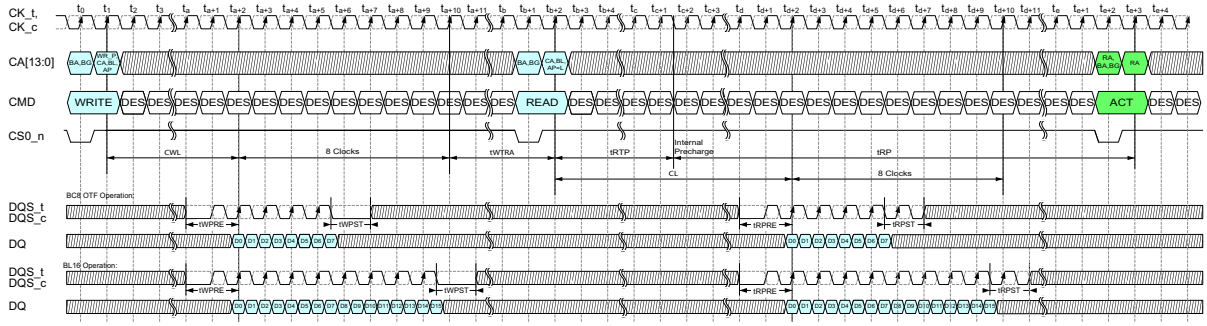
5. tWTRA must be satisfied instead of tWTR_L for same bank access when Read w/AutoPrecharge

6. tWTRA = tWR - tRTP, allows the precharge generated by the Read AutoPrecharge to meet tWR from the preceding Write when it occurs within the same bank.



Note(s):
1. BC OTF=8 or BL=16, Preamble = 2tCK - 0010 pattern, Postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at Ta+10.
tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 40 — Timing Diagram for Write to Read



Note(s):
1. BC OTF=8 or BL=16, Preamble = 2tCK - 0010 pattern, Postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at Ta+10.
   The internal precharge after the Read AutoPrecharge command cannot begin before tWR is satisfied, which is equivalent to tWTRA + tRTP

Figure 41 — Timing Diagram for Write to Read AutoPrecharge in same bank

4.7.5 Read and Write Command Interval for Optional BL32 Modes

Table 39 — Minimum Read to Read Timings - Same Bank Group

From	To		Units	Notes
	BL16 in BL32 OTF Mode	BL32 in BL32 OTF Mode		
BL16 in BL32 OTF Mode	tCCD_L	tCCD_L		1
BL32 in BL32 OTF Mode	16 Clocks	16 Clocks		1

Note(s):
1. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Table 40 — Minimum Read to Read Timings - Different Bank Group

From	To		Units	Notes
	BL16 in BL32 OTF Mode	BL32 in BL32 OTF Mode		
BL16 in BL32 OTF Mode	tCCD_S	tCCD_S		1
BL32 in BL32 OTF Mode	16 Clocks	16 Clocks		1

Note(s):
1. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Table 41 — Minimum Write to Write Timings - Same Bank Group

From	To		Units	Notes
	BL16 in BL32 OTF Mode	BL32 in BL32 OTF Mode		
BL16 in BL32 OTF Mode	tCCD_L_WR	tCCD_L_WR		1
BL32 in BL32 OTF Mode	TBD	TBD		1

Note(s):
1. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

DDR5 x8 and x16 devices will have different write to write same bank group timings, based on whether the second write requires a read-modify-write (RMW), the Burst Length mode of the device set by MR0: OP[1:0], and whether data masking is enabled by MR5:OP[5]. BL16 Partial Writes and BC8 Writes require a RMW on x8/x16 devices. BL16 non-partial writes do not require RMW. See Timing parameters per speed grade for details on parametric timings.

Table 42 — Minimum Write to Write Same Bank Group Timings, x8/x16 Devices

From	To			Units	Notes
	BC8	BL16 Partial Write	BL16 not Partial Write		
BC8 or BL16	tCCD_L_WR	tCCD_L_WR	tCCD_L_WR2		

Table 43 — Minimum Write to Write Timings - Different Bank Group

From	To		Units	Notes
	BL16 in BL32 OTF Mode	BL32 in BL32 OTF Mode		
BL16 in BL32 OTF Mode	tCCD_S	tCCD_S		1
BL32 in BL32 OTF Mode	16 Clocks	16 Clocks		1

Note(s):
1. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

4.7.6 Read and Write Command Interval for 3DS

Table 44 — Minimum Read and Write Command Timings for x4 2H and 4H 3DS - 4400 thru 4800

Logical Rank	Bank Group	Parameter Name	Timing Parameter	DDR5 4400 3DS	DDR5 4800 3DS	Units	Note
same	same	tCCD_L_slr	Minimum Read to Read	See Chapter 13, Timing Parameters by Speed Grade for 3DS		nCK	
		tCCD_L_WR_slr	Minimum Write to Write			nCK	
		tCCD_L_RTW_slr	Minimum Read to Write			nCK	
		tCCD_L_WTR_slr	Minimum Write to Read			nCK	
	different	tCCD_S_slr	Minimum Read to Read			nCK	
		tCCD_S_slr	Minimum Write to Write			nCK	
		tCCD_S_RTW_slr	Minimum Read to Write			nCK	
		tCCD_S_WTR_slr	Minimum Write to Read			nCK	
different	same or different	tCCD_S_dlr	Minimum Read to Read			nCK	
		tCCD_S_dlr	Minimum Write to Write			nCK	
		tCCD_S_RTW_dlr	Minimum Read to Write			nCK	
		tCCD_S_WTR_dlr	Minimum Write to Read			nCK	

Table 45 — Minimum Read and Write Command Timings for x4 2H and 4H 3DS - 5200 thru 5600

Logical Rank	Bank Group	Parameter Name	Timing Parameter	DDR5 5200 3DS	DDR5 5600 3DS	Units	Note
same	same	tCCD_L_slr	Minimum Read to Read	See Chapter 13, Timing Parameters by Speed Grade for 3DS		nCK	
		tCCD_L_WR_slr	Minimum Write to Write			nCK	
		tCCD_L_RTW_slr	Minimum Read to Write			nCK	
		tCCD_L_WTR_slr	Minimum Write to Read			nCK	
	different	tCCD_S_slr	Minimum Read to Read			nCK	
		tCCD_S_slr	Minimum Write to Write			nCK	
		tCCD_S_RTW_slr	Minimum Read to Write			nCK	
		tCCD_S_WTR_slr	Minimum Write to Read			nCK	
different	same or different	tCCD_S_dlr	Minimum Read to Read			nCK	
		tCCD_S_dlr	Minimum Write to Write			nCK	
		tCCD_S_RTW_dlr	Minimum Read to Write			nCK	
		tCCD_S_WTR_dlr	Minimum Write to Read			nCK	

Table 46 — Minimum Read and Write Command Timings for x4 8H and 16H 3DS - 4400 thru 4800

Logical Rank	Bank Group	Parameter Name	Timing Parameter	DDR5 4400 3DS	DDR5 4800 3DS	Units	Note
same	same	tCCD_L_slr	Minimum Read to Read	See Chapter 13, Timing Parameters by Speed Grade for 3DS		nCK	
		tCCD_L_WR_slr	Minimum Write to Write			nCK	
		tCCD_L_RTW_slr	Minimum Read to Write			nCK	
		tCCD_L_WTR_slr	Minimum Write to Read			nCK	
	different	tCCD_S_slr	Minimum Read to Read			nCK	
		tCCD_S_slr	Minimum Write to Write			nCK	
		tCCD_S_RTW_slr	Minimum Read to Write			nCK	
		tCCD_S_WTR_slr	Minimum Write to Read			nCK	
different	same or different	tCCD_S_dlr	Minimum Read to Read			nCK	
		tCCD_S_dlr	Minimum Write to Write			nCK	
		tCCD_S_RTW_dlr	Minimum Read to Write			nCK	
		tCCD_S_WTR_dlr	Minimum Write to Read			nCK	

Table 47 — Minimum Read and Write Command Timings for x4 8H and 16H 3DS - 5200 thru 6400

Logical Rank	Bank Group	Parameter Name	Timing Parameter	DDR5 5200 3DS	DDR5 5600 3DS	Units	Note
same	same	tCCD_L_slr	Minimum Read to Read	See Chapter 13, Timing Parameters by Speed Grade for 3DS		nCK	
		tCCD_L_WR_slr	Minimum Write to Write			nCK	
		tCCD_L_RTW_slr	Minimum Read to Write			nCK	
		tCCD_L_WTR_slr	Minimum Write to Read			nCK	
	different	tCCD_S_slr	Minimum Read to Read			nCK	
		tCCD_S_slr	Minimum Write to Write			nCK	
		tCCD_S_RTW_slr	Minimum Read to Write			nCK	
		tCCD_S_WTR_slr	Minimum Write to Read			nCK	
different	same or different	tCCD_S_dlr	Minimum Read to Read			nCK	
		tCCD_S_dlr	Minimum Write to Write			nCK	
		tCCD_S_RTW_dlr	Minimum Read to Write			nCK	
		tCCD_S_WTR_dlr	Minimum Write to Read			nCK	

4.8 Write Operation

The Write Operation stores data to the DRAM. It is initiated by the Write command during which the beginning column address and bank/group address for the data to be written to the array is provided. The data is provided to the DRAM on the DQ inputs CAS Write Latency (CWL) cycles after the Write command along with the proper waveform on the DQS inputs. CAS Write Latency is defined and measured from final cycle of the Write command to the first effective rising DQS (excluding write preamble).

4.8.1 Write Data Mask

One write data mask (DM_n) pin for each byte data group is supported on x8 and x16 DDR5 SDRAMs. The DM_n pin/function is enabled via mode register. For the x4 configuration SDRAM, the DM mode register setting must be disabled. The DM_n pin has identical timings and termination functionality on write operations as the DQ pins, as shown in Figure 43. The DM_n pin is not used for read cycles and the pin should behave like a DQ pin driving high or be terminated to RTT_PARK. When the DM function is disabled by MR, the DRAM disables the DM input and output receiver and does not expect nor drive any valid logic level.

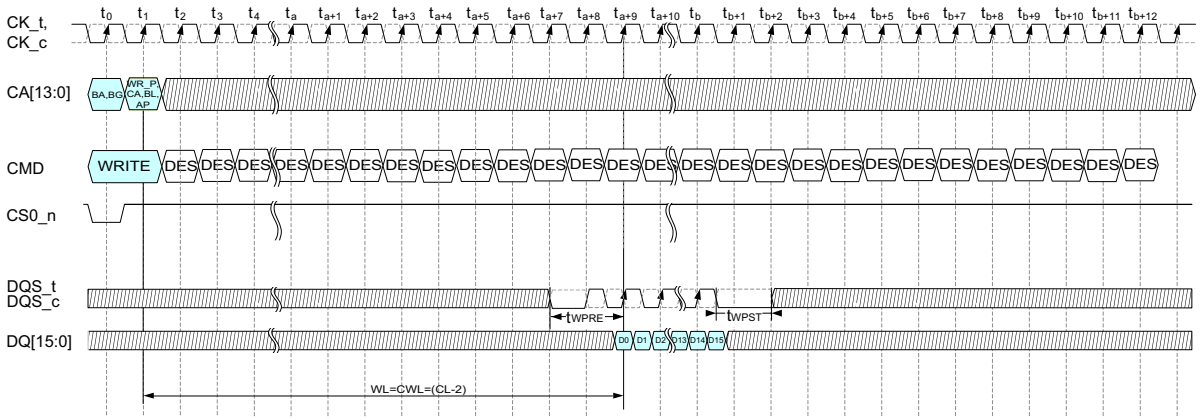
Each data mask burst bit position corresponds to the same bit position in the DQ data burst across the corresponding byte group.

The WR_partial = Low as part of the write command must be used in conjunction with the DM_n data. The WR_partial = Low is to help DRAM start an internal read for 'read modify write' during masked writes. If WR_partial = High during write, then the mask data on DM_n must be high. If DM is disabled, MR5 OP[5] = 0, WR_Partial must be “H”. DM_n may be high or low.

4.8.2 Write Burst Operation

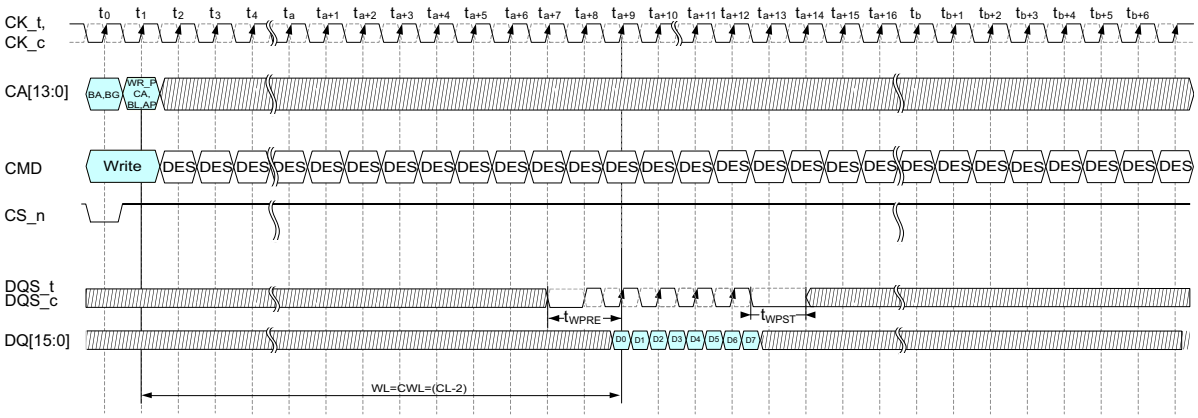
The following write timing diagrams are to help understand the meaning of each write parameter; the diagrams are just examples. The details of each parameter are defined separately.

In these write timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be appropriate.



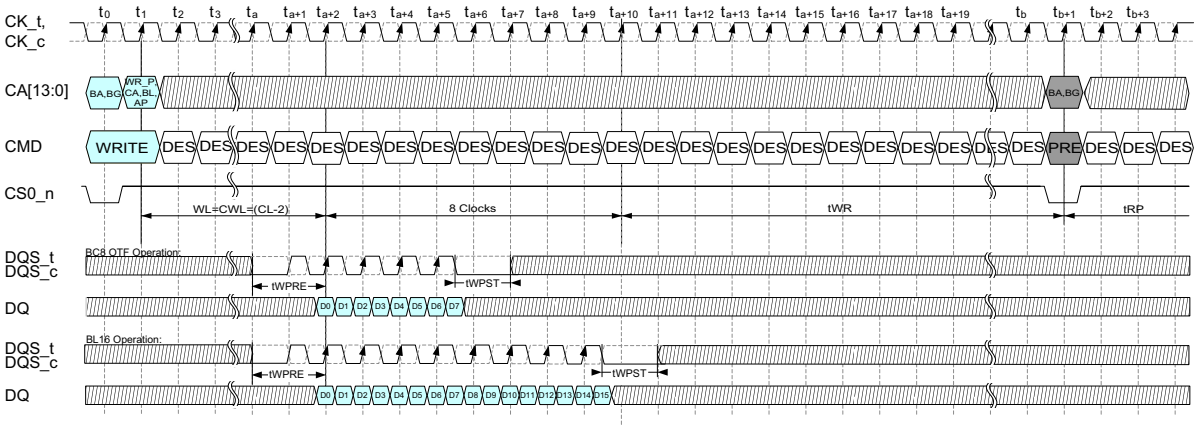
Note(s):
1. BL=16, 2tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 42 — WRITE Burst Operation (BL16)



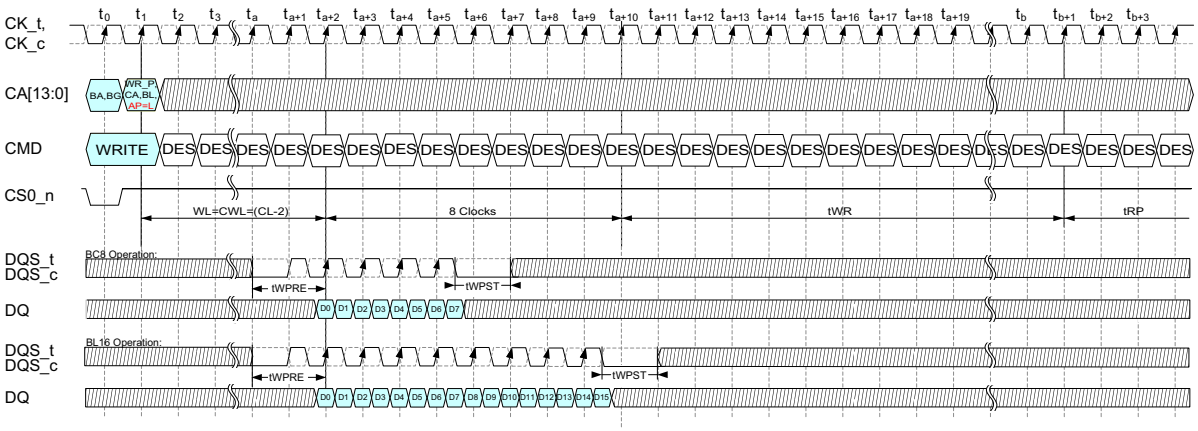
Note(s):
1. BC=8, 2tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.

Figure 43 — Write Burst Operation (BC8)



Note(s):
1. BC=8 or BL=16, Preamble = 2tCK - 0010 pattern, Postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at Ta+10
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 44 — WRITE (BL16) to PRECHARGE Operation with 2tCK Preamble



Note(s):
1. BC OTF=8 or BL=16, Preamble = 2tCK - 0010 pattern, Postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at Ta+10.
   WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 45 — WRITE (BL16) with Auto PRECHARGE Operation and 2tCK Preamble

4.8.3 Write Timing Parameters

The following figure is for example only to enumerate the strobe edges for a particular write burst. For a valid burst, all timing parameters for each edge of a burst must be satisfied.

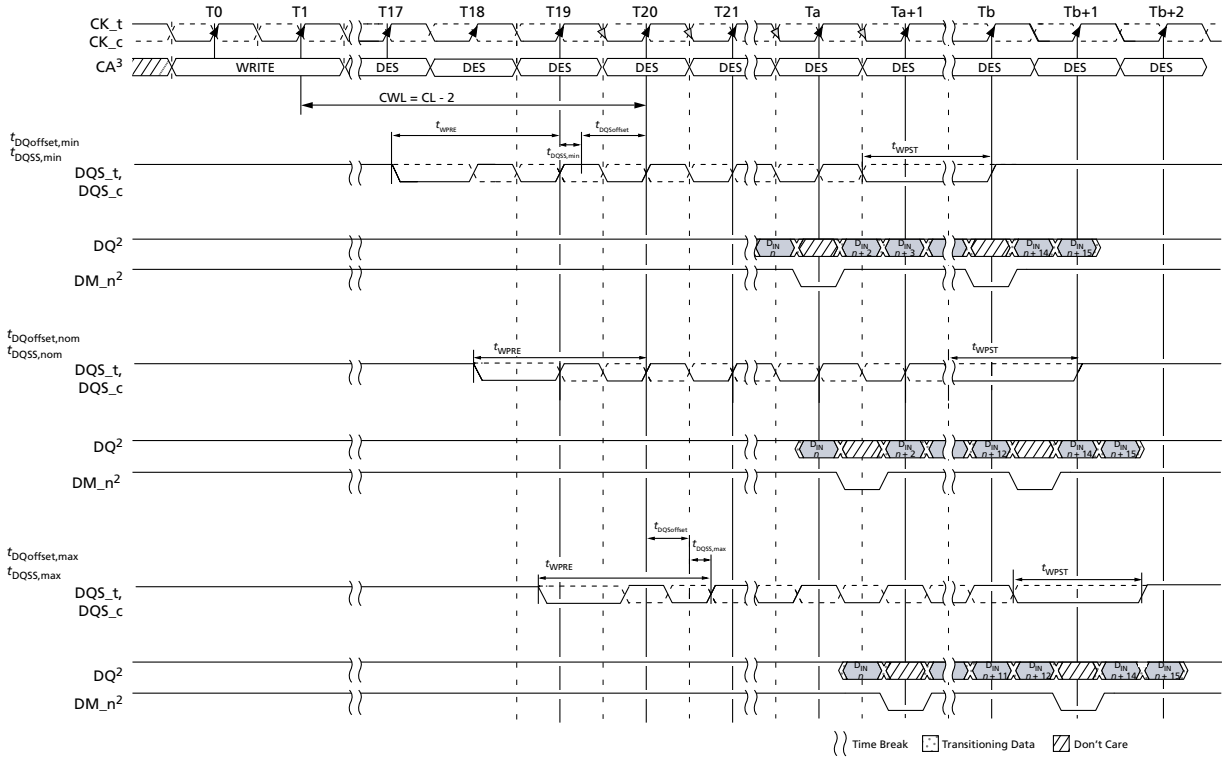


Figure 46 — DDR5 Write Timing Parameters

Notes

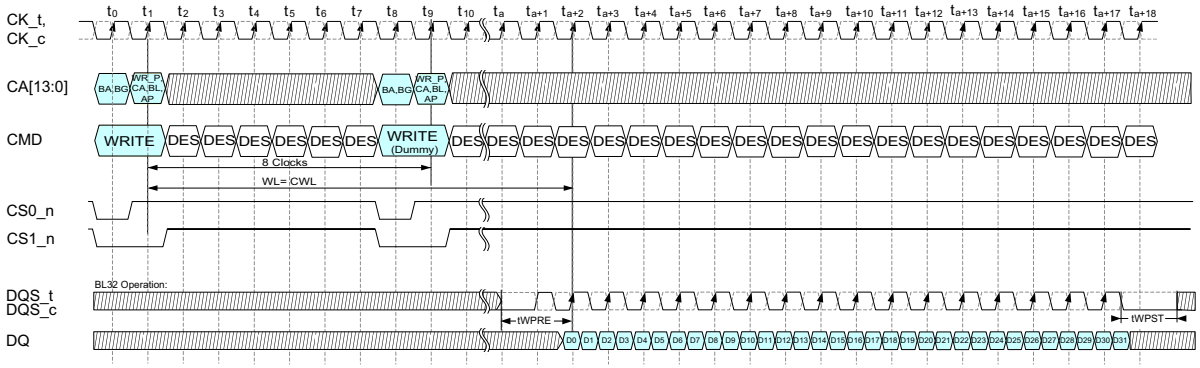
1. BL=16, Preamble=2CK - 0010 pattern, Postamble=1.5CK,
2. DES commands are shown for ease of illustration, other commands may be valid at these times.
3. t_{DQSS} must be met at each rising clock edge.
4. Figure assumes DRAM internal WL training complete.
5. DQ/DM_n pulse timing and DQS to DQ skew defined by Rx Strobe Jitter Sensitivity Specifications for the respective speed bin.

4.8.4 Write Burst Operation for Optional BL32 Mode

The following write timing diagrams cover write timings for fixed BL32, BL32 in BL32 OTF mode and BL16 in BL32 OTF mode for x4 devices only.

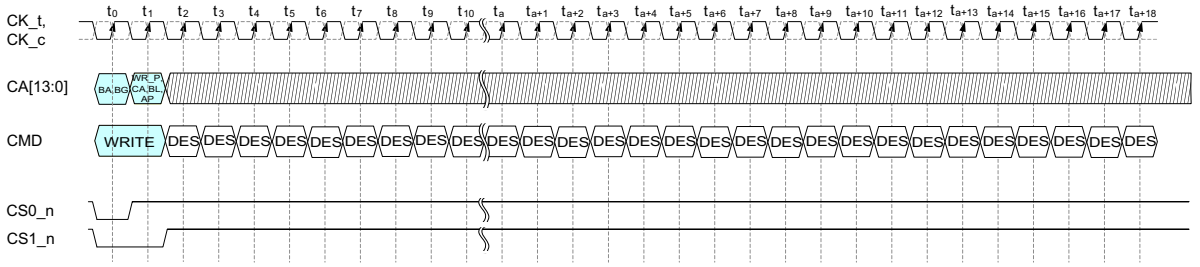
In these write timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be appropriate.

A dummy CAS command is required for second half of the transfer of BL32. If non-target ODT is needed in the system then a dummy ODT command must be issued to the non-target rank for second half of the transfer of BL32



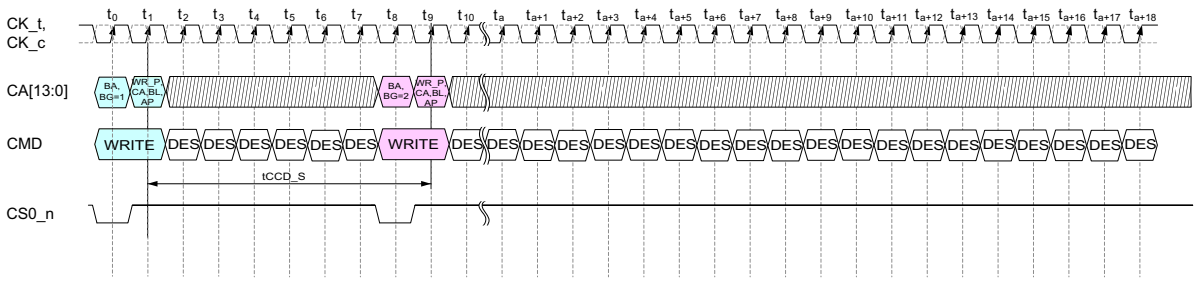
Note(s):
1. BL=32, 2tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. A dummy WR command is required for the second half of the transfer with a delay of 8 clocks from the first WR command.
4. The figure also shows a dummy ODT command being issued to non-target rank 1 for the second half of the transfer.
5. C10 is used for burst ordering and shall be LOW for the first WR command, and be HIGH for dummy WR command.
6. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.
7. CA bits other than C10 and AP in dummy CAS command are the same as the first CAS command.

Figure 47 — Write Timing for fixed BL32 and BL32 in BL32 OTF mode



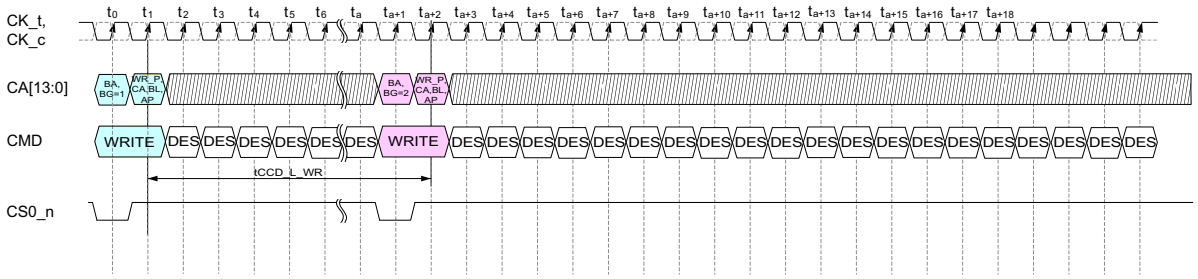
Note(s):
1. Figure shows BL16 write operation when MR0 is programmed to use BL32 OTF mode. In this case, no dummy WR command is required as transfer size is BL16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times including commands to allow data transfer from the same die after transfer of BL16.
3. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 48 — Write Timings for BL16 in BL32 OTF mode



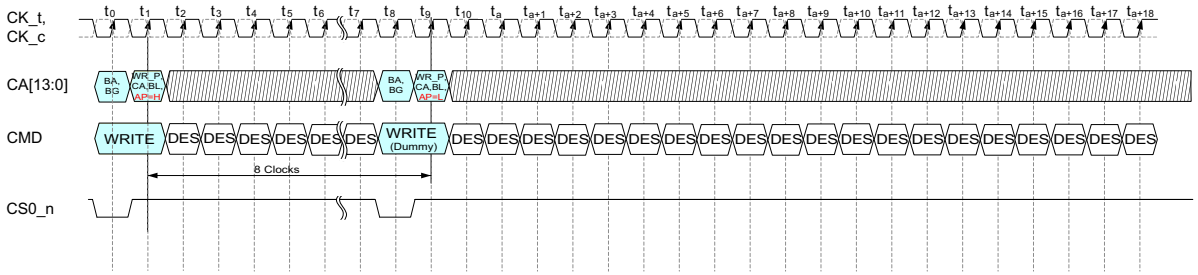
Note(s):
1. Figure shows back to back BL16 writes to different bank groups.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 49 — Write to Write to Different Bank Group for BL16 in BL32 OTF



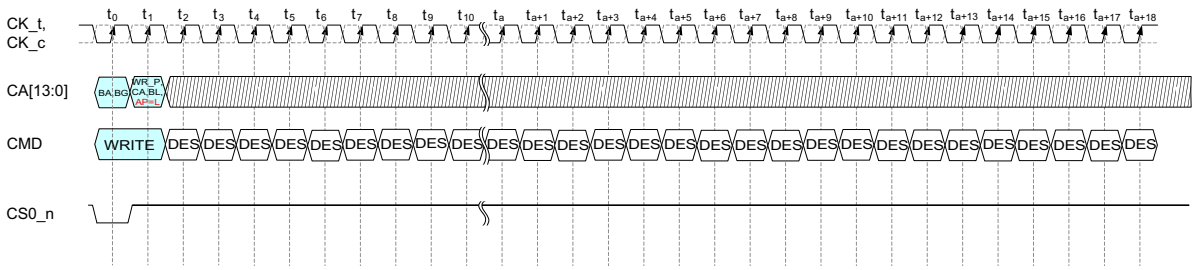
Note(s):
1. Figure shows back to back BL16 writes to same bank group using a timing of tCCD_L_WR.
2. Back to Back BL32 writes to same bank group shall have a minimum separation of 16 clocks.
3. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 50 — Write to Write to Same Bank Group for BL16 in BL32 OTF



Note(s):
1. AP bit must be set HIGH for first CAS and LOW for dummy CAS command.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.
3. CA bits other than C10 and AP in dummy CAS command are the same as the first CAS command.

Figure 51 — Write with Auto-Precharge for Fixed BL32 and BL32 in BL32 OTF Mode



Note(s):

1. AP bit must be set to LOW with the CAS command.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 52 — Write with Auto-Precharge for BL16 in BL32 OTF Mode

4.8.5 Same Bank Group Write to Write Timings

DDR5 devices will have separate same bank group write timings, based on whether the second write requires an RMW (Read-Modify-Write) access or JW (Just-Write) access. In JW access, DDR5 updates all 128 bits of data on the addressed codeword, while in RMW access, a part of 128 bits is updated.

Table 48 — JW (Just-Write) Access and RMW (Read-Modify-Write) Access Definition

Configuration	BL16		BC8		Optional BL32	Notes
	Normal	Data Mask	Normal	Data Mask		
x4	RMW	—	RMW	—	JW	1,2,3
x8 / x16	JW	RMW			—	1,2,3

Note(s):
1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01_B, where Write command is issued with BL=L in CA5.
2. Optional BL32 refers to BL32 fixed mode enabled by MR0 OP[1:0]=10_B or BL32 OTF mode enabled by MR0 OP[1:]=11_B, where Write command is issued with BL=L in CA5.
3. Data Mask refers to Data Mask mode enabled by MR5 OP[5]=1_B, where Write command is issued with WP=L in CA11.

Table 49 — Same Bank-Group Write Access to RMW Access Timings

From	To		Notes
	BL16	BC8	
BL16	tCCD_L_WR	tCCD_L_WR	1,2,3
BC8	tCCD_L_WR	tCCD_L_WR	1,2,3
Optional BL32	8nCK+tCCD_L_WR	—	1,2,3,4

Note(s):
1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01_B, where Write command is issued with BL=L in CA5.
2. Optional BL32 refers to BL32 fixed mode enabled by MR0 OP[1:0]=10_B or BL32 OTF mode enabled by MR0 OP[1:]=11_B, where Write command is issued with BL=L in CA5.
3. In Optional BL32 case, this timing table affects to the 1st Write command only, not the dummy Write command.
4. There is no BL32 to BC8 case.

Table 50 — Same Bank-Group Write Access to JW Access Timings

From	To		Notes
	BL16	Optional BL32	
BL16	tCCD_L_WR2	tCCD_L_WR2	1,2,3
BC8	tCCD_L_WR2	—	1,2,3,4
Optional BL32	—	8nCK+tCCD_L_WR2	1,2,3

Note(s):
1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01_B, where Write command is issued with BL=L in CA5.
2. Optional BL32 refers to BL32 fixed mode enabled by MR0 OP[1:0]=10_B or BL32 OTF mode enabled by MR0 OP[1:]=11_B, where Write command is issued with BL=L in CA5.
3. In Optional BL32 case, this timing table affects to the 1st Write command only, not the dummy Write command.
4. There is no BC8 to BL32 case.

4.8.6 Different Bank-Group Write to Write Timings

Table 51 — Different Bank-Group Write to Write Timings

From	To			Notes
	BL16	BC8	Optional BL32	
BL16	8nCK	8nCK	8nCK	1,2,3
BC8	8nCK	8nCK	—	1,2,3,4
Optional BL32	16nCK	—	16nCK	1,2,3,4

Note(s):
1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01_B, where Write command is issued with BL=L in CA5.
2. Optional BL32 refers to BL32 fixed mode enabled by MR0 OP[1:0]=10_B or BL32 OTF mode enabled by MR0 OP[1:]=11_B, where Write command is issued with BL=L in CA5.
3. In Optional BL32 case, this timing table affects to the 1st Write command only, not the dummy Write command.
4. There is no BC8 to BL32 case.

4.8.7 Write Timing Violations

4.8.7.1 Motivation

Generally, if Write timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain violations as specified below, the DRAM is guaranteed to not “hang up,” and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

4.8.7.2 Data to Strobe Eye Height or Width Violations

Should the required data to strobe timing or voltage parameters be violated (Such as: tRx_RDQ_tMargin, tRx_DQS2DQ_Skew, VRx-_DQS, VRx_DQ, etc.), for any of the data/strobe timing edges or data/strobe voltage limits associated with a write burst data eye, then incorrect data might be written to the memory locations addressed with this WRITE command.

In the example, Figure X (add example timing diagram reference) the relevant strobe edges for a write burst are associated with the clock edges: Tn,Tn+0.5,Tn+1,...,Tn+8.5

Subsequent reads from that location might results in unpredictable read data, however the DRAM will work properly otherwise.

4.8.7.3 Strobe and Strobe to Clock Timing Violations

Should the strobe timing requirements (tWPRE, tWPST) or the strobe to clock timing requirements (tDQSS, tDQSoffset) be violated for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise with the following constraints:

(1) Both Write CRC and data burst OTF are disabled; timing specifications other than tWPRE, tWPST, tDQSS, tDQSoffset are not violated.

(2) The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the Write-Latency position.

(3) A Read command following an offending Write command from any open bank is allowed.

(4) One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued tCCD_L later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.

(5) One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued tCCD_S later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.

(6) Once one or more precharge commands (PREpb, PREsb, or PREab) are issued to DDR5 after offending WRITE command and all banks become precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.

(7) DQS strobes including preamble must align to each Write commands data burst length configuration. If the DRAM fails to capture or incorrectly de-serializes the incoming data stream because of misalignment or missing strobe edges, errors may occur. These errors will propagate indefinitely until the DRAM is put into an idle state, i.e., all banks are in the precharged state with tRP satisfied.

4.8.8 Write Enable Timings

4.8.8.1 Introduction

The following specifies the relationship between the write enable timing window tWPRE_EN_ntck and the DRAM related DQS to CK drift window tDQSD as well as the system related DQS to CK drift window tDQSS around the final DQS to CK offset trained pass/fail point tDQSoffset based on write leveling feedback in order to support n-tck pre-amble mode. Functional operation requires that the following condition is met:

- tWPRE_EN_ntck >= |tDQSSmin|+tDQSSmax+|tDQSDmin|+tDQSDmax

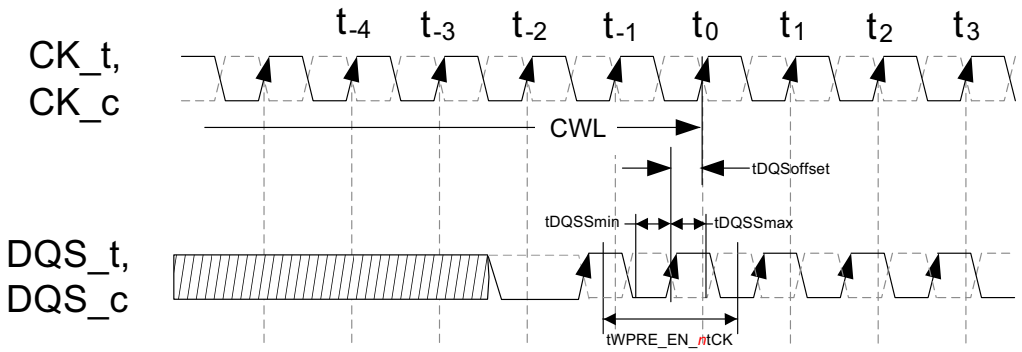


Figure 53 — tDQSS: DRAM external CLK-to-DQS Variation

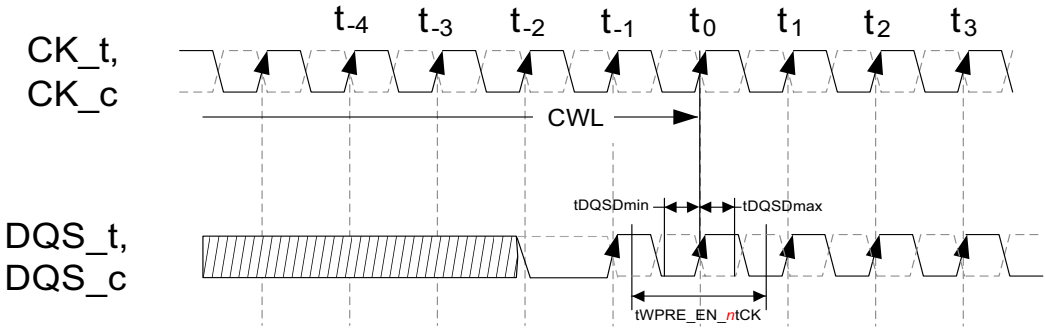


Figure 54 — tDQSD: DRAM internal CLK-to-DQS Variation

Table 52 — Write enable timing parameters DDR5 3200 to 5600

Parameter	Symbol	Speed Bins DDR5 3200-6400		Unit	Notes
		Min	Max		
2-tck Write pre-amble enable window	tWPRE_EN_2tck	1.5	-	tCK	2
3-tck Write pre-amble enable window	tWPRE_EN_3tck	2.5	-	tCK	2
4-tck Write pre-amble enable window	tWPRE_EN_4tck	2.5	-	tCK	2
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	tDQSoffset	-0.5	0.5	tCK	3
DRAM voltage/temperature drift window of first rising DQS_t pre-amble edge relative to CWL CK_t-CK_c edge	tDQSD	-0.25* tWPRE_EN_*n*t CK(min)	0.25* tWPRE_EN_*n*t CK(min)	tCK	1
Host and system voltage/temperature drift window of first rising DQS_t pre-amble edge relative to CWL CK_t-CK_c edge	tDQSS	-0.25* tWPRE_EN_*n*t CK(min)	0.25* tWPRE_EN_*n*t CK(min)	tCK	1,4

Note(s):

1. Measured relative to the write leveling feedback, after write leveling training has been completed.
2. Includes min DQS and CK timing terms TBD.
3. When measuring the tDQSoffset, tWLS/H are reflected in the tDQSoffset result.
4. DDR5-3200 timings apply for data rates <2933 MT/s. For example, at 2000 MT/s, tDQSS(max) = (2000/2933)*0.25*tWPRE_EN_*n*tck(min) = 0.17*tWPRE_EN_*n*tck(min).

Symbol	Description	Min	Max	Unit
tWLS/H	Write Leveling Setup/Hold Time	-80	+80	ps

4.9 Self Refresh Operation

The Self-Refresh command can be used to retain data in the DDR5 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR5 SDRAM retains data without external clocking. The DDR5 SDRAM device has a built-in timer to accommodate Self-Refresh operation. While in Self Refresh, the DDR5 SDRAM adjusts and updates its internal average periodic refresh interval, as needed, based on its own temperature sensor. The internal average periodic refresh interval adjustment (increasing, decreasing or staying constant) does not require any external control.

Self Refresh entry is command based (SRE), while the Self-Refresh Exit Command is defined by the transition of CS_n LOW to HIGH with a defined pulse width tCSH_SRexit, followed by three or more NOP commands (tCSL_SRexit) to ensure DRAM stability in recognizing the exit. This is described below in more detail.

Before issuing the Self-Refresh-Entry command, the DDR5 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, etc. satisfied), no data bursts are in progress, and all timings from previous operations are satisfied (tMRD, tRFC, etc.). A Deselect command must be registered on the last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect commands must also be registered at the next positive clock edges until tCPDED is satisfied. After tCPDED has been satisfied, CS_n must transition low. After CS_n transitions low at the end of tCPDED, the CS_n shall stay low until exit. The DDR5 SDRAM may switch to a CMOS based receiver to save more power and that transition should coincide with CS_n going low.

When the CS_n is held low, the DRAM automatically disables ODT termination and sets Hi-Z as termination state regardless RTT configuration for the duration of Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set RTT_PARK (for DQs) asynchronously during tXSDLL when RTT_PARK is enabled. CA/CS/CK ODT shall revert to its strapped or its MR ODT Setting state if previously applied. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR5 SDRAM has entered Self-Refresh mode, all of the external control signals, except CS_n and RESET_n, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSS and VPP) must be at valid levels. DRAM internal VrefDQ and/or VrefCA generator circuitry may remain ON or turned OFF depending on DRAM design. If DRAM internal VrefDQ and/or VrefCA circuitry is turned OFF in self refresh, when DRAM exits from self refresh state, it ensures that VrefDQ and/or VrefCA and generator circuitry is powered up and stable within tXS period. First Write operation or first Write Leveling Activity may not occur earlier than tXS after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within tSR period once it enters Self-Refresh mode.

The clocks must stay on until tCKLCS but can be DON'T CARE after tCKLCS expires but it should be noted that shortly after tCPDED, the termination for the clocks will be off. The clock is internally disabled (in the DRAM) during Self-Refresh Operation to save power. The minimum time that the DDR5 SDRAM must remain in Self-Refresh mode is tCSL. The user may change the external clock frequency or halt the external clock tCKLCS after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. Since the DRAM will switch to a CMOS based driver to save power, the DRAM will trigger Self-Refresh exit upon seeing the CS_n transition from low to high and stay high for tCSH_SRExit. tCASRX prior to CS_n transitioning high, the CA bus must be driven high. Once tCSH_SRExit is satisfied, three NOP commands must be issued, otherwise the DRAM could be put into an unknown state. The clocks must be valid for tCKSRX prior to issuing the NOP commands that completes the Self Refresh exit sequence. Once a Self-Refresh Exit is registered, the following timing delay must be satisfied:

1. Commands that do not require locked DLL:
tXS - ACT, MPC, MRW, PDE, PDX, PRE(ab,sb,pb), REF(ab,sb), RFM(ab,sb), SRE, VREFCA & WRP

2. Commands that require locked DLL:
tXS_DLL - RD, MRR & WR

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands". To issue ZQ calibration commands, applicable timing requirements must be satisfied.

Upon exiting Self Refresh, one additional refresh shall be issued in addition to refreshes normally scheduled. This refresh counts toward the maximum number of refreshes which may be postponed. The extra refresh consists of a single REFab command or n * REFsb, where n is the number of banks in a bank group. If Self Refresh is to be re-entered and no regularly scheduled periodic refresh commands have been issued, a minimum of one REFab or n*REFsb commands shall be issued prior to Self Refresh re-entry.

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is tXS.
The value of tXS is (tRFC). This delay is to allow for any refreshes started by the DRAM to complete. tRFC continues to grow with higher density devices so tXS will grow as well.

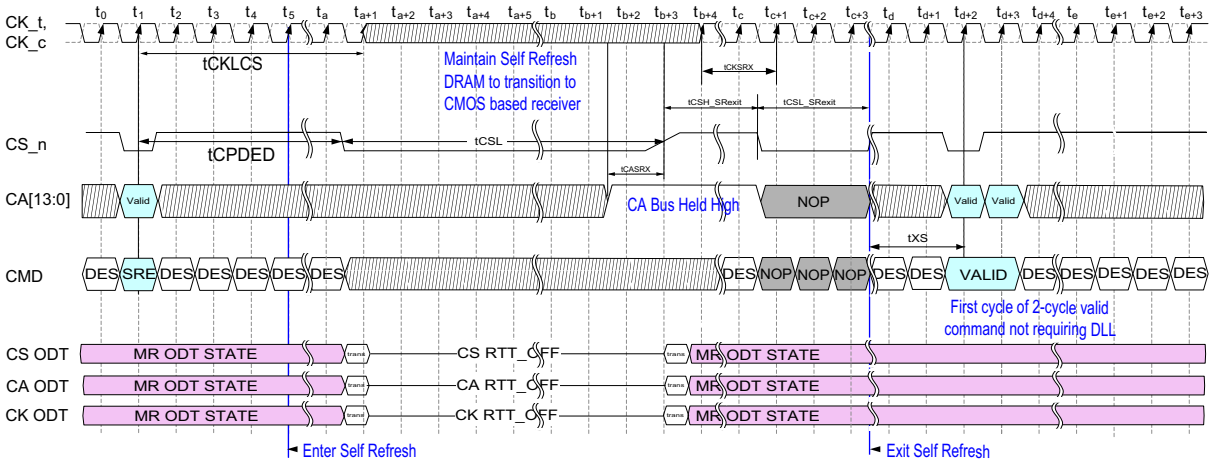


Figure 55 — Self-Refresh Entry/Exit Timing w/ 2-Cycle exit command

Note(s):
1 - While in 2N mode, tCSL_SRexit will not be statically held low (as shown above), as it will pulse for each 2 cycle period. Refer to the 2N mode section for more details.
2 - Both tCSH_SRexit and tCSL_SRexit timings must be satisfied to guarantee DRAM operation.
3 - When tCSH_SRexit,min expires, the CA bus is allowed to transition from all bits High to any valid (V) level. Prior to CS_n being registered Low at tc+1, the CA bus must transition to NOP conforming to the CAI state of the DRAM and complying with applicable DRAM input timing parameters.

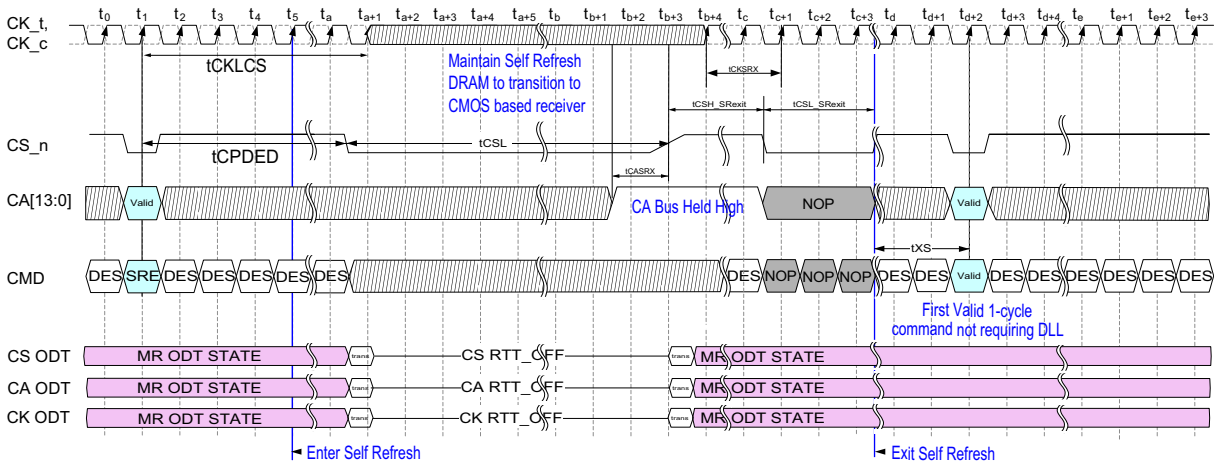


Figure 56 — Self-Refresh Entry/Exit Timing w/ 1-Cycle exit command

Note(s):
1 - While in 2N mode, tCSL_SRexit will not be statically held low (as shown above), as it will pulse for each 2 cycle period. Refer to the 2N mode section for more details.
2 - Both tCSH_SRexit and tCSL_SRexit timings must be satisfied to guarantee DRAM operation.
3 - When tCSH_SRexit,min expires, the CA bus is allowed to transition from all bits High to any valid (V) level. Prior to CS_n being registered Low at tc+1, the CA bus must transition to NOP conforming to the CAI state of the DRAM and complying with applicable DRAM input timing parameters.

Table 53 — Self-Refresh Timing Parameters

Parameter	Symbol	Min	Max	Unit	Note
Command pass disable delay	tCPDED	max(5ns, 8nCK)	-	nCK, ns	
Self-Refresh CS_n low Pulse width	tCSL	10	-	ns	
Self-Refresh exit CS_n High Pulse width	tCSH_SRexit	13	30	ns	
Self-Refresh exit CS_n Low Pulse width	tCSL_SRexit	3nCK	30ns	nCK, ns	1
Valid Clock Requirement before SRX	tCKSRX	max(3.5ns, 8tCK)	-	nCK, ns	
Valid Clock Requirement after SRE	tCKLCS	tCPDED + 1nCK	-	nCK, ns	
Self-Refresh exit CS_n high	tCASRX	0		ns	
Exit Self-Refresh to next valid command NOT requiring a DLL	tXS	tRFC1	-	ns	
Exit Self-Refresh to next valid command NOT requiring a DLL in same logical layer	tXS_slr	tRFC1_slr+10ns	-	ns	2,3,4
Exit Self-Refresh to next valid command NOT requiring DLL in a different logical layer	tXS_dlr	tRFC1_slr+10ns	-	ns	2,3,4
Exit Self-Refresh to next valid command requiring a DLL	tXS_DLL	tDLLK		ns	

Note(s):

1 - While in 2N mode, tCSL_SRexit will not be statically held low, as it will pulse for each 2-cycle period for a min of 6nCK. Refer to the 2N mode section for more details.

2 - Upon exit from Self-Refresh, the 3D Stacked DDR5 SDRAM requires a minimum of one extra refresh command to all logical ranks before it is put back into Self-Refresh Mode.

3 - This parameter utilizes a value that varies based on density. Refer to the 3DS Refresh section for more information.

4 - These timings are for x4 2H and 4H 3Ds devices.

4.9.1 Self Refresh in 2N Mode

The timing diagram below shows details for Self Refresh entry/exit in 2N Mode. Only SRX, with a pulsing CS_n (NOP-DES-NOP-DES-NOP) during tCSL_SRexit, to a 1-cycle command is shown, but behavior is similar for SRX to a 2-cycle command. Behavior is similar for Frequency Change during Self Refresh, with or without VREF and/or ODT changes. Pulsing CS_n during tCSL_SRexit is not required for Self Refresh exit (e.g. CS_n may optionally be held low for the full tCSL_SRexit duration).

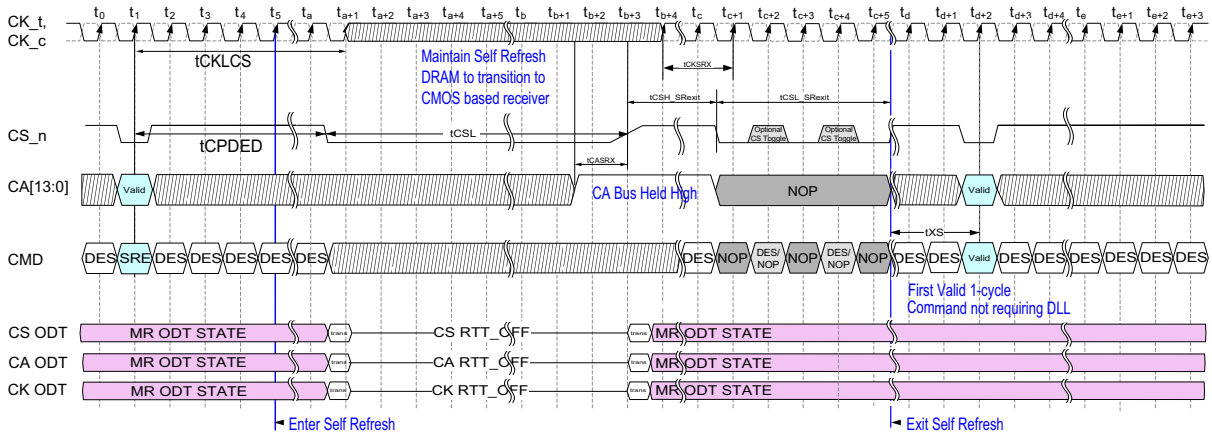


Figure 57 — Self-Refresh Entry/Exit Timing in 2N Mode w/ 1-Cycle exit command

Note(s):

1 - Both tCSH_SRexit and tCSL_SRexit timings must be satisfied to guarantee DRAM operation.

2 - When tCSH_SRexit,min expires, the CA bus is allowed to transition from all bits High to any valid (V) level. Prior to CS_n being registered Low at tc+1, the CA bus must transition to NOP conforming to the CAI state of the DRAM and complying with applicable DRAM input timing parameters.

4.9.2 Partial Array Self Refresh (PASR)

DDR5 DRAMs may contain an optional feature that disables refresh to selected segments in each bank when in self refresh. The feature allows for lower self refresh power if portions of the DRAMs are not required to retain data. Each bank is divided into six or eight segments based on the three highest row address bits supported by the DRAM device's density. Non-Binary density devices are divided into 6 segments as the 110 and 111 encodings of the PASR segment row bits are not used.
Binary densities are divided into 8 segments.

MR60 provides the segment mask for all banks, with one bit per segment. A 0 (default) in the bit position provides normal refresh operation for the segment while a 1 masks that segment. Masked segments are NOT refreshed during self refresh. Note that this affects Self Refresh only. All segments are refreshed by refresh command when out of self refresh.

Segments which are masked are not guaranteed to retain their data if self refresh is entered. ECS Transparency will not produce accurate results if any mask bit is set, but ECS scrubbing will still occur if enabled.

MR19 bit 7 is indicates whether the DRAM supports PASR. 0 = Not Supported, 1 = Supported

Table 54 — MR60 Definition

Segment(PASR Row Bits)	Type	Operand	Data	Notes
Segment 0 (000)	W	OP0	0=Normal, 1=Masked	
Segment 1 (001)	W	OP1	0=Normal, 1=Masked	
Segment 2 (010)	W	OP2	0=Normal, 1=Masked	
Segment 3 (011)	W	OP3	0=Normal, 1=Masked	
Segment 4 (100)	W	OP4	0=Normal, 1=Masked	
Segment 5 (101)	W	OP5	0=Normal, 1=Masked	
Segment 6 (110)	W	OP6	0=Normal, 1=Masked	Must be 0 for 24Gbit and 48Gbit devices.
Segment 7 (111)	W	OP7	0=Normal, 1=Masked	Must be 0 for 24Gbit and 48Gbit devices.

Table 55 — PASR Segment Row Address Bits

DRAM Density	PASR Row Bits	Segments
8Gbit	R15:13	8
16Gbit	R15:13	8
24Gbit	R16:14	6
32Gbit	R16:14	8
48Gbit	R17:15	6
64Gbit	R17:15	8

4.10 Power down Mode

DDR5's power down mode is new to the DDR family, as it no longer has a CKE pin to control entry and exit. Instead, the PDE/PDX move to command based, triggered by the CS_n. Once in PD mode, the CS_n acts effectively like the historic CKE pin, waiting for it to transition from HIGH to LOW (with its command). In PDE mode, it should be sampled on every edge.

4.10.1 Power-Down Entry and Exit

Power-down is entered when the command is registered. Unlike Self Refresh Mode, CS_n will NOT be held low constantly while in Power-Down. Timing diagrams are shown in Figure 58 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. SDRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation as long as DRAM controller complies with SDRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CS_n, RESET_n. If CA11=L during the PDE command, CA1 and CA4 will also be excluded, allowing the appropriate NT ODT command to be passed through and decoded by the non-target SDRAM while the target SDRAM remains in power down (i.e. the SDRAM will monitor commands that utilize NT ODT via CA1 and CA4 and will not exit Power Down if a valid NT ODT command is registered). If CA11=H during the PDE command, only the PDX command, qualified by CS_n, is legal during power down. If CA11=L during the PDE command, only NT ODT commands and PDX commands, qualified by CS_n, are legal during power down. Refer to the command truth table for more information.

MRR NT ODT commands during Power Down are not support with Burst on the fly (OTF) modes in MR0:OP[1:0].

When power-down is entered with ODT control enabled (CA11=L) the DRAM will continue to accept NT termination commands throughout the power-down process, including entry and exit. Upon entry, during the tCPDED period, the DRAM will be switching from decoding all CA bus command bits to only decoding CA1 and CA4. During this time all CA command bits must be valid when CS_n is asserted with the full RD or WR command, as the DRAM may still be decoding the full command. Following tCPDED, only CA1 and CA4 need be valid as the DRAM will be ignoring the others. Following the PDX command, all CA command bits must be valid for NT termination commands also, as the DRAM will be transitioning to decoding all bits. It is only the time between tCPDED completion and tXP start that CA13:5, 3:2, & 0 need not be valid

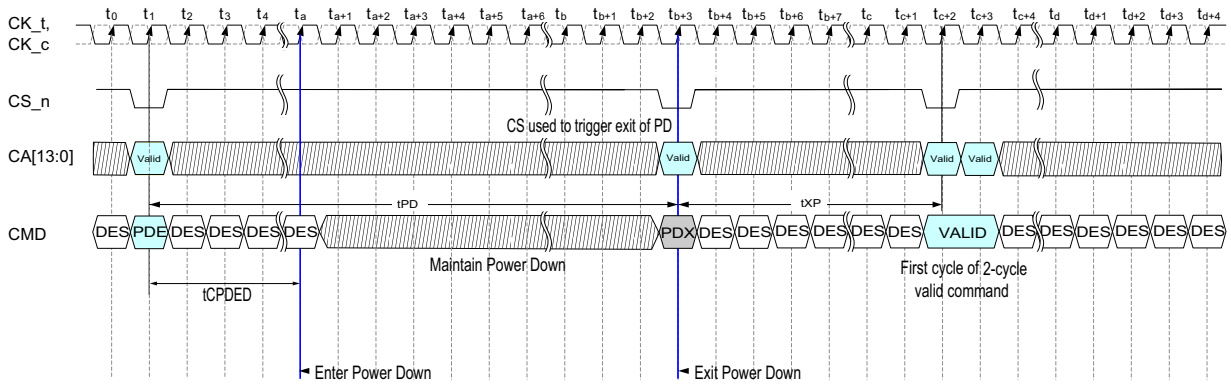


Figure 58 — Power-Down Entry and Exit Mode

Note(s):

1. There is no specific PDX command. In the case of systems with register using CAI, the encoding out of the register may be inverted from a NOP type command.
2. Diagram above is shown with a valid 2-cycle command after tXP for simplicity. 1-cycle valid commands are also legal.
3. CS_n shall be held HIGH, not toggled, during Power-Down, except Non-Target ODT command when PDE with CA11=L is asserted.

Table 56 — Power-Down Entry Definitions

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	On	Fast	tXP to any valid command.

The DLL is kept enabled during precharge power-down or active power-down. (If RESET_n goes low during Power-Down, the DRAM will be out of PD mode and into reset state). Power-down duration is limited by tPD(max) of the device.

Table 57 — Power Down Timing Parameters

Parameter	Symbol	Min	Max	Unit	Note
Command pass disable delay	tCPDED	max(5ns, 8nCK)	-	ns	
Power Down Time	tPD	max(7.5ns, 8nCK)	5 * tREFI1 (Normal) 9 * tREFI2 (FGR)	ns	
Exit Power Down to next valid command	tXP	max(7.5ns, 8nCK)		ns	
Timing of ACT command to Power Down Entry command	tACTPDEN	2		nCK	1
Timing of PREab, PREsb or PREpb to Power Down Entry command	tPRPDEN	2		nCK	1
Timing of RD or RD w/AP to Power Down Entry command	tRDPDEN	RL+RBL/2+1		nCK	4
Timing of WR to Power Down Entry command	tWRPDEN	WL+WBL/2+(tWR/tCK(avg))+1		nCK	2, 4
Timing of WR w/AP to Power Down Entry command	tWRAPDEN	WL+WBL/2+WR+1		nCK	3, 4
Timing of REFab or REFsb command to Power Down Entry command	tREFPDEN	2		nCK	
Timing of MRR to command to Power Down Entry command	tMRRPDEN	RL+8+1		nCK	4
Timing of MRW command to Power Down Entry command	tMRWPDEN	tMRD(min)		nCK	
Timing of MPC command to Power Down Entry command	tMPCPDEN	tMPC_delay		nCK	5

Note(s):
1. Powerdown command can be sent while operations such as row activation, precharge, auto-precharge or refresh are in progress but IDD spec will not be applied until the operations are finished.
2. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK.
3. WR in clock cycles as programmed in MR6.
4. RD/WR/MRR can refer to both Target command and Non-Target command when CA11=H during PDE command.
5. tMPD_delay is a valid timing parameter for all MPC commands except:
   a) Enter CS training Mode, Enter CA Training Mode, PDA Enumerate ID Program Mode because Power Down Entry is not supported for these MPC commands.
   b) Apply VrefCA, VrefCS and RTT_CA/CS/CK because this MPC command requires waiting for VrefCA_time/VREFCS_time.

Table 58 — Valid Command During Power Down with ODT enabled

CA1	CA4	Command	Operation of DRAM in Power Down
L	L	Write	DRAM will enable ODT_WR_NOM
L	H	Read	DRAM will enable ODT_RD_NOM
H	L	Illegal	Illegal. CS_n will NOT be asserted to a powered down DRAM with this combination
H	H	PDX(NOP)	Exit Power Down

Note(s):
1 - MRR NT ODT commands during Power Down are not supported with Burst on the fly (OTF) modes in MR0:OP[1:0].

4.11 Input Clock Frequency Change

Once the DDR5 SDRAM is initialized, the DDR5 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under Self Refresh w/Frequency Change mode. Outside Self-Refresh w/Frequency Change mode, it is illegal to change the clock frequency.

Prior to entering Self-Refresh w/ Frequency Change mode, the host must program tCCD_L/tDLLK via MR13:OP[3:0] to the desired target frequency and configure VREFCA, RTT_CK, RTT_CS and RTT_CA if needed.

Once the DDR5 SDRAM has been successfully placed into Self-Refresh w/Frequency Change mode and tCKLCS has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. During tCSL_FreqChg and prior to exiting Self-Refresh, the DRAM will automatically apply the changes to tCCD_L/tDLLK, VREFCA, RTT_CK, RTT_CS and RTT_CA. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in Section 4.9 “Self-Refresh Operation”. For the new clock frequency, Mode Registers may need to be configured (to program the appropriate CL, Preambles, Write Leveling Internal Cycle Alignment, etc.) prior to normal operation.

The DDR5 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade.

4.11.1 Frequency Change Steps

The following steps must be taken:

1. Prior to SRE command, there are several modes that must or can be configured:
   1a. The host MUST program tCCD_L/tDLLK via MR13:OP[3:0] to the desired target frequency. During this stage, the values are set but not enabled.
   1b. The host can configure the appropriate CS/CA/CK ODT settings via Mode Register (MR32 & MR33) if new values are needed for the new target frequency. During this stage, the values are set but not enabled.
   1c. The host can configure the VREFCA & VREF CS via the VREFCA or VREFCS command(s). During this stage, the values are set but not enabled.
2. Enter SREF (Self Refresh Entry w/ Frequency Change) by sending the appropriate command (Similar to SRE with CA9=’L’).
3. After tCPDED, the CS_n will transition low, indicating to the DRAM that the terminations are safe to turn off.
4. After tCKLCS, the clocks can be turned off.
5. Device enters Self Refresh.
6. At this time, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX
7. Exiting Self-Refresh w/Frequency Change follows the same process as normal Self-Refresh exit.
8. After tXS, any additional mode registers that are needed for the new frequency can be configured or other commands not requiring a DLL may be issued. (ACT, MPC, MRW, PDE, PDX, PRE(ab,sb,pb), REF(ab,sb), RFM(ab,sb), SRE, VREFCA & WRP)
9. After tXS_DLL, normal operations resume and all commands are legal.

Table 59 — Self Refresh w/Freq Change (for reference)

Function	Abbreviation	CS	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Self Refresh Entry w/ Frequency Change	SREF	L	H	H	H	L	H	V	V	V	V	L	L	V	V	V	9

Note - See Command Truth Table for details

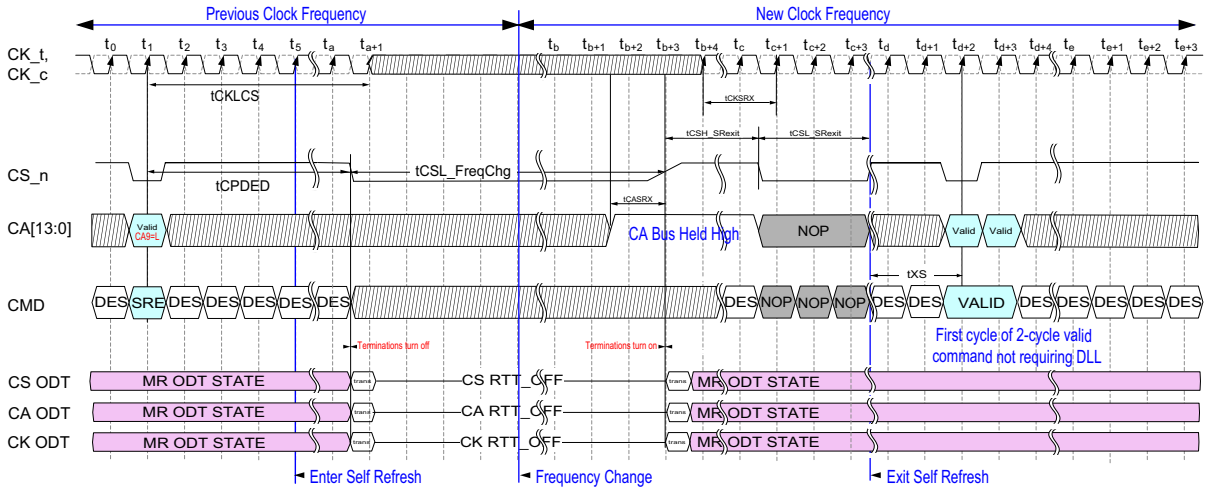


Figure 59 — Frequency Change during Self Refresh

Note(s):

1. While in 2N mode, tCSL_SRexit will not be statically held low (as shown above), as it will pulse for each 2 cycle period. Refer to the 2N mode section for more details.
2 - Both tCSH_SRexit and tCSL_SRexit timings must be satisfied to guarantee DRAM operation.
3. Diagram above is shown with a valid 2-cycle command after tXS for simplicity. 1-cycle valid commands are also legal.
4 - When tCSH_SRexit,min expires, the CA bus is allowed to transition from all bits High to any valid (V) level. Prior to CS_n being registered Low at tc+1, the CA bus must transition to NOP conforming to the CAI state of the DRAM and complying with applicable DRAM input timing parameters.

Table 60 — Self-Refresh Frequency Change Timing Parameters

Parameter	Symbol	Min	Max	Unit	Note
Self-Refresh CS_n low Pulse width with Freq Change	tCSL_ FreqChg	VrefCA_time	-	ns	1

Note(s):

1 - Since frequency can require VREFCA and CA/CK/CS ODT Changes, the min time is longer than the traditional tCSL when the SRE command with CA9=L is used.

4.12 Maximum Power Saving Mode (MPSM)

When Maximum Power Saving Mode is enabled by setting the MPSM enable (MR2:OP[3]) bit to '1' using MRW command, the device enters Maximum Power Saving Mode Idle (MPSM Idle) state. When Maximum Power Saving Mode for Device 15 is enabled by setting the Device 15 MPSM enable bit (MR2:OP[5]) to '1' using MRW command, and the device's PDA Enumerate ID (MR1 bits OP[3:0]) are equal to 15, the device enters Maximum Power Saving Mode Idle (MPSM Idle) state. Setting the Device 15 MSPM enable bit to '1' must be done after PDA device enumeration is complete. Once the DRAM is placed into the MPSM Idle state, it can stay in that state indefinitely, or it can further enter either Maximum Power Saving Mode Power Down (MPSM Power Down) state or Maximum Power Saving Mode Self Refresh (MPSM Self Refresh) state.

Data retention is not guaranteed when DRAM is in any of MPSM states. Mode register status and Soft PPR information is preserved.

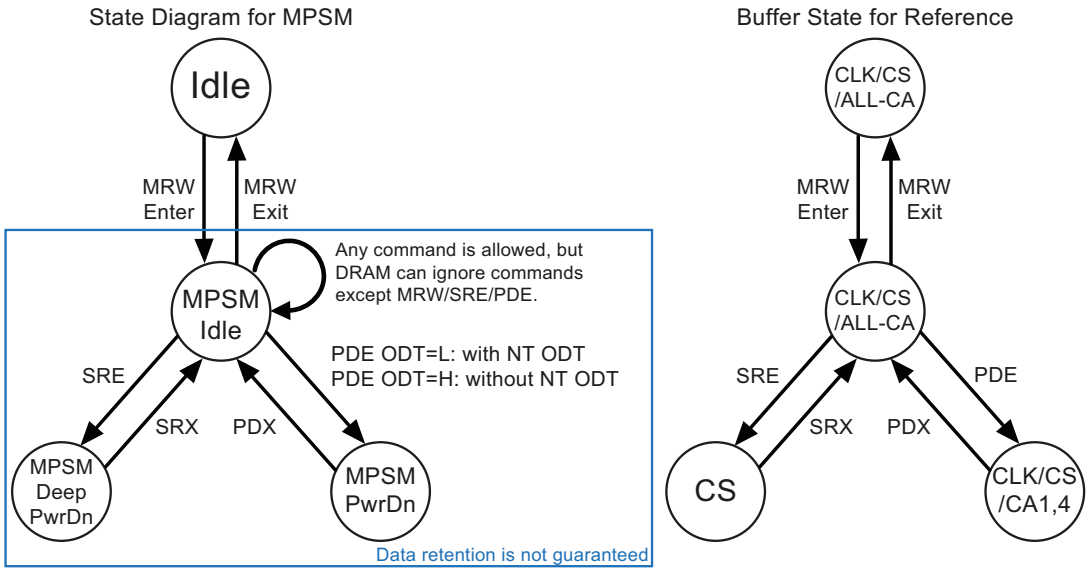


Figure 60 — State diagram for Maximum Power Saving Mode

Table 61 — MPSM Configuration Options

MPSM MR2:OP[3]	Device 15 MPSM MR2:OP[5]	PDA Enumeration ID MR1:OP[3:0]	Action
1	X	X	Enter MPSM on MRW
X	1	1111	Enter MPSM on MRW
0	0	X	Exit MPSM on MRW
0	X	Not equal to 1111	Exit MPSM on MRW

4.12.1 MPSM Idle State

When DDR5 SDRAM is in this state, it ignores all types of commands except MRW, ODT, Power Down Entry (PDE) and Self Refresh Entry (SRE) commands. MRW, ODT, PDE and SRE commands are executed normally. DRAM shall not respond to any other command except these four command types. DLL status is same as in normal idle state. DRAM continues to drive CA ODT as programmed.

Normal command timing parameters are applied in this state, except that tREFI doesn't need to be satisfied as Refresh command doesn't need to be issued in this state.

4.12.2 MPSM Power Down State

MPSM Power Down state is entered by Power Down Entry command from MPSM Idle state. When DDR5 SDRAM is in this state, it responds to ODT command normally as it does in precharged power down state. DLL status is same as in normal precharged power down state.

When the Power Down Exit command is issued, the DRAM goes back to the MPSM Idle state after tXP.
Normal Power Down command timings are applied in this state, except the tREFI requirement.

4.12.3 MPSM Deep Power Down State

MPSM Deep Power Down (DPD) state is entered and exited by Self Refresh Entry and Exit commands from/to MPSM Idle state. Input signal requirements to the DRAM in this state are same to those in the Self Refresh mode. DRAM shall not execute any internal Refresh operation in this state.

When the Power Down Exit command is issued, the DRAM goes back to the MPSM Idle state after tXS. tXS_DLL must be met prior to issuing any commands that require a locked DLL.
Normal Self Refresh command timings are applied in this state.

4.12.4 MPSM command timings

The device can exit from the MPSM Idle state by programming the MPSM enable (MR2:OP[1]) bit to '0' using the MRW command. MPSM exit to the first valid command delay is tMPSMX.

Table 62 — Maximum Power Saving Mode Timing Parameters

Symbol	Description	min	max	unit
tMPSMX	MPSM exit to first valid command delay	tMRD	-	ns
			-	

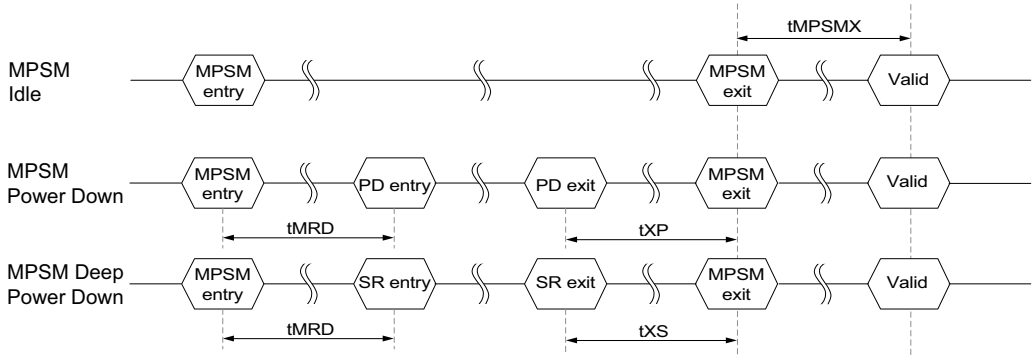


Figure 61 — Maximum Power Saving Mode exit timings

4.13 Refresh Operation

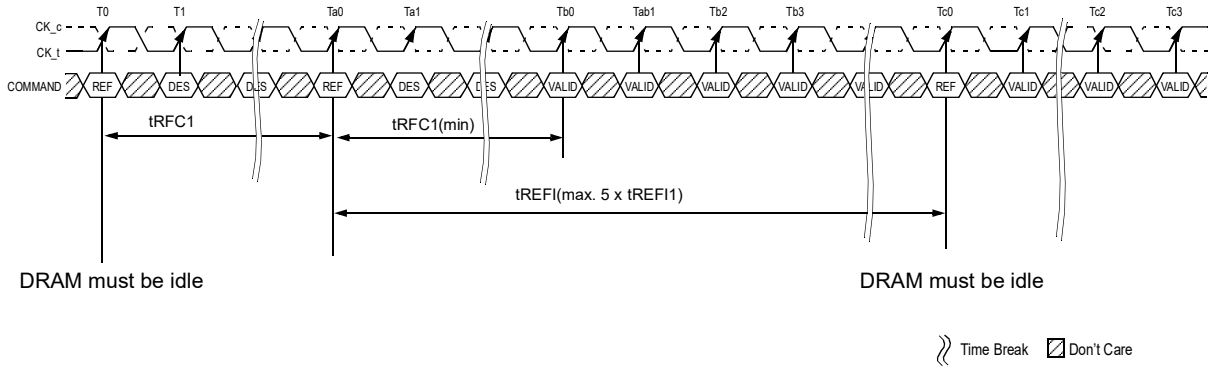
The Refresh command (REF) is used during normal operation of the DDR5 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR5 SDRAM requires Refresh cycles at an average periodic interval of tREFI.

There are three types of refresh operations supported by DDR5 SDRAMs.

- Normal Refresh: By issuing All Bank Refresh (REFab) command in Normal Refresh mode
- Fine Granularity Refresh: By issuing All Bank Refresh (REFab) command in Fine Granularity Refresh mode
- Same Bank Refresh: By issuing Same Bank Refresh (REFsb) command in Fine Granularity Refresh mode

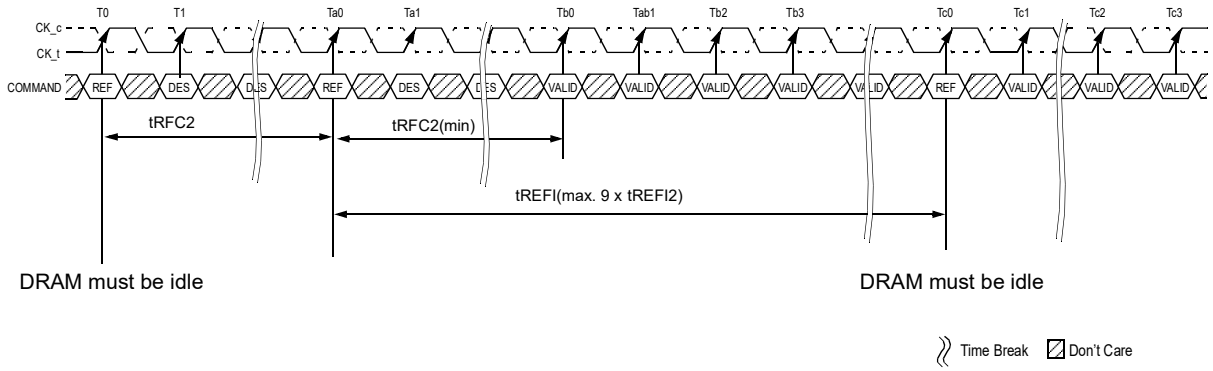
This section describes the details of the refresh operations and requirements for each of the refresh operation types as well as the transitions between the refresh operation types.

For Normal Refresh and Fine Granularity Refresh operations, all banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the All Bank Refresh command (REFab) can be issued. The refresh addressing is generated by the internal refresh controller during the refresh cycle. The external address bus is only required to be in a valid state once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh command and the next valid command, except DES, PDE and non-Target ODT commands, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in Figure 62 and Figure 63. Note that the tRFC timing parameter depends on memory density and the refresh mode setting, which can be set to Normal Refresh mode or Fine Granularity Refresh (FGR) mode.



NOTE: 1. Only DES or non-Target ODT commands are allowed after Refresh command is issued until tRFC1(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 5 x tREFI1.

Figure 62 — Refresh Command Timing (Example of Normal Refresh Mode)



NOTE: 1. Only DES or non-Target ODT commands are allowed after Refresh command is issued until tRFC2(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 x tREFI2.

Figure 63 — Refresh Command Timing (Example of Fine Granularity Refresh Mode)

4.13.1 Refresh Modes

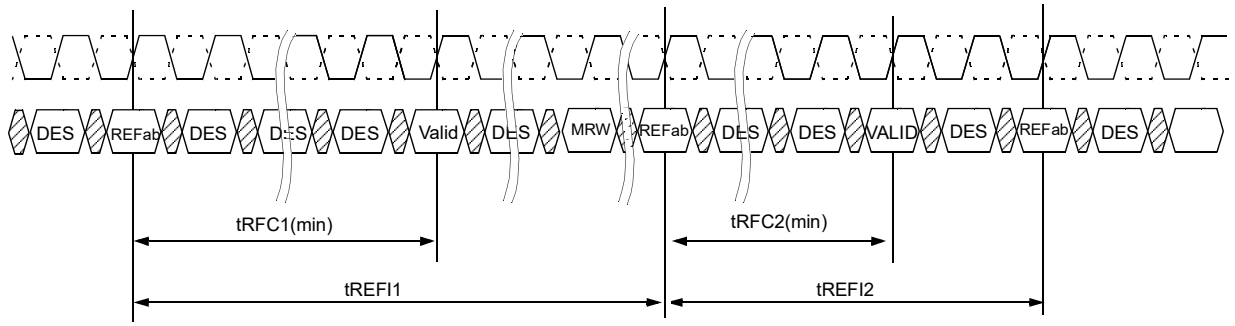
The DDR5 SDRAM has two different Refresh modes with two different refresh cycle time (tRFC) settings. There is a Normal Refresh mode setting and a Fine Granularity Refresh (FGR) mode setting. The FGR mode provides a shorter refresh cycle time (tRFC2) but also requires All Bank Refresh commands (REFab) to be provided twice as often (tREFI is divided by two, i.e. tREFI2 = tREFI1/2). The Refresh mode setting is programed by MRW command as shown in Table 63. The Refresh Modes are fixed until changed by MRW command to MR4 OP[4]. No on-the-fly Refresh mode change is supported.

Table 63 — Mode Register definition for Refresh Mode

MR4 OP[4]	Refresh Mode (tRFC setting)
0	Normal Refresh Mode (tRFC1)
1	Fine Granularity Refresh Mode (tRFC2)

4.13.2 Changing Refresh Mode

If Refresh Mode is changed by MRW, the new tREFI and tRFC parameters would be applied from the moment of the rate change. As shown in Figure 64, when an All Bank Refresh command is issued to the DRAM in Normal Refresh mode, then tRFC1 and tREFI1 are applied from the time that the command (REFab) was issued. And when an All Bank Refresh command is issued in Fine Granularity Refresh (FGR) mode, then tRFC2 and tREFI2 should be satisfied.



NOTE: 1. Refresh mode is Normal Refresh mode before the MRW and FGR mode after the MRW

Figure 64 — Refresh Mode Change Command Timing

The following conditions must be satisfied before the Refresh mode can be changed. Otherwise, data retention of DDR5 SDRAM cannot be guaranteed.

1. In the Normal Refresh mode, the REFab command must complete and tRFC1 must be satisfied before issuing the MRW command to change the Refresh Mode.
2. If performing REFab commands in the Fine Granularity Refresh mode, it is recommended that an even number of REFab commands are issued to the DDR5 SDRAM since the last change of the Refresh mode with an MRW command before the Refresh mode is changed again by another MRW command. If this condition is met, no additional Refresh commands are required upon the Refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the DDR5 SDRAM upon Refresh mode change. This extra Refresh command is not counted toward the computation of the average refresh interval (tREFI). See Figure 65.
3. If performing REFsb commands in the Fine Granularity Refresh mode, it is recommended that all banks have received an even number of REFsb command since the last change of the Refresh mode with an MRW command before the Refresh mode is changed again by another MRW command, since a REFab command will reset the internal bank counter. If this condition is met, no additional refresh commands are required upon the Refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the DDR5 SDRAM upon Refresh mode change. This extra Refresh commands is not counted toward the computation of the average refresh interval (tREFI). See Figure 66 for 16Gb and higher density DRAM with 4 banks in a bank group example.

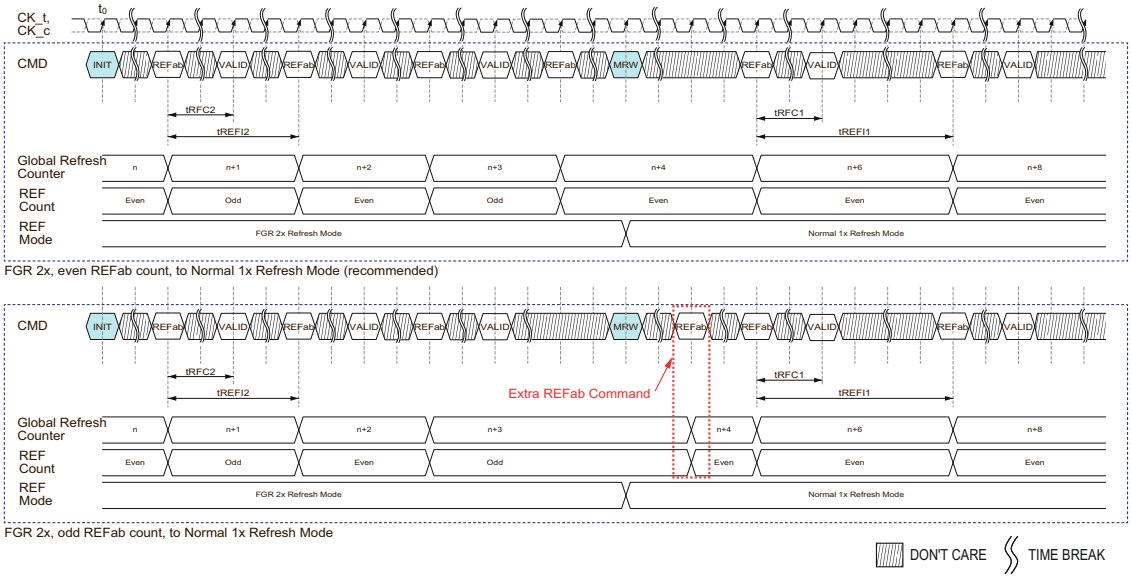
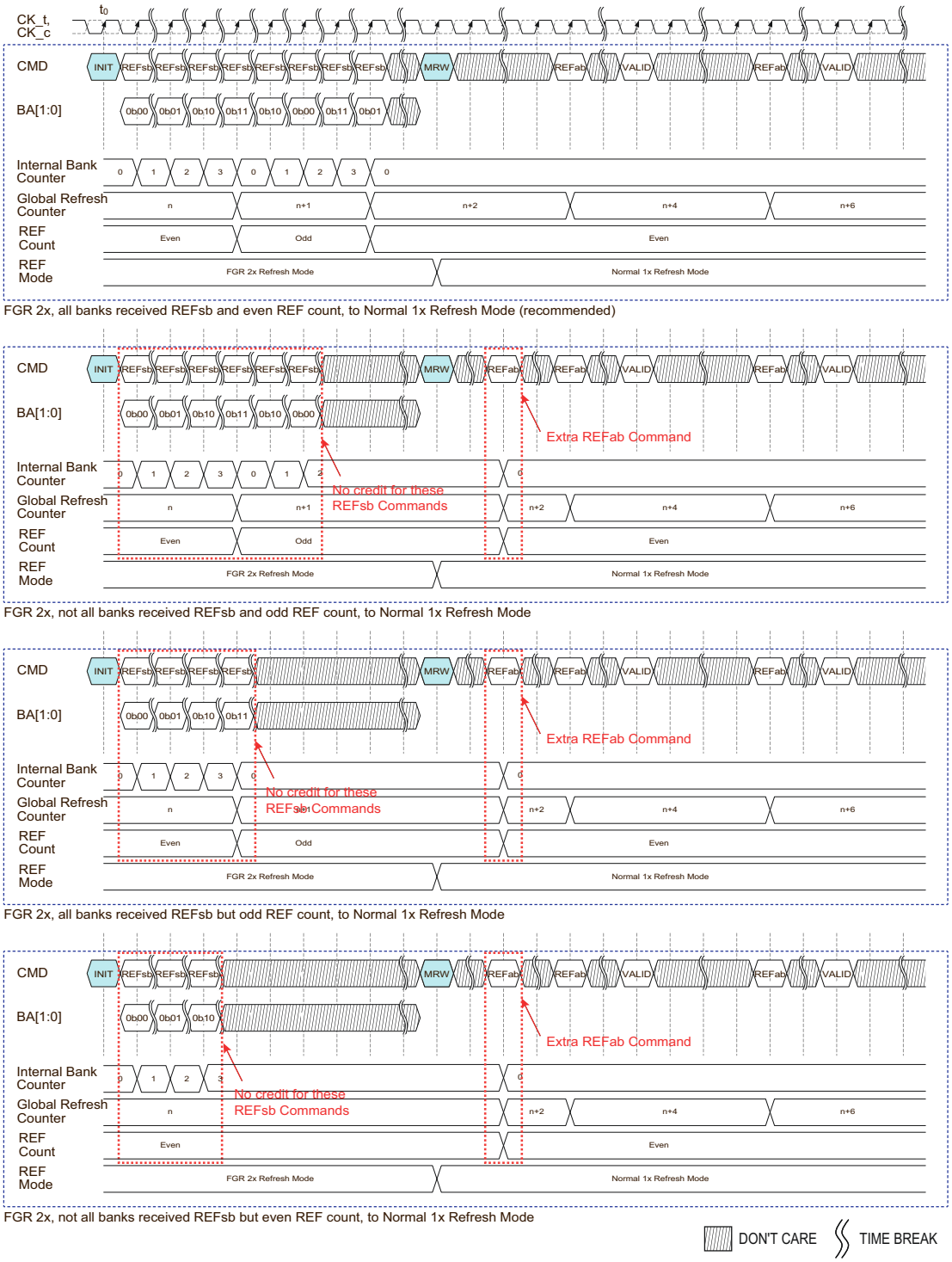


Figure 65 — Refresh Mode Change from FGR 2x to Normal 1x Command Timing



FGR 2x, all banks received REFsb and even REF count, to Normal 1x Refresh Mode (recommended)

FGR 2x, not all banks received REFsb and odd REF count, to Normal 1x Refresh Mode

FGR 2x, all banks received REFsb but odd REF count, to Normal 1x Refresh Mode

FGR 2x, not all banks received REFsb but even REF count, to Normal 1x Refresh Mode

Figure 66 — 16Gb and Higher Density DRAM Refresh Mode Change from FGR 2x REFsb to Normal 1x Command Timing

4.13.3 Same Bank Refresh

Same Bank Refresh command (REFsb) allows the DDR5 DRAM to apply the refresh process to a specific bank in each bank group unlike the All Bank Refresh command (REFab) which applies the refresh process to all banks in every bank group. The determination whether a Same Bank Refresh or an All Bank Refresh is executed by the DRAM depends on whether REFsb or REFab command is issued, as shown in the command truth table. The REFsb command is only allowed in FGR mode (MR4[OP4]=1).

The first Same Bank Refresh command (REFsb) to each bank increments an internal bank counter and once the bank counter equals the number of available banks in a bank group, it will reset and start over on the next subsequent REFsb. Each time the internal bank counter resets and starts over on the next subsequent REFsb, the global refresh counter will also increment. A REFsb command can be issued to any bank and in any bank order. A subsequent REFsb command issued to the same bank prior to every bank receiving a REFsb command will repeat refreshing the same row since the SDRAM's global refresh counter will not increment until all banks in a bank group receive a REFsb command. The first REFsb command issued is the "Synchronization" REFsb command and the "Synchronization" count resets the internal bank counter to zero when either (a) every bank has received one REFsb command, (b) RESET is applied, (c) entering/exiting self refresh mode, or (d) REFab is issued. The DRAM's global refresh counter increments when either a REFab is issued or when all banks have received their one REFsb command and the "Synchronization" count reset to zero. If a REFab command is issued when the bank counter is not zero, i.e. in the middle of same-bank refreshing, the SDRAM's global refresh counter will not increment until the completion of REFab, effectively losing the credits for any REFsb commands issued prior to the REFab. See the 16Gb and Higher Density DRAM Bank and Refresh counter increment behavior table for details.

Table 64 — 16Gb and Higher Density DRAM Bank and Refresh counter increment behavior

Count #	Command	BA0	BA1	Refresh Bank #	Internal Bank Counter #	Global Refresh Counter # (Row Address #)
0	RESET, REFab or SRE/SRX command and FGR mode on (MR4[OP4]=1)				To 0	-
1	REFsb	0	0	0	0 to 1	n
2	REFsb	0	1	1	1 to 2	
3	REFsb	1	0	2	2 to 3	
4	REFsb	1	1	3	3 to 0	
5	REFsb	1	0	2	0 to 1	n+1
6	REFsb	0	0	0	1 to 2	
7	REFsb	1	1	3	2 to 3	
8	REFsb	0	1	1	3 to 0	
9	REFsb	0	0	0	0 to 1	n+2
10	REFsb	0	1	1	1 to 2	
11	***REFab***	***V***	***V***	***0-3***	***To 0***	
12	REFsb	1	1	3	0 to 1	n+3
13	REFsb	0	1	1	1 to 2	
14	REFsb	0	0	0	2 to 3	
15	REFsb	1	0	2	3 to 0	
16	***REFab***	***V***	***V***	***0-3***	***To 0***	n+4
17	***REFab***	***V***	***V***	***0-3***	***To 0***	n+5
18	***REFab***	***V***	***V***	***0-3***	***To 0***	n+6
19	REFsb	1	1	3	0 to 1	n+7
20	***REFab***	***V***	***V***	***0-3***	***To 0***	
21	REFsb	1	0	2	0 to 1	n+8
22	REFsb	0	1	1	1 to 2	
23	REFsb	0	0	0	2 to 3	
24	REFsb	1	1	3	3 to 0	

The REFsb command must not be issued to the device until the following conditions are met:

-tRFC1 or tRFC2 has been satisfied after the prior 1x or 2x REFab command(s), respectively

-tRFCsb has been satisfied after the prior REFsb command

-tRP has been satisfied after the prior PRECHARGE command to that bank

-tRRD_L has been satisfied after the prior ACTIVATE command (e.g. tRRD_L has to be met from ACTIVATE of a different bank in the same bank group to the REFsb targeted at the same bank group)

Additional restrictions for issuing the REFsb command:
-tFAW has not been met (each REFsb counts as an ACTIVATE command for the four activate window timing restriction)

Once a REFsb is issued, the target banks (one in each Bank Group) are inaccessible during the same-bank refresh cycle time (tRFCsb); however, the other banks in each bank group are accessible and can be addressed during this same-bank refresh cycle. When the same-bank refresh cycle has completed, the banks refreshed via the REFsb will be in idle state.

After issuing REFsb command, the following conditions must be met:
-tRFCsb must be satisfied before issuing a REFab command
-tRFCsb must be satisfied before issuing an ACTIVATE command to the same bank
-tREFSBRD must be satisfied before issuing an ACTIVATE command to a different bank.

Table 65 — Refresh command scheduling separation requirements

Symbol	Min Delay From	To	NOTE
tRFC1	REFab	REFab	1
		ACTIVATE command to any bank	
tRFC2	REFab	REFab	2
		ACTIVATE command to any bank	
		REFsb	
tRFCsb	REFsb	REFab	2
		ACTIVATE command to same bank as REFsb	
		REFsb	
tREFSBRD	REFsb	ACTIVATE command to different bank from REFsb	2
tRRD_L	ACTIVATE	REFsb to different bank from ACTIVATE	2

NOTES:
1 - MR4(OP[4]) set to Normal Refresh mode.
2 - MR4(OP[4]) set to FGR mode. REFsb command is valid only in FGR mode.

Where *n* is the number of banks in a bank group, a single REFab command can be replaced with *n* REFsb commands for the purpose of scheduling postponed refresh commands.

4.13.4 tREFI and tRFC parameters

The maximum average refresh interval (tREFI) requirement for the DDR5 SDRAM depends on the refresh mode setting (Normal or FGR), and the device's case temperature (Tcase). When the refresh mode is set to Normal Refresh mode, REFab commands are issued (tRFC1), and Tcase<=85°C, the maximum average refresh interval (tREFI1) is tREFI. When the refresh mode is set to FGR mode, REFab commands are issued (tRFC2) and Tcase<=85°C, the maximum average refresh interval (tREFI2) is tREFI/2. This same tREFI/2 interval value is also appropriate if the refresh mode is set to Normal Refresh mode and REFab commands are issued (tRFC1) but 85°C<Tcase<=95°C. Finally, if the refresh mode is set to FGR mode, REFab commands are issued (tRFC2), and 85°C<Tcase<=95°C, the maximum average refresh interval (tREFI2) is tREFI/4.

The DDR5 SDRAM includes an optional method for the host to indicate when Refresh commands are being issued at the 2x (tREFI2) refresh interval rate. The 2x Refresh Interval Rate indicator (MR4:OP[3]) alerts the DRAM if the host supports the refresh interval rate indication as part of the REF command using CA8. If enabled (MR4:OP[3]=1), the host will issue 1x REF commands with CA8=H (Tcase<=85°C), and the host will issue 2x REF commands with CA8=L (Tcase any allowable temperature). MR4:OP[3] is a Status Read/Write "SR/W" MR bit which shows DDR5 SDRAM support of this optional feature. Reading MR4:OP[3] will return a "1" if the 2x Refresh Interval Rate indicator is supported. A "0" will be returned if not supported.
tREFI is based on the 8,192 refresh commands that need to be issued within the baseline tREF=32ms refresh period on the DDR5 SDRAM.

4.13.5 tREFI and tRFC parameters for 3DS devices

Typical platforms are designed with the assumption that no more than one physical rank is refreshed at the same time. In order to limit the maximum refresh current (I_{DD5B1}) for a 3D stacked SDRAM, it will be required to stagger the refresh commands to each logical rank in a stack.

The tRFC time for a single logical rank is defined as tRFC_slr and is specified as the same value as for a monolithic DDR5 SDRAM of equivalent density. The minimum amount of stagger between refresh commands sent to different logical ranks (tRFC_dlr) or physical ranks (tRFC_dpr) is specified to be approximately tRFC_slr/3 - Table 68.

Table 66 — tREFI parameters for REFab and REFsb Commands (including 3DS)

Command	Refresh Mode	Symbol & Range		Expression	Value	Unit	Notes
REFab	Normal	tREFI1	0°C <= TCASE <= 85°C	tREFI	3.9	us	1,2
			85°C < TCASE <= 95°C	tREFI/2	1.95	us	1,2
REFab	Fine Granularity	tREFI2	0°C <= TCASE <= 85°C	tREFI/2	1.95	us	1,2
			85°C < TCASE <= 95°C	tREFI/4	0.975	us	1,2
REFsb	Fine Granularity	tREFIsb	0°C <= TCASE <= 85°C	tREFI/(2*n)	1.95/n	us	1,2,3
			85°C < TCASE <= 95°C	tREFI/(4*n)	0.975/n	us	1,2,3

Note(s):

1 - All 3D Stacked (3DS) devices follow the same requirements as the monolith die regardless of logical rank.

2 - 3DS specification covers up to 16Gb density. Future densities such as 24Gb or 32Gb could require different tREFI requirements.

3 - *n* is the number of banks in a bank group (e.g. 8G: n=2; 16G: n=4).

Table 67 — tRFC parameters by device density

Refresh Operation	Symbol	16Gb	Units	Notes
Normal Refresh (REFab)	tRFC1(min)	295	ns	
Fine Granularity Refresh (REFab)	tRFC2(min)	160	ns	
Same Bank Refresh (REFsb)	tRFCsb(min)	130	ns	

Table 68 — 3DS tRFC parameters by logical rank density

Refresh Operation	Symbol	8Gb	16Gb	24Gb	32Gb	Units	Notes
Normal Refresh with 3DS same logical rank	tRFC1_slr(min)	tRFC1(min)				ns	1
Fine Granularity Refresh with 3DS same logical rank	tRFC2_slr(min)	tRFC2(min)				ns	1
Same Bank Refresh with 3DS same logical rank	tRFCsb_slr(min)	tRFCsb(min)				ns	1
Normal Refresh with 3DS different logical rank	tRFC1_dlr(min)	tRFC1(min)/3				ns	3
Normal Refresh with 3DS different physical rank	tRFC1_dpr(min)	tRFC1min/3				ns	2, 3
Fine Granularity Refresh with 3DS different logical rank	tRFC2_dlr(min)	tRFC2(min)/3				ns	3
Fine Granularity Refresh with 3DS different physical rank	tRFC2_dpr(min)	tRFC2min/3				ns	2, 3
Same Bank Refresh with 3DS different logical rank	tRFCsb_dlr(min)	tRFCsb(min)/3				ns	3

Note(s):

1. All 3D Stacked (3DS) devices follow the same requirements as the monolith die for same logical ranks
2. Parameter applies to dual-physical-rank (36 and 40 placement) 3DS-based DIMMs built with JESD301-1 “PMIC 50x0 Specification”, but may not apply to DIMMs built with higher current capacity PMICs.
3. 3DS tRFC parameters are to be rounded up to the nearest 1ns after the “tRFC*min”/3 calculation.

Table 69 — Same Bank Refresh parameters

Refresh Mode	Symbol	16Gb	Units
Same Bank Refresh to ACT delay	tREFSBRD(min)	30	ns

Table 70 — Same Bank Refresh parameters for 3DS 2H, 4H

Refresh Mode	Symbol	16Gb	Units
Same Bank Refresh to ACT delay SLR	tREFSBRD_slr(min)	30	ns
Same Bank Refresh to ACT delay DLR	tREFSBRD_dlr(min)	15	ns

4.13.6 Refresh Operation Scheduling Flexibility

In general, a Refresh command needs to be issued to the DDR5 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

In Normal Refresh mode, a maximum of 4 REFab commands can be postponed, meaning that at no point in time more than a total of 4 Refresh commands are allowed to be postponed. In case that 4 REFab commands are postponed in a row, the resulting maximum interval between the surrounding REFab commands is limited to 5 × tREFI1 (see Figure 67). At any given time, a maximum of 5 REFab commands can be issued within 1 x tREFI1 window. Self-refresh mode may be entered with a maximum of 4 REFab commands being postponed. After exiting Self-Refresh mode with one or more REFab commands postponed, additional REFab commands may be postponed to the extent that the total number of postponed REFab commands (before and after the Self-Refresh) will never exceed 4. During Self-Refresh Mode, the number of postponed REFab commands does not change.

In FGR Mode, the maximum REFab commands that may be postponed is 8, with the resulting maximum interval between the surrounding REFab commands limited to 9 x tREFI2 (see Figure 68). At any given time, a maximum of 9 REFab commands can be issued within 1 x tREFI2 window. The same maximum count of 8 applies to postponed REFab commands around self-refresh entry and exit.

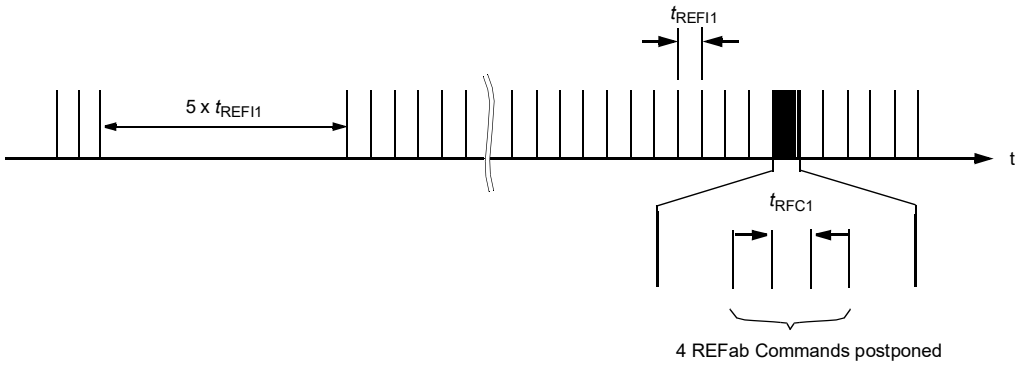


Figure 67 — Postponing Refresh Commands (Example of Normal Refresh Mode - tREFI1, tRFC1)

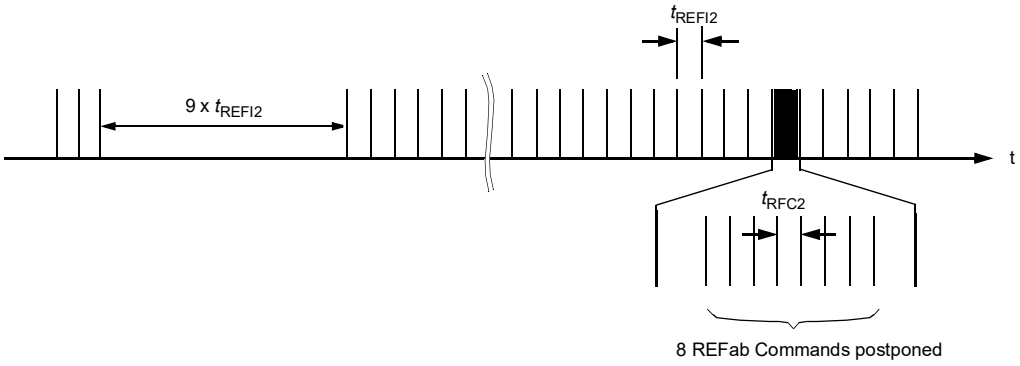


Figure 68 — Postponing Refresh Commands (Example of Fine Granularity Refresh Mode - tREFI2, tRFC2)

4.13.7 Self Refresh entry and exit

DDR5 SDRAM can enter Self Refresh mode anytime in Normal Refresh and FGR mode without any restriction on the number of Refresh commands that have been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows:

1. There are no special restrictions for the Normal Refresh mode.
2. If performing REFab commands in FGR mode, it is recommended that there should be an even number of REFab commands before entry into Self Refresh since the last Self Refresh exit or MRW command that set the FGR mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. If this condition is not met, one extra REFab command is required to be issued to the DDR5 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI2). See Figure 69.
3. If performing REFsb commands, it is recommended that all banks have received a REFsb command prior to entering Self Refresh, since entering and exiting Self Refresh will reset the internal bank counter. If this condition is met, no additional refresh commands are required upon Self Refresh exit, and REFsb commands again can be issued to any bank in any bank order. If this condition is not met, one extra REFab command or an extra REFsb command to each bank is required to be issued to the DDR5 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (16Gb and higher density DRAM with 4 banks per bank group example: tREFI2 - see Figure 70).

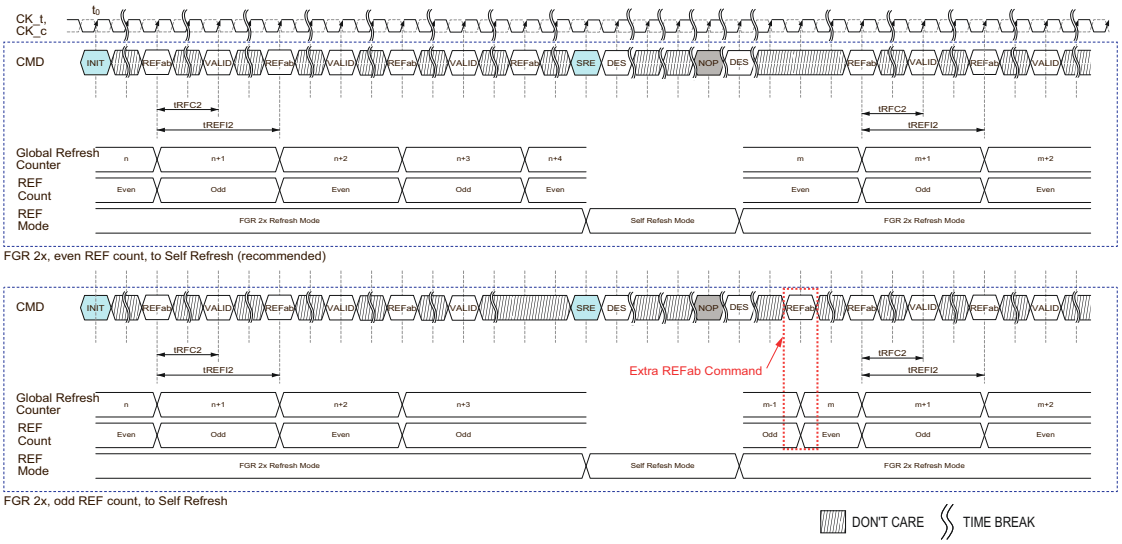
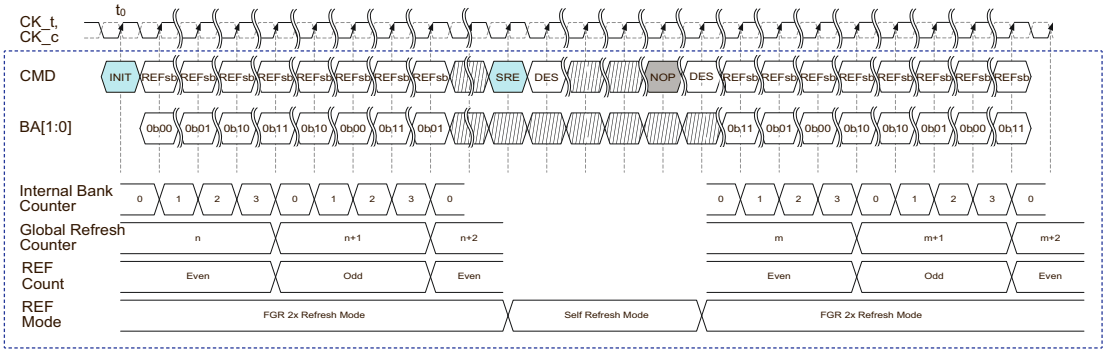
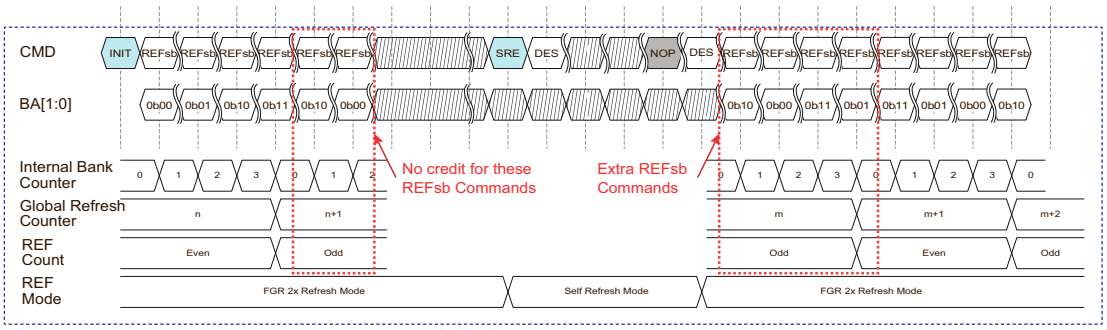


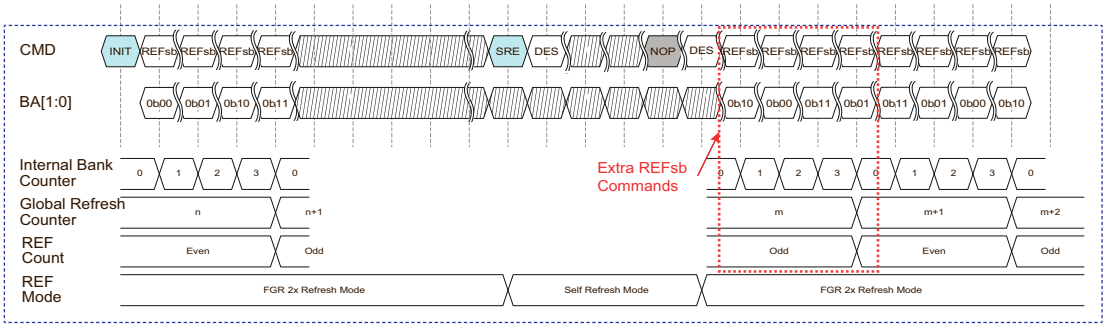
Figure 69 — FGR 2x to SREF Command Timing



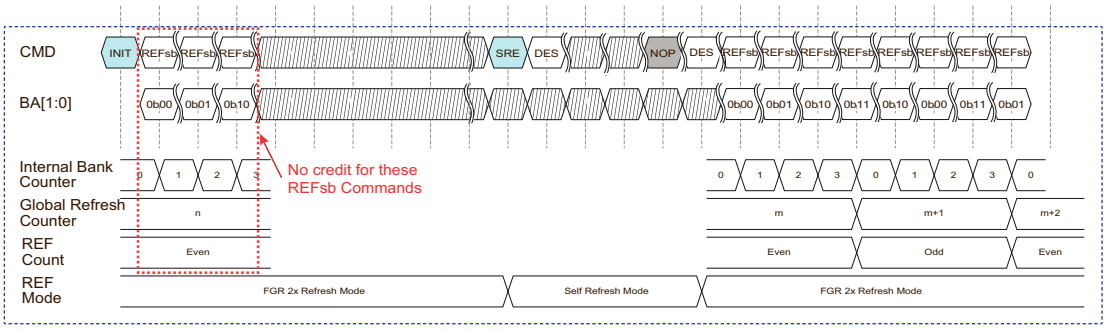
FGR 2x all banks received REFsb and even REF count, to Self Refresh (recommended)



FGR 2x not all banks received REFsb and odd REF count, to Self Refresh



FGR 2x all banks received REFsb but odd REF count, to Self Refresh



FGR 2x not all banks received REFsb but even REF count, to Self Refresh

Figure 70 — 16Gb and Higher Density DRAM FGR 2x REFsb to SREF Command Timing

4.14 Temperature Sensor

DDR5 devices feature a temperature sensor whose status can be read. This sensor can be used to determine an appropriate refresh rate (MR4). Either the temperature sensor readout or the device TOPER may be used by the system to determine whether the refresh rate and operating temperature requirements are being met.

DDR5 devices shall monitor device temperature and update MR4 according to tTSI. Upon completion of device initialization, the device temperature status bits shall be no older than tTSI. MR4 will be updated even when device is in Self Refresh state.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4:OP[2:0]=010B. DDR5 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly.

The four thresholds of the temperature sensor will be nominally 80°C, 85°C, 90°C and 95°C. The 2nd threshold (nominally 85°C) is used by the system to switch to 2x refresh. The 4th threshold (nominally 95°C) is used by the system to throttle activity to keep the DRAM at a safe operating temperature. The 1st threshold (nominally 80°C) allows the system to take actions which delay reaching the 2nd threshold. The 3rd threshold (nominally 90°C) allows the system to take actions which delay reaching the 4th threshold.

To ensure proper operation using the temperature sensor, applications should consider the following factors:
• TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C, measured in the range of interest 80-100°C.
• ReadInterval is the time period between MR4 reads from the system.
• TempSensorInterval (tTSI) is the maximum delay between internal updates of MR4.
• SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq TempMargin$$

Table 71 — Temperature Sensor Parameters

Parameter	Symbol	Min/Max	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	1
Temp Sensor Accuracy, 2nd threshold trip point	TempSensorAcc2	Min	78	°C	1,2
Temp Sensor Accuracy, 4th threshold trip point	TempSensorAcc4	Min	88	°C	1,2
Relative Trip Point, 2nd threshold minus 1st threshold	RelativeTrip2m1	Min/Max	Min 3 / Max 7	°C	1,3
Relative Trip Point, 3rd threshold minus 2nd threshold	RelativeTrip3m2	Min/Max	Min 3 / Max 7	°C	1,4
Relative Trip Point, 4th threshold minus 3rd threshold	RelativeTrip4m3	Min/Max	Min 3 / Max 7	°C	1,4

Note(s):

1. Verified by design and characterization, and may not be subject to production test.
2. Only the minimum (negative side) is specified for the second and fourth thresholds. The DRAM vendor is responsible for guaranteeing correct operation of 1x refresh for MR4 <= 010b, and correct operation of 2x refresh for MR4 <= 100b. This puts a vendor-specific constraint on the Temperature Sensor Accuracy on the positive side.
3. The 1st threshold is defined relative to the 2nd threshold.
4. The 3rd threshold is defined relative to the 2nd and 4th thresholds.

For example, if TempGradient is 10°C/s and the SysRespDelay is 100 ms:

(10°C/s) x (ReadInterval + 32ms + 100ms) ≤ 2°C
In this case, ReadInterval shall be no greater than 68 ms.

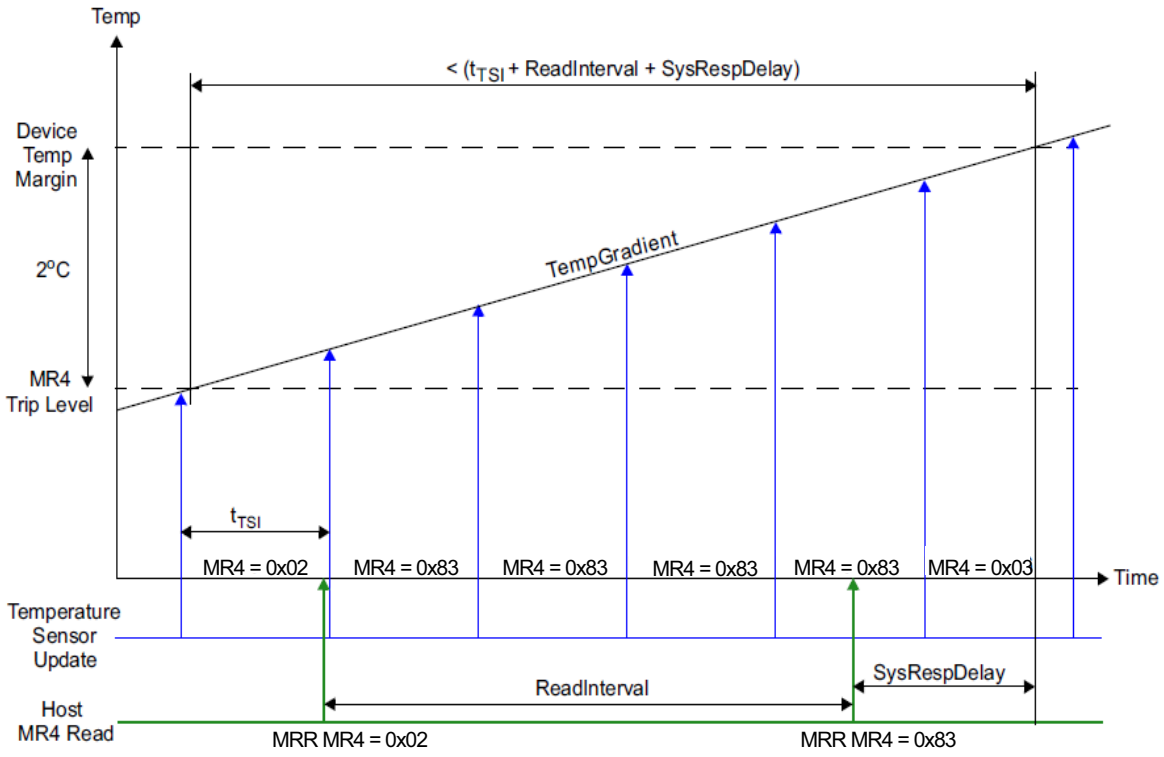


Figure 71 — Temp Sensor Timing Diagram

Note: MR4 encodings in the above figure are examples only and assume that MR4:OP[4]=0

4.14.1 Temperature Sensor usage for 3D Stacked (3DS) Devices

In the case of 3D Stacked devices, the Refresh Rate (MR4) is related to the hottest die in the stack only.

4.14.2 Temperature Encoding

The DDR5 DRAM provides temperature related information to the controller via an encoding on MR4:OP[2:0]. The encodings define the proper refresh rate expected by the DRAM to maintain data integrity.

4.14.3 MR4 Definition for Reference only - See Mode Register Section for details

Table 72 — MR4 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	RFU		Refresh tRFC Mode	Refresh Interval Rate Indicator	Refresh Rate		

Table 73 — MR4 Register Encoding

Function	Register Type	Operand	Data	Notes
Refresh Rate	R	OP[2:0]	000_B: RFU 001_B: tREFI x1 (1x Refresh Rate), <80°C nominal 010_B: tREFI x1 (1x Refresh Rate), 80-85°C nominal 011_B: tREFI /2 (2x Refresh Rate), 85-90°C nominal 100_B: tREFI /2 (2x Refresh Rate), 90-95°C nominal 101_B: tREFI /2 (2x Refresh Rate), >95°C nominal 110_B: RFU 111_B: RFU	1,2,3,4,5, 6,7
Refresh Interval Rate Indicator	SR/W	OP[3]	DRAM Status Read (SR): 0_B: Not implemented (Default) 1_B: Implemented Host Write (W): 0_B: Disabled (Default) 1_B: Enabled	
Refresh tRFC Mode	R/W	OP[4]	0_B: Normal Refresh Mode (tRFC1) 1_B: Fine Granularity Refresh Mode (tRFC2)	
RFU	R/W	OP[6:5]	RFU	
TUF (Temperature Update Flag)	R	OP[7]	0_B: No change in OP[2:0] since last MR4 read (default) 1_B: Change in OP[2:0] since last MR4 read	

Note(s):

1. The refresh rate for each OP[2:0] setting applies to tREFI1 and tREFI2. Each OP[2:0] setting specifies a nominal temperature range. The five ranges defined by OP[2:0] are determined by four temperature thresholds.
2. The four temperature thresholds are nominally at 80°C, 85°C, 90°C and 95°C. The 85°C and 95°C thresholds have a specified minimum temperature value, but the maximum temperature value is not specified.
3. DRAM vendors must report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The 2x Refresh Rate must be provided by the system before the DRAM Tj has gone up by more than 2°C (Temperature Margin) since the first report out of OP[2:0]=011B. This condition is reset when OP[2:0] is equal to 010B.
5. The device may not operate properly when OP[2:0]=101B, if the DRAM Tj has gone up by more than 2°C (Temperature Margin) since the first report out of OP[2:0]=101B. This condition is reset when OP[2:0] is equal to 100B. OP[2:0]=101B must be a temporary condition of the DRAM, to be addressed by immediately reducing the Tj of the DRAM by throttling its power, and/or the power of nearby devices.
6. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence (Te).
7. See the section on “Temperature Sensor” for information on the recommended frequency of reading MR4

4.15 Multi-Purpose Command (MPC)

4.15.1 Introduction

DDR5-SDRAMs use the Multi-Purpose Command (MPC) to issue commands associated with interface initialization, training, and periodic calibration. The MPC command is initiated with CS_n, and CA[4:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has eight operands (OP[7:0]) that are decoded to execute specific commands in the SDRAM.

The MPC command uses an encoding that includes the command encoding and the opcode payload in a single clock cycle. This enables the host to extend the setup and hold for the CA signals beyond the single cycle when the chip select asserts. In addition, the MPC command will support multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the DRAM will capture the MPC command during at least one rising CK_t/CK_c edge.

Table 74 — MPC Command Definition

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
MPC	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	

Note - See Command Truth Table for details

4.15.2 MPC Opcodes

The following table specifies the opcode assignments for the MPC operations:

Table 75 — MPC Command Definition for OP[7:0]

Function	Operand	Data	Notes
Initialization and Training Modes	OP[7:0]	$0000\ 0000_B$: Exit CS Training Mode $0000\ 0001_B$: Enter CS Training Mode $0000\ 0010_B$: DLL RESET $0000\ 0011_B$: Enter CA Training Mode $0000\ 0100_B$: ZQCal Latch $0000\ 0101_B$: ZQCal Start $0000\ 0110_B$: Stop DQS Interval Oscillator $0000\ 0111_B$: Start DQS Interval Oscillator $0000\ 1000_B$: Set 2N Command Timing $0000\ 1001_B$: Set 1N Command Timing $0000\ 1010_B$: Exit PDA Enumerate Programming Mode $0000\ 1011_B$: Enter PDA Enumerate Programming Mode 0000 1100B: Manual ECS Operation 0000 1101B: RFU ...thru 0001 1110B: RFU 0001 1111B: Apply VrefCA, VrefCS and RTT_CA/CS/CK 0010 0xxxB: Group A RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0010 1xxxB: Group B RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0011 0xxxB: Group A RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0011 1xxxB: Group B RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0100 0xxxB: Group A RTT_CA = xxx (See MR33:OP[2:0] for encoding) 0100 1xxxB: Group B RTT_CA = xxx (See MR33:OP[2:0] for encoding) 0101 0xxxB: Set DQS _RTT_PARK = xxx (See MR33:OP[5:3] for encoding) 0101 1xxxB: Set RTT_PARK = xxx (See MR34:OP[2:0] for encoding) 0110 xxxxB: PDA Enumerate ID = xxxx (See encoding table below) 0111 xxxxB: PDA Select ID = xxxx (See encoding table below) 1000 xxxxB: Configure tDLLK/tCCD_L = xxxx (See MR13:OP[3:0] for encoding) All Others: Reserved	1,2,3, 4,5,6,7,8, 9,10, 11

Notes:

1. See command truth table for more information.
2. Refer to the CS Training Mode section for more information regarding CS Training Mode Entry and Exit.
3. Refer to the CA Training Mode section for more information regarding CA Training Mode Entry.
4. Refer to the ZQ Calibration section for more information regarding ZQCal Start and ZQCal Latch.
5. Refer to the DQS Interval Oscillator section for more information regarding Start DQS Interval Oscillator and Stop DQS Interval Oscillator
6. Refer to the Per DRAM Addressability section for more information regarding Enter PDA Mode and Exit PDA Mode.
7. Refer to the CA_ODT Strap Operation section for more information regarding Group A and Group B configurations for RTT_CA, RTT_CS, and RTT_CK.
8. “Apply VrefCA, VrefCS and RTT_CA/CS/CK” applies the settings previously sent with the VrefCA or VrefCS command and “MPC Set RTT_CA/CS/CK”. Until this “MPC Apply VrefCA, VrefCS and RTT_CA/CS/CK” command is sent, the values are in a shadow register. Any MRR to the VrefCA, VrefCS and RTT_CA/CS/CK settings should return only the applied value. The shadow register shall retain the previously set value, so that any time the “MPC Apply VrefCA, VrefCS and RTT_CA/CS/CK” command is sent, there is no change in the applied value unless a new VrefCA , VrefCS or RTT_CA/CS/CK value was sent to the shadow register since the previous “MPC Apply VrefCA, VrefCS and RTT_CA/CS/CK” command.
9. The PDA Enumerate ID and PDA Select ID opcodes include a 4-bit value, designated by xxxxB in the table. This is the value that is programmed into the MR for these fields. The PDA Enumerate ID can only be changed while in PDA Enumerate Programming Mode.
10. For any MPC command that is associated with a Mode Register, the only way to program that Mode Register is via the MPC command. Those Mode Registers will be read only and will not support MRW.
11. MPC command “tDLLK/tCCD_L” sets the settings to the MR13 shadow registers and applies the settings to MR13 when the DRAM encounters MPC command “DLL RESET” or SRE with CA9=”L”.

Table 76 — PDA Enumerate and Select ID encoding

MPC Function	OP[7:4]	OP[3:0]	Notes
PDA Enumerate ID	0110	0000_B: ID 0 0001_B: ID 1 0010_B: ID 2 0011_B: ID 3 0100_B: ID 4 0101_B: ID 5 0110_B: ID 6 0111_B: ID 7 1000_B: ID 8 1001_B: ID 9 1010_B: ID 10 1011_B: ID 11 1100_B: ID 12 1101_B: ID 13 1110_B: ID 14 1111_B: ID 15 - default	
PDA Select ID	0111	0000_B: ID 0 0001_B: ID 1 0010_B: ID 2 0011_B: ID 3 0100_B: ID 4 0101_B: ID 5 0110_B: ID 6 0111_B: ID 7 1000_B: ID 8 1001_B: ID 9 1010_B: ID 10 1011_B: ID 11 1100_B: ID 12 1101_B: ID 13 1110_B: ID 14 1111_B: ID 15 - This selects all devices regardless of their enumerate ID.	

4.15.3 MPC Command Timings

As shown in the following figure, the MPC CMD timings can be extended to any number of cycles. The CS_n can also be asserted many consecutive cycles, limited by tMCP_CS. All timings will be relative to the final rising CK_t/CK_c within the CS_n assertion window. The min delay from when the MPC command is captured to the next valid command is specified as tMPC_Delay. Prior to CS Training, the CA will be driven with additional setup and hold beyond the CS_n assertion. For the DRAM to latch the MPC command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state and provide at least three cycles prior to CS_n transitioning from high to low, CS_n must remain low for tMPC_CS, and CA must remain in the proper command state for and provide at least three cycles after CS_n transitions from low to high. This additional setup and hold is only needed when MR2:OP[2] is set to 0 (Multi-cycle MPC mode).

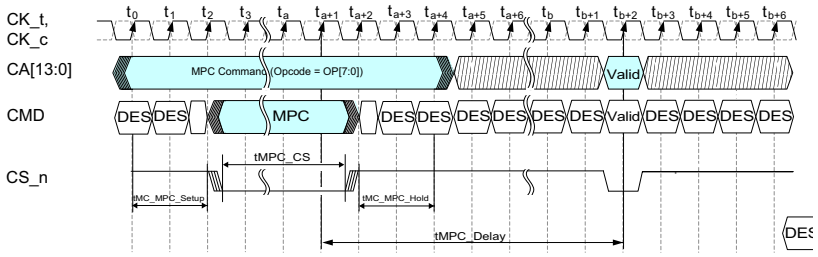


Figure 72 — MPC Command Timing to 1-Cycle Command

The DDR5 DRAM will support a MR setting to indicate when a multi-cycle CS_n assertion may be used for the MPC, VrefCA and VrefCS commands.

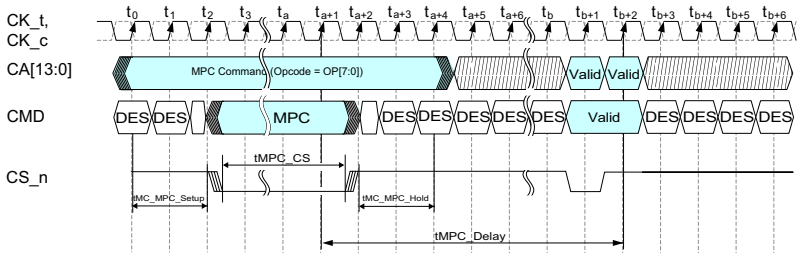


Figure 73 — MPC Command Timing to 2-Cycle Command

Table 77 — MPC, VrefCA and VrefCS CS Assertion Duration

MR Address	Operating Mode	Description
MR2:OP[4]	CS Assertion Duration	0_B: **Only** Multiple cycles of CS assertion supported for MPC, VrefCA and VrefCS commands 1_B: Only a single cycle of CS assertion supported for MPC, VrefCA and VrefCS commands

Default value for the CS Assertion Duration is 0, which allows for multi-cycle CS assertions during training. The DRAM shall support going in and out of this mode many times during the DRAM initialization and training sequence.

Table 78 — AC parameters for MPC Command

Symbol	Description	Min	Max	Unit	Note
tMPC_Delay	MPC to any other valid command delay	tMRD	-	nCK	
tMC_MPC_Setup	Min time between stable MPC command and first falling CS edge (SETUP)	3	-	nCK	2
tMC_MPC_Hold	Min time between first rising CS edge and stable MPC command (HOLD)	3	-	nCK	2
tMPC_CS	Time CS_n is held low to register MPC command	3.5	8	nCK	1

1 - The minimum tMPC_CS constraint only applies when the CS Assertion Duration setting is 0. The CS Assertion Duration MR setting must be set to enable single cycle MPC commands. The earliest time to set the CS Assertion Duration MR is after CA training is complete, when MRW commands can be sent to the DRAM.
2 - This applies only to Multi-Cycle MPC commands when MR2:OP[4]=0_B

Table 79 — MPC Truth Table

Current State	MPC Command	Next State
All Banks Idle	CSTM (Enter/Exit)	All Banks Idle
	DLL RESET	
	CATM (Enter)	
	ZQCAL (Latch/Start)	
	DQS Interval Oscillator (Start/Stop)	
	Set 1N/2N Command	
	PDA Enumerate Programming (Enter/Exit)	
	Manual ECS Operation	
	Apply VrefCA, VrefCS and RTT_CA/CS/CK	
	Configure Group A/B RTT_CA/CS/CK	
	Set DQS_RTT_PARK	
	Set RTT_PARK	
	PDA Enumerate/Select ID	
	Configure tDLLK/tCCD_L	
Active	ZQCAL (Latch/Start)	Active
	DQS Interval Oscillator (Start/Stop)	
	Set 1N/2N Command	
	Configure Group A/B RTT_CA/CS/CK	
	Configure tDLLK/tCCD_L	

4.16 Per DRAM Addressability (PDA)

DDR5 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank. The Per DRAM Addressability (PDA) applies to MRW, MPC, and VrefCA commands. Some per DRAM settings will be required prior to any training of the CA and CS timings and the DQ write timings. The MPC and VrefCA command timings with extended setup/hold and multi-cycle CS assertion may be used for PDA commands if the CA and CS timings have not yet been trained.

DDR5 introduces a CA interface-only method for Per DRAM Addressability, by having a unique PDA Enumerate ID in each DRAM, and the ability to Group A PDA Select ID in all DRAMs. The unique PDA Enumerate ID requires the use of the DQ signals and a PDA Enumerate Programming Mode in the DRAM to program. Once the PDA Enumerate ID has been programmed, subsequent commands must not use the DQ signals (Legacy PDA mode) to designate which DRAM is selected for the command. The PDA Enumerate ID is a 4-bit field, and the PDA Select ID is also a 4-bit field. When the PDA Select ID is the same as the PDA Enumerate ID or when the PDA Select ID is set to the “All DRAM” code of 1111_B, the DRAM will apply the MPC, MRW, or VrefCA command. There are a few MPC commands that do not use the PDA Select ID to determine if the command will be applied. Among these MPC commands that do not use the PDA Select ID are the MPC opcodes to set the PDA Enumerate ID and the opcode to set the PDA Select ID. During RESET procedure, the receive FIFO must be initialized with all ones in order to ensure that the PDA enumerate flow does not program an enumerate ID when the strobes are not toggling. The table summarizing which MPC commands are dependent on the PDA Select ID values is included below:

Table 80 — Commands that support or don’t support PDA Select ID Usage

Command	Opcode	Uses PDA Select ID to determine when to execute command	NOTE
MRW	All	Yes	
VrefCA	All	Yes	
VrefCS	All	Yes	
MPC	(Group A and B) RTT_CA	Yes	
MPC	(Group A and B) RTT_CS	Yes	
MPC	(Group A and B) RTT_CK	Yes	
MPC	Set RTT_PARK	Yes	
MPC	Set DQS_RTT_PARK	Yes	
MPC	Apply VrefCA and RTT_CA/CS/CK	No	
MPC	Enter PDA Enumerate Programming Mode	No	
MPC	Exit PDA Enumerate Programming Mode	No	
MPC	PDA Enumerate ID	No	1
MPC	PDA Select ID	No	
MPC	All other MPC opcodes	No	

Note 1: The PDA Enumerate ID is the only command that utilizes the PDA Enumerate ID Programming mode.

The following mode register fields are associated with Per DRAM Addressable operation:

Table 81 — PDA Mode Register Fields

MR Address	Operating Mode	Description
MR1:OP[3:0]	PDA Enumerate ID[3:0]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Enumerate ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Enumerate ID opcode. This can only be set when PDA Enumerate Programming Mode is enabled and the associated DRAM's DQ0 is asserted LOW. The PDA Enumerate ID opcode includes 4 bits for this encoding. Default setting is 1111_B
MR1:OP[7:4]	PDA Select ID[3:0]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Select ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Select ID opcode. The PDA Select ID opcode includes 4 bits for this encoding. 1111_B = all DRAMs execute MRW, MPC, and VrefCA commands For all other encodings, DRAMs execute MRW, MPC, and VrefCA comands only if PDA Select ID[3:0] = PDA Enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA Select ID. Default setting is 1111_B

4.16.1 PDA Enumerate ID Programming

1. PDA Enumerate Programming Mode is enabled by sending one or more MPC command cycles with OP[7:0]=0000 1011B. Data Mask and PDA Enumerate are not supported for use at the same time. Either data mask shall be disabled or DM_n driven high, while PDA Enumerate Programming Mode is enabled.
2. In the PDA Enumerate Programming Mode, only the MPC command with PDA Enumerate ID opcode is qualified with DQ0 for x4/x8 and DQL0 for x16. The DRAM captures DQ0 for x4/x8 and DQL0 for x16 by using DQS_c and DQS_t for x4/x8 DQSL_c and DQSL_t for x16 signals as shown in Figure 74, where DQ is driven low after the SET PDA Enumerate ID command, and DQS starts toggling after tPDA_DQS_DELAYmin, and stops toggling prior to tPDA_DQS_DELAYmax, and DQ is held until after DQS stops toggling. An alternate method is shown in Figure 75 where DQ is driven low and DQS toggles continuously starting prior to the SET PDA Enumerate ID command, and remains toggling until tPDA_DQS_Delay(max) is satisfied, and the Exit PDA Enumerate Programming Mode command has finished. If the value on DQ0 for x4/x8 or DQL0 for x16 is 0 then the DRAM executes the MPC command to set the PDA Enumerate ID. The controller may choose to drive all the DQ bits. Only the MPC command with PDA Enumerate ID opcodes will be supported in PDA Enumerate Programming Mode, and the MPC command to exit PDA Enumerate Programming Mode does not require a DQ qualification.
3. For the "don't enumerate" case where the SDRAM ignores the PDA Enumerate ID MPC command in the PDA Enumerate Programming Mode, the DQS_t/DQS_c and DQ signals (DQSL_t/DQSL_c and DQL/DQU for x16) may be high (driven or due to RTT_PARK termination) prior to sending the MPC command to enter PDA Enumerate Programming Mode. After entering PDA Enumerate Programming Mode, the DQS and DQ signals must remain high (driven or due to RTT_PARK termination) until exiting PDA Enumerate Programming Mode. Holding the signals high will ensure that this DRAM is never set to a PDA Enumerate ID other than the default setting of 0xFH (15). Timing diagram example shown in Figure 74.

Table 82 — PDA Enumerate Results

DQS_t/DQS_c for x4/x8 DQSL_t/DQSL_c for x16	DQ0 for x4/x8 DQL0 for x16	PDA Enumerate Result	Notes
Toggling	Low - "0"	Enumerate	
Toggling	High - "1"	Don't Enumerate	
High - "1"	Low - "0"	Unknown	1
High - "1"	High - "1"	Don't Enumerate	2
Differentially Low	Valid	Don't Enumerate	3

Note 1: DQS_t/DQS_c are differential signals and small amounts of noise could appear as "toggling", resulting in "Unknown" PDA Enumerate Results".

Note 2: The expected usage case where the DQS signals are high is to have the DQs held high as well.

Note 3: "Differentially Low" is defined as DQS_t low and DQS_c high (DQSL_t low and DQSL_c high for x16)

4. A minimum of one complete BL16 set of strobe edges (8 rising edges and 8 falling edges) must be sent by the host within the tPDA_DQS_DELAY min/max range after the MPC command. The DQ value is captured during any strobe edge during the valid low duration of the target DQ. Valid low time is defined as the time between tPDA_S and tPDA_H. If the DRAM captures a 0 on DQ0 (or DQL0 for x16 devices) at any strobe edge in the strobe sequence, the PDA Enumerate ID command shall be executed by the DRAM. Since the write timings for the DQ bus have not been trained, the host must ensure a minimum of 16 strobe edges occurs after a period of tPDA_DQS_Delay(min) after the associated MPC command. The BC8 mode register setting in the DRAM is ignored while in PDA Enumerate Programming mode. The DQS assumes preamble/postamble requirements.
5. Prior to when the MPC command for PDA Enumerate Programming Mode entry is sent by the host, the host must drive DQS_t and DQS_c differentially low, other than when the burst of 16 strobe edges is sent in association with the PDA Enumerate ID MPC command. The host must send preamble and postamble DQS_t/DQS_c toggles during the qualification of the PDA command. Once PDA Enumerate Programming Mode is enabled in the DRAM, the host memory controller shall wait tMPC_Delay to the time the first PDA Enumerate ID MPC command is issued.
6. In the PDA Enumerate Programming Mode, only PDA Enumerate ID MPC commands and Exit PDA Enumerate Programming Mode MPC command are allowed.
7. In the PDA Enumerate Programming Mode, the default (or previously programmed) RTT_PARK value will be applied to the DQ signals.
8. The MPC PDA Enumerate ID command cycle time is defined as tPDA_DELAY. This time is longer than the normal MPC_Delay and must be met in order to provide the DRAM time to latch the asserted DQ and complete the write operation to the PDA Enumerate ID mode register (MR1:OP[3:0], prior to the next MPC PDA Enumerate ID command shown in Figure 74.
9. To remove the DRAM from PDA Enumerate Programming Mode, send an Exit PDA Enumerate Programming MPC command, OP[7:0]=0000 1010_B. The Exit PDA Enumerate Programming Mode MPC command is never qualified by the DQ settings and is applied to all DRAMs in the rank.
10. During the PDA Enumerate ID Programming mode, only one enumerate command is allowed to a device. Once the PDA Enumerate ID is programmed, any change for the PDA Enumerate ID requires DRAM to enter into PDA Enumerate ID Programming mode.

As an example, the following sequence to program the PDA Enumerate ID per device is as follows:

1. Send MPC with ‘Enter PDA Enumerate Programming Mode’ opcode
2. For (i = 0, i < MAX_DRAMS, i++)
    a. Send PDA Enumerate ID with i in the opcode (4-bit value), with device i’s DQ signals low
3. Send MPC with ‘Exit PDA Enumerate Programming Mode’ opcode

The following figure shows a timing diagram for setting the PDA Enumerate ID value for one device. In this case only one device is programmed prior to exiting PDA Enumerate Programming Mode, but many devices may be programmed prior to exiting PDA Enumerate Programming Mode.

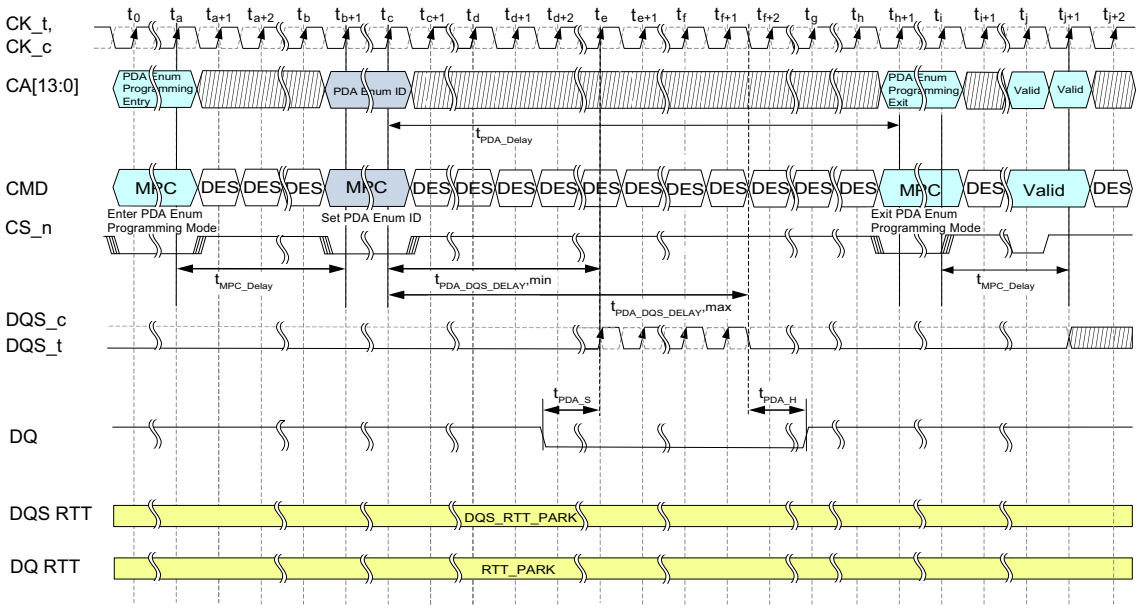


Figure 74 — Timing Diagram showing PDA Enumerate Programming Mode Entry, Programming of PDA Enumerate ID, and PDA Enumerate Programming Mode Exit

Note(s)

1 - The diagram above assumes preamble/postamble requirements for DQS.

2 - The 2nd MPC command at tA+1 is assuming a multi-cycle command and the timings are adjusted to visually show separation between spacing timings such as tMPC_Delay (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY.

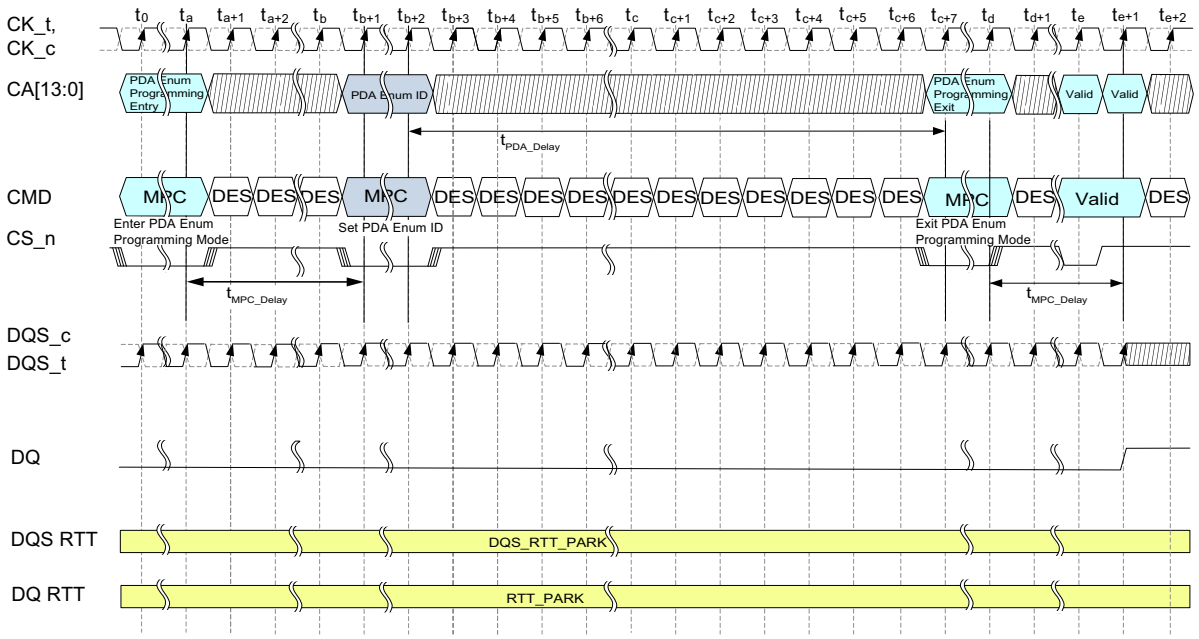


Figure 75 — PDA Enumerate Programming Mode w/Continuous DQS Toggle Timing Diagram

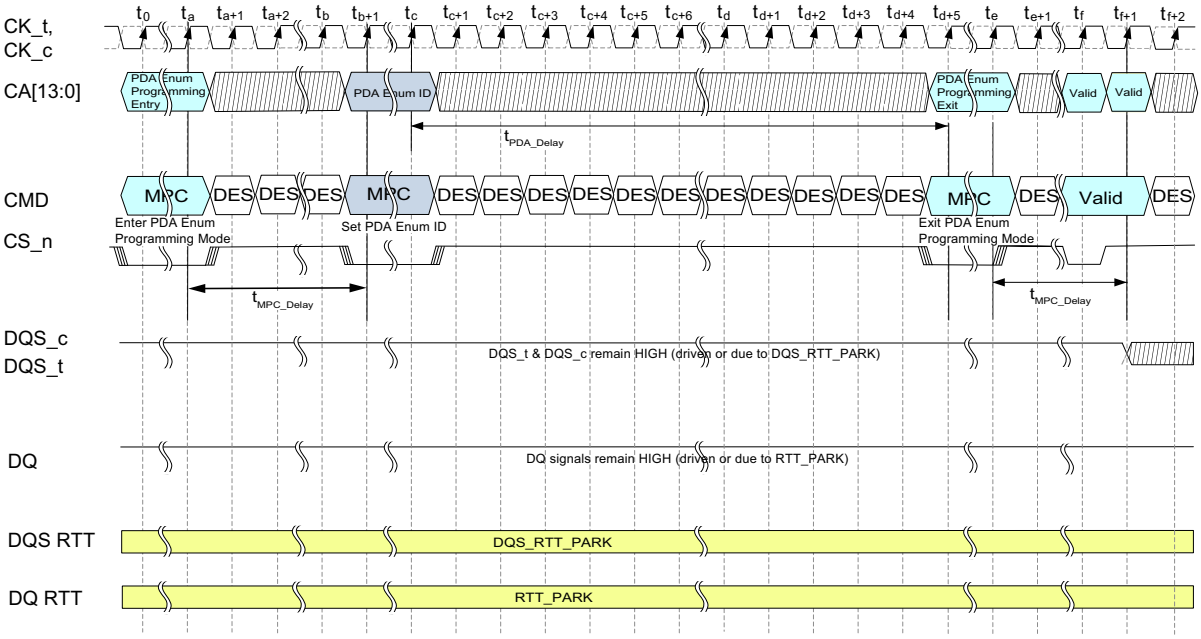


Figure 76 — Timing Diagram showing “Don’t enumerate” case.

4.16.2 PDA Select ID Operation

Once the PDA Enumerate ID's have been programmed in all the DRAMs, the execution of future MPC/MRW/VrefCA commands depend on the value of the PDA Select ID and the type of MPC command. If the PDA Select ID is set to 1111_B, all DRAMs will execute the command. For all MRW commands and VrefCA commands, and some of the MPC commands (RTT_CA/CS/CK and RTT_PARK opcodes), the PDA Select ID will be compared to the PDA Enumerate ID to determine if the DRAM will execute the commands. For all other MPC commands (i.e. not the RTT_CA/CS/CK and RTT_PARK opcodes), the DRAM will execute the command regardless of the PDA Select ID value.

As an example, the following sequence could be used to program unique MR fields per device:

1. Send MPC with 'PDA Select ID' opcode, with encoding 0000 included in the opcode
2. Send MRW's for field settings specific to Device 0000. this can be any number of MRW's
3. Send MPC with 'PDA Select ID' opcode, with encoding 0001 included in the opcode
4. Send MRW's for field settings specific to Device 0001. this can be any number of MRW's
5. Repeat for any number of devices
6. Send MPC with 'PDA Select ID' opcode, with encoding 1111 included in the opcode to enable all DRAMs to execute all MRW, VrefCA, and MPC commands.

The following timing diagram shows an example sequencing of the programming of the PDA Select ID and MPC, VrefCA, or MRW commands.

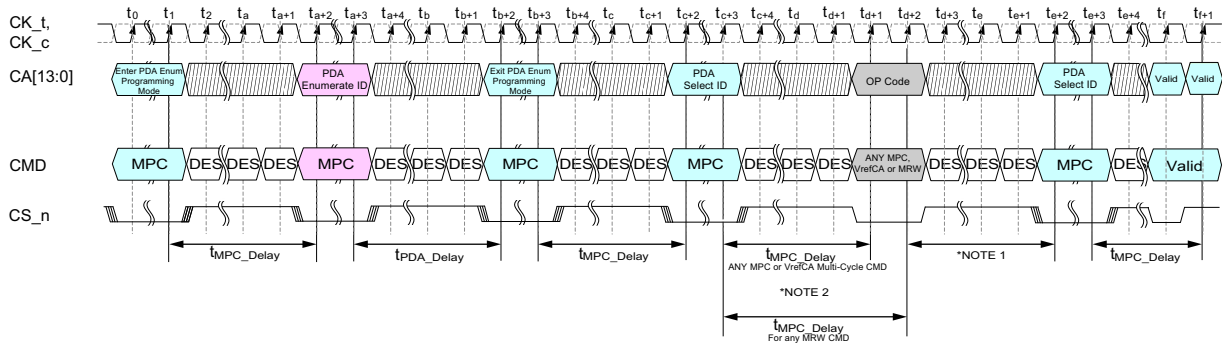


Figure 77 — Timing Diagram showing multi-cycle MPC command sequencing with PDA Enumerate & PDA Select ID

Note(s):

1. Commands used such as VREFCA or MRW have different command spacing requirements. Please refer to those specific sections in the document for details.
2. ANY Multi-cycle MPC or VREFCA command spacing is measured from the last valid command cycle to the first following valid command cycle, while standard command spacing goes from last valid command cycle to last valid command cycle. See MRW command period diagrams for details.

The following table summarizes the electrical parameters associated with PDA Enumerate Programming Mode:

Table 83 — PDA Parametric Timings

Parameter	Symbol	DDR5-3200 to 4800		DDR5-5200 to 6400		Units	NOTE
		Min	Max	Min	Max		
PDA Enumerate ID Command to any other command cycle time	tPDA_DELAY	tPDA_DQS_Delay _max+BL/2+19ns	-	TBD	-	ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	tPDA_DQS_DELAY	5	18	TBD	TBD	ns	1
DQ Setup Time during PDA operation	tPDA_S	3	-	TBD	-	nCK	
DQ Hold Time during PDA operation	tPDA_H	3	-	TBD	-	nCK	

Note 1: The range of tPDA_DQS_DELAY specifies the full range of when the minimum of 16 strobe edges can be sent by the host controller.

4.17 Read Training Pattern

4.17.1 Introduction

Training of the Memory Interface requires the ability to read a known pattern from the DRAM, prior to enabling writes into the DRAM. Due to the increased frequencies supported by DDR5, a simple repeating pattern will not be sufficient for read training. A Linear-Feedback Shift Register (LFSR) for a pattern generator will also be required. The read training pattern is accessed when the host issues an MRR command to the MR31 address, and CRC must be disabled prior to issue this command. In this case, the returned data will be a pattern instead of the contents of a mode register. The timing of the read data return is the same as for an MRR or Read command, including the operation of the strobes (DQSL_t, DQSL_c, DQSU_t, DQSU_c). The DRAM shall also support non-target ODT.

An alternate continuous burst mode is available and is configured with MRW to MR25:OP[3]=1. Once this mode is configured, any subsequent MRR (it does not need to be an explicit MRR to MR31) to that DRAM will start the pattern output and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or issuing an MRW MR25:OP[3]=0 command that reverts it to the “MRR command based (Default)” mode as shown in Figure 81. Once the MR25:OP[3]=0 “MRR command based (Default)” is registered by the DRAM, it will stop all pattern traffic by tCont_Exit. Since there is no min time for tCont_Exit, the DRAM may stop the pattern prior to tCont_Exit, potentially truncating any current burst pattern. To ensure that the DRAM’s state-machine doesn’t get into some meta-stability while turning off the output pattern, the host must issue a second MR25:OP[3]=0 “MRR command based (Default)” after waiting tMRR, which will then start tCont_Exit_delay. After tCont_Exit_delay has expired, any other valid command is then legal. All Read Training Patterns (modes) are supported in continuous burst mode. The host shall disable Read CRC, if enabled, prior to using continuous burst mode.

Prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode), the initial seed value will need to be programmed in MR26-MR30 else the power on default values will be used.

The default value for the **Read Pattern Data0/LFSR0** (MR26) register setting is: 0x5A and the default value for the **Read Pattern Data1/LFSR1 (MR27)** register setting is: 0x3C. The **Read Pattern Invert** (MR28, MR29) register settings default to 0. The **Read LFSR Assignments** (MR30) register setting default is 0xFE.

The DRAM will not store the current LFSR state when exiting the Continuous Burst Output Mode and may clear the pattern values stored in MR26-MR30, therefore any subsequent pattern reads will require the host to reprogram the seed, pattern, inversion and LFSR assignments in MR26-MR30.

The Read Training Pattern has 2 primary supported modes of operation. One of the modes is referred to as the serial format. The second mode is LFSR mode. The LFSR mode is required due to the higher frequency bus operation for DDR5. There is a secondary mode associated with the LFSR mode, which enables the generation of a simple high frequency clock pattern instead of the LFSR pattern. The Read Training Pattern is a full BL16 pattern for each MRR command issued to the Read Training Pattern address.

The Read Training Pattern has a command burst length 16 regardless of the MR0 setting, and it should not be disturbed by an ACT command until the completion of training.

Table 84 — Read Training Pattern Address

MR Address	Operating Mode	Description
MR31	Read Training Pattern	This MR address is reserved. There are no specific register fields associated with this address. In response to the MRR to this address the DRAM will send the BL16 read training pattern. All 8 bits associated with this MR address are reserved.

The following table shows the MR field and encodings for the Read Training Pattern format settings.

Table 85 — Read Training Mode Settings

MR Address	Operating Mode	Description
MR25 OP[0]	Read Training Pattern Format	**0_B: Serial** **1_B: LFSR**
MR25 OP[1]	LFSR0 Pattern Option	**0_B: LFSR** **1_B: Clock**
MR25 OP[2]	LFSR1 Pattern Option	**0_B: LFSR** **1_B: Clock**
MR25 OP[3]	Continuous Burst Mode	**0_B: MRR command based (Default)** **1_B: Continuous Burst Output**

The default value for the **Read Training Pattern Format** register setting is: 0x0.

For Serial Read Training Pattern Format mode, the following Mode Registers are programmed with the data pattern. There are two 8-

bit registers to provide a 16 UI pattern length and two 8-bit registers to provide up to x16 data width for per-DQ-lane inversion.

The LFSR mode requires an 8-bit Mode Register to program the seed for the 8-bit LFSR. The details of the LFSR polynomial and outputs are explained in the following section. The **Read Pattern Data0/LFSR0** and **Read Pattern Data1/LFSR1** registers are re-purposed to program the LFSR seed when the **Read Training Pattern Format** is set to LFSR.

Table 86 — Read Pattern Data0 / LFSR0

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR26	UI	7	6	5	4	3	2	1	0

The default value for the **Read Pattern Data0/LFSR0** register setting is: 0x5A.

Table 87 — Read Pattern Data1 / LFSR1

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR27	UI	15	14	13	12	11	10	9	8

The default value for the **Read Pattern Data1/LFSR1** register setting is: 0x3C.

The values for the **Read Pattern Data0/LFSR0** and **Read Pattern Data1/LFSR1** registers may be restored to the default values under the following conditions:

- Self Refresh
- Power-down entry
- Exiting Continuous Burst Output Mode

If any of the above conditions occur, the Host will need to reprogram the contents of MR26 and MR27, prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode).

In both cases, when the **Read Training Pattern Format** is set to Serial mode or LFSR mode, the **Read Pattern Invert - Lower DQ Bits** and **Read Pattern Invert - Upper DQ Bits** settings will additionally invert the pattern, per DQ bit. The **Read Pattern Invert - Lower DQ Bits** register will apply to x4, x8, and x16 devices. The **Read Pattern Invert - Upper DQ Bits** register only applies to x16 devices, for the upper byte.

Table 88 — Read Pattern Invert - Lower DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR28	DQ Invert	DQL7	DQL6	DQL5	DQL4	DQL3	DQL2	DQL1	DQL0

The default value for the **Read Pattern Invert - Lower DQ Bits** register setting is: 0x00.

Table 89 — Read Pattern Invert - Upper DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR29	DQ Invert	DQU7	DQU6	DQU5	DQU4	DQU3	DQU2	DQU1	DQU0

The default value for the **Read Pattern Invert - Upper DQ Bits** register setting is: 0x00.

The values for both **Read Pattern Invert - Lower and Upper DQ Bit** registers may be restored to the default values under the following conditions:

- Self Refresh
- Power-down entry
- Exiting Continuous Burst Output Mode

If any of the above conditions occur, the Host will need to reprogram the contents of MR28 and MR29 if non-default values are desired, prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode).

A value of 0 in any bit location of the **Read Pattern Invert - Lower DQ Bits** or **Read Pattern Invert - Upper DQ Bits** registers will leave the pattern un-inverted for the associated DQ. A value of 1 in any bit location of the **Read Pattern Invert - Lower DQ Bits** or **Read Pattern Invert - Upper DQ Bits** registers will invert the pattern for the associated DQ.

4.17.2 LFSR Pattern Generation

The LFSR is an 8-bit Galois LFSR. The polynomial for the Galois LFSR is $x^8+x^6+x^5+x^4+1$. The figure below shows the logic to implement the LFSR. The numbered locations within the shift register show the mapping of the seed/state positions within the register. There are two instances of the same LFSR polynomial. These two instances will have unique seeds/states and supply patterns to any of the DQ outputs.

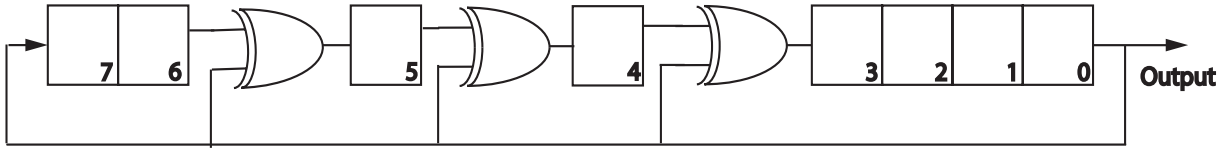


Figure 78 — Read Training Pattern LFSR

The seed location in the figure clarifies the mapping for the **Read Pattern Data0/LFRS0** and **Read Pattern Data1/LFSR1** mode registers relative to the LFSR logic. The LFSR output is directed to any number of the DQ outputs, depending on the LFSR assignment programming. These assignments between LFSR0 and LFSR1 to each DQ output will create a unique pattern sequence for better coverage of DQ to DQ crosstalk interactions. The LFSR assignments are programmed according to the following table:

Table 90 — Read LFSR Assignments

MR Address	MRW OP	LFSR Assignment	MR Setting
MR30	OP0	DQL0/DQU0	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP1	DQL1/DQU1	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP2	DQL2/DQU2	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP3	DQL3/DQU3	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP4	DQL4/DQU4	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP5	DQL5/DQU5	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP6	DQL6/DQU6	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP7	DQL7/DQU7	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**

The default value for the **Read LFSR Assignments** register setting is: 0xFE.

The values for the **Read LFSR Assignments** register may be restored to the default values under the following conditions:

- Self Refresh
- Power-down entry
- Exiting Continuous Burst Output Mode

If any of the above conditions occur, the Host will need to reprogram the contents of MR30 if non-default values are desired, prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode).

The LFSR output will change at the UI frequency, producing a new output value on every UI. The LFSR will only change state to support the read data after the MRR to the specific (MR31) Read Training Pattern address. When there are no MRR accesses to the (MR31) Read Training Pattern address, the LFSR will retain its previous state (from the end of the previous Read Training Pattern MRR access completion). Therefore, the full state space of the LFSR may be traversed through a series of 16 MRR commands, each of which accesses 16 UI's of LFSR output. The BL for the LFSR data will always be BL16. The state of the LFSR can also be changed by sending a new MRW command to reset the LFSR0 and LFSR1 seed mode registers (MR26 and MR27) or through the

reset conditions listed for those registers. A setting of 0x00 in either of the LFSR seed registers (MR26 and MR27) will not produce a pattern with any transitions to 1. When set to this value the LFSR will produce a constant 0 pattern.

When the **LFSR0 Pattern Option** MR25:OP[1] is set to 1, the pattern that is supplied by the DRAM is a high frequency clock pattern, instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 0 in the corresponding DQ Opcode location in the **Read LFSR Assignments register**. The first UI of the pattern will have a value of 0. The second UI will have a value of 1, and this will continue to toggle for each subsequent UI.

When the **LFSR1 Pattern Option** MR25:OP[2] is set to 1, the pattern that is supplied by the DRAM is a high frequency clock pattern, instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 1 in the corresponding DQ Opcode location in the **Read LFSR Assignments register**. The first UI of the pattern will have a value of 0. The second UI will have a value of 1, and this will continue to toggle for each subsequent UI.

The state of the LFSR will not change when an MRR to MR31 occurs if the associated **LFSR Pattern Option** is set to 1 in MR25[1] for LFSR0 or MR25[2] for LFSR1, designating the clock pattern. The state of both LFSR0 and LFSR1 will also not change when an MRR to MR31 occurs if the serial mode is selected by setting MR25[0] = 0. The **Read LFSR Assignments** settings have no impact on whether or not the LFSR state progresses with each MRR to MR31. Only the **Read Training Pattern Format** and **LFSR Pattern Option** settings determine whether the LFSR is actively computing next states.

4.17.3 Read Training Pattern Examples

The following table shows the bit sequence of the Read Training Pattern, for the following programming:
Read Training Pattern Format = 0 (Serial)
LFSR0 Pattern Option = 0 (These are don't cares when in Serial Read Training Pattern Format)
LFSR1 Pattern Option = 0 (These are don't cares when in Serial Read Training Pattern Format)
Read Pattern Data0/LFSR0 = 0x1C
Read Pattern Data1/LFSR1 = 0x59
Read Pattern Invert - Lower DQ Bits = 0x55
Read Pattern Invert - Upper DQ Bits = 0x55

Table 91 — Serial Bit Sequence Example

Pin	Invert	Bit Sequence															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

The following table shows the bit sequence of the Read Training Pattern, for the following programming:
Read Training Pattern Format = 1 (LFSR)
LFSR0 Pattern Option = 0
LFSR1 Pattern Option = 0
Read Pattern Data0/LFSR0 = 0x5A
Read Pattern Data1/LFSR1 = 0x3C
Read LFSR Assignments = 0xFE
Read Pattern Invert - Lower DQ Bits = 0x00
Read Pattern Invert - Upper DQ Bits = 0xFF

Table 92 — LFSR Bit Sequence Example

Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	0 (No)	0	0	0	1	1	0	0	0	0	0	0	1	1	1	0	1	0
DQL1	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL2	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL3	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL4	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL5	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL6	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL7	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQU0	1 (Yes)	0	1	1	0	0	1	1	1	1	1	1	0	0	0	1	0	1
DQU1	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU2	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU3	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU4	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU5	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU6	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU7	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1

The following table shows the bit sequence of the Read Training Pattern, for the following programming:
Read Training Pattern Format = 1 (LFSR)
LFSR0 Pattern Option = 0
LFSR1 Pattern Option = 1 (Clock Pattern Option)
Read Pattern Data0/LFSR0 = 0x00 (When the LFSR seed is set to 0, this produces a constant 0 pattern)
Read Pattern Data1/LFSR1 = 0x3C (This value is a don't care when LFSR1 Pattern Option = 1)
Read LFSR Assignments = 0x04
Read Pattern Invert - Lower DQ Bits = 0xFB
Read Pattern Invert - Upper DQ Bits = 0xFB

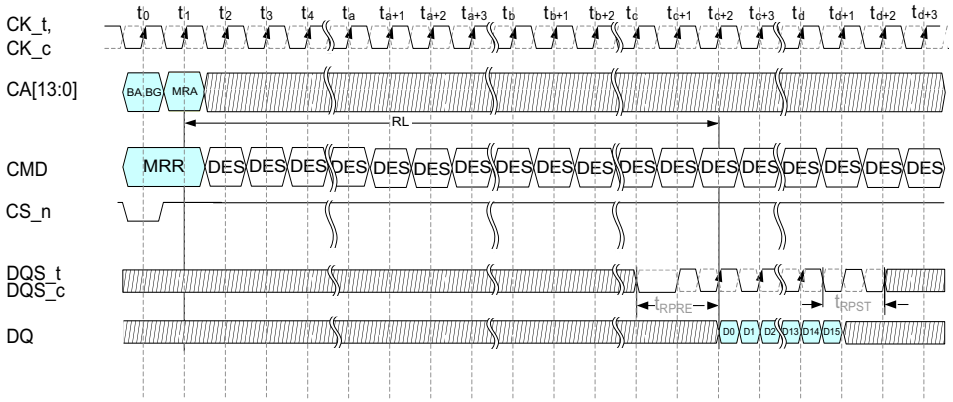
Table 93 — LFSR Bit Sequence Example

Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQL3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQU3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

4.17.4 Read Training Pattern Timing Diagrams

The timing of the data return and strobe sequence should match that of a Read operation. The timing of the Read Training Pattern will be similar to the MRR operation, with the exception that the MRR to the address that invokes the Read Training Pattern will be a full BL16 pattern. The timing between MRR commands to access the Read Training Pattern is defined as tMRR_p, which supports back to back data patterns. This is faster than a normal MRR to MRR condition which is defined as tMRR.

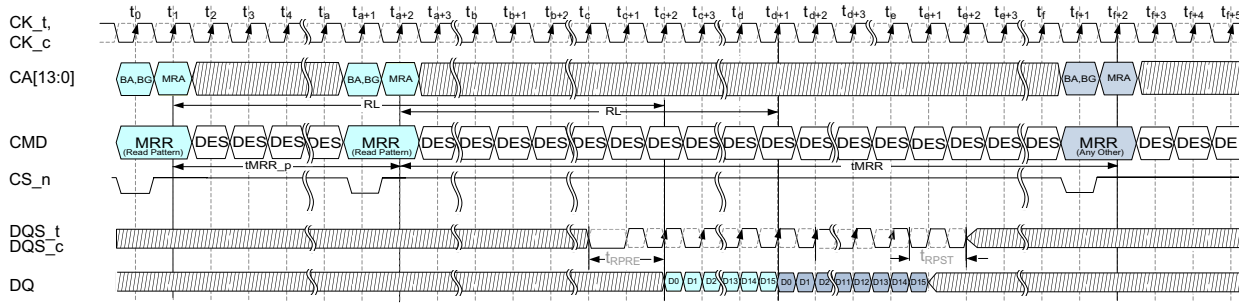
The following timing diagram shows the general timing sequence for an MRR that accesses the Read Training Pattern:



Note - The Read Training Pattern shall align to the DDR5 preamble timings.

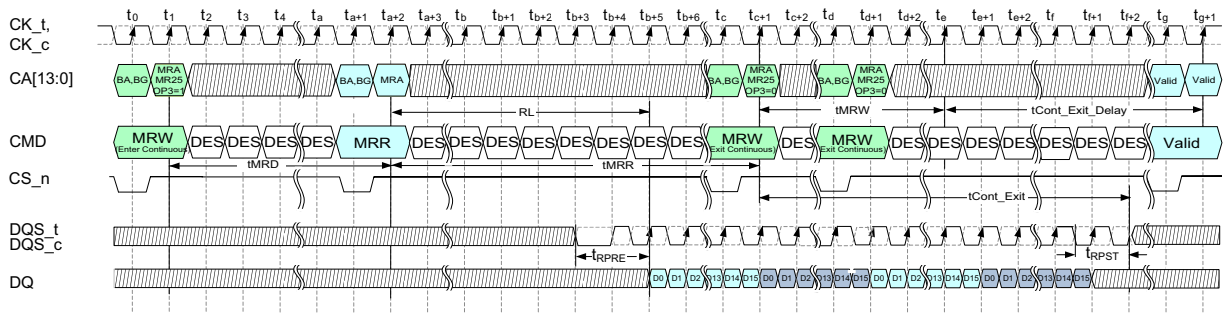
Figure 79 — Timing Diagram for Read Training Pattern

The Read Training Pattern must also support back to back traffic, for any number of MRR commands sequenced every 8 tCK. The following timing diagram shows a back to back pattern example:



Note - The Read Training Pattern shall align to the DDR5 preamble timings.

Figure 80 — Timing Diagram for Back to Back Read Training Patterns



Note - The Read Training Pattern shall align to the DDR5 preamble timings and will exit after the MRW (Continuous Exit encoding) has been received and but before tCont_Exit has expired. During tCont_Exit, the data output may not follow the read pattern data.

Figure 81 — Timing Diagram for Continuous Burst Mode Read Training Patterns

Table 94 — Timing parameters for Read Training Patterns

Parameter	Symbol	Min	Max	Units	Notes
Registration of MRW Continuous Burst Mode Exit to next valid command delay	tCont_Exit_Delay	-	tCont_Exit+ tMRW	ns	
Registration of MRW Continuous Burst Mode Exit to end of training mode	tCont_Exit	-	RL+BL/ 2+10nCK	ns	

4.18 Read Preamble Training Mode

4.18.1 Introduction

Read preamble training supports read leveling of the host receiver timings. This mode supports MRR transactions that access the Read Training Pattern, and cannot be used during any other data transactions. Just like Read Training Pattern, Read Preamble Training needs to be entered with CRC disabled. Read preamble training changes the read strobe behavior such that the strobes are always driven by the DRAM, and only toggle during a 1tCK preamble plus the actual burst of the read data. There is no toggle during postamble time. This mode enables the host to detect the timing of when the first data and associated strobe is returned after a read command.

4.18.2 Entry and Exit for Preamble Training Mode

The DRAM enters Read Preamble Training Mode by setting MR2:OP[0] = 1. Read Preamble Training Mode is exited by setting MR2:OP[0] = 0. Read Preamble Training should not be disturbed by an ACT command until the completion of the training.

Table 95 — MR2 Register Information - for Reference only - See Mode Register Section for details

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Internal Write Timing	RFU	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training

Function	Register Type	Operand	Data	Notes
Read Preamble Training	R/W	OP[0]	0B: Normal Mode (Default) 1B: Read Preamble Training	

4.18.3 Preamble Training Mode Operation

Once the DRAM is placed in Read Preamble Training Mode, the only data transactions supported are MRR commands. All non-data commands, such as MRW, are still supported in this mode. Once READ Preamble Training is enabled, the device will drive DQS_t LOW and DQS_c HIGH within tSDOn and remain at these levels until an MRR command is issued.

During read preamble training, a 1 tCK preamble will be used instead of the programmed DQS preamble setting. Once the MRR command is issued, the device will drive DQS_t/DQS_c after CL-tRPRE (where tRPRE=1CK), like a normal READ burst with the Read DQS Offset setting programmed in MR40 applied. In response to the MRR to the designated Read Training Pattern Address, the device must also drive the DQ pattern as per the Read Pattern configuration while in this mode. The MRR commands may be sequenced to enable back to back bursts on the DQ bus.

Read preamble training mode is exited within tSDOff after setting MR2:OP[0].

The following figure shows the timing for the strobe driven differential low after Read Preamble Training Mode is enabled, and also shows the strobe timings including a 1tCK Preamble, after an MRR command to access the Read Training Pattern:

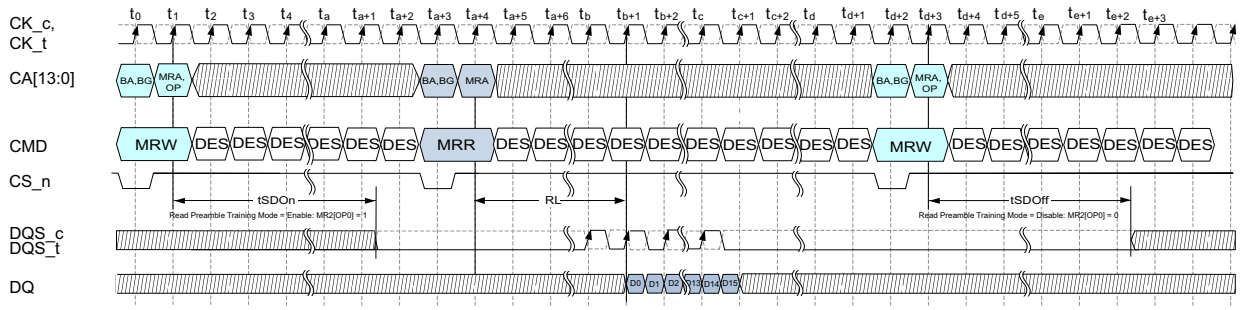


Figure 82 — Timing Diagram for Read Preamble Training Mode Entry, Read Training Pattern Access and Read Preamble Training Mode Exit

Table 96 — Timing parameters for Preamble Training Mode

Parameter	Symbol	Min	Max
Delay from MRW Command to DQS Driven	tSDOn	-	Max(12nCK, 20ns)
Delay from MRW Command to DQS Disabled	tSDOff	-	Max(12nCK, 20ns)

4.19 CA Training Mode (CATM)

4.19.1 Introduction

The CA Training Mode is a method to facilitate the loopback of a logical combination of the sampled CA[13:0] signals. In this mode, the CK is running, and the CS_n qualifies when the CK samples the CA signals. A loopback equation that includes all the CA signals results in an output value that is sent asynchronously on the DQ signals back to the host memory controller. The host timings between CS_n, CK, and CA[13:0] signals can then be optimized for proper alignment. When the DRAM is in this mode, no functional commands are executed in the DRAM. The functional command interface is restored only after exiting this mode, which requires a CS_n assertion of two or more consecutive tCK. Prior to entering the CA Training Mode, the CS_n signal must be aligned to the CK to meet the CS_n to CK timing specifications. This assumes that CS Training has been completed to determine the correct CS_n timings on the host, so the timing window for the CS to be met to ensure enought setup or hold timing margin prior to entering Command/Address training mode. Chip select training, through CSTM, can be used to accomplish this.

4.19.2 Entry and Exit for CA Training Mode

The CA Training Mode is enabled through an MPC command, with the opcode designated for CA Training Mode Entry**.** Once this MPC command has executed no other commands will be interpreted by the DRAM. Only the sampling of the CA signals, evaluation of the XOR result, and loop back to the DQ's will occur. While in CA Training Mode, the CS_n signal will only assert for a single tCK at a time. The maximum sampling rate on the CA signals will be every 4tCK.

The CA Training Mode is disabled by asserting CS_n for 2 or more cycles in a row, while sending a NOP command on the CA bus.

4.19.3 CA Training Mode (CATM) Operation

In CA Training Mode, the CA values are sampled in the same way as for functional operation, where the CS_n qualifies which cycle the sampling occurs, and the sample is captured by the rising CK edge. Unlike functional operation, there is no concept of multiple cycle commands in CA Training Mode. Sampling of the CA signals ONLY occurs when CS_n is asserted. Once the CA signals are sampled, the values are XOR'd to produce an output value. This output value is driven on all the DQ pins, as a pseudo-static value. These output values will be held until the next sample is captured on the CA bus, according to the CS_n assertion.

During CA Training Mode the CA ODT is enabled as for functional operation. The VrefCA is Group According to the functional setting. The timing requirements for the CA bus, CK_t, CK_c, and CS_n are the same as for functional operation.

The delay from when the CA signals are sampled during the CS_n assertion and when the output of the XOR computation is driven on the DQ pins is specified as t_{CATM_Valid}, as shown in the following figure. CS_n shall be asserted every 4tCK or with greater than 4tCK separation between assertions, and thus the CA XOR output shall transition every 4tCK or greater. The following figure demonstrates an example where two CS_n assertions occur with a separation of 4tCK. The DRAM will exit CA Training Mode when the CS_n is asserted for 2 or more consecutive cycles but limited to 8 cycles.

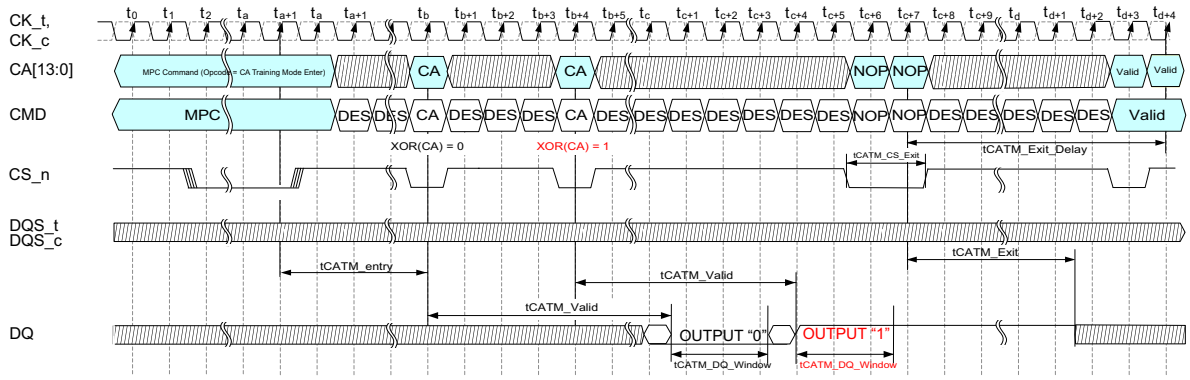


Figure 83 — Timing Diagram for CA Training Mode

Note(s):

Table 97 — AC parameters for CA Training Mode

Symbol	Description	Min	Max	Unit	Note
tCATM_Entry	Registration of CATM entry command to start of training samples time	20	-	ns	
tCATM_Exit	Registration of CATM exit CS_n assertion to end of training mode. This is when DQ is no longer driven by the DRAM	-	14	ns	
tCATM_Exit_Delay	Registration of CATM exit to next valid command delay	20	-	ns	
tCATM_Valid	Time from sample evaluation to output on DQ bus	-	20	ns	
tCATM_DQ_Window	Time output is available on DQ Bus	2	-	nCK	1
tCATM_CS_Exit	CS_n assertion duration to exit CATM	2	8	nCK	

Note(s):
1. This timing parameter is applied to each DQ independently, not all-DQs valid window perspective.

4.19.3.1 CA Loopback Equations

The CATM Output is computed based on the CS_n assertion and the values of the CA inputs. The following table clarifies the output computation.

Table 98 — CA Training Mode Output

CS_n	CATM Output
0	XOR(CA[13:0])[1]
1	Hold previous value

1. The XOR function occurs after mirroring/inversion recovery, and only includes signals supported on the DRAM, i.e. may not include CA[13], depending on density (including stacking). If CA[13] is not needed for the DRAM's density, the logical value shall be considered 0 for the XOR computation, though as indicated in the pin description table for MIR, the ball location associated with CA13's logical input (which switches with CA12) shall be connected to VDDQ.

4.19.3.2 Output equations

The following table shows which signals will transmit the output of the CA Training Mode loopback equation. These values are driven asynchronously as pseudo-static values, updating with a new output at a time t_{CATM_Valid} after each CS_n assertion.

Table 99 — Output Equations per Interface Width

Output	X16	X8	X4
DQ0	CATM Output	CATM Output	CATM Output
DQ1	CATM Output	CATM Output	CATM Output
DQ2	CATM Output	CATM Output	CATM Output
DQ3	CATM Output	CATM Output	CATM Output
DQ4	CATM Output	CATM Output	
DQ5	CATM Output	CATM Output	
DQ6	CATM Output	CATM Output	
DQ7	CATM Output	CATM Output	
DML			
TDQS_c			
DQSL_t			
DQSL_c			
DQ8	CATM Output		
DQ9	CATM Output		
DQ10	CATM Output		
DQ11	CATM Output		
DQ12	CATM Output		
DQ13	CATM Output		
DQ14	CATM Output		
DQ15	CATM Output		
DMU			
DQSU_t			
DQSU_c			

4.20 CS Training Mode (CSTM)

4.20.1 Introduction

The CS Training Mode is a method to facilitate the loopback of a sampled sequence of the CS_n signal. In this mode, the CK is running, and the CA signals are held in a NOP command encoding state. Once this mode is enabled and the DRAM devices are selected to actively sample and drive feedback, The DRAM will sample the CS_n signal on the rising edge of CK. Every set of four CK rising edge samples will be included in a logical computation to determine the CSTM Output result that is sent back to the host on the DQ bus. Once sampling begins, the DRAM must maintain the consecutive grouping of the samples every 4 tCK. When the CS_n Sample[0] and Sample[2] results in a logic 0 and the CS_n Sample[1] and Sample[3] results in a logic 1, the DRAM will drive a 0 on all the DQ signals. There is no requirement to drive any strobes, and the output signal could transition as often as every 4 tCK.

4.20.2 Entry and Exit for CS Training Mode

The CS Training Mode is enabled when the host sends an MPC command with the opcode for CS Training Mode Entry. Since CS Training must occur prior to establishing alignment between CK and CS_n signals, the MPC command extends beyond multiple tCK cycles, during which the CS_n signal is asserted. When the DRAM is in this mode, commands are still actively processed. The only commands that should be sent by the host memory controller while CS Training Mode is enabled are the NOP command and the MPC to exit CS Training Mode. Any other command may produce unreliable results. Once the DRAM has CS Training Mode enabled, the DRAM begins sampling on every rising CK edge, with the 4-sample groups looping consecutively. Depending on the value of the samples, the DQ signals are driven high or low. Prior to entering CS Training Mode, the DQ signals are not driven by the DRAM and are terminated according to the default RTT_PARK setting. After CS Training Mode is enabled, the DQ signal will begin driving the output values based on the CS Training Mode samples. Once the DQ signals are driven by the DRAM, RTT_PARK termination will no longer be applied, similar to a READ operation.

To exit CS Training Mode, an MPC command must be sent to disable CS Training Mode. Since the timing relationship between CS_n and CK is understood when exiting CS Training Mode, the host can either send a multi-cycle CS_n assertion during the MPC command or a single tCK assertion.

4.20.3 CS Training Mode (CSTM) Operation

In CS Training Mode, the CS_n values are sampled on all CK rising edges. Each group of 4 consecutive samples is evaluated in pairs, and then the two pairs are combined with a logical OR prior to sending to the DQ output. The samples evaluation to determine the output is as follows:

Table 100 — Sample Evaluation for Intermediate Output[0]

Output[0]	CS_n Sample[0]	CS_n Sample[1]
1	0	0
0	0	1
1	1	0
1	1	1

Table 101 — Sample Evaluation for Intermediate Output[1]

Output[1]	CS_n Sample[2]	CS_n Sample[3]
1	0	0
0	0	1
1	1	0
1	1	1

Table 102 — Sample Evaluation for final CSTM Output

CSTM Output*	Output[0]	Output[1]
0	0	0
1	0	1
1	1	0
1	1	1

*When there is no change on the CSTM Output from previous evaluation, DQ shall continue to drive same value continuously with no switching on the bus.

During CS Training Mode the CA ODT is enabled as for functional operation. The VrefCA is Group According to the functional setting (through the VrefCA Command).

The delay from when the CS_n signals are sampled during the fourth CK rising edge (Sample[3]) to when the output of the sample evaluation is driven to a stable value on the DQ pins is specified as tCSTM_Valid, as shown in the following figure. The details of the tCSTM_entry, tCSTM_exit, and tCSTM_DQ_Window are also illustrated.

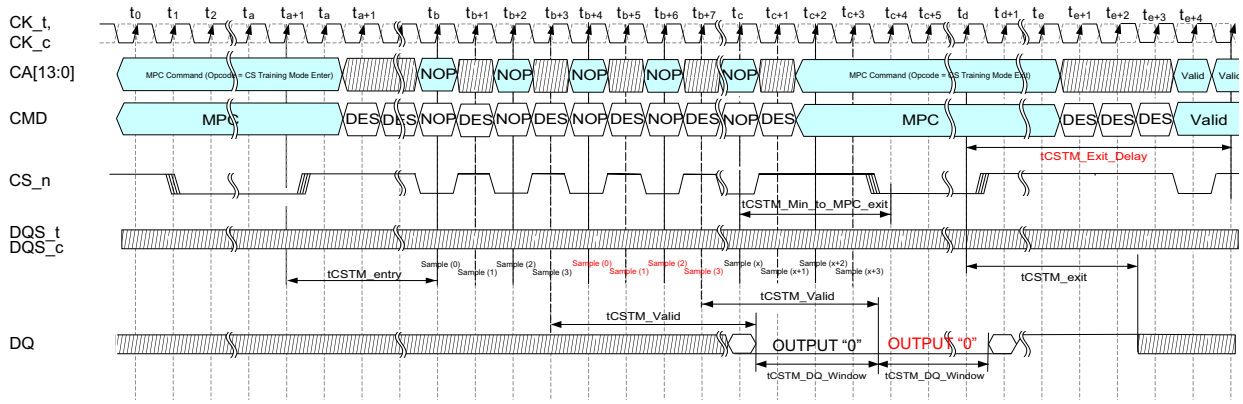


Figure 84 — Timing Diagram for CS Training Mode with Consecutive Output Samples = 0

The following figure illustrates an example where the DQ Output switches from a logic 0 to a logic 1 value, demonstrating the minimum tCSTM_DQ_Window:

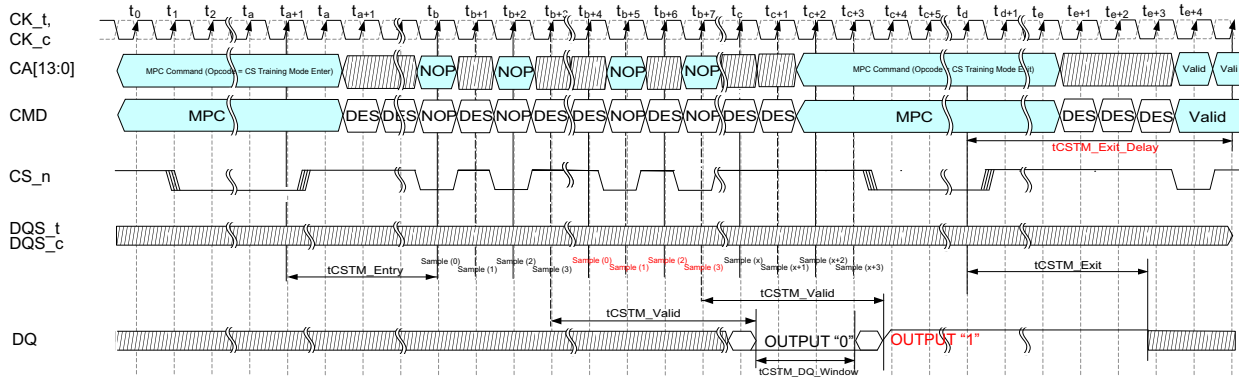


Figure 85 — Timing Diagram for CS Training Mode with Output Sample Toggle

Note 1 - See MPC Command for details on Setup, Hold and command register time.
Note 2 - The CA bus must meet setup and hold times on any clock where it is possible that CS_n might be sampled low while in CS training mode.

When host trains CS_n timing for DDR5 by using CSTM, CS_n sampling timing for each DRAM could be different from each other because the variation of internal timing is different for each DRAM. Therefore, even though the CS setup/hold time is appropriate for each DRAM, 4-tCK CS_n sampling window which may have different starting points could appear differently as shown in Figure 86. Host should train CS_n timing based on asserting every edge of CS_n to cover multiple DRAMs without exiting CSTM.

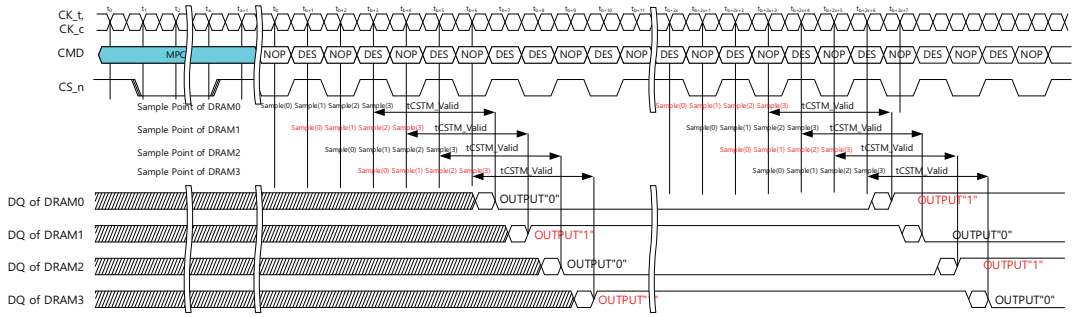


Figure 86 — Timing Diagram for CS Training Mode with Multiple DRAMs Output Sample Toggle

Note 1 - See MPC Command for details on Setup, Hold and command register time.

Table 103 — AC parameters for CS Training Mode

Symbol	Description	Min	Max	Unit	Note
tCSTM_Entry	Registration of CSTM entry command to start of training samples time	20	-	ns	
tCSTM_Min_to_MPC_exit	Min time between last CS_n pulse and first pulse of MPC Command to exit CSTM	4	-	nCK	
tCSTM_Exit	Registration of CSTM exit command to end of training mode	-	20	ns	
tCSTM_Valid	Time from sample evaluation to output on DQ bus	-	20	ns	
tCSTM_DQ_Window	Time output is available on DQ Bus	2	-	nCK	1
tCSTM_Exit_Delay	Registration of CATM exit to next valid command delay	20	-	ns	

Note(s):
1. This timing parameter is applied to each DQ independently, not all-DQs valid window perspective.

4.20.3.1 Output signals

The following table shows which signals will transmit the output of the CS Training Mode loopback sample evaluation. These values are driven asynchronously, but may switch as often as every 4tCK.

Table 104 — CS Sampled Output per Interface Width

Output	X16	X8	X4
DQ0	CSTM Output	CSTM Output	CSTM Output
DQ1	CSTM Output	CSTM Output	CSTM Output
DQ2	CSTM Output	CSTM Output	CSTM Output
DQ3	CSTM Output	CSTM Output	CSTM Output
DQ4	CSTM Output	CSTM Output	
DQ5	CSTM Output	CSTM Output	
DQ6	CSTM Output	CSTM Output	
DQ7	CSTM Output	CSTM Output	
DML			
TDQS_c			
DQSL_t			
DQSL_c			
DQ8	CSTM Output		
DQ9	CSTM Output		
DQ10	CSTM Output		
DQ11	CSTM Output		
DQ12	CSTM Output		
DQ13	CSTM Output		
DQ14	CSTM Output		
DQ15	CSTM Output		
DMU			
DQSU_t			
DQSU_c			

4.21 Write Leveling Training Mode

4.21.1 Introduction

The DDR5 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the memory controller to set the timings of the WRITE DQS signaling according to the Write Latency timing specification at the DRAM. Therefore, the DDR5 SDRAM supports a 'write leveling' feature to allow the controller to compensate for channel skew. The DDR5 Write Leveling Training also allows for an unmatched path between CK and DQS within the DRAM, and thus supports an internal Write Leveling Training flow to account for the difference in internal delays.

The DDR5 DRAM also provides a programmable timing in its write logic, controlled by the Write Leveling Internal Cycle Alignment (WICA) mode register (MR3), which provides a means for improved performance of the device's receiver. The proper setting of this register shall be determined by the memory controller, either as described in the sections below, or by some other means. This delay setting is specific to each DRAM, its Write Preamble setting, and the operating frequency being used. Once the proper setting has been determined for a given WICA byte, Write preamble setting, and operating frequency, that setting may be subsequently restored to the DRAM after reset, power-cycle, or return to a previously used operating frequency.

The memory controller can use the 'write leveling' feature and feedback from the DDR5 DRAM to adjust the controller's differential DQS (DQS_t - DQS_c) output delay to align to the phase and cycle that corresponds to the CAS Write Latency (CWL) delay after the WRITE command. The memory controller involved in the leveling must have an adjustable delay setting on the DQS pins to align the rising edge of differential DQS with the timing at the receiver that is the pin-level Write Latency (External Write Leveling Training), and to align DQS with the internal DRAM Write Latency timing point (Write Leveling Internal Cycle Alignment). The internal DRAM Write Latency timing point may be skewed from the pin-level Write Latency timing point. The host will minimize this skew (tDQSoffset) through the Write Leveling Training flow.

Since the system and DIMM delays vary, the DRAM will support the ability for the host to align the DQS timings with a pin-level Write Latency differential CK (CK_t-CK_c) edge. This alignment is referred to as External Write Leveling. Once the DQS host timings are aligned at the DRAM Write Latency timing, the internal DRAM timings are optimized for lowest power and internal delay. This is accomplished when the host enables the Internal Write Timing setting in MR2. In order to compensate for the difference in delay, the host will execute an Internal Write Leveling Training sequence, which includes sweeping the Write Leveling Internal Cycle Alignment (WICA) settings in MR3 (Write Leveling Internal Cycle Alignment Operation) and then finalizing the differential DQS phase and offset (Write Leveling Internal Phase Alignment and Final Host DQS Timing Operation).

During Write Leveling Training (both External and Internal), the DQS pattern shall include the full programmed write preamble and only the first toggle of the normal data burst sequence. The DRAM will sample the Internal Write Leveling Pulse relative to the first DQS toggle of the data burst sequence (last rising differential DQS edge sent by the host) and asynchronously feed back the result of this sample on the DQ bus, transitioning between tWLOmin and tWLOmax. If the DQ bus output is LOW at tWLOmax, the Internal Write Leveling Pulse signal was sampled while it was deasserted (LOW). Likewise, if the DQ bus output is HIGH at tWLOmax, the Internal Write Leveling Pulse signal was sampled while it was asserted (HIGH). The sampled feedback state will remain on the DQ bus until a subsequent Write Leveling sample changes the state, or until Write Leveling Training is exited.

The Internal Write Leveling Pulse is generated in response to a WRITE command, and held statically low otherwise. To perform the Write Leveling training, the controller repeatedly sends a WRITE command, delays DQS, and monitors the DQ feedback after tWLOmax until a transition from 0 to 1 is detected, indicating alignment with the Internal Write Leveling Pulse.

During Internal Write Leveling Training flows, the host will apply an offset to the starting point or the final setting of the DQS-signals. The offsets are referred to as WL_ADJ_start and WL_ADJ_end. This will minimize the tDQSoffset variation across different DRAM devices. The WL_ADJ_start and WL_ADJ_end values depend on the tWPRE setting.

When External and Internal Write Leveling Training flows are complete and the final WL_ADJ_end offset has been applied to the DQS timings, the DQS is phase aligned and cycle aligned for write operations. During the training sequence the DRAM in Write Leveling training mode will apply ODT to the strobes in the same way as for functional operation. All non-target ranks (which will not be in Write Leveling Training Mode) will apply ODT as defined for functional operation. Prior to executing the DDR5 Write Leveling Training Flow, the DRAM tWPRE value must be configured to the functional operation setting.

Note: DQS ODT is based on a DQS PARK Mode and is not enabled and disabled with DQ ODT timings.

4.21.2 Write Leveling Mode Registers

The MR fields for Write Leveling Training, Internal Write Timing, and Write Leveling Internal Cycle Alignment are part of MR2 and MR3. To enter Write Leveling Training Mode, the controller shall program MR2:OP[1]=1. Likewise, to exit ~~the~~ Write Leveling Training Mode, the controller will program MR2:OP[1]=0. Write Leveling Internal ~~e~~Cycle ~~a~~Alignment offers two nibbles to control the upper and lower DQ bytes. The lower byte WL internal Cycle alignment is intended for x4, x8 and x16 configurations, while the upper byte is only for x16 configurations.The Internal Write Timing, once enabled (MR2:OP[7]=1), shall remain enabled through the Internal Write Leveling Training flow and for functional operation. The host is responsible for incrementing the Write Leveling Internal Cycle Alignment setting until the Internal Write Leveling Pulse is pulled early enough to align with the differential DQS_~~t~~ ~~DQS_c~~ signal~~s~~ that ~~were~~ was previously aligned with the pin-level Write Latency timing. The Write Leveling Internal Cycle Alignment setting only applies when the Internal Write Timing is enabled.

Only BL16 Mode is supported in Write Leveling Training Mode.

4.21.3 External Write Leveling Training Operation

When Write Leveling Mode is enabled (MR2:OP[1]=1) and the Internal Write Timing is disabled (MR2:OP[7]=0), the DRAM will have an Internal Write Leveling pulse that indicates how the DQS signals shall be aligned to match the pin-level Write Latency timings. The rising edge of the Internal Write Leveling Pulse will align to the rising edge of the differential CK signal that coincides with CAS Write Latency (CWL), as shown in the following diagrams.

The differential DQS signals driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits shall carry the leveling feedback to the controller across the DRAM configurations x4, x8, and x16. On a x16 device, both byte lanes shall be leveled independently. Therefore, a separate feedback mechanism shall be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to Internal Write Leveling Pulse relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to Internal Write Leveling Pulse relationship. When training a x16 device, the data bits of a byte will remain in the “don’t care” state until its applicable DQS signals are toggled. Once the DQS signals are toggled, the DQs will follow the behavior previously described.

The following diagram shows the timing sequence to enter Write Leveling Training Mode, operation during Write Leveling Training Mode (with Internal Write Timings disabled), and the timing sequence to exit Write Leveling Training mode. An MRW command is sent to enable Write Leveling Training Mode. Prior to sending the MRW command to enable Write Leveling Training Mode, the host memory controller must drive the DQS signals differentially low. After tWLPEN time, the controller can send a WRITE command, followed by strobe pulses. The DQS signals shall always drive differentially low, except during the WRITE preamble and burst strobe sequence . There is no restriction as to how early the strobe pulses are sent, so long as they are no earlier than CWL/2 after the WRITE command. The DRAM will sample the Internal Write Leveling Pulse relative to the first DQS toggle of the data burst sequence and asynchronously feed back the result of this sample on the DQ bus, transitioning between tWLOmin and tWLOmax.

While in Write Leveling Training mode, the host controller may send ACT and PRE commands. The DRAM will ignore these commands. The address associated with the ACT and the WRITE commands may be any value. The following timing diagrams demonstrate the timing requirements associated with Write Leveling Training Mode Entry, the Internal Write Leveling Pulse alignment during External Write Leveling Training, and the DQ sample feedback timing.

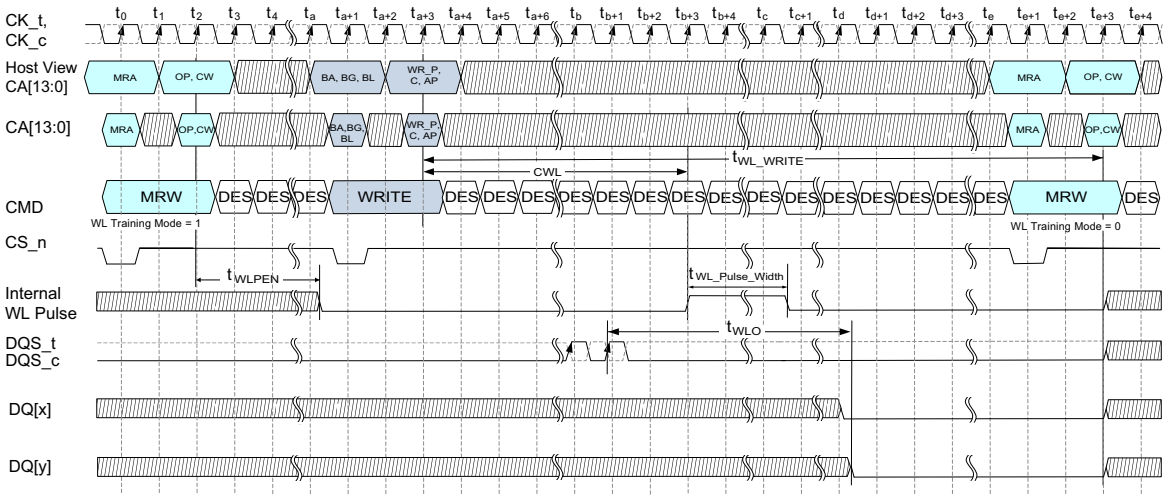


Figure 87 — Write Leveling Training Mode Timing Diagram (External Training, 2N Mode, 0 Sample)

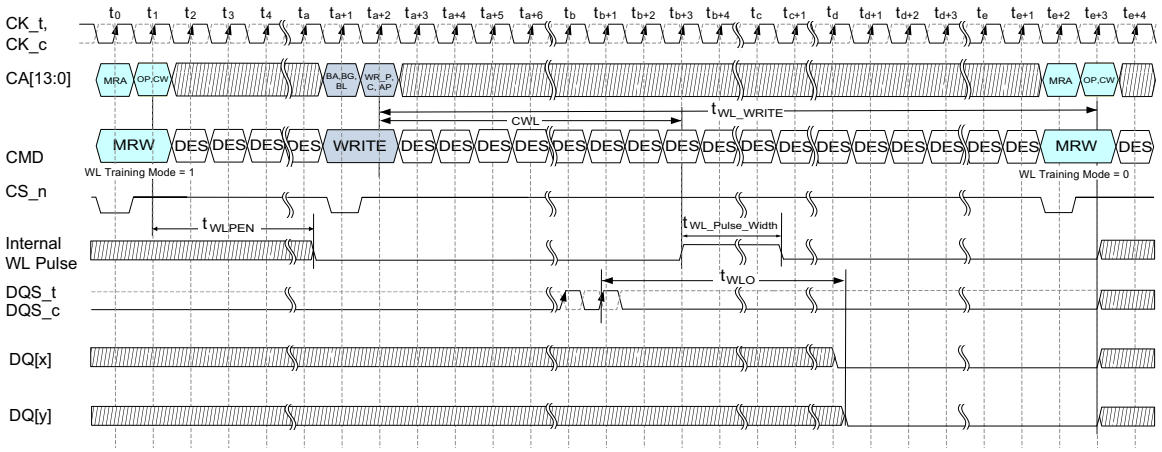


Figure 88 — Write Leveling Training Mode Timing Diagram (External Training, 1N Mode, 0 Sample)

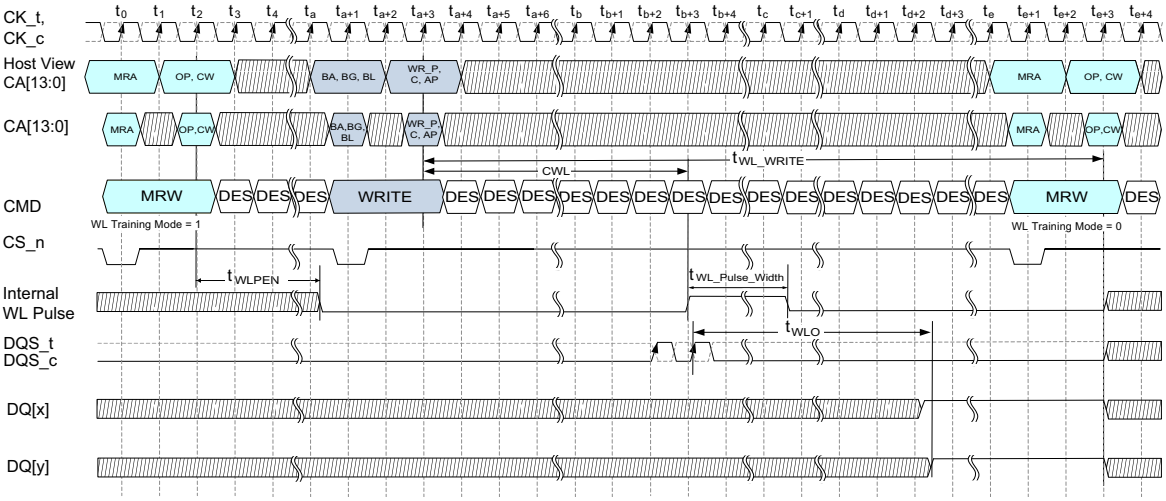


Figure 89 — Write Leveling Training Mode Timing Diagram (External Training, 2N Mode, 1 Sample)

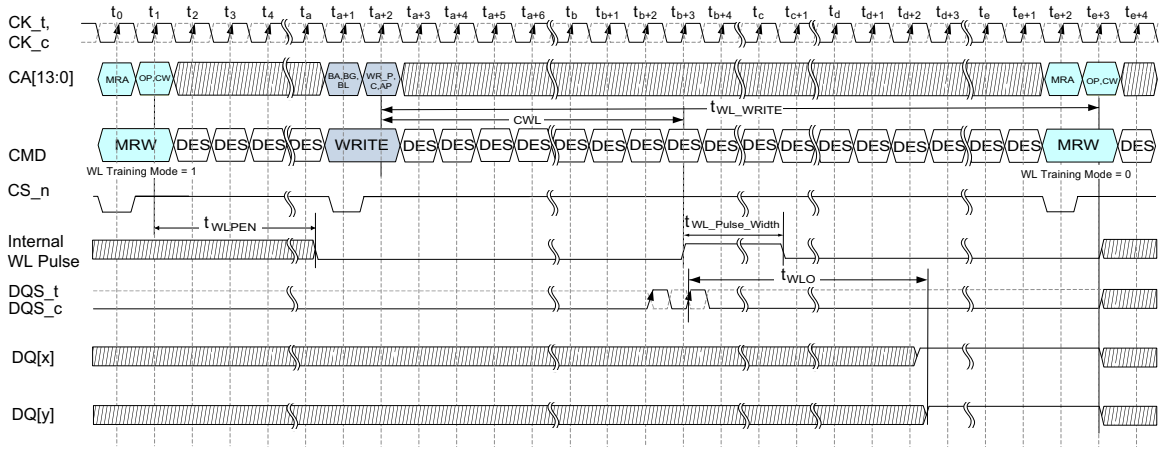


Figure 90 — Write Leveling Training Mode Timing Diagram (External Training, 1N Mode, 1 Sample)

The Memory controller initiates Write Leveling mode of all DRAMs in a rank by setting MR2:OP[1]=1. When entering write leveling mode, the DQ pins are in undefined driving mode. Since the controller levels one rank at a time, all non-target ranks will set Write Leveling Mode to disabled. The Controller may assert non-target ODT through the normal WRITE command protocol. DQS_RT-T_PARK termination will apply to the DQS_t and DQS_c signals.

The Controller shall drive DQS differentially LOW prior to sending the MRW command to enable Write Leveling Training Mode. The WRITE command must occur after a delay of tWLPEN relative to when the MRW enabled Write Leveling Training Mode.

The DRAM will sample the Internal Write Leveling Pulse and asynchronously feed back the result of this sample on the DQ bus, transitioning between tWLOmin and tWLOmax. The controller can sample the state of any DQ bit after tWLOmax. Based on the sampled state, the controller decides to increment or decrement the DQS delay setting and launches the next WRITE command with associated DQS_t/DQS_c pulse (or pulse sequence) after some time, which is controller dependent. Once a 0 to 1 transition on the DQ bus is detected, the controller locks DQS delay setting and external write leveling is achieved for the device.

Write Leveling Training may be executed by issuing consecutive Write commands after entering Write Leveling Mode has been enabled (no requirement to exit and reenter between each Write command). The minimum Write to Write command spacing during Write Leveling Mode is tWL_Write and is defined as “max(CWL, last DQS differential toggle) + tWLO(max)+ 2nCK”. An example of consecutive Write commands given during Write Leveling Training is shown in Figure 91:

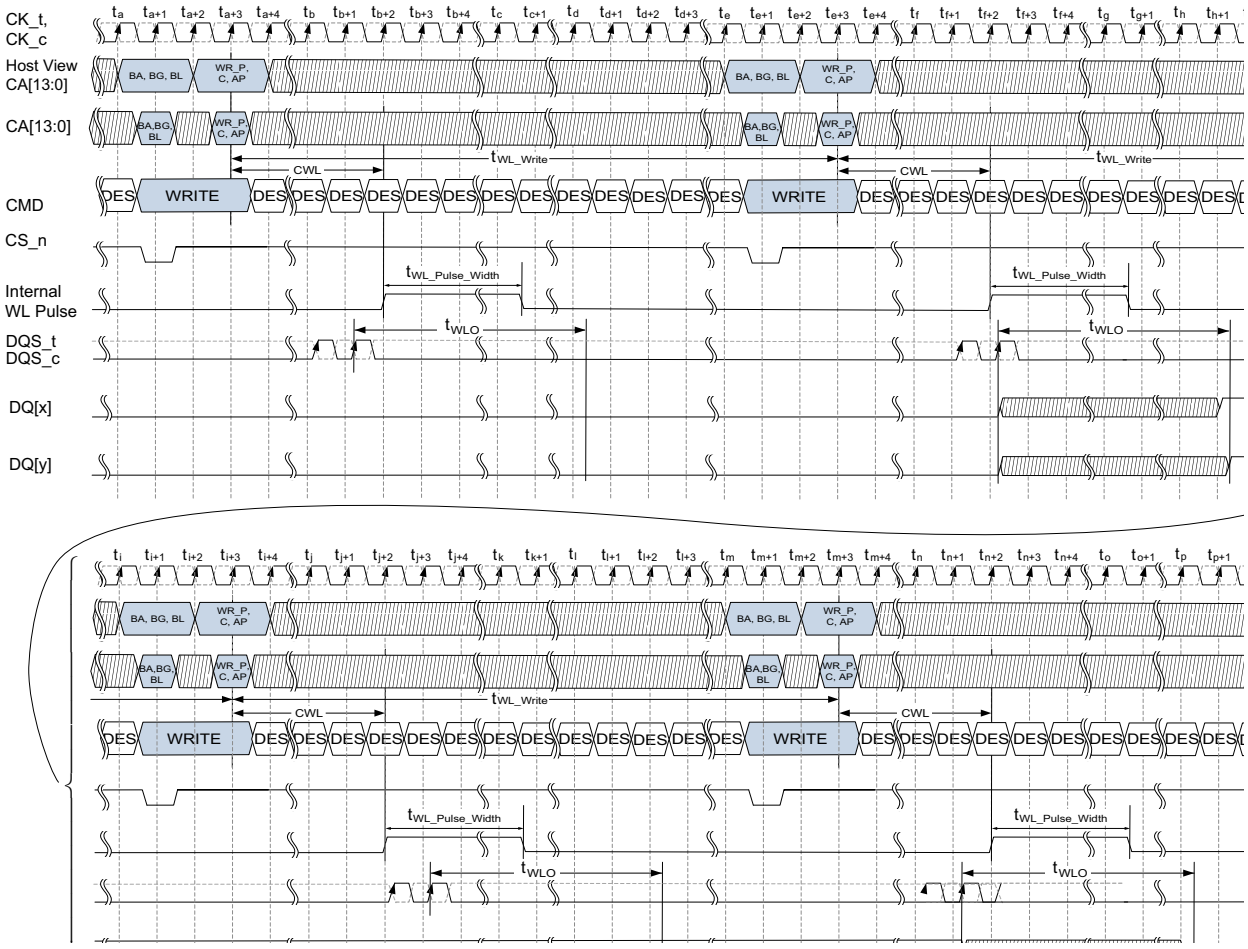


Figure 91 — Consecutive Write commands during Write Leveling Training Mode Example (External Training, 2N Mode, 4 Samples)

4.21.4 Write Leveling Internal Cycle Alignment Operation

After the external Write Leveling Training step is completed, and after the host DQS signals have been aligned to the pin-level Write Latency timing, the host will apply a negative offset (WL_ADJ_start) to the DQS timing. The WL_ADJ_start offset moves the DQS timing prior to the Internal Write Leveling Pulse (causing LOW observed on the DQ pins), and it is dependent on the tWPRE setting (shown in table below). This will be a reference point for aligning the Internal Write Leveling Pulse via the WICA settings in MR3.

The Internal Cycle Alignment training begins when an MRW command is issued to enable Internal Write Timing in MR2 (keeping OP[1]=1 and setting MR2:OP[7]=1). The host sweeps the Write Leveling Internal Cycle Alignment (WICA) delay settings in MR3, starting with the 0tCK offset default. Increasing the WICA mode register offset setting speeds up the timing of the WRITE command by reducing the WRITE Command to Internal Write Pulse delay until the DQS is aligned with the internal Write Leveling Pulse assertion. Alignment results in a logic HIGH on the DQ pins.

The following table summarizes the WL_ADJ_start and WL_ADJ_end values per tWPRE setting:

WL_ADJ term	Description	tWPRE = 2 tCK	tWPRE = 3 tCK	tWPRE = 4 tCK[1]
WL_ADJ_start	Offset that the host applies to the DQS_t/ DQS_c timing just after external Write Leveling alignment to Write Latency and prior the internal cycle alignment training.	-0.75 tCK	-1.25 tCK	-2.25 tCK
WL_ADJ_end	Offset that the host applies to the DQS_t/ DQS_c timing after final phase alignment to the rising edge of the Write Leveling Internal Pulse. This will center the Write Leveling Internal Pulse rising edge within the preamble window.	1.25 tCK	1.75 tCK	2.75 tCK

Note 1: For tWPRE = 4 tCK, CL is required to be ≥ 30 during Write Leveling Training Mode operation. This is irrespective of the CL setting for tWPRE = 4 tCK during normal operation.

Due to potential measurement errors that can occur during the internal Write Leveling Training, the DRAM may include an optional 0.5 tCK adjustment for optimizing the Internal Cycle Alignment. MR7:OP[0]=1 adds a +0.5 tCK adjustment for the lower byte of the DQs, while MR7:OP[1]=1, adds a +0.5 tCK adjustment for the upper byte of the DQs.

Figure 92 is an example of an Internal Write Leveling training flow with the addition of the +0.5tCK WICA adjustment (additional flow shown in blue).

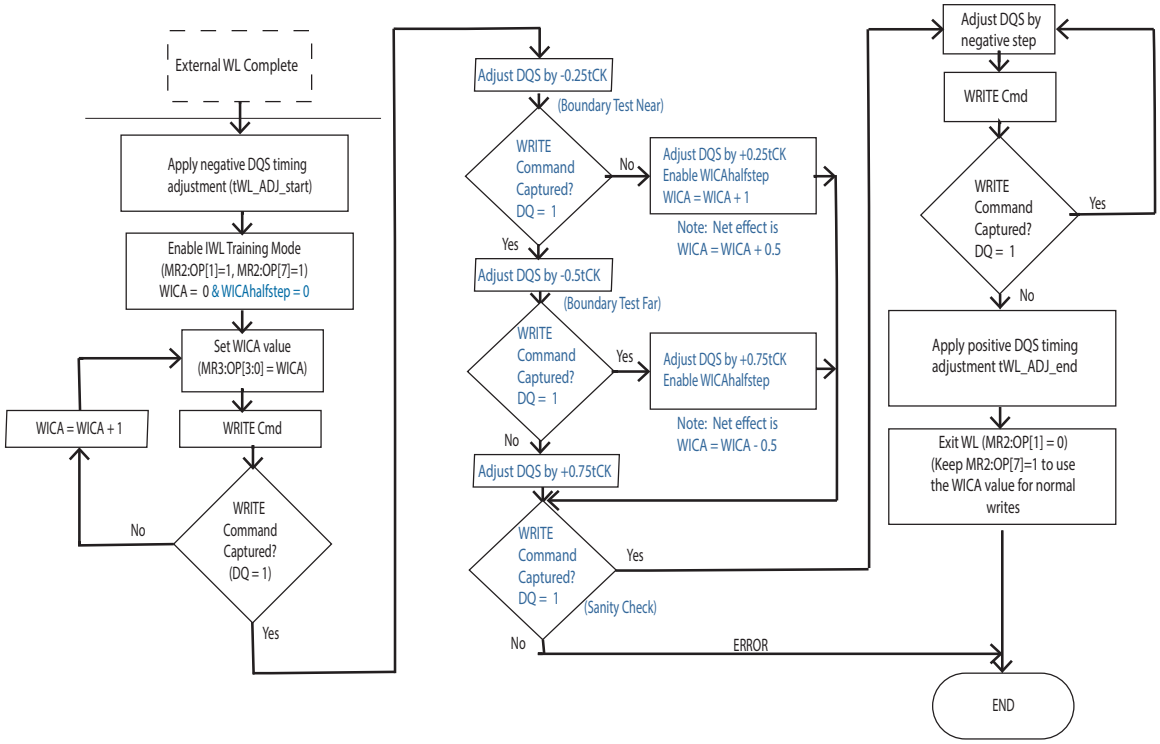


Figure 92 — Write Leveling Training Flow with half step WICA

As previously noted, the DDR5 x16 devices allow for independent lower and upper byte Write Leveling Training and setting.Although unique values are preferred to optimize (minimize) tDQSoffset, setting both the lower and upper bytes to use the same WICA offset is allowed since the internal paths for both bytes are expected to be closely matched, meaning Internal Write Leveling Training that results in a differentbyte settings per byte indicates the internal paths are on a boundary between the two settings.When choosing a common WICA offset value, the startingvalues of the lower and upper WICA offset should differ by no more than one. The higher (smallest absolute value since the WICA values apply a negative offset) of the two values shall be programmed in both bytes of the DRAM to minimize the impact on the final training sweep.

Lower Byte WICA	Upper Byte WICA	Common WICA
-4	-3	-3
-2	-3	-2

When choosing a common 0.5tCK WICA offset value, the WICA value programmed in both bytes of the DRAM shall be the same beforeapplying the 0.5tCK offset (if the byte values are different, the higher value shall be programmed in both bytes of the DRAM as noted above and the 0.5tCK offset step is skipped). If the 0.5tCK training indicates that one byte requires the +0.5tCK offset but the other byte does not, this also indicates the two bytes are on a boundary between the two settings. In this case, the +0.5tCK shall be applied to both bytes, resulting inthe higher (smallest absolute) value being used.

Lower Byte WICA	Lower Byte +0.5tCK WICA	Upper Byte WICA	Upper Byte +0.5tCK WICA	Common WICA
-4	n/a	-3	n/a	-3
-4	Yes	-4	No	-4+0.5 (-3.5 total)
-3	No	-3	Yes	-3+0.5 (-2.5 total)

When using a common WICA offset value approach to the Internal Write Leveling training, both bytes shall do the final training sweep after applying the common WICA offset value (both the full cycle and 0.5tCK WICA, if applicable).

The following two timing diagrams demonstrates Write Leveling Training operation when Internal Write Timings are enabled and the Internal Cycle Alignment is set such that the Internal Write Leveling Pulse has not yet reached the host DQS toggles.

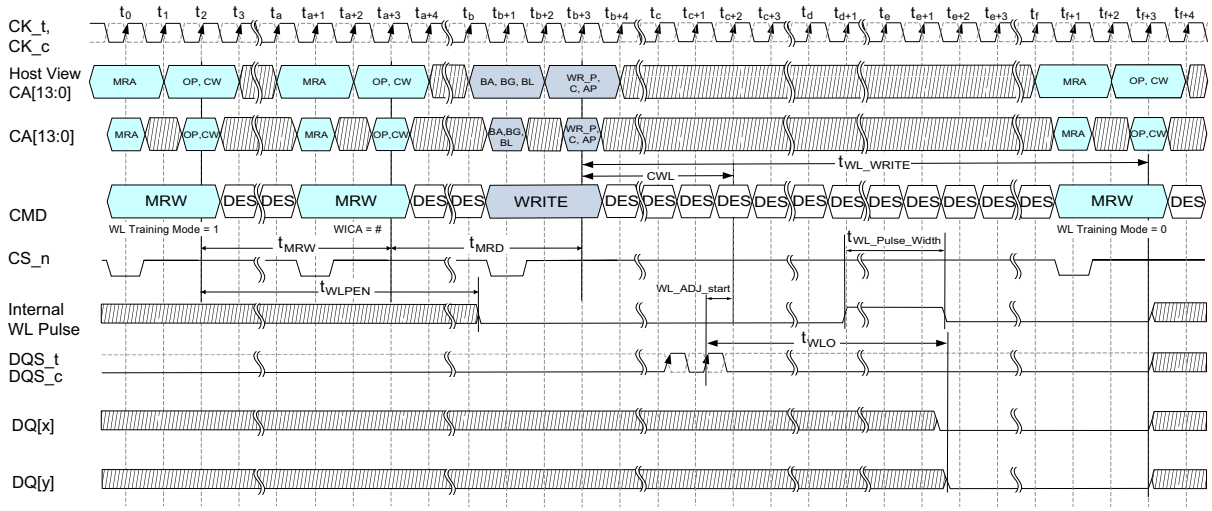


Figure 93 — Write Leveling Training Mode Timing Diagram (Internal Cycle Alignment, 2N Mode, 0 Sample)

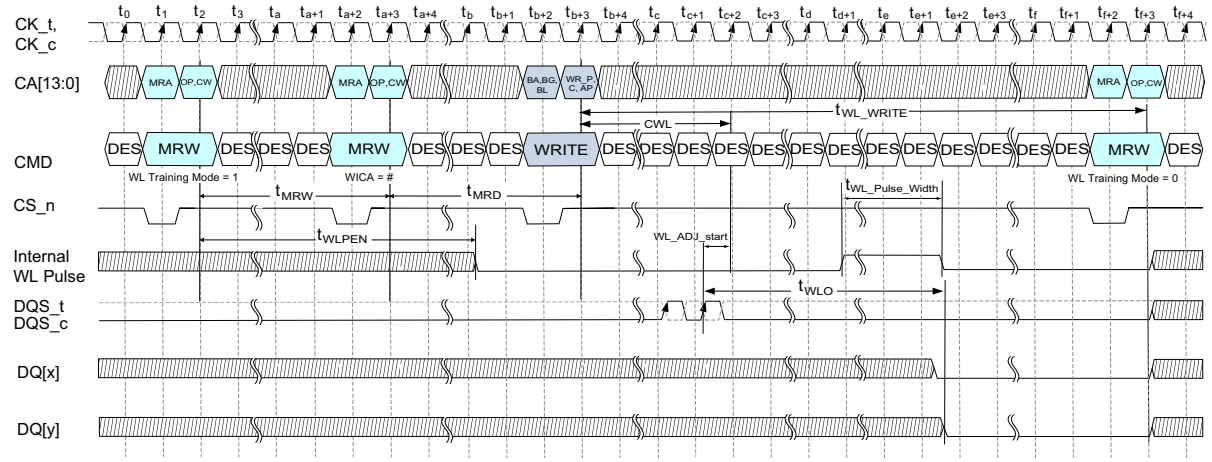


Figure 94 — Write Leveling Training Mode Timing Diagram (Internal Cycle Alignment, 1N Mode, 0 Sample)

The following two timing diagrams demonstrate Write Leveling Training operation when Internal Write Timings are enabled and the Internal Cycle Alignment is set such that the Internal Write Leveling Pulse has completed the coarse alignment to the host DQS timing.

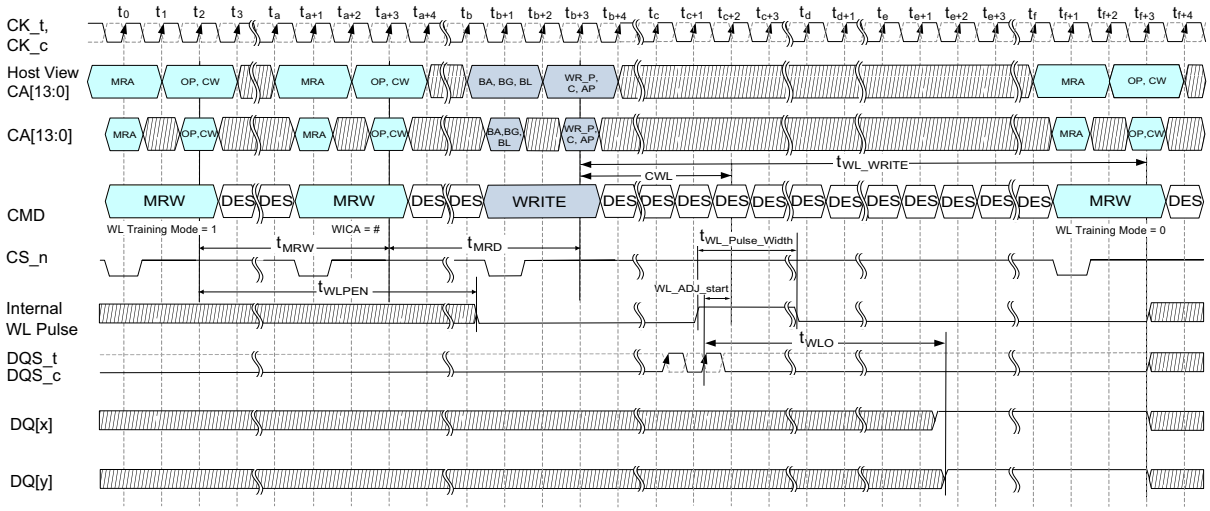


Figure 95 — Write Leveling Training Mode Timing Diagram (Internal Cycle Alignment, 2N Mode, 1 Sample)

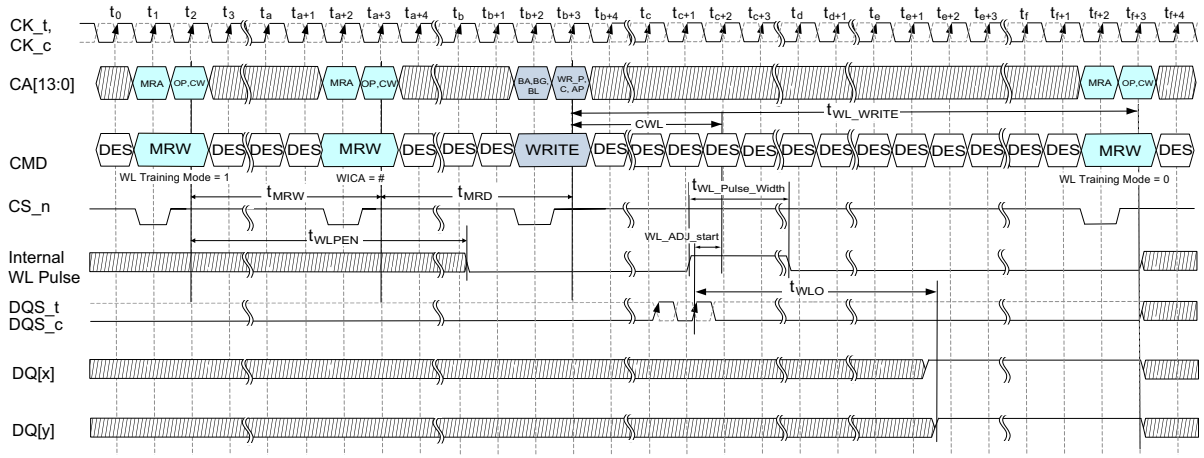


Figure 96 — Write Leveling Training Mode Timing Diagram (Internal Cycle Alignment, 1N Mode, 1 Sample)

An example of Write Leveling Training internal Cycle Alignment executed by issuing consecutive Write commands after entering Write Leveling Mode has been enabled (no requirement to exit and reenter between each Write command) is shown in Figure 97:

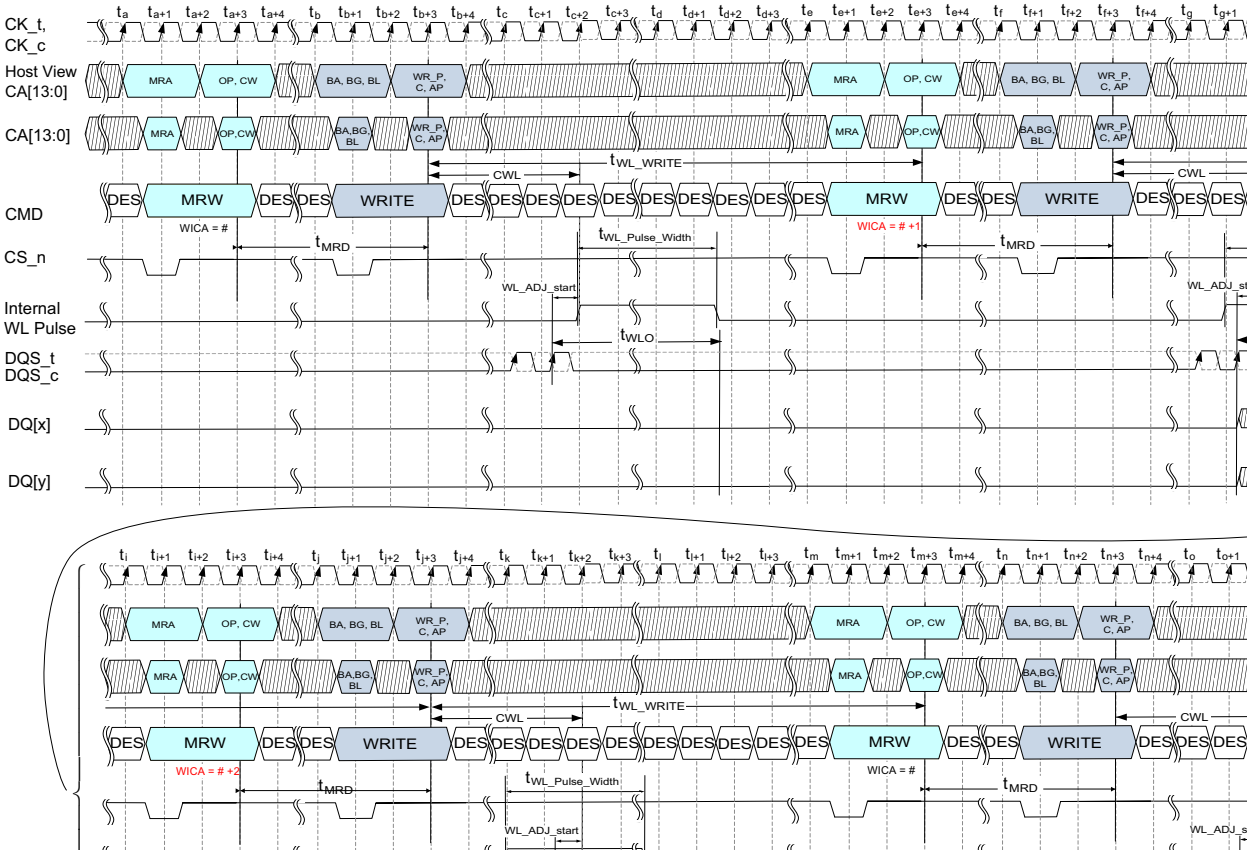


Figure 97 — Consecutive Write commands during Write Leveling Training Mode Example (Internal Training, 2N Mode, 4 Samples)

4.21.5 Write Leveling Internal Phase Alignment and Final Host DQS Timing Operation

Once the Internal Cycle Alignment is achieved, the host shall perform a final fine sweep of the DQS timings with Internal Write Timing enabled (MR2:OP[7]=1) to ~~determine~~ establish an even closer phase alignment to the rising edge of the internal Write Leveling Pulse. Once this is complete, the host will then add a positive offset of WL_ADJ_end (dependent upon tWPRE) to the DQS timings. This results in a tDQSoffset between -0.5tCK and +0.5tCK with measurement adjustments of tWLS/tWLH, placing the rising edge of the Internal Write Leveling Pulse within the preamble. If the optional half step WICA process is used during Write Leveling training, this results in a tDQSoffset between -0.25tCk and +0.25tCK with measurement adjustments of tWLS/tWLH. After the WL_ADJ_end offset has been applied, the host will disable Write Leveling Training Mode (MR2:OP[1]=0). The Internal Write Timing will remain enabled and the Internal Cycle Alignment setting will retain the coarse setting that was trained. After every reset, the host must either restore these settings or execute the full Write Leveling Training flow.

The following figure shows the timing relationships for the final placement of the host DQS-timings relative to the Internal Write Leveling Pulse. However, it is not necessary to execute this Write Leveling Training Mode Measurement to finalize the setting - this is only for illustration.

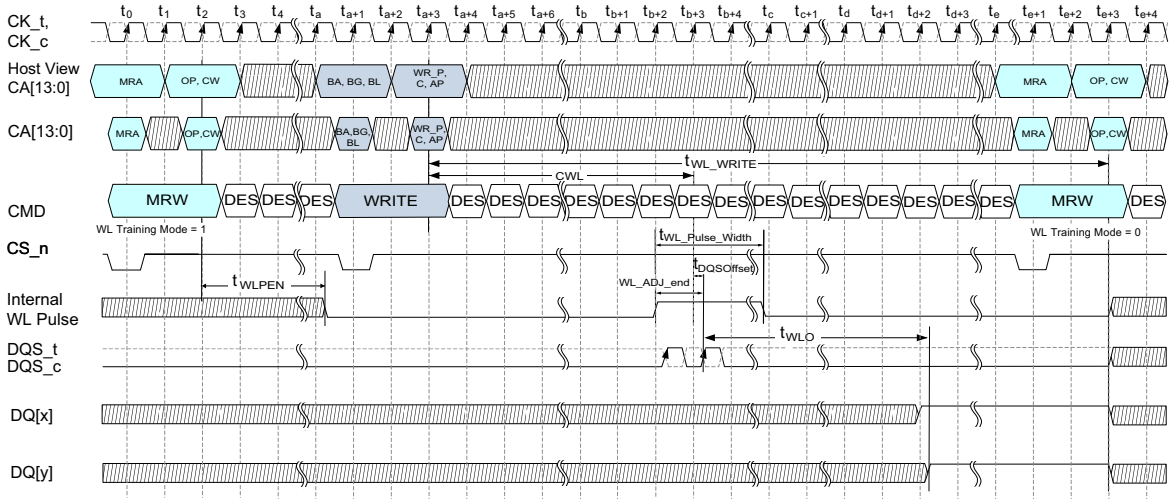


Figure 98 — Timing Diagram for final timings after Write Leveling Training is complete (2N Mode)

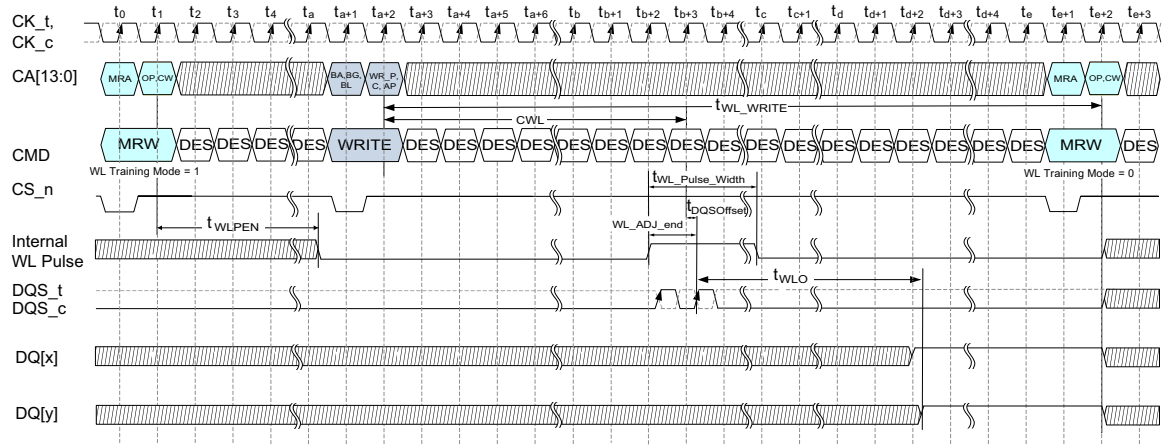


Figure 99 — Timing Diagram for final timings after Write Leveling Training is complete (1N Mode)

The following table summarizes the timing parameter ranges associated with Write Leveling Training Mode:

Parameter	Symbol	Min	Max	Units	NOTE
Write Leveling Pulse Enable - Time from Write Leveling Training Enable MRW to when Internal Write Leveling Pulse logic level is valid	tWLPEN	-	15	ns	
Write leveling output	tWLO	-	9.5	ns	
Width of the Write Leveling Internal Pulse	tWL_Pulse_Width	2	-	tCK	1
Write Leveling Write to subsequent command spacing	tWL_Write	max(CWL, last DQS differential toggle) + tWLO(max)+ 2nCK	-		

Notes:
1. There is no Max limit for the tWL_Pulse_Width, but the Write Leveling Internal Pulse must begin at zero for each WRITE command.

4.21.6 DRAM Termination During Write Leveling

When the DRAM is in Write Leveling Mode, the DQS_c/DQS_t termination (DQS_RTT_PARK) and the Command and Control termination (RTT_CA, RTT_CK, RTT_CS) will be the same as for functional operation. The DQ signals will not be terminated in the DRAM, but instead will be driving values to the controller. The host controller will apply termination for the DQ signals.

ODT Enabled	DQS_t/DQS_c Termination	DQ Termination
RTT_WR	DQS_RTT_PARK	Off
RTT_PARK, RTT_WR disabled	DQS_RTT_PARK	Off

Note: Termination for TDQS/DM is not included since TDQS and DM are disabled during Write Leveling Training Mode.

4.22 Connectivity Test (CT) Mode

4.22.1 Introduction

The DDR5 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR5 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for **all** DRAM devices independent of density and interface width. This applies to x4, x8, and x16 interface widths. Contrary to other conventional shift register based test modes, where test patterns are shifted in and out of the memory devices serially in each clock, DDR5's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR5 memory device at the same time, significantly enhancing the speed of the connectivity check.

Prior to entering CT Mode, RESET_n is registered to High. The CT Mode is enabled by asserting the Test Enable (TEN) pin.

Once put in the CT mode by asserting the TEN pin, the DDR5 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay. A reset of the DDR5 memory device is required after exiting the CT mode.

4.22.2 Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the DDR5 memory device are classified as one of the following types:

1. Test Enable (TEN) pin: when asserted high, this pin causes the DDR5 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR5 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent. The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.
2. Chip Select (CS_n) pin: when asserted low, this pin enables the test output pins in the DDR5 memory device. When de-asserted, the output pins in the DDR5 memory device will be Hi-z. The CS_n pin in the DDR5 memory device serves as the CS_n pin when in CT mode.
3. Test Input: a group of pins that are used during normal DDR5 DRAM operation are designated as test input pins. These pins are used to enter the test pattern in CT mode. Most Test Input pins are input pins during normal operation. The ALERT_n pin is the only output pin that will be used as a Test Input during CT mode. The CK_t and CK_c pins are single-ended Test Input pins during CT Mode.
4. Test Output: a group of pins that are used during normal DDR5 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.
5. Reset: Fixed high level for RESET_n is required during CT mode, same as normal function.

Table 105 below shows the pin classification of the DDR5 memory device.

Table 105 — Pin Classification of DDR5 Memory Device in Connectivity Test(CT) Mode

Pin Type in CT Mode		Pin Names during Normal Memory Operation
Test Enable		TEN
Chip Select		CS_n
Test Inputs	A	CA[13:0]
	B	CK_t, CK_c
	C	ALERT_n
Test Outputs		DQL[7:0], DQU[7:0], DQSU_t, DQSU_c, DQSL_t, DQSL_c, DML_n, DMU_n, DM_n/TDQS_t, TDQS_c
Reset		RESET_n

NOTE: Test Outputs may contain the Upper and Lower label identification used with x16 devices. In the case of x4/x8 devices, the lower (L) identification may be removed.
NOTE2. CAI and MIR input level do not affect to "Test Outputs" values.

Table 106 — Signal Description

Symbol	Type	Function
TEN	Input	Connectivity Test Mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation TEN is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDDQ.

4.22.3 Logic Equations

4.22.3.1 Min Term Equations

MTx is an internal signal to be used to generate the signal to drive the output signals. These internal signals are the same across all interface widths and densities.

Table 107 — Min Term Equations

Min Term	Intermediate Logic Nodes
MT0	XOR(CA[0,1,2,3,8,9,10,11])
MT1	XOR(CA[0,4,5,6,8,12,13], ALERT_n)
MT2	XOR(CA[1,4,9,12], CK_t, CK_c)
MT3	XOR(CA[2,5,7,10,13], CK_t)
MT4	XOR(CA[3,6,7,11], CK_c, ALERT_n)
MT0_B	!(MT0)
MT1_B	!(MT1)
MT2_B	!(MT2)
MT3_B	!(MT3)
MT4_B	!(MT4)

4.22.3.2 Output equations

Table 108 — Output Equations per Interface Width

Output	X16	X8	X4
DQL0	MT0	MT0	MT0
DQL1	MT1	MT1	MT1
DQL2	MT2	MT2	MT2
DQL3	MT3	MT3	MT3
DQL4	MT0_B	MT0_B	
DQL5	MT1_B	MT1_B	
DQL6	MT2_B	MT2_B	
DQL7	MT3_B	MT3_B	
DML	MT4	MT4	
TDQS_c		MT4_B	
DQSL_t	MT4	MT4	MT4
DQSL_c	MT4_B	MT4_B	MT4_B
DQU0	MT0		
DQU1	MT1		
DQU2	MT2		
DQU3	MT3		
DQU4	MT0_B		
DQU5	MT1_B		
DQU6	MT2_B		
DQU7	MT3_B		
DMU	MT4		
DQSU_t	MT4		
DQSU_c	MT4_B		

NOTE: Test Outputs may contain the Upper and Lower label identification used with x16 devices. In the case of x4/x8 devices, the lower (L) identification may be removed.

4.23 ZQ Calibration Commands

4.23.1 ZQ Calibration Description

The MPC command is used to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation.

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the SDRAM's calibration procedure, and ZQCal Latch captures the result and loads it into the SDRAM's drivers.

A ZQCal Start command may be issued anytime the DDR5-SDRAM is in a state in which it can receive valid commands. There are two timing parameters associated with ZQ Calibration. tZQCAL is the time from when the ZQCal Start MPC command is sent to when the host can send the ZQCal Latch MPC command. tZQLAT is the time from when the ZQCal Latch MPC command is sent by the host to when the CA bus (and subsequently the DQ bus) can be used for normal operation. A ZQCal Latch Command may be issued anytime outside of power-down after tZQCAL has expired and all DQ bus operations have completed. The CA Bus must maintain a Deselect state during tZQLAT to allow CA ODT calibration settings to be updated.

After a ZQCal Start and until tZQCAL finishes, neither another ZQCal Start nor a ZQCal Latch is allowed.

Table 109 — ZQ Calibration timing Parameters

Parameter	Symbol	Min/Max	Value	Unit
ZQ Calibration Time	tZQCAL	MIN	1	us
ZQ Calibration Latch Time	tZQLAT	MIN	max(30ns,8nCK)	ns

4.23.2 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and VSS.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQCals don't overlap.

The total capacitive loading on the ZQ pin must not exceed the max external loading of 25pf with the addition of the device ZQ pincap (5pf) for a total capacitive loading of 30pf.

4.24 VrefCA Command

4.24.1 Introduction

The VrefCA setting must be set prior to training the CS_n and CA bus timings relative to CK. In order to accomplish this, DDR5-SDRAMs will support a single UI command specifically for setting the VrefCA setting. This avoids any timing and/or default VrefCA setting issues with sending a 2UI MRW command, by enabling the host to extend the setup and hold time for the CA signals. In addition, the VrefCA command will support multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the DRAM will capture the VrefCA command during at least one rising CK_t/CK_c edge.

Table 110 — VrefCA Command Definition

Function	Abbreviation	CS	CA Pins													NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
VrefCA Command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	L	V	21,22,23

4.24.2 VrefCA Command Timing

The following diagram illustrates a timing sequence example for the VrefCA command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK_t/CK_c. The host must ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK_t/CK_c transitions, but it will satisfy the setup/hold requirements relative to at least one CK_t/CK_c rising edge.

There is no separate mode that enables the multi-cycle CS_n assertion. This timing relationship can always be used by the host to send the VrefCA commands even after training has been completed for the interface. For the DRAM to latch the VrefCA command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state at least three cycles prior to CS_n transitioning from high to low, CS_n must remain low for tVrefCA_CS, and CA must remain in the proper command state for at least three cycles after CS_n transitions from low to high.

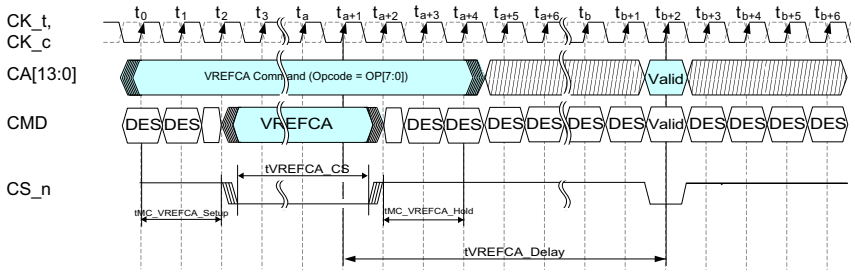


Figure 100 — Timing Diagram for VrefCA Command

Table 111 — AC parameters for VrefCA Command

Symbol	Description	Min	Max	Unit	Note
tVrefCA_Delay	VrefCA command to any other valid command delay	tMRD	-	nCK	
tVrefCA_CS	Time CS_n is held low to register VrefCA command	3.5	8	nCK	1,2
tMC_VREFCA_Setup	Min time between stable VREFCA command and first falling CS edge (SETUP)	3	-	nCK	3
tMC_VREFCA_Hold	Min time between first rising CS edge and stable VREFCA command (HOLD)	3	-	nCK	3

Note(s):
1 - Multiple cycles are used to avoid possible metastability of CS_n.
2 - At the end of CSTM, it is assumed that the host should be able to place the CS_n appropriately and the VrefCA command could be issued as a single cycle command.
3 - This applies only to Multi-Cycle VREFCA commands when MR2:OP[4]=0_B.

4.25 VrefCS Command

4.25.1 Introduction

The VrefCS setting should be set, if needed, prior to training the CS_n and CA bus timings relative to CK. In order to accomplish this, DDR5-SDRAMs will support a single UI command specifically for setting the VrefCS setting (similar to VrefCA). This avoids any timing and/or default VrefCS setting issues with sending a 2UI MRW command, by enabling the host to extend the setup and hold time for the CA signals. In addition, the VrefCS command will support multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the DRAM will capture the VrefCS command during at least one rising CK_t/CK_c edge.

NOTE: The operation, functionality and timings for VrefCS are effectively the same as VrefCA with the exception of a different explicit command noted below and the fact that it modifies the VREF of the chip select pin vs the CA pins.

Table 112 — VrefCS Command Definition

Function	Abbreviation	CS	CA Pins													NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
VrefCS Command	VrefCS	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	H	V	21,22,23

4.25.2 VrefCS Command Timing

The following diagram illustrates a timing sequence example for the VrefCS command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK_t/CK_c. The host must ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK_t/CK_c transitions, but it will satisfy the setup/hold requirements relative to at least one CK_t/CK_c rising edge.

There is no separate mode that enables the multi-cycle CS_n assertion. This timing relationship can always be used by the host to send the VrefCS commands even after training has been completed for the interface. For the DRAM to latch the VrefCS command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state at least three cycles prior to CS_n transitioning from high to low, CS_n must remain low for tVrefCS_CS, and CA must remain in the proper command state for at least three cycles after CS_n transitions from low to high.

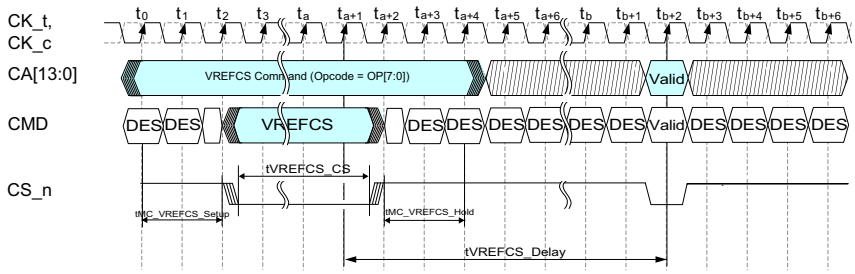


Figure 101 — Timing Diagram for VrefCS Command

Table 113 — AC parameters for VrefCS Command

Symbol	Description	Min	Max	Unit	Note
tVrefCS_Delay	VrefCS command to any other valid command delay	tMRD	-	nCK	
tVrefCS_CS	Time CS_n is held low to register VrefCS command	3.5	8	nCK	1,2
tMC_VREFCS_Setup	Min time between stable VREFCS command and first falling CS edge (SETUP)	3	-	nCK	3
tMC_VREFCS_Hold	Min time between first rising CS edge and stable VREFCS command (HOLD)	3	-	nCK	3

Note(s):
1 - Multiple cycles are used to avoid possible metastability of CS_n.
2 - At the end of CSTM, it is assumed that the host should be able to place the CS_n appropriately and the VrefCS command could be issued as a single cycle command.
3 - This applies only to Multi-Cycle VREFCS commands when MR2:OP[4]=0_B.

4.26 VrefCA Training Specification

The DRAM internal VrefCA specification parameters are voltage operating range, stepsize, VrefCA set tolerance, VrefCA step time and Vref valid level.

The voltage operating range specifies the minimum required VrefCA setting range for DDR5 DRAM devices. The minimum range is defined by VrefCAmax and VrefCAmin as depicted in Figure 102 below.

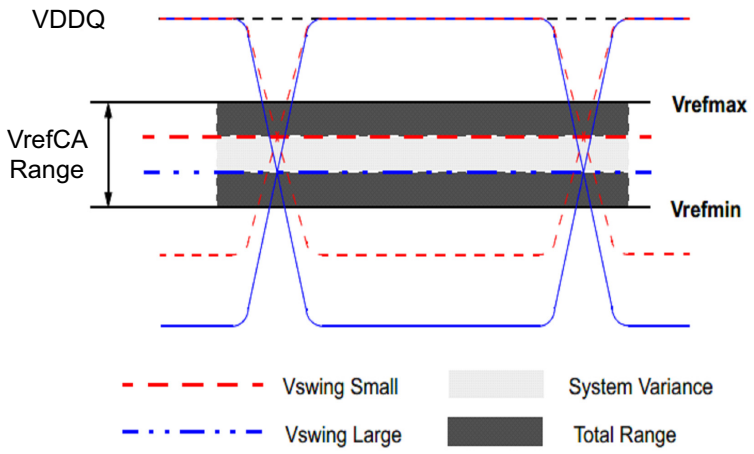


Figure 102 — VrefCA operating range(Vrefmin, Vrefmax)

The VrefCA stepsize is defined as the stepsize between adjacent steps. For a given design the DRAM VrefCA step size must be within the range specified.

The VrefCA set tolerance is the variation in the VrefCA voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VrefCA set tolerance uncertainty. The range of VrefCA set tolerance uncertainty is a function of number of steps n.

The VrefCA set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VrefCA values for a specified range. An illustration depicting an example of the stepsize and VrefCA set tolerance is below.

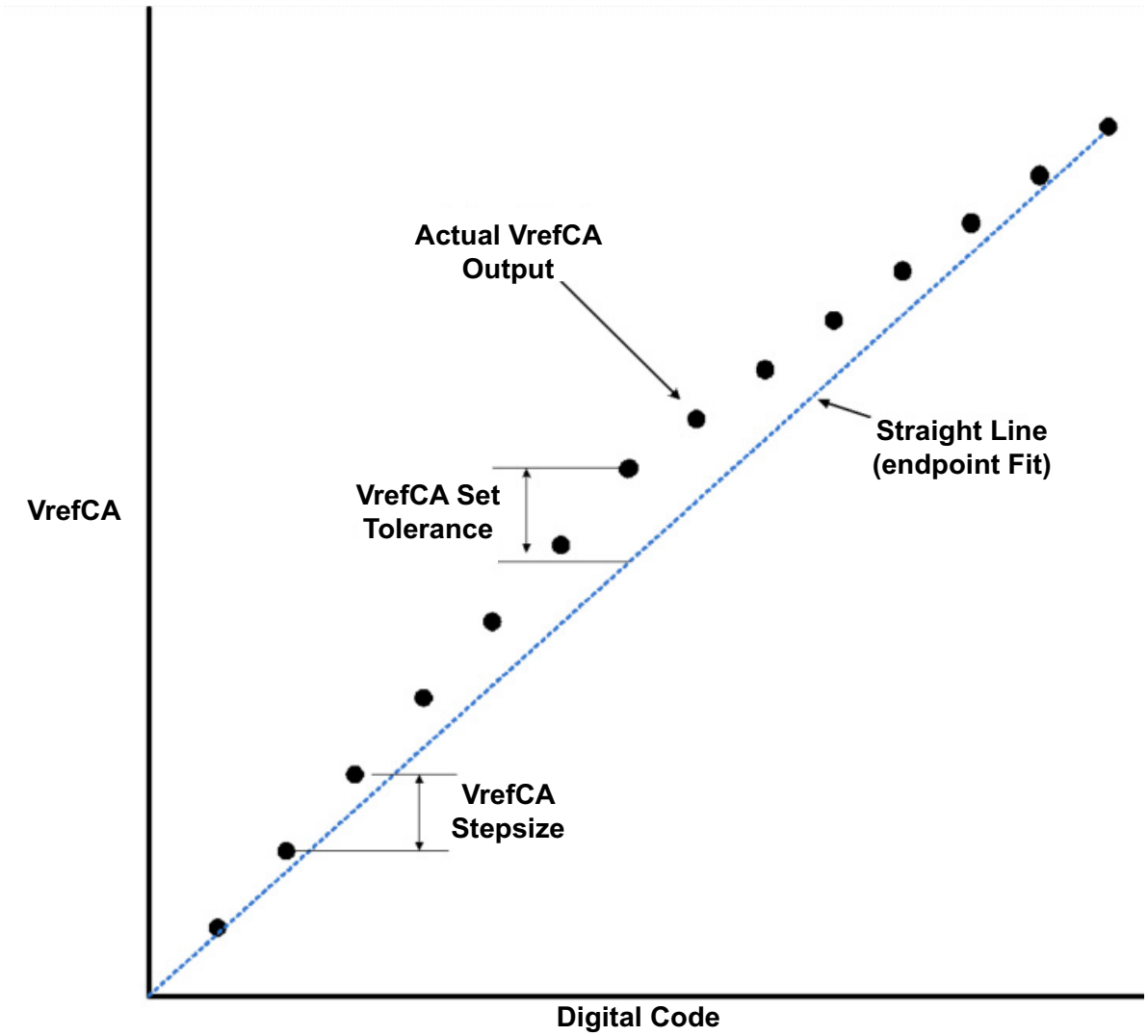


Figure 103 — Example of Vref set tolerance (max case only shown) and stepsize

The VrefCA increment/decrement step times are defined by VrefCA_time. The VrefCA_time is defined from t0 to t1 as shown in the Figure 104 below where t1 is referenced to when the VrefCA voltage is at the final DC level within the VrefCA valid tolerance (Vref_val_tol).

The VrefCA valid level is defined by VrefCA_val tolerance to qualify the step time t1 as shown in Figure 104. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VrefCA increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to MPC Apply VREFCA and RTT_CA/CS/CK

t1 - is referenced to the VrefCA_val_tol

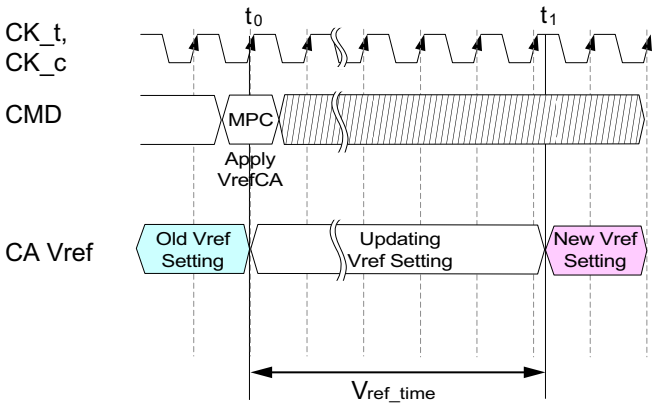


Figure 104 — Vref_time timing diagram

The minimum time required between two Vref commands is VrefCA_time, shown as Vref_time in images above.

Table 114 — VREF CA Mode Register

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR11	UI	**VrefCA Calibration Value**							

A VrefCA command is used to store the VREF values into the VREF CA MR11. This mode register is only programmed via the command but is readable via a normal MRR.

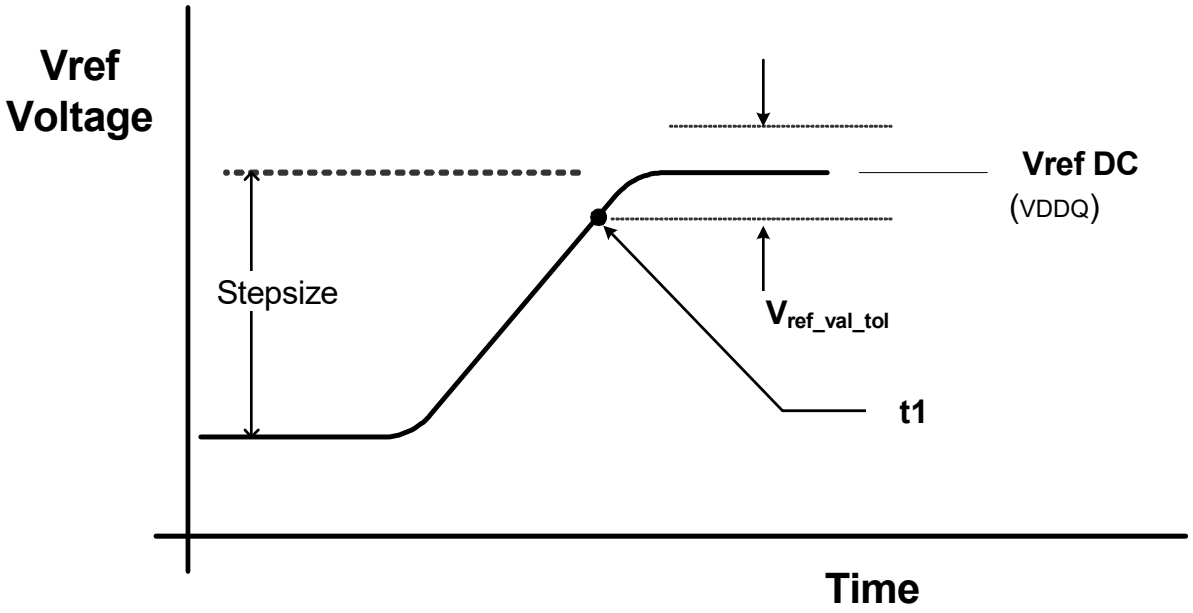


Figure 105 — Vref step single stepsize increment case.

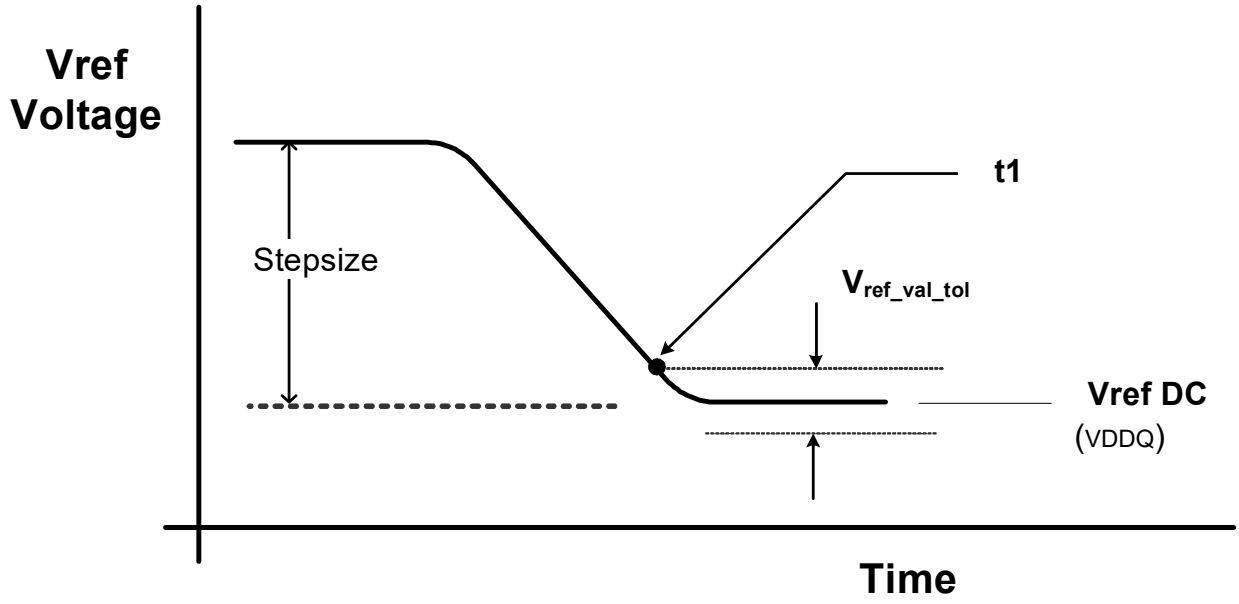


Figure 106 — Vref step single stepsize decrement case

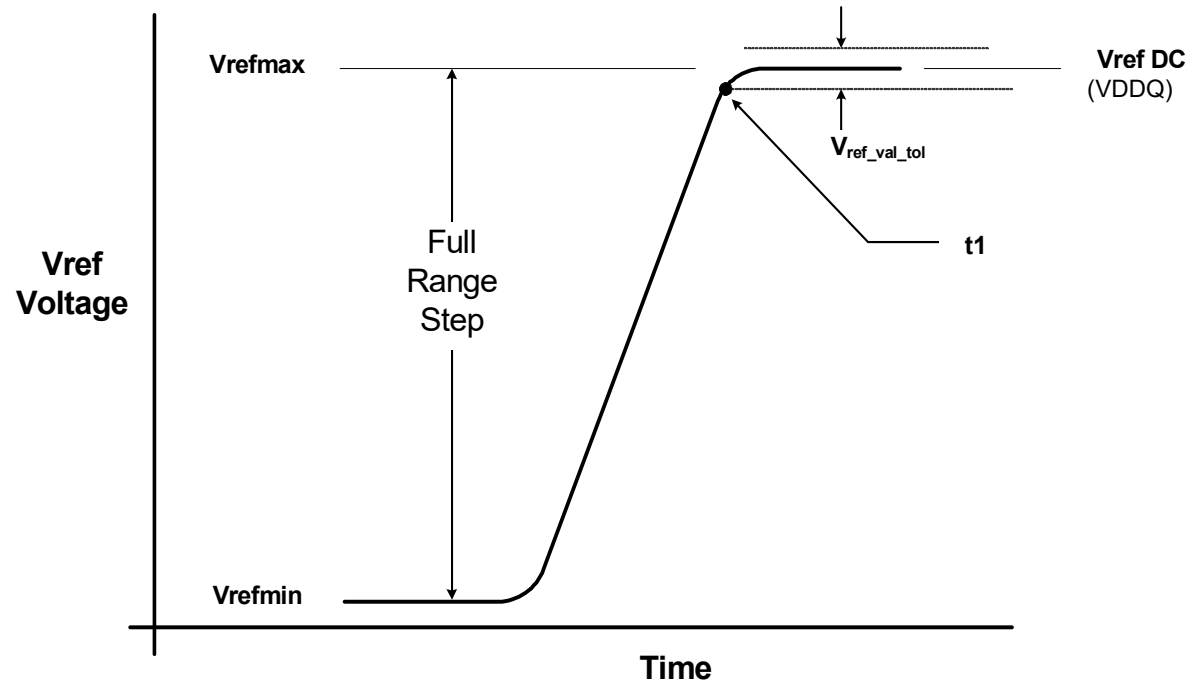


Figure 107 — Vref full step from Vrefmin to Vrefmax case

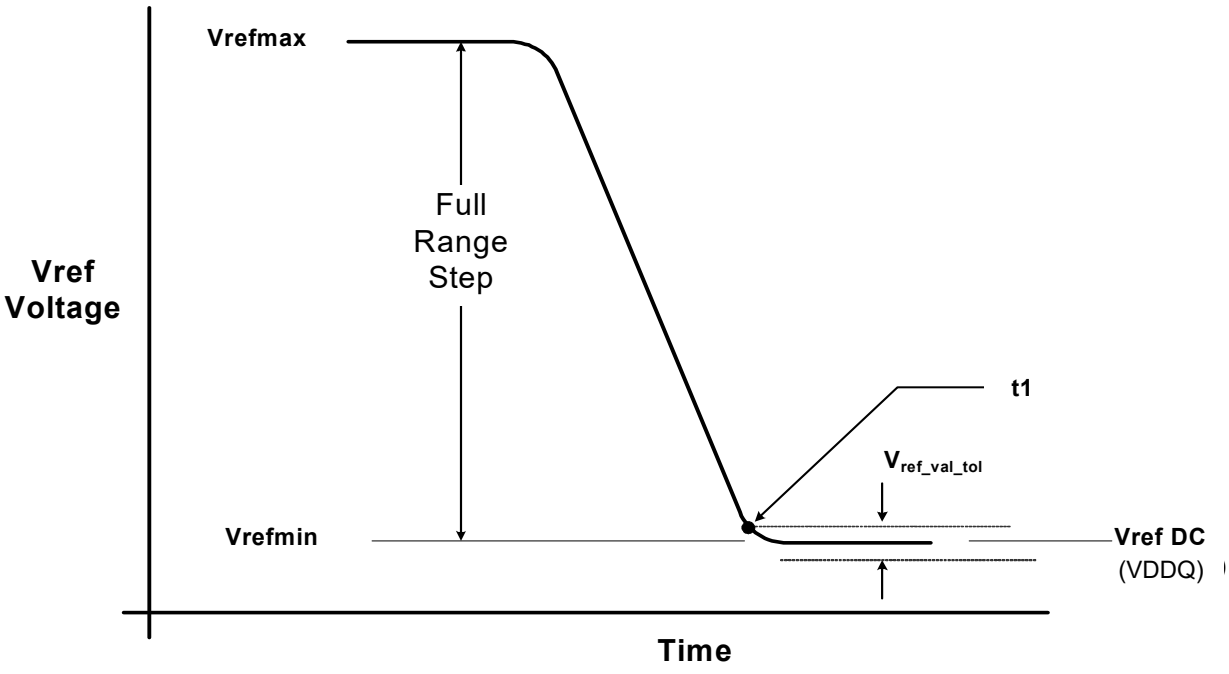


Figure 108 — Vref full step from Vrefmax to Vrefmin case.

The table below contains the CA internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

Table 115 — CA Internal VREF Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VrefCA Max operating point	V_{refCA_max}	97.5%	-	-	VDDQ	1
VrefCA Min operating point	V_{refCA_min}	-	-	45%	VDDQ	1
VrefCA Stepsize	V_{refCA_step}	0.41%	0.50%	0.59%	VDDQ	2
VrefCA Set Tolerance	$V_{refCA\_set\_tol}$	-1.625%	0.00%	1.625%	VDDQ	3,4,6
	$V_{refCA\_set\_tol}$	-0.15%	0.00%	0.15%	VDDQ	3,5,7
VrefCA Step Time	VrefCA_time	-	-	300	ns	8
VrefCA Valid Tolerance	$V_{refCA\_val\_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

NOTES:

1 - VrefCA DC voltage referenced to VDDQ_DC.

2 - VrefCA stepsize increment/decrement range. VrefCA at DC level.

3 - VrefCA_new = VrefCA_old $\pm$ n*VrefCA_step; n= number of steps; if increment use "+"; If decrement use "-"

4 - The minimum value of VrefCA setting tolerance = VrefCA_new - 1.625%*VDDQ. The maximum value of VrefCA setting tolerance = VrefCA_new + 1.625%*VDDQ. For n>4

5 - The minimum value of VrefCA setting tolerance = VrefCA_new - 0.15%*VDDQ. The maximum value of VrefCA setting tolerance = VrefCA_new + 0.15%*VDDQ. For n$\leq$ 4

6 - Measured by recording the min and max values of the VrefCA output over the range, drawing a straight line between those points and comparing all other VrefCA output settings to that line

7 - Measured by recording the min and max values of the VrefCA output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other VrefCA output settings to that line

8 - Time from MPC (Apply VREFCA, VREFCS, RTT_CK/CS/CA) command to increment or decrement

9 -Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VrefCA valid is to qualify the step times which will be characterized at the component level

4.27 VrefCS Training Specification

The DRAM internal VrefCS specification parameters are voltage operating range, stepsize, VrefCS set tolerance, VrefCS step time and Vref valid level.

The voltage operating range specifies the minimum required VrefCS setting range for DDR5 DRAM devices. The minimum range is defined by VrefCSmax and VrefCSmin as depicted in Figure 109 below.

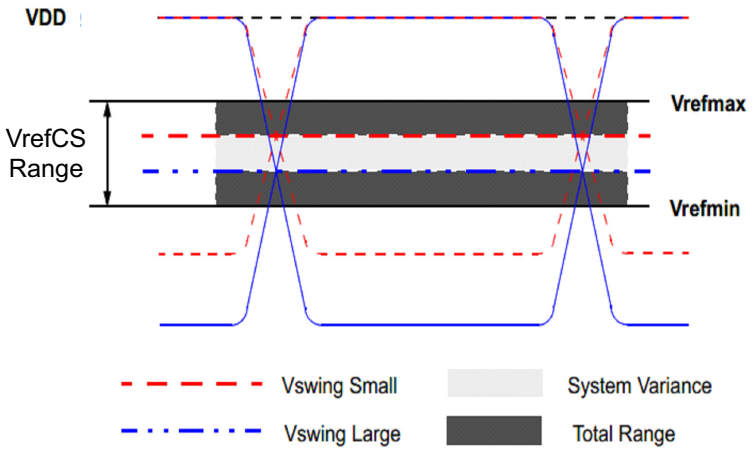


Figure 109 — VrefCS operating range(Vrefmin, Vrefmax)

The VrefCS stepsize is defined as the stepsize between adjacent steps. For a given design the DRAM VrefCS step size must be within the range specified.

The VrefCS set tolerance is the variation in the VrefCS voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VrefCS set tolerance uncertainty. The range of VrefCS set tolerance uncertainty is a function of number of steps n.

The VrefCS set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VrefCS values for a specified range. An illustration depicting an example of the stepsize and VrefCS set tolerance is below.

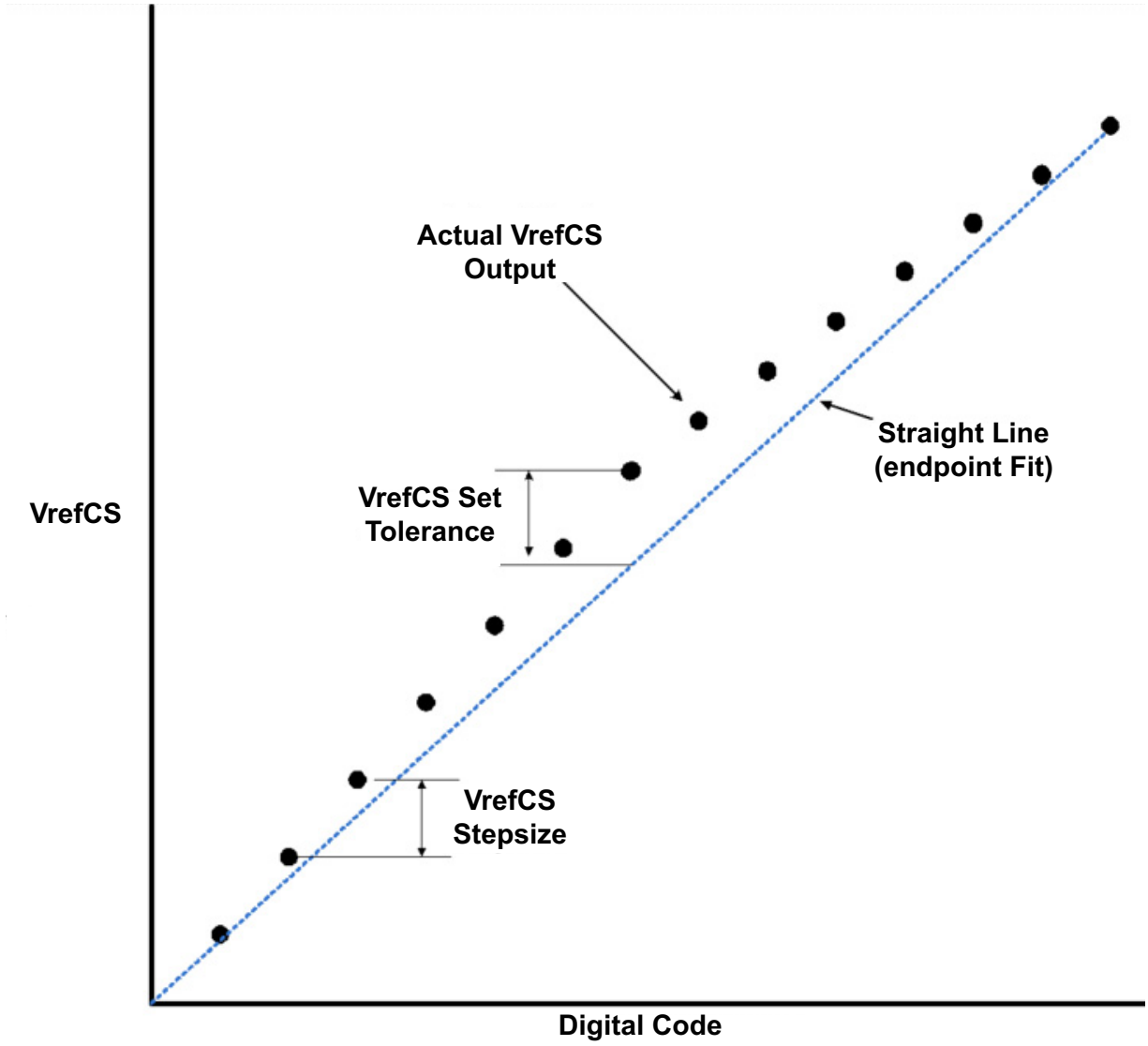


Figure 110 — Example of Vref set tolerance (max case only shown) and stepsize

The VrefCS increment/decrement step times are defined by VrefCS_time. The VrefCS_time is defined from t0 to t1 as shown in the Figure 111 below where t1 is referenced to when the VrefCS voltage is at the final DC level within the VrefCS valid tolerance (VrefCS_val_tol).

The VrefCS valid level is defined by VrefCS_val tolerance to qualify the step time t1 as shown in Figure 111. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VrefCS increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to MPC Apply VREFCS and RTT_CA/CS/CK

t1 - is referenced to the VrefCS_val_tol

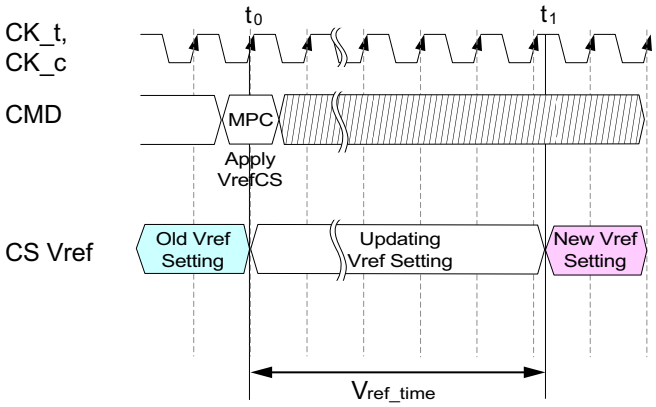


Figure 111 — Vref_time timing diagram

The minimum time required between two Vref commands is VrefCS_time, shown as Vref_time in images above.

Table 116 — VREF CS Mode Register

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR12	UI	**VrefCS Calibration Value**							

A VrefCS command is used to store the VREF values into the VREF CS MR12. This mode register is only programmed via the command but is readable via a normal MRR.

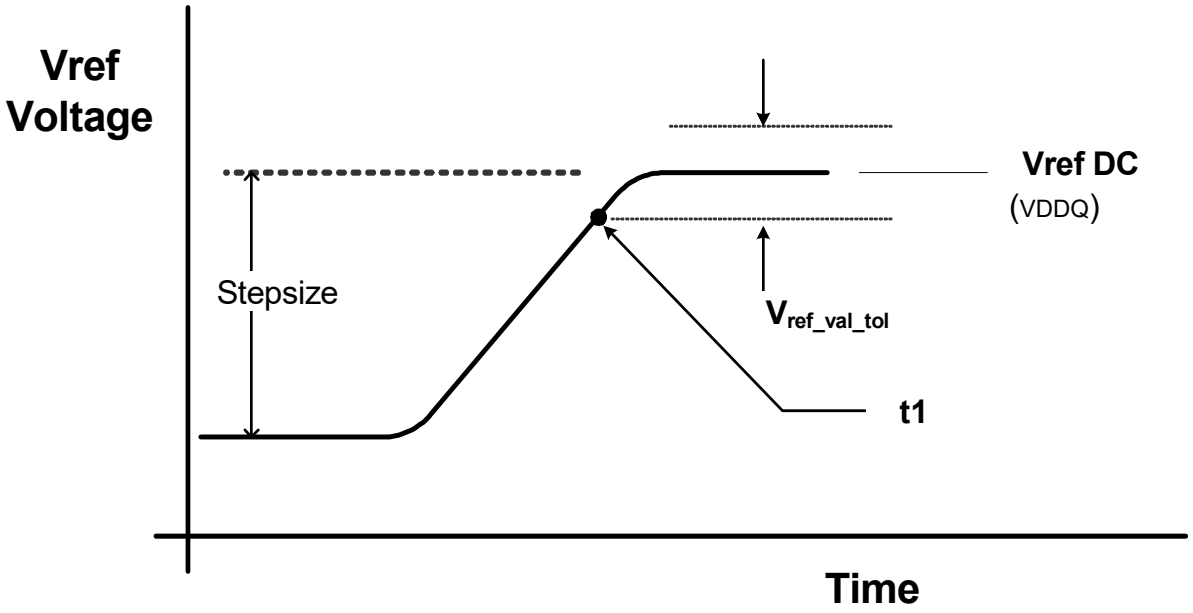


Figure 112 — Vref step single stepsize increment case.

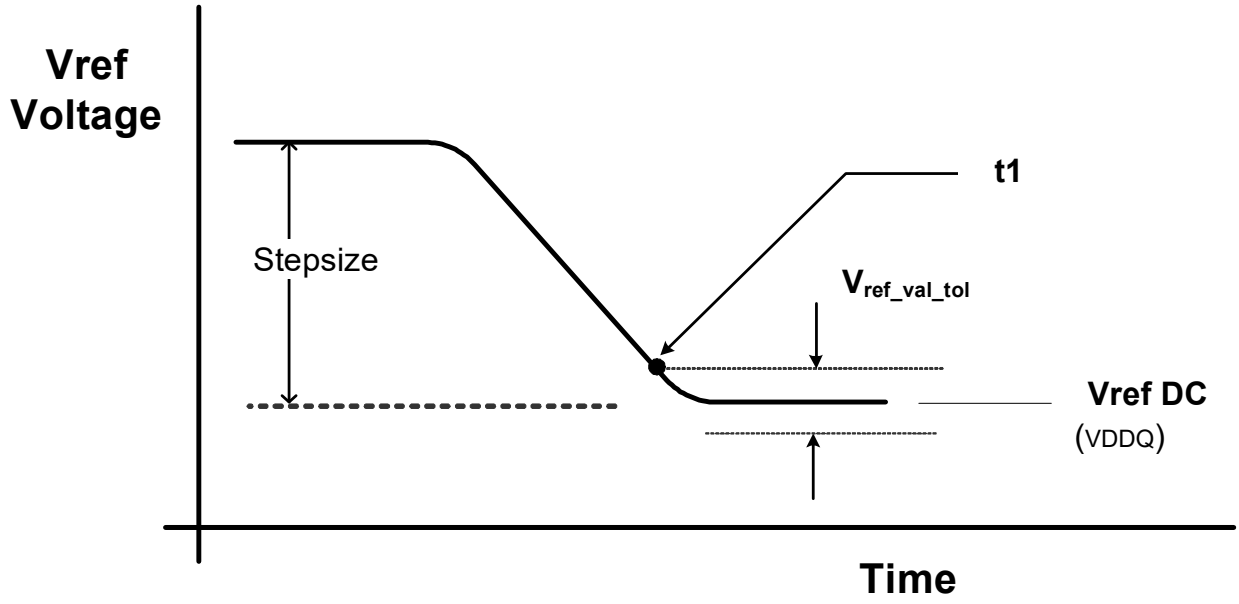


Figure 113 — Vref step single stepsize decrement case

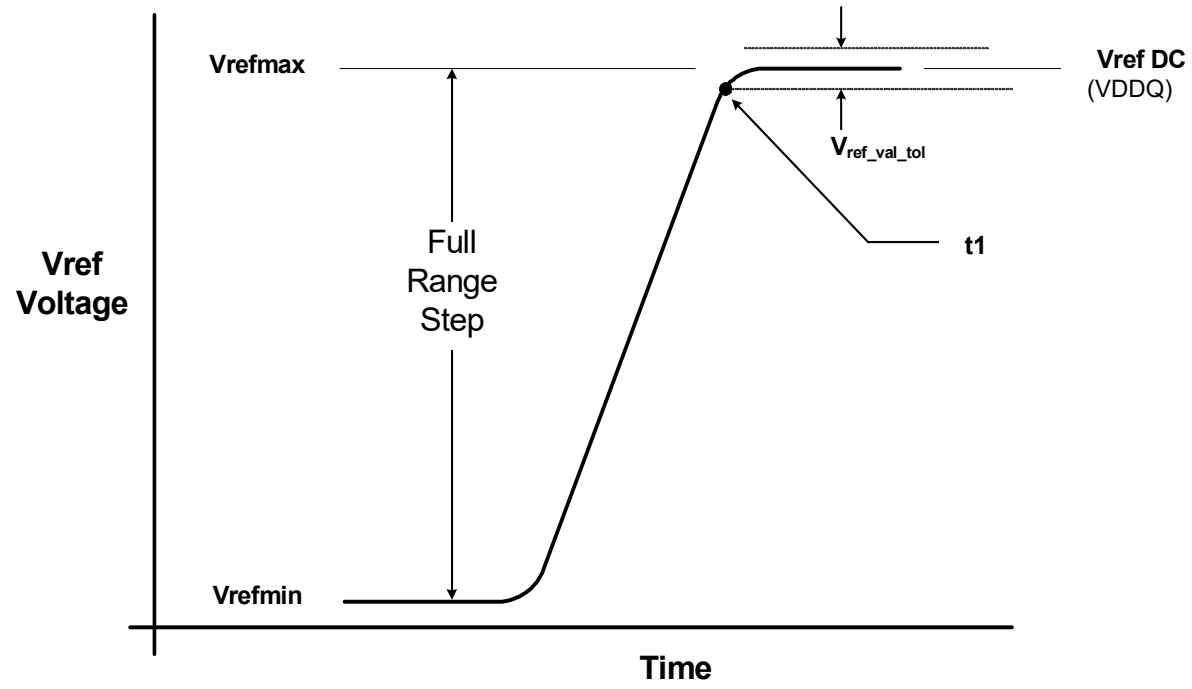


Figure 114 — Vref full step from Vrefmin to Vrefmax case

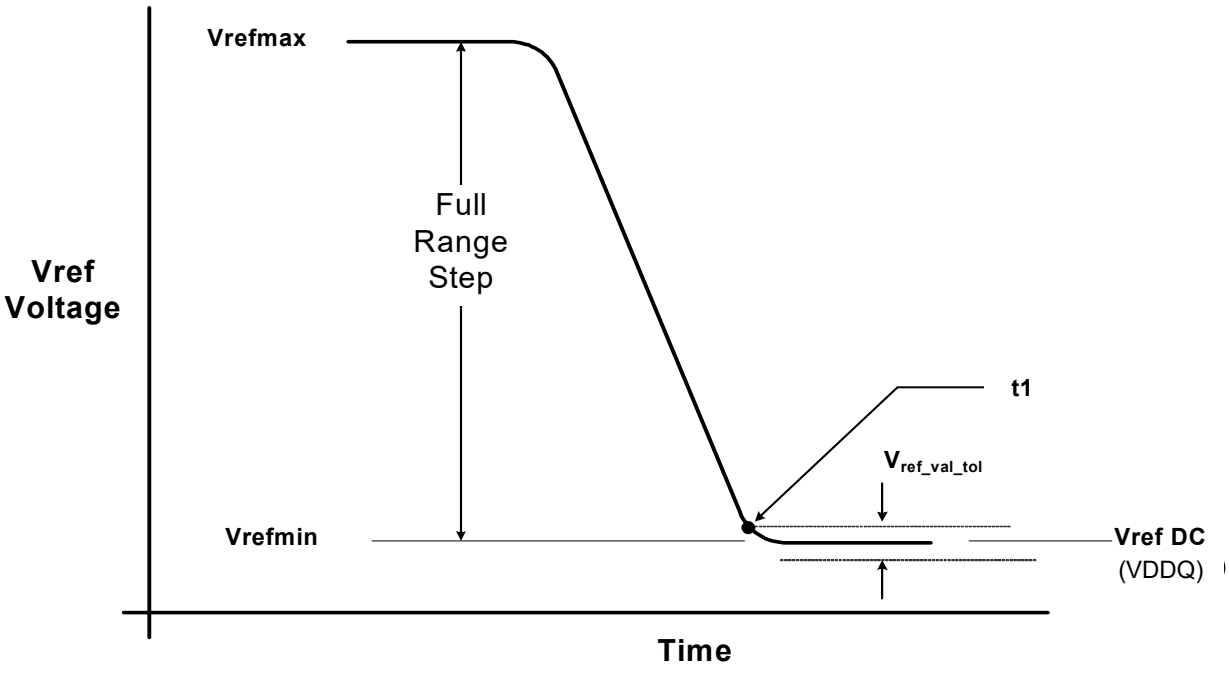


Figure 115 — Vref full step from Vrefmax to Vrefmin case.

The table below contains the CS internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

Table 117 — CS Internal VREF Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VrefCS Max operating point	V_{refCS_max}	97.5%	-	-	VDDQ	1
VrefCS Min operating point	V_{refCS_min}	-	-	45%	VDDQ	1
VrefCS Stepsize	V_{refCS_step}	0.41%	0.50%	0.59%	VDDQ	2
VrefCS Set Tolerance	$V_{refCS\_set\_tol}$	-1.625%	0.00%	1.625%	VDDQ	3,4,6
	$V_{refCS\_set\_tol}$	-0.15%	0.00%	0.15%	VDDQ	3,5,7
VrefCS Step Time	V_{refCS_time}	-	-	300	ns	8
VrefCS Valid Tolerance	$V_{refCS\_val\_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

NOTES:

1 - VrefCS DC voltage referenced to VDDQ_DC.

2 - VrefCS stepsize increment/decrement range. VrefCS at DC level.

3 - VrefCS_new = VrefCS_old + n*VrefCS_step; n= number of steps; if increment use "+"; If decrement use "-"

4 - The minimum value of VrefCA setting tolerance = VrefCS_new - 1.625%*VDDQ. The maximum value of VrefCS setting tolerance = VrefCS_new + 1.625%*VDDQ. For n>4

5 - The minimum value of VrefCS setting tolerance = VrefCS_new - 0.15%*VDDQ. The maximum value of VrefCS setting tolerance = VrefCSnew + 0.15%*VDDQ. For n< 4

6 - Measured by recording the min and max values of the VrefCS output over the range, drawing a straight line between those points and comparing all other VrefCS output settings to that line

7 - Measured by recording the min and max values of the VrefCS output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other VrefCS output settings to that line

8 - Time from MPC (Apply VREFCA, VREFCS, RTT_CK/CS/CA) command to increment or decrement

9 -Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VrefCS valid is to qualify the step times which will be characterized at the component level

4.28 VrefDQ Calibration Specification

The DRAM internal VrefDQ specification parameters are voltage operating range, stepsize, VrefDQ set tolerance, Vref step time and VrefDQ valid level.

The voltage operating range specifies the minimum required VrefDQ setting range for DDR5 DRAM devices. The minimum range is defined by VrefDQmax and VrefDQmin as depicted in Figure 116 below.

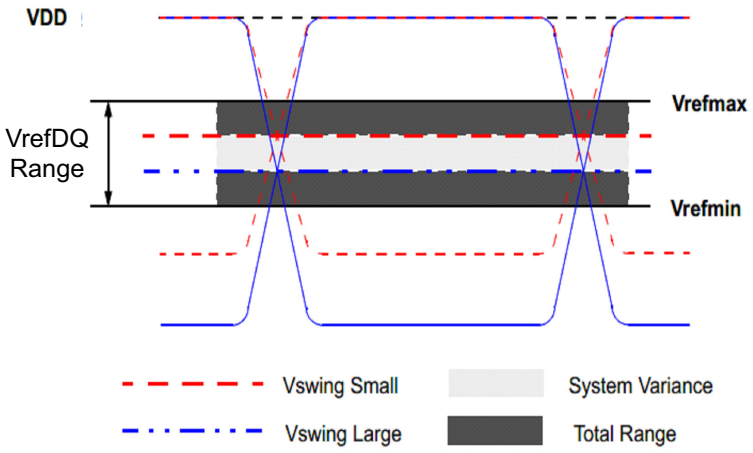


Figure 116 — VrefDQ operating range (VrefDQmin, VrefDQmax)

The VrefDQ stepsize is defined as the stepsize between adjacent steps. For a given design the DRAM VrefDQ step size must be within the range specified.

The VrefDQ set tolerance is the variation in the VrefDQ voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VrefDQ set tolerance uncertainty. The range of VrefDQ set tolerance uncertainty is a function of number of steps n.

The VrefDQ set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VrefDQ values for a specified range. An illustration depicting an example of the stepsize and VrefDQ set tolerance is below.

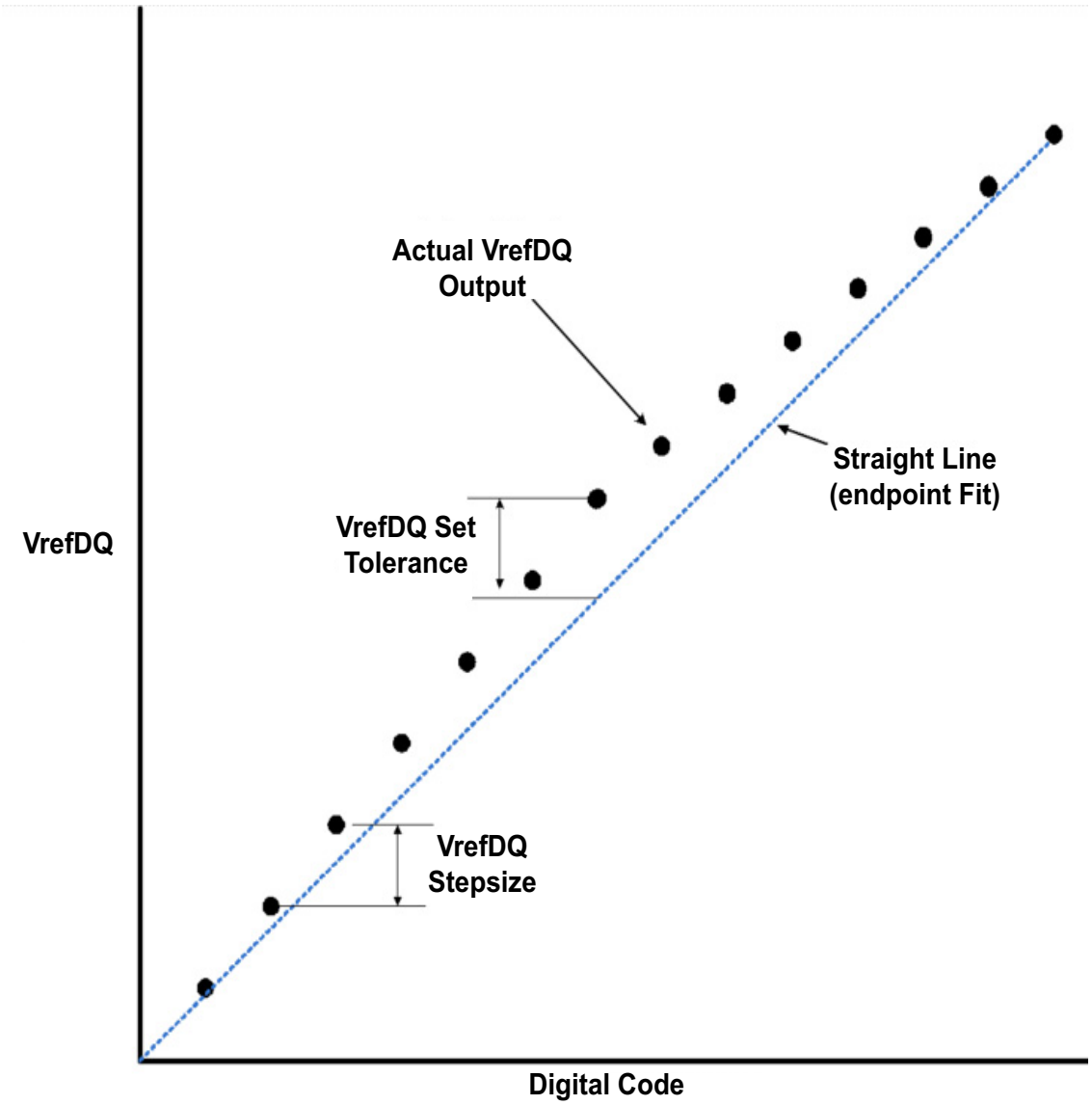


Figure 117 — Example of Vref set tolerance (max case only shown) and stepsize

The VrefDQ increment/decrement step times are defined by VrefDQ_time. The VrefDQ_time is defined from t0 to t1 as shown in the Figure 118 below where t1 is referenced to when the VrefDQ voltage is at the final DC level within the VrefDQ valid tolerance (VrefDQ_val_tol).

The VrefDQ valid level is defined by VrefDQ_val tolerance to qualify the step time t1 as shown in Figure 118. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VrefDQ increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to the MRW command which updates VrefDQ value

t1 - is referenced to the VrefDQ_val_tol

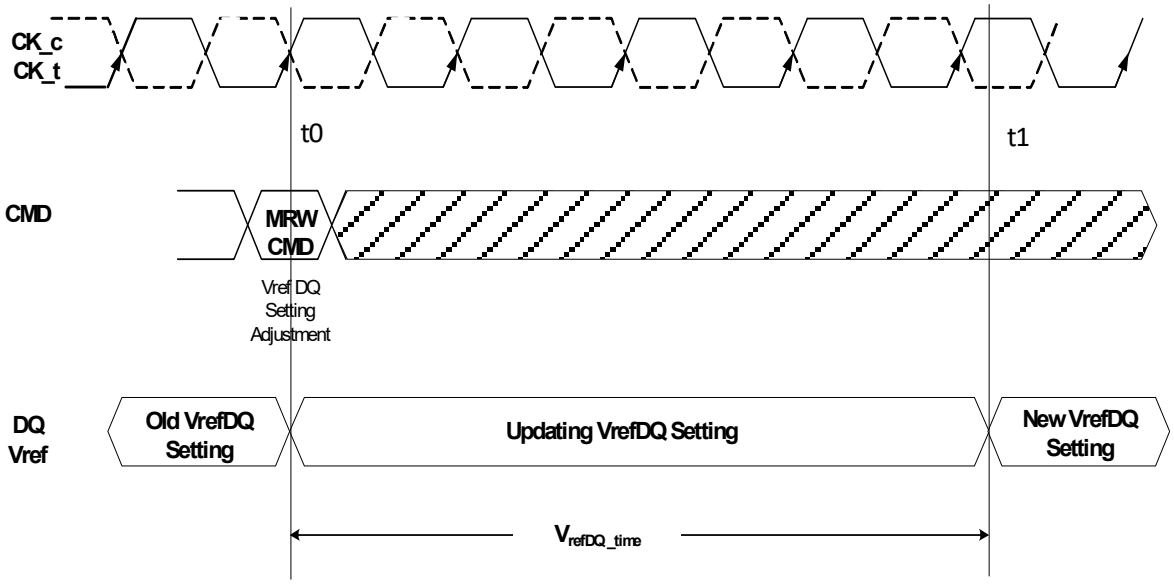


Figure 118 — VrefDQ_time timing diagram

The minimum time required between two MRW commands which update VrefDQ settings is VrefDQ_time.

Table 118 — VrefDQ Mode Register

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR10	UI	VrefDQ Calibration Value							

An MRW command is used to store the global VrefDQ values into the VrefDQ bits of MR10.

Additional per-pin VrefDQ trims are available for programming in MR118, MR126, MR134, ..., MR254, OP[7:4], up to a maximum of +/-3 VrefDQ steps. The combined global and per-pin VrefDQ settings shall never exceed the available VrefDQ range from 35.0% to 97.5%.

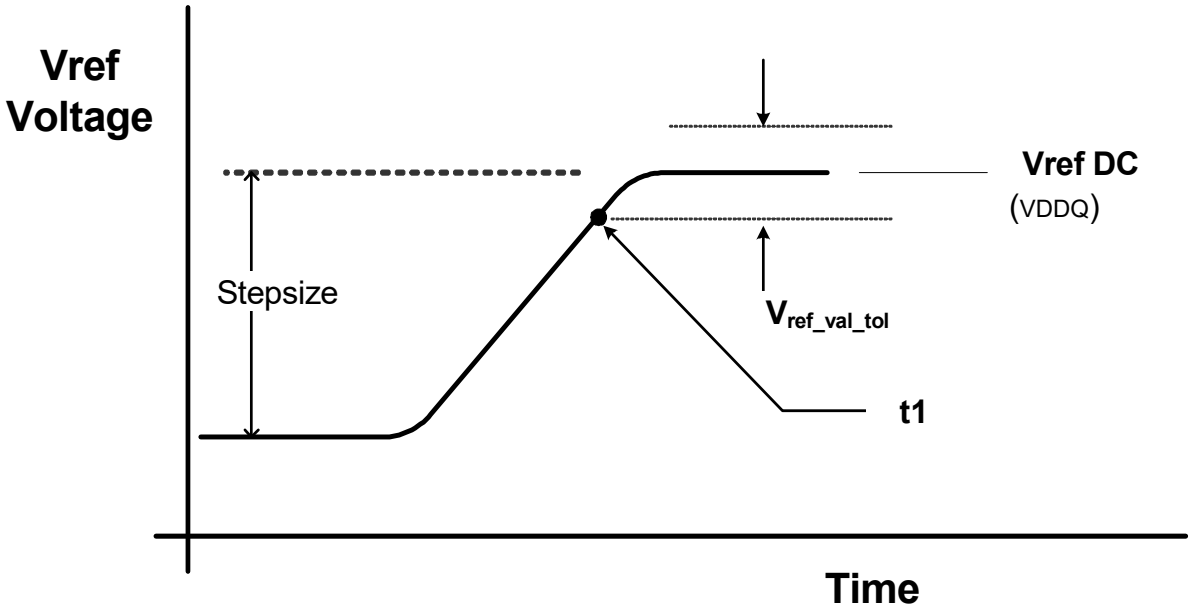


Figure 119 — VrefDQ step single stepsize increment case.

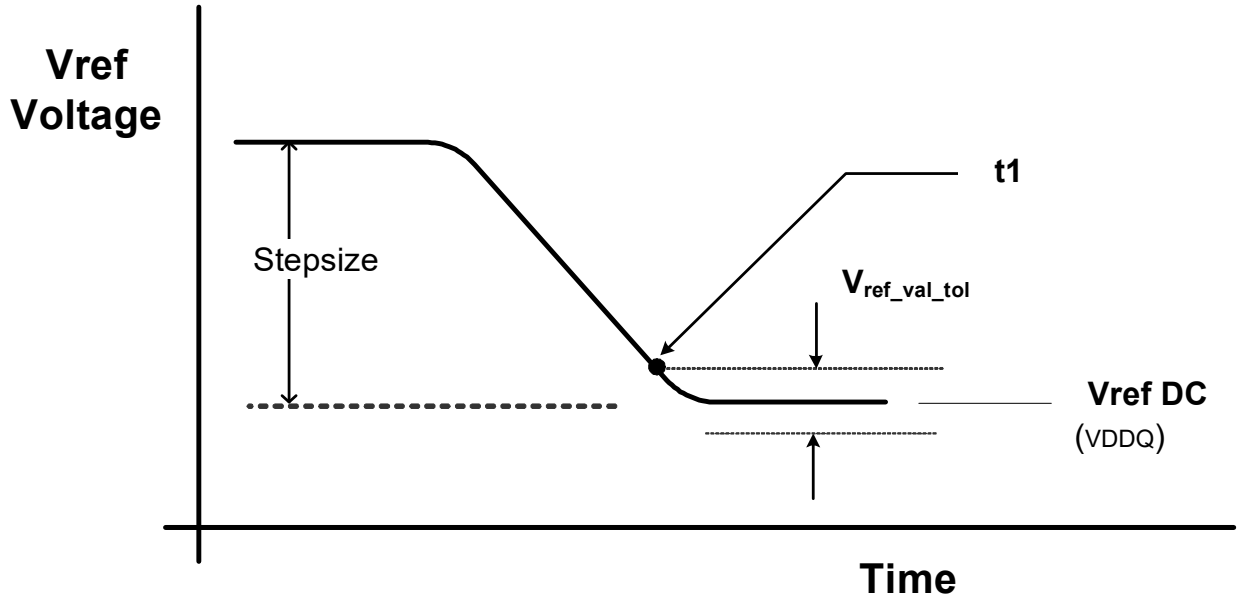


Figure 120 — VrefDQ step single stepsize decrement case

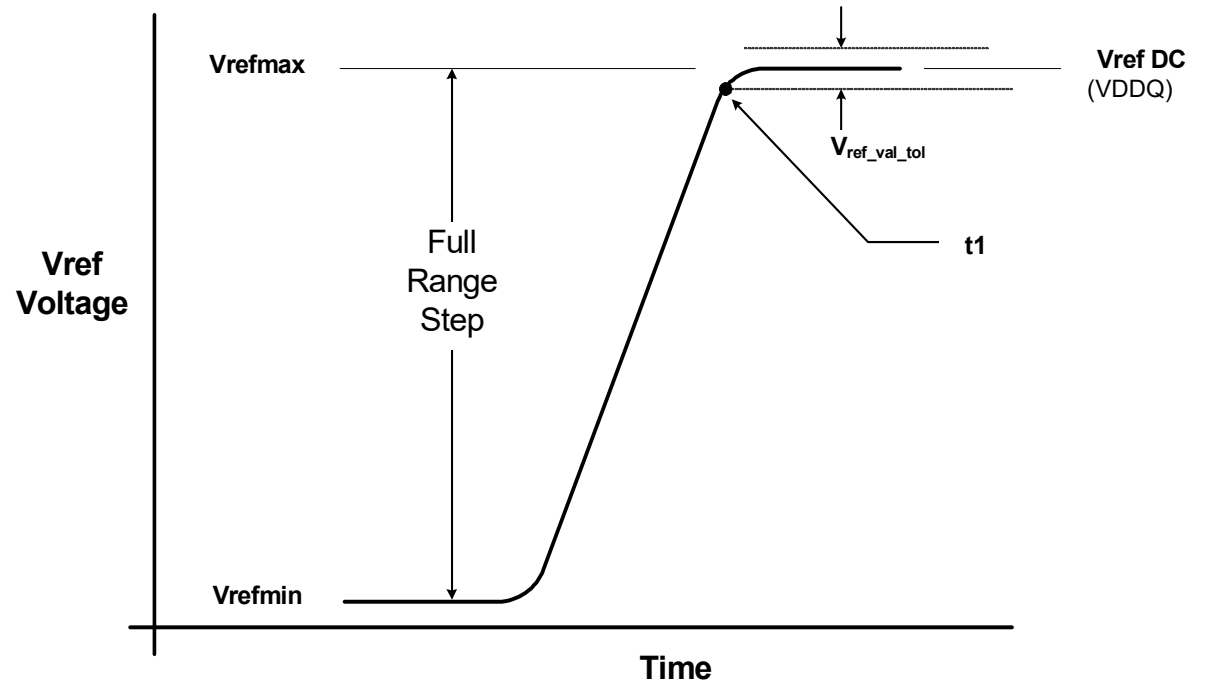


Figure 121 — VrefDQ full step from VrefDQmin to VrefDQmax case

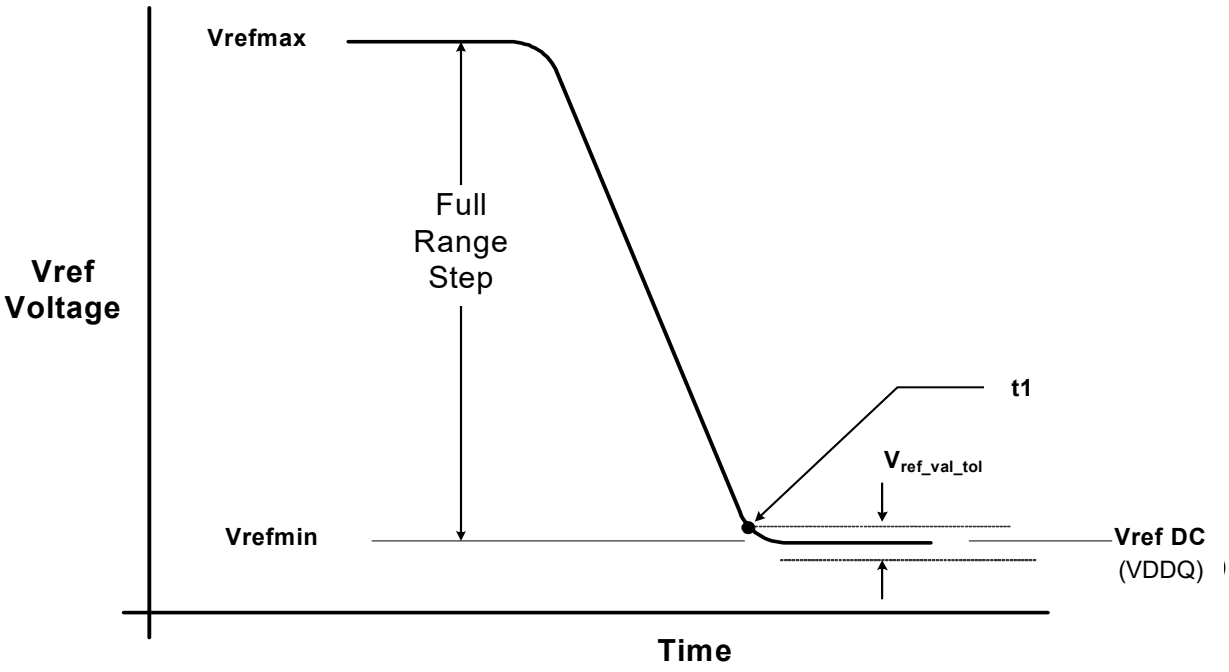


Figure 122 — VrefDQ full step from VrefDQmax to VrefDQmin case.

The table below contains the internal VrefDQ specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

Table 119 — VrefDQ Internal Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VrefDQ Max operating point	V_{refDQ_max}	97.5%	-	-	VDDQ	1
VrefDQ Min operating point	V_{refDQ_min}	-	-	45%	VDDQ	1
VrefDQ Stepsize	V_{refDQ_step}	0.41%	0.50%	0.59%	VDDQ	2
VrefDQ Set Tolerance	$V_{refDQ\_set\_tol}$	-1.625%	0.00%	1.625%	VDDQ	3,4,6
	$V_{refDQ\_set\_tol}$	-0.15%	0.00%	0.15%	VDDQ	3,5,7
VrefDQ Step Time	V_{refDQ_time}	-	-	150	ns	8,10
		-	-	500	ns	
VrefDQ Valid Tolerance	$V_{refDQ\_val\_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

Note(s):

1 - VrefDQ DC voltage referenced to VDDQ_DC.

2 - VrefDQ stepsize increment/decrement range. VrefDQ at DC level.

3 - VrefDQ_new = VrefDQ_old $\pm$ n*VrefDQstep; n= number of steps; if increment use "+"; If decrement use "-"

4 - The minimum value of VrefDQ setting tolerance = VrefDQ_new - 1.625%*VDDQ. The maximum value of VrefDQ setting tolerance = VrefDQ_new + 1.625%*VDDQ. For n>4.

5 - The minimum value of VrefDQ setting tolerance = VrefDQ_new - 0.15%*VDDQ. The maximum value of VrefDQ setting tolerance = VrefDQ_new + 0.15%*VDDQ. For n$\leq$ 4.

6 - Measured by recording the min and max values of the VrefDQ output over the range, drawing a straight line between those points and comparing all other VrefDQ output settings to that line.

7 - Measured by recording the min and max values of the VrefDQ output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other VrefDQ output settings to that line.

8 - Time from MRW command updating VrefDQ to increment or decrement.

9 - Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VrefDQ valid is to qualify the step times which will be characterized at the component level.

10 - The maximum value of VrefDQ step time = 150ns for n<16 and 500ns for n≥16, where n = number of steps.

4.29 Post Package Repair (PPR)

DDR5 supports Fail Row address repair, PPR which allows a simple and easy repair method in a system. Two methods are provided: Hard Post Package Repair (hPPR) for a permanent Row repair and Soft Post Package Repair (sPPR) for a temporary Row repair. DDR5 also optionally supports MBIST PPR (mPPR) which is to be used in conjunction with the MBIST feature to automatically repair failling addresses based on the results of MBIST.

Entry into hPPR, sPPR, MBIST and mPPR is protected through a sequential MRW guard key to prevent unintentional PPR programming. The sequential MRW guard key is the same for hPPR, sPPR, MBIST and mPPR.

The hPPR/sPPR/MBIST/mPPR guard key requires a sequence of four MRW commands to be issued immediately after entering hPPR/sPPR/MBIST/mPPR, as shown in Figure 123. The guard key sequence must be entered in the specified order as stated and shown in the spec below and in Table 120. Any interruptions of the guard key sequence from other MRW/R commands or non-MR commands such as ACT, WR, RD is not allowed. Although interruption of the guard key entry is not allowed, if the guard key is not entered in the required order or is interrupted by other commands, the hPPR/sPPR/MBIST/mPPR mode will not execute and the offending command terminated the hPPR/sPPR/MBIST/mPPR entry may or may not execute correctly however the offending command will not cause the DRAM to lock up. Offending commands which will interrupt hPPR/sPPR/MBIST/mPPR include:

- Any interruptions of the guard key sequence from other MRW/R commands or non-MR commands
- MRW with CW = high
- 2 cycle commands with CS_n low on the 2nd cycle

Additionally, when the hPPR/sPPR/MBIST/mPPR entry sequence is interrupted, subsequent ACT and WR commands will be conducted as normal DRAM commands. If a hPPR/sPPR/MBIST/mPPR operation was prematurely interrupted and/or terminated, the MR23 OP[4:0] must be reset to "0" prior to performing another hPPR/sPPR/MBIST/mPPR operation. The DRAM does not provide an error indication if an incorrect hPPR/sPPR/MBIST/mPPR guard key sequence is entered.

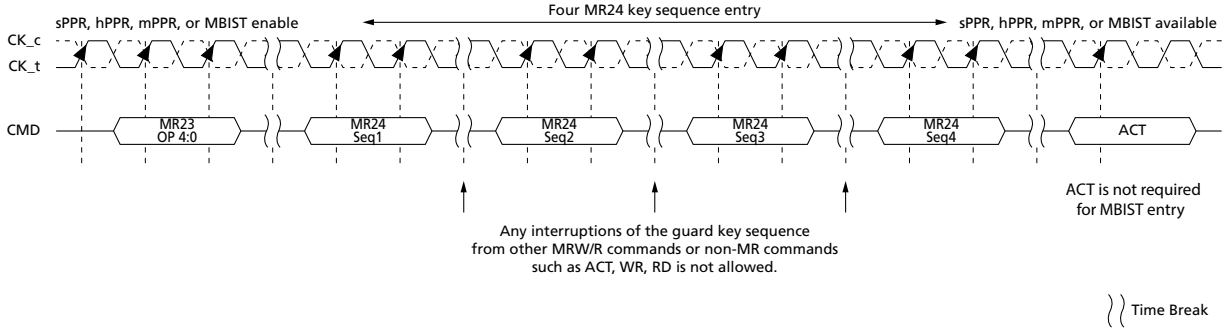


Figure 123 — Guard Key Timing Diagram

Table 120 — Guard Key Encoding for MR24

Guard Keys	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]	Notes
MR24 Seq1	1	1	0	0	1	1	1	1	
MR24 Seq2	0	1	1	1	0	0	1	1	
MR24 Seq3	1	0	1	1	1	0	1	1	
MR24 Seq4	0	0	1	1	1	0	1	1	

Table 121 — sPPR vs hPPR vs mPPR

	sPPR	hPPR	mPPR	Note
Persistence of Repair	Volatile – Repaired as long as VDD is within Operating Range	Non-Volatile – repair is permanent after the repair cycle.	Non-Volatile – repair is permanent after the repair cycle	Soft Repair is erased when Vdd removed, device reset, or sPPR undo command performed to an unlocked sPPR row.
Length of time to complete repair cycle	WL+ 8tCK+tWR	tPGM_hPPRa or tPGM_hPPRb	tSELFREPAIR	
# of Repair elements per repair region[1]	one per BG (Default) one per Bank (Optional)	at least one per BG	Vendor specific	There is no ability to know how many mPPR elements remain in an given repair region. Host must rely on MBIST transparency in MR to determine mPPR success
Simultaneous use of soft and hard repair within a repair region[1]	Previous hPPR are allowed before sPPR	Any outstanding sPPR must be cleared before an hPPR	Any outstanding sPPR must be cleared before MBIST or mPPR	
Repair Command	1 method - WR	1 method - WRA	1 method - WRA	
DRAM retains array data	Yes	No	No	

Note 1: Repair region is defined as the address space for which a single repair can be used. A repair region is either a BG or bank, depending on vendor implementation.

4.29.1 Hard PPR (hPPR)

With hPPR, DDR5 can correct at least one row address per Bank Group. The hPPR resource designation (MR54,55,56,57) will indicate the hPPR resource availability, and can be read/checked prior to implementing a repair. It is important to note that hPPR repairs are permanent; the Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the hPPR mode entry and repair. (i.e. During the Command/Address training period). Entry into hPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. After tRCD time, a BL16 WRA command is used to select the individual DRAM through the DQ bits and to transfer the repair address to the DRAM. After program time, and PRE, the hPPR mode can be exited and normal operation can resume.

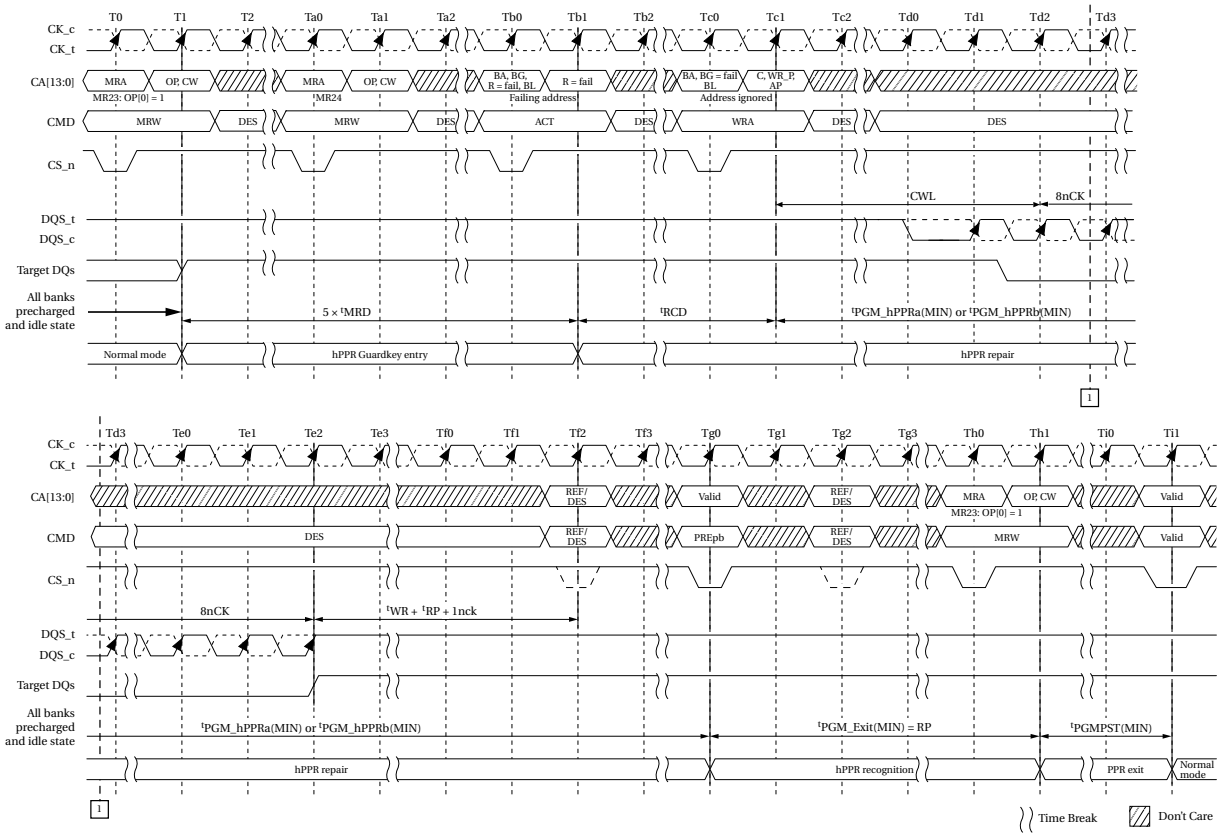
4.29.1.1 hPPR Fail Row Address Repair

1. Since the mode register address operand allows the user to execute hPPR resource, MRR of hPPR resource designation (MR 54, 55, 56, 57) needs to be read. After user's checking the hPPR resource availability of each bank from MRR, hPPR mode can be entered. If the MRR of hPPR resource designation (MR 54, 55, 56, 57) appears to not be available, the host controller should not issue hPPR mode.
2. Before entering 'hPPR' mode, all banks shall be in a precharged and idle state, and CRC Mode must be disabled.
3. Enable hPPR using MR23:OP[0]=1 and wait tMRD.
4. Issue guard key as four consecutive MR24 OP[7:0] MRW commands each with a unique address field OP[7:0]. Each MRW command should be spaced by tMRD.
5. Issue ACT command with the CID bits, Bank Group, Bank and Row fail address. Write data is used to select the individual DRAM in the rank for repair. For non 3DS DRAMs the CID bits need only be Valid, and are ignored by the DRAM.
6. After tRCD, Issue WRA with a valid address. The DRAM will ignore the address given with the WRA command.
7. After WL(WL=RL-2), DQ{3:0] of target DRAM must be LOW for 8tCK. If HIGH is driven to DQ[3:0] of a DRAM for 8tCK, then DRAM does not conduct hPPR and retains data if REF/REFsb command is properly issued. If more than one DRAM shares the same command bus, DRAMs that are not being repaired must have DQ[3:0] driven HIGH for 8tCK. If all of the DQ[3:0] data bits are neither all LOW nor all HIGH for 8tCK, then hPPR mode execution is unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't cares. Note that a previous versions of the spec required ALL DQs to be high or low, but this was changed to DQ[3:0] to accomodate ECC UDIMMs and SoDIMMs. Check with the DRAM vendor for their specific implementation.
8. Wait tPGM_hPPRa or tPGM_hPPRb to allow DRAM repair at the target row address to occur internally, and then issue PRE command.
9. Wait tPGM_Exit(min) after PRE command to allow DRAM to recognize repaired row address.
10. Exit hPPR by setting MR23:OP[0]=0.
11. DDR5 will accept any valid command after tPGMPST(min).
12. In the case of multiple addresses to be repaired, repeat Steps 3 to 10.
13. For a 3DS device, the target die for the hPPR is selected by the CID[3:0] bits in the ACT, WRA and PRE commands. The CID bits must match in all three commands.

During hPPR mode, REF, REFsb commands are allowed, but array contents are not guaranteed. Upon receiving a REF or REFsb command in hPPR mode, the DRAM may ignore the Refresh operation but will not disrupt the repair operation. Other commands except REF/REFsb during tPGM can cause incomplete repair so no other command except REF is allowed during tPGM.

Once hPPR mode is exited with MR23:OP[0]=0 and tPGMPST, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back.

Figure 124 — hPPR Fail Row Repair



Note1. Allow REFab/REFsb(1X) from WL+8tCK+tWR+tRP+1tCK after WR, but does not guarantee array contents are refreshed during hPPR
Note2. Timing diagram shows possible commands but not all shown can be issued at same time; for example if REF is issued at Te1, DES must be issued at Te2 as REF would be illegal at Te2. Likewise, DES must be issued tRFC prior to PRE at Tf0. All regular timings must still be satisfied.

4.29.1.2 Required Timing Parameters

Repair requires additional time period to repair Fail Row Address into Spare Row Address and the following timing parameters are required for PPR.

Table 122 — hPPR Timings

Parameter	Symbol	DDR5-3200 to 6400		Unit	Note
		min	max		
hPPR Programming Time: x4/x8	tPGMa	1,000	-	ms	
hPPR Programming Time: x16	tPGMb	2,000	-	ms	
hPPR RecognitionTime	tPGM_Exit	tRP	-	ns	
hPPR Program Exit and New Address Setting time	tPGMPST	50	-	us	

4.29.2 Soft Post Package Repair (sPPR)

Soft Post Package Repair (sPPR) is a way to quickly, but temporarily, repair one row address per Bank Group on a DDR5 DRAM device, contrasted to hPPR which takes longer but is permanent repair of a row address. There are some limitations and differences between Soft Repair and a Hard Repair. Entry into sPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. After tRCD time, a BL16 WR command is used to select the individual DRAM through the DQ bits and to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE, the sPPR mode can be exited and normal operation can resume. Care must be taken that refresh is not violated for the other rows in the array during soft repair time. Also note that the DRAM will retain the soft repair information inside the DRAM as long as VDD remains within the operating region. If DRAM power is removed or the DRAM is RESET, the soft repair will revert to the un-repaired state. hPPR and sPPR may not be enabled at the same time. sPPR must have been disabled, cleared and unlocked (if DRAM supports optional sPPR undo/lock) prior to entering hPP,R, MBIST or mPPR modes.

With sPPR, DDR5 can repair one Row address per BG (Default) or one row address per bank (Optional). If the hPPR resources for a BG are used up, the bank group will have no more available resources for soft PPR. If a repair sequence is issued to a BG with no repair resources available, the DRAM will ignore the programming sequence.

Note that MR54 through MR57 are NOT updated by an sPPR. The host controller must remember which sPPR resources have been used since the last DRAM Reset.

The DRAM device may optionally support the sPPR Undo and sPPR Lock functions. The sPPR undo command will undo a previous sPPR and cause the sPPR resource to be taken back to its unused condition. The original row will appear back in the memory map at its original location following an sPPR undo. The sPPR Lock function will lock the specific sPPR resource at its current location and not allow another sPPR or an sPPR undo to be performed to that resource.

A row that has been replaced by a spare row need not be refreshed by the DRAM. Likewise a spare row that is not in the memory map, either from never being in the memory map, or from an sPPR undo need not be refreshed by the DRAM. If moving a spare row in and out of the memory map, the host controller is responsible for sending enough Activate commands to any mapped out row to assure any required data retention. The host controller is also responsible for any data copy operations between the original row and spare row.

The host controller should read MR23 OP2 to determine whether the sPPR undo and sPPR lock functions are supported. 0=unsupported, 1=supported.The two features are supported together.

4.29.2.1 sPPR Repair of a Fail Row Address

The following is the procedure of sPPR with WR command. Note that during the soft repair sequence, no refresh is allowed.

1. User should back up the data of the target row address for sPPR in the bank before sPPR execution. The backup data should be one row per bank. After sPPR has been completed, user restores the data in the repaired array.
2. sPPR resources are shared with hPPR. The hPPR resource designation registers (MR 54, 55, 56, 57) should be checked prior to sPPR. If the MRR of hPPR resource designation (MR 54, 55, 56, 57) shows that hPPR resources in the bank that is targeted for sPPR repair is not available, the host controller should not issue sPPR mode.
3. Before entering 'sPPR' mode, all banks shall be in a precharged and idle state. and CRC mode must be disabled.
4. Enable sPPR using MR23 bits "OP[2:1]=01" and wait tMRD.
5. Issue Guard Key as four consecutive MRW commands each with a unique address field OP[7:0] Each MRW command shall be separated by tMRD. The Guard Key sequence is the same as hPPR in Table 120.
6. Issue ACT command with the CID bits, Bank Group, Bank and Row Fail address, Write data is used to select the individual DRAM in the Rank for repair. For non-3DS DRAMs, the CID bits need only be Valid, and are ignored by the DRAM.
7. A WR command is issued after tRCD, with valid column address. The DRAM will ignore the column address given with the WR command.
8. After WL (WL=WL=RL-2), DQ[3:0] of the individual Target DRAM must be LOW for 8tCK. If more than one DRAM shares the same command bus, DRAMs that are not being repaired must have DQ[3:0] driven HIGH for 8tCK. If all of the DQ[3:0] data bits are neither all LOW nor all HIGH for 8tCK, then sPPR mode will be unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't cares. Note that a previous versions of the spec required ALL DQs to be high or low, but this was changed to DQ[3:0] to accomodate ECC UDIMMs and SoDIMMs. Check with the DRAM vendor for their specific implementation.
9. Wait tPGM_sPPR(min) for the internal repair register to be written and then issue PRE to the Bank.
10. Wait tRP after PRE command to allow the DRAM to recognize repaired Row address.
11. Exit sPPR with setting MR23 bit "OP[2:1]=00" and wait tMRD.
12. sPPR can be performed without affecting the hPPR previously performed provided a row is available in that repair region. When more than one sPPR request is made to the same repair region, the most recently issued sPPR address would replace the early issued one associcated with given bank and row addresses. In the case of conducting soft repair address in a different repair region, repeat step 4 to 11. During a soft repair, refresh command is not allowed between sPPR MRS entry and exit.

For a 3DS device, the target die for the sPPR is selected by the CID[3:0] bits in the ACT, WR, and PRE commands. The CID bits must match in all three commands.

Figure 125 — sPPR Fail Row Repair

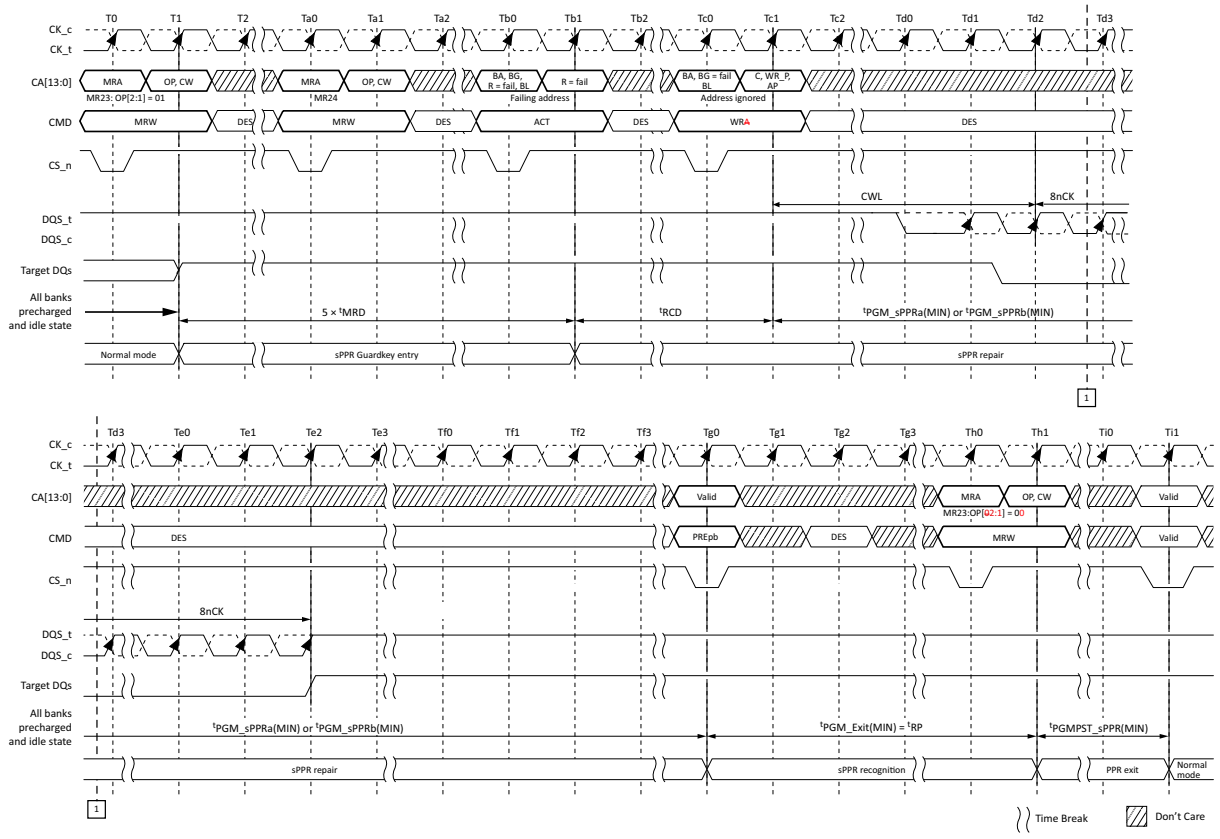


Table 123 — sPPR Timings

Parameter	Symbol	DDR5-3200 to 6400		Unit	Note
		min	max		
sPPR Programming Time: x4/x8, x16	tPGM_sPPR	WL+8tCK +tWR	-	tCK	
sPPR Exit Recognition Time	tPGM_Exit	tRP	-	ns	
sPPR Exit and New Address Setting time	tPGMPST _sPPR	tMRD	-	ns	

4.29.2.2 sPPR Undo

sPPR Undo is a method of setting the sPPR resource back to its unused state, as it was following Reset. It follows the exact same protocol as the sPPR sequence, but with MR23 OP[2:1] set to 10. The host controller must send the same CID bits, BG bits, Bank bits, and row address in the Activate command as it did for the most recent sPPR for this resource. The DRAM may ignore the bank and row address bits if it so chooses, as the CID and BG bits may be enough to uniquely identify the sPPR resource depending on number of repair elements. For non 3DS DRAMs the CID bits need only be Valid, and are ignored by the DRAM. If the Bank and/or row address does NOT match that of the most recent sPPR to this resource, the DRAM may or may not perform the undo. Any required copying of data is the host controller's
responsibility.

Following an sPPR Undo, a later sPPR may be done to assign the resource to a new or the same location. Data is retained in the sPPR resource, but it need not be refreshed by the DRAM. If the host controller requires the data to remain valid, it must send enough ACT commands to the row while it is mapped in to guarantee the data.

This feature is optional. The sPPR undo function should only be done to DRAMs in which MR23 bit 2 is read as a 1 upon an MRR.

4.29.2.3 sPPR Lock

sPPR Lock allows an sPPR resource to be locked in place. Locks are done to sPPR resources individually. Following an sPPR Lock any sPPR or sPPR undo is blocked to that spare resource. A hardware reset or power cycle must be done to undo the lock. The hardware reset or power cycle must also be done before any hPPR operation can be done if any sPPR resources are locked.

The sPPR Lock uses the same protocol as the sPPR function except that MR23 OP[2:1] is set to 11. The Activate command must contain the CID bits, BG bits, bank bits and row address of the most recent sPPR for that resource. The DRAM may ignore the bank and row address bits if it so chooses, as the CID and BG bits may be enough to uniquely identify the sPPR resource depending on number of repair elements. For non 3DS DRAMs the CID bits need only be Valid, and are ignored by the DRAM. If the Bank and/or row address does NOT match that of the most recent sPPR to this resource, the DRAM may or may not perform the lock.

This feature is optional. The sPPR lock function should only be done to DRAMs in which MR23 bit 2 is read as a 1 upon an MRR.

4.30 MBIST/mPPR

DDR5 devices can support optional Memory Built-In Self Test (MBIST) and Memory Built-In Self Test-Post Package Repair (mPPR) to help with hard failures such as single-bit or multi-bit failures in a single device so that weak cells can be scanned and repaired during the initialization phase. There are two distinct associated phases, MBIST (Self-test phase) and mPPR (Self-repair phase). During MBIST, the DRAM will use vendor specific patterns to test the memory array, detect hard failures. During mPPR, addresses of hard-failures will be automatically repaired out. MBIST and mPPR may only be entered from the All Banks Idle state. MBIST may be ran any time after the device has been properly initialized according to Ch. 3.3.1 “Power-up Initialization Sequence”, but must be run prior to mPPR. After MBIST completes, MR22 transparency must be read. If transparency says that fails remain and the controller chooses to run mPPR, it must perform mPPR immediately after the DRAM transparency is read.

mPPR resources are separated from normal hPPR/sPPR resources. mPPR resources will be used for initial scan and repair, and hPPR/sPPR resources still must satisfy the number of repair elements as specified in Table 127. Once MBIST is done, DRAM will update the MBIST/mPPR transparency status in MR22:OP[2:0]. Detailed transparency status is described in 3.5.24

There are two timings associated with MBIST/mPPR, tSELFTEST and tSELFREPAIR. The time to test the array and detect failures is defined as tSELFTEST. The time to repair failures detected in the previous MBIST run using mPPR is defined as tSELFREPAIR. Multiple iterations of MBIST and mPPR may be required to repair all failures, and the transparency status will inform the host of this.

For 3DS devices, MBIST must be run on each logical rank in the 3DS package independently by configuring MR14:OP[3:0] prior to invoking MBIST. After MBIST is run on a single logical rank, MBIST/mPPR transparency in MR22 must subsequently be read to determine whether mPPR is needed on that logical rank. The controller may choose to run MBIST on all ranks before performing mPPR on all ranks sequentially, or it may perform MBIST on one rank followed by mPPR to the same rank, proceeding through each logical rank.

4.30.1 MBIST Sequence

The controller is required to issue an MRW command to enter the MBIST operation. Controller sets the MR23:OP[4] to HIGH, subsequently followed by the MR24 commands for the guard key, then the DRAM enters MBIST operation and the DRAM drives ALERT_n to LOW. Once the MBIST is completed, the DRAM drives ALERT_n to HIGH to notify the controller that this operation is completed. MBIST/mPPR transparency will be updated in MR22, and will signify to the host whether mPPR must be performed to repair any found fails. If mPPR is required, the controller will follow the mPPR sequence described in section 4.30.2, and transparency will be updated once mPPR is complete. DRAM data will not be guaranteed after MBIST PPR operation. During MBIST mode, only DESELECT command is allowed. The DQ/DQS may either float (Hi-Z) or perform RTT_PARK/DQS_RTT_PARK termination during tSELFTEST depending on vendor specific implementation, while CA/CS/CK ODT will remain unchanged from its programmed state prior to MBIST.

Table 124 — MBIST Timing Parameter

Parameter	Density			Min/Max	Unit	Notes
	8Gb/16Gb	24Gb	32Gb			
tSELFTEST	9	14	19	Max	s	1

Note(s):
1. tSELFTEST applies per logical-rank.

MBIST procedure is detailed in Figure 126.

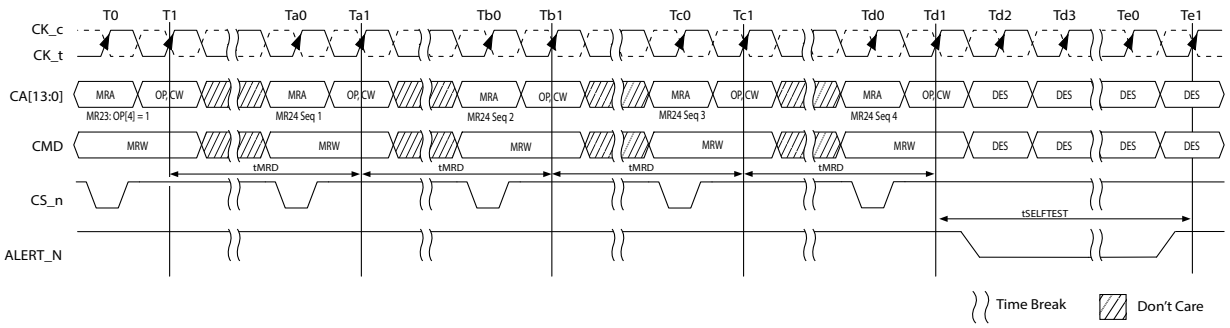


Figure 126 — MBIST Procedure

4.30.2 mPPR Sequence

MBIST-PPR (mPPR) may be used after MBIST in order to repair failures found during the self-test phase. mPPR may only be performed after MR22 MBIST/mPPR transparency is read, and MR22 MBIST/mPPR transparency must be read after mPPR completes in order to determine if an additional mPPR or MBIST is required. If fails remain after the read of MR22 transparency, the mPPR sequence is described as follows:

1. All banks shall be in a precharged and idle state, and CRC mode must be disabled prior to entering mPPR mode.
2. Enable mPPR using MR23:OP[3]=1 and wait tMRD.
3. Issue guard key sequence as four consecutive MR24:OP[7:0] MRW commands each with a unique address field OP[7:0]. Each MRW command must be spaced by tMRD.
4. Issue ACT command with valid address. The DRAM will ignore the address given with the ACT command. Write data is used to select the individual DRAM in the rank for repair. For 3DS devices, CID on the ACT must be set to the same value programmed in MR14:OP[3:0] which determined which logical rank MBIST was last run on.
5. After tRCD, issue WRA with a valid address. The DRAM will ignore the address given with the WRA command. For 3DS devices, CID on the WRA must be set to the same value programmed in MR14:OP[3:0] which determined which logical rank MBIST was last run on.
6. After WL (WL=RL-2), DQ[3:0] of the individual target DRAM must be LOW for 8tCK. Only DRAMs in which most recently have had an MR22 transparency result of 001_B may be considered “target DRAMs”. If more than one DRAM shares the same command bus, DRAMs that are not being repaired must have DQ[3:0] driven HIGH for 8tCK. If all of the DQ[3:0] data bits are neither all LOW or all HIGH for 8tCK, the mPPR mode execution is unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don’t cares. Note that a previous versions of the spec required ALL DQs to be high or low, but this was changed to DQ[3:0] to accomodate ECC UDIMMs and SoDIMMs. Check with the DRAM vendor for their specific implementation.
7. Wait tSELFREPAIR to allow DRAM to self repair the address(es) identified internally by MBIST, and then issue a PREab command.
8. Wait tPGM_exit after PREab command to allow DRAM to update MR22 transparency status.
9. Exit mPPR by setting MR23:OP[3]=0. Wait tPGMPST.
10. Read MR22 transparency status.
11. If additional fails remain, the controller may repeat steps 2-10. If no fails remain or the controller chooses not to perform additional mPPR, the DRAM may continue to the next planned operation.

Figure 127 — mPPR Row Repair

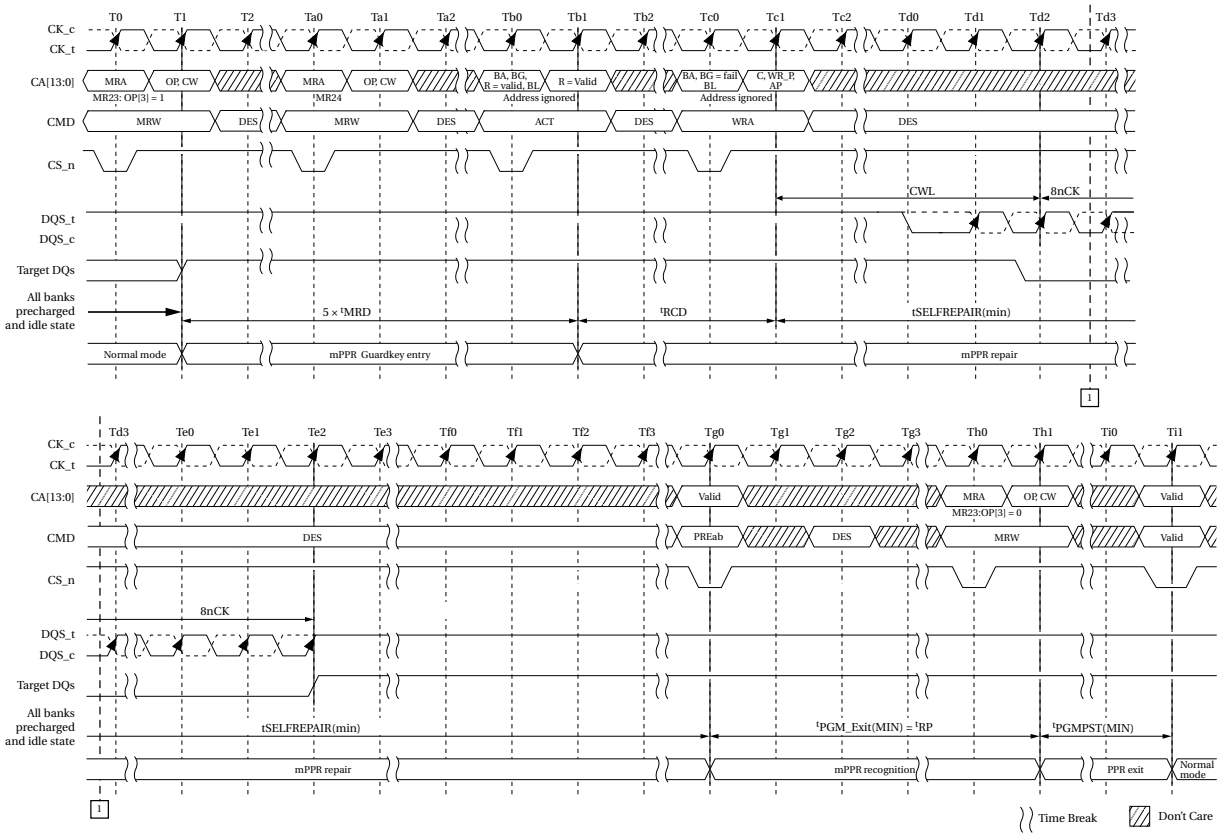
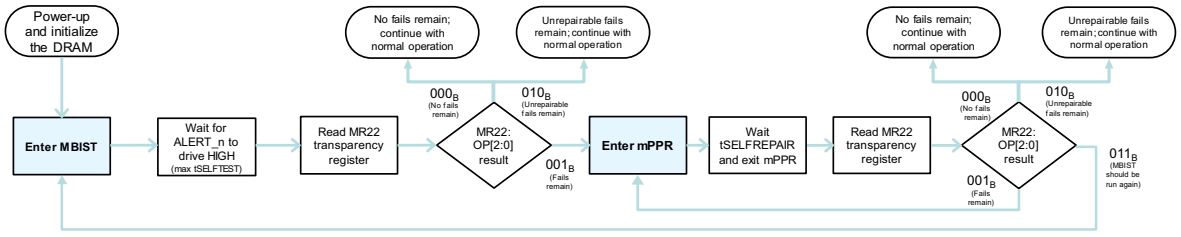


Table 130 — mPPR Timings

Parameter		DDR5-3200 to 5600		Unit	Notes
	Symbol	min	max		
mPPR programming time: x4,x8,x16	tSELFREPAIR	1000	-	ms	

Figure 126 for contains a detailed flow chart of the MBIST/mPPR procedure.

Figure 128 — MBIST/mPPR Flow Chart



Note 1) mPPR may only be performed after an MR22 transparency result of 001_B.

Note 2) 011_B = “MBIST should be run again” indicates that some fails were repaired with mPPR, but MBIST should be run again to load internal fail addresses for mPPR.

Note 3) 011_B = “Unrepairable fails remain” indicates that there are not enough mPPR elements remaining to repair fail addresses latched during MBIST. It may be updated in MR22 after either MBIST or mPPR, depending on vendor implementation.

4.31 Decision Feedback Equalization

4.31.1 Introduction

At data rates >= 2933MT/s, signal degradation due to Inter Symbol Interference (ISI) is expected to increase and the data eye at the DRAM ball is expected to be closed. Since the memory channel is very reflective due to the many impedance mismatched points that exist along the memory subsystem, ISI due to reflections are expected to increase. Traditional methods of characterizing the Receiver using the input eye mask is no longer sufficient. DDR5 requires equalization to help improve (or open up) the data eyes after the data is latched by the receiver. A 4-tap DFE is chosen to help equalize the DQ signals without amplifying the noise due to insertion loss and reflections, which is a common side effect of other equalization techniques (example CTLE). **Figure 129** shows an example of a memory subsystem with DFE circuit included on the DRAM. At the 1980-2100MT/s data rates, the DRAM's DFE shall be disabled. Setting either the Global DFE Gain and Tap 1-4 Enable bits to "Disable" or setting all DFE Gain and Tap 1-4 Bias bits to "Step 0" will disable the DFE.

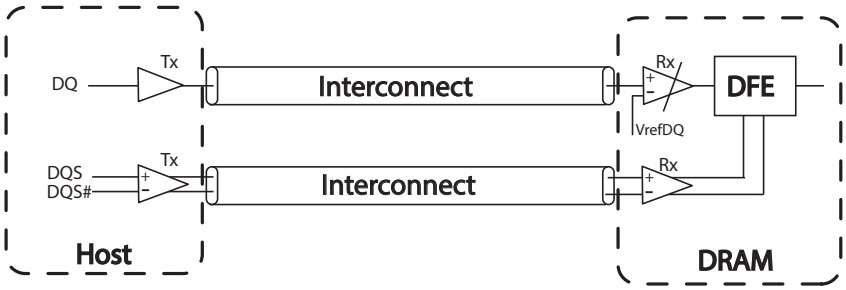


Figure 129 — Example of Memory Subsystem with DFE Circuit on the DRAM

4.31.2 Pulse Response of a Reflective Memory Channel

A reflection dominated channel such as those found in a memory subsystem is anticipated to have substantially reduced data eye at the DRAM ball due to the effects of insertion loss and reflections. Figure represents how a pulse response of a very reflective channel might look like. The attenuation as well as the ringing of the signal can cause the data eye to close at the DRAM ball. Moreover, the ringing can impact future bits that are being sent into the channel, i.e., if the pulse response is for bit n, then the ringing from bit n can impact the signal integrity of future bits n+1, n+2, n+3, n+4, etc. Putting it another way, the signal integrity of any bit, for example bit n, can be impacted by the signals of the previous bits n-1, n-2, n-3, n-4, etc.

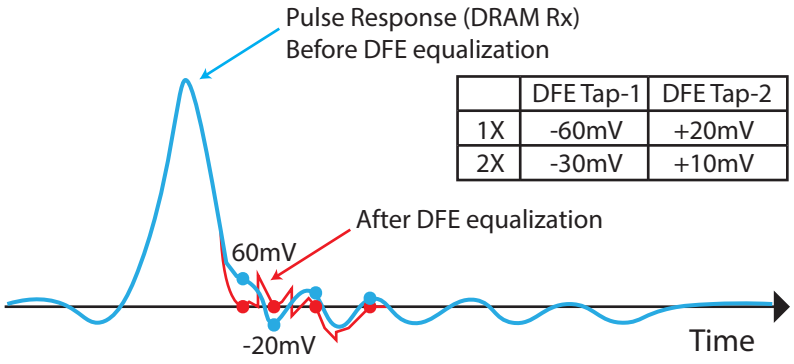


Figure 130 — Example of Pulse Response of a Reflective Channel

4.31.3 Components of the DFE

The 4-tap DFE subsystem consists of a gain amplifier, a DFE summer, 4 DQ slicers (also called Taps) with outputs that loop back to the DFE summer, and a coefficient multiplier for each Tap (**Figure 131**). The gain control of the front end is used to ensure that the cursor or the current bit is in a congruent relationship with the ISI correction required for the channel. The taps T1, T2, T3, T4 coefficients provide the corrections needed to the current bit by adding or subtracting the effects of ISI of the previous bits.

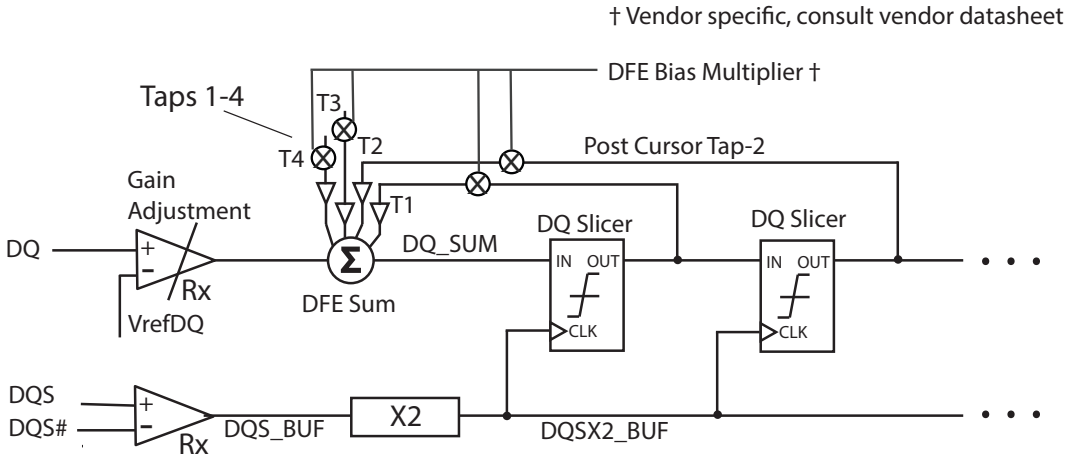


Figure 131 — 4-Tap DFE Example

The Mode Registers shown in **Table 131** and **Table 132** are used by the memory controller to set the strengths of the gain amplifier and the strengths of the correction of the Taps to adapt the ISI cancellation in accordance with the channel performance. Optimal values used for the strengths of the gain amplifier and of the Taps are system dependent, and are usually obtained through a combination of simulations, platform characterizations, and other methods.

Table 131 — Min/Max Ranges for the DFE Gain Adjustment

Description	DDR5 3200-4800			DDR5 5200-6400			Unit	Notes
	Min	Typ	Max	Min	Typ	Max		
DFE Gain Bias Max	6	-	-	6	-	-	dB	1,2,3,4
DFE Gain Bias Min	-	-	-6	-	-	-6	dB	1,2,3,4
DFE Gain Bias Average Step Size		2			2		dB	1,2,3,4
DFE Gain Bias DNL	-1	-	1	-1	-	1	dB	1,2,3,4
DFE Gain Bias INL	-1	-	1	-1	-	1	dB	1,2,3,4
DFE Gain Bias Time	tDFE	-	-	tDFE	-	-	ns	1,2,3,4

Note(s):
1. All parameters are defined over the Vref ranges from 0.5*VDDQ to 0.9*VDDQ
2. DFE Gain Bias are for all voltage and temperature range
3. These values are defined over the entire voltage and temperature range
4. These parameters are suggested to evaluate relative ratio of DFE gain bias settings, and absolute values of all parameters are not subject to silicon validation nor production test.

Table 132 — Min/Max Ranges for the DFE Tap Coefficients

Description	DDR5 3200-4800			DDR5 5200-5600			Unit	Notes
	Min	Typ	Max	Min	Typ	Max		
DFE Tap-1 Bias Max	50	-	-	50	-	-	mV	1,2,4,5,7
DFE Tap-1 Bias Min	-	-	-200	-	-	-200	mV	1,2,4,6,7
DFE Tap-2 Bias Max	75	-	-	75	-	-	mV	2,4,5,7
DFE Tap-2 Bias Min	-	-	-75	-	-	-75	mV	2,4,6,7
DFE Tap-3 Bias Max	60	-	-	60	-	-	mV	2,4,5,7
DFE Tap-3 Bias Min	-	-	-60	-	-	-60	mV	2,4,6,7
DFE Tap-4 Bias Max	45	-	-	45	-	-	mV	2,4,5,7
DFE Tap-4 Bias Min	-	-	-45	-	-	-45	mV	2,4,6,7
DFE Tap Bias Average Step Size	TBD	5	TBD	TBD	5	TBD	mV	2,3,4,7
DFE Tap Bias DNL	-2.5	-	+2.5	-2.5	-	+2.5	mV	2,3,4,7
DFE Tap Bias INL	-2.5	-	+2.5	-2.5	-	+2.5	mV	2,3,4,7
DFE Tap Bias Step Time	tDFE			tDFE			ns	2,3,4

Note(s):
1. As speed increases, the impact of loss from the channel makes the bias range of the first cursor asymmetric
2. Values are defined for the entire voltage, temperature and the Rx Vref range from 0.5*VDDQ to 0.9*VDDQ.
3. Values are identical for Taps 1-4.
4. These parameters are suggested to evaluate relative ratio of DFE Taps 1~4, and absolute values of all parameters are not subject to silicon validation nor production test.
5. For the pulse response shown in Fig 118 (...000010000... pulse pattern), a positive value corrects a negative post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to '0' to apply a positive correction.
6. For the pulse response shown in Fig 118 (...000010000... pulse pattern), a negative value corrects a positive post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to '1' to apply a negative correction. For example, in a memory channel where the ISI during the first post-cursor is dominated by bandwidth loss, the expected tap-1 bias sign bit will be set to '1'.
7. Users refer to DRAM supplier's datasheet to check the multiplier which is applied to the DFE Tap Bias setting (MR113, MR114, MR115, etc.) for total DFE feedback swing implemented in hardware.

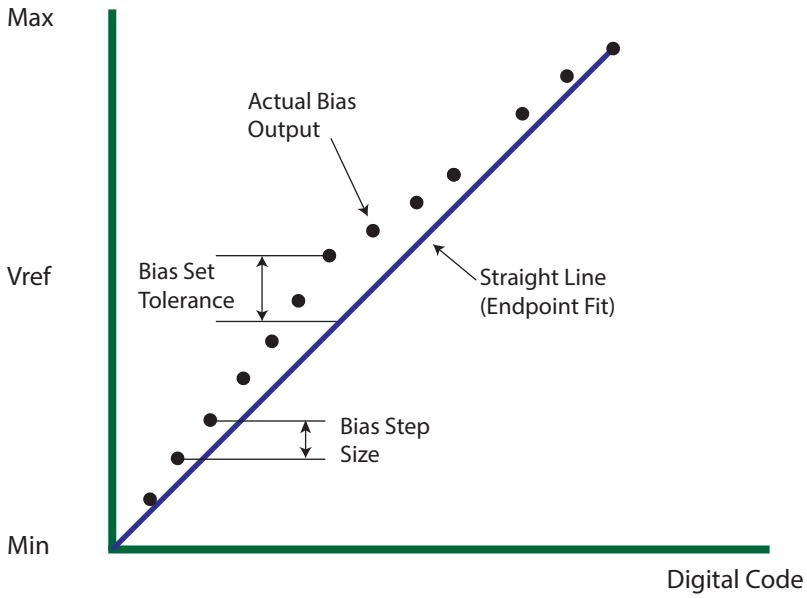


Figure 132 — Example of to be revised for INL/DNL

The DRAM may implement 1-way interleave, 2-way interleave, or 4-way interleave 4-tap DFE memory circuitry. The 1-way interleaved 4-tap DFE architecture (Figure 133) requires a strobe multiplier, which is at Nyquist rate, and the output of the DQ slicer runs at same speed as received data.

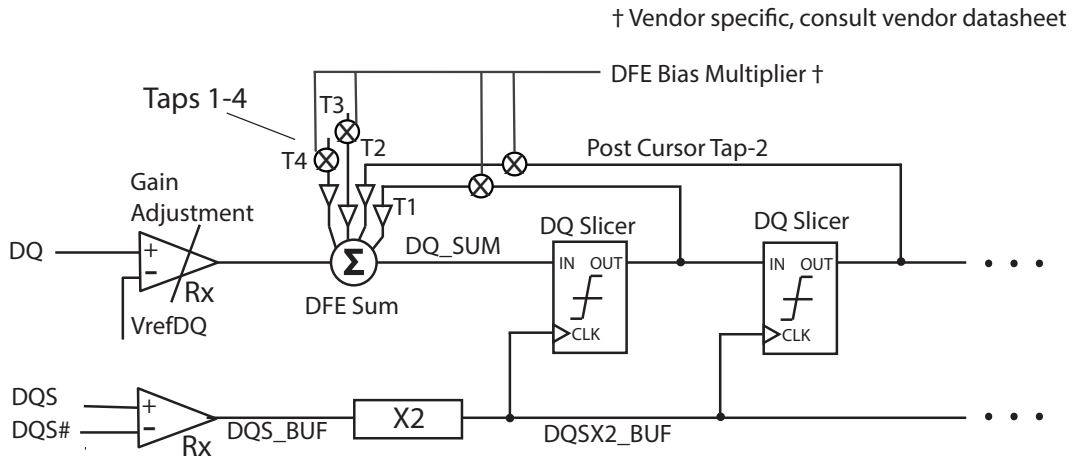


Figure 133 — 1-Way Interleave 4-Tap DFE Example

A 2-way interleaved 4-tap DFE architecture (**Figure 134**) can use the strobe as is. In this case, the output of the DQ slicer runs at half the speed as received data.

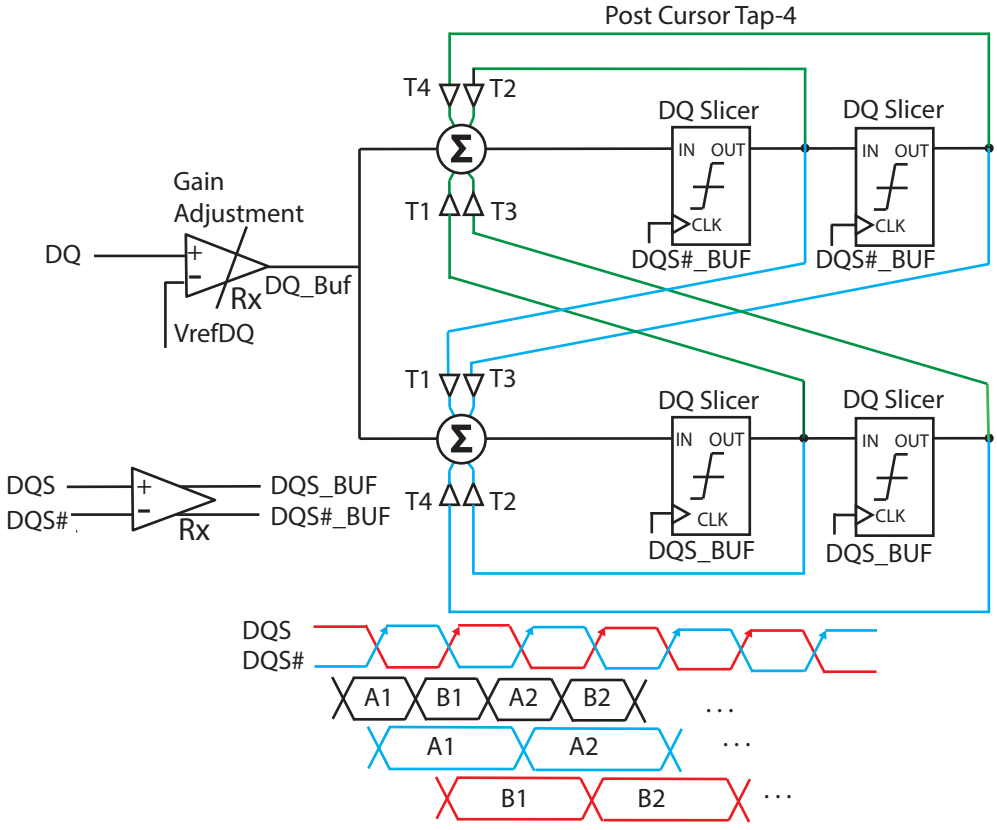


Figure 134 — 2-Way Interleave 4-Tap DFE Example A 4-way interleaved 4-tap DFE architecture (**Figure 135**) requires a divided clock. In this case, the output of the DQ slicer runs at 1/4 the speed as received data.

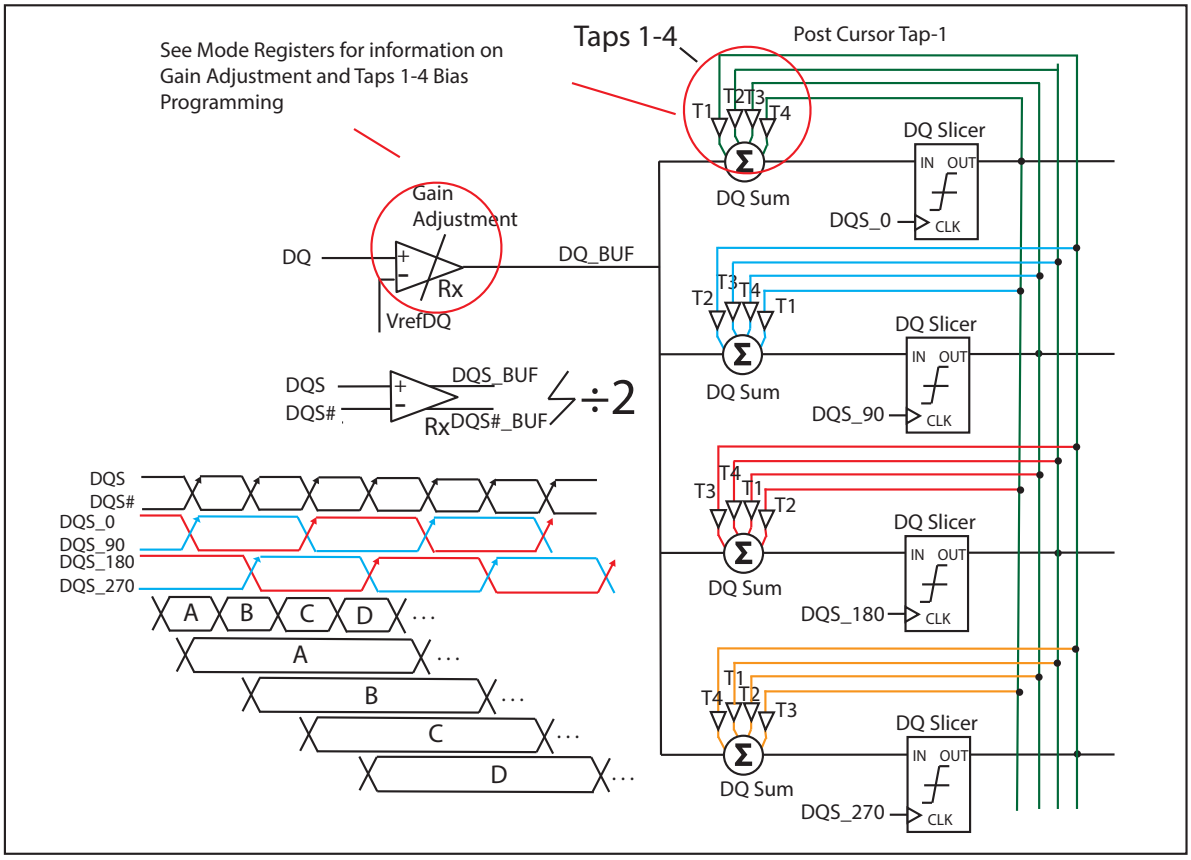


Figure 135 — 4-Way Interleave 4-Tap DFE Example

4.32 DQS Interval Oscillator

As voltage and temperature change on the SDRAM die, the DQS clock tree delay will shift and may require re-training. The DDR5-SDRAM includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error.

The DQS Interval Oscillator is started by issuing an MPC [Start DQS Osc] command with OP[0000 0111B] set as described in the MPC Operation section, which will start an internal ring oscillator that counts the number of times a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator may be stopped by issuing an MPC [Stop DQS Osc] command with OP[0000 0110_B] set as described in the MPC Operation section, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR45,46 & 47 for more information). If MR45 is set to automatically stop the DQS Oscillator, then the MPC [Stop DQS Osc] command shall not be used. When the DQS Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR46 and MR47 after the oscillator is stopped and within tOSCOA for the automatic mode and tOSCOM for the manual mode.

MRW commands to MR45 during an ongoing DQS Interval Oscillator operation are not permitted. MR45 may be reprogrammed tMRD after the oscillator is stopped by the automatic stop.

The DRAM shall respond in one of two ways if an MPC Start DQS Osc is issued during an ongoing DQS Interval Oscillator operation (automatic or manual). One option is the DRAM will ignore the concurrent start command, in which case the DQS Interval Oscillator operation will proceed as normal with all timing constraints referencing the original start command. The other option is for the DRAM to restart the DQS Interval Oscillator operation, in which case all timing constraints will reference the most recent (subsequent) start command. The host must account for the worst-case option in the event that a concurrent start command is issued. If issuing a concurrent MPC [Start DQS Osc] results in a loss of run time tracking, the results stored in MR46 and MR47 should be ignored and the full operation restarted.

Entering Self Refresh during an ongoing DQS Interval Oscillator operation is permitted. Upon exiting Self Refresh, an operation started in automatic mode shall be allowed to complete naturally based upon the specified number of clocks (cumulative before and after Self Refresh). If a manual operation started prior to entering Self Refresh is not stopped prior as well, the operation shall be manually stopped upon Self Refresh exit. The results stored in MR46 and MR47 for a DQS Interval Oscillator operation that spans Self Refresh entry/exit should be ignored and the full operation restarted.

The controller may adjust the accuracy of the result by running the DQS Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\textit{DQS Oscillator Granularity Error} = \frac{\textit{2 * (DQS delay)}}{\textit{Run Time}}$$

Where:
Run Time = total time between start and stop commands
DQS delay = the value of the DQS clock tree delay (tRX_DQS2DQ min/max)

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific.

Therefore, the total accuracy of the DQS Oscillator counter is given by:

$$\textit{DQS Oscillator Accuracy} = 1 - \textit{Granularity Error} - \textit{Matching Error}$$

Example: If the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 400ps (tRX_DQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (0.4ns)}{100ns} = 0.8\%$$

This equates to a granularity timing error of 3.2ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\textit{DQS Oscillator Accuracy} = 1 - \frac{3.2 + 5.5}{400} = 97.8\%$$

Example: Running the DQS Oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 250ns, and the maximum DQS clock tree delay is 400ps (tRX_DQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (0.4ns)}{250ns} = 0.32\%$$

This equates to a granularity timing error or 1.28ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\textit{DQS Oscillator Accuracy} = 1 - \frac{1.28 + 5.5}{400} = 98.3\%$$

The result of the DQS Interval Oscillator is defined as the number of DQS Clock Tree Delays that can be counted within the “run time,” determined by the controller. The result is stored in MR46 and MR47. MR46 contains the least significant bits (LSB) of the result, and MR47 contains the most significant bits (MSB) of the result. MR46 and MR47 are overwritten by the SDRAM when an MPC-1 [Stop DQS Osc] command is received. The SDRAM counter will count to its maximum value (=2^16) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest “run time” for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\textit{Longest Run Time Interval} = 2^{16} * \textit{tRX\_DQS2DQ(min)}$$

The interval oscillator matching error is defined as the difference between the DQS training circuit (interval oscillator) and the actual DQS clock tree across voltage and temperature.

- Parameters:
  - tRX_DQS2DQ: Actual DQS clock tree delay
  - tDQSOSC: Training circuit (interval oscillator) delay
  - OSCOffset: Average delay difference over voltage and temp
  - OSCMatch: DQS oscillator matching error

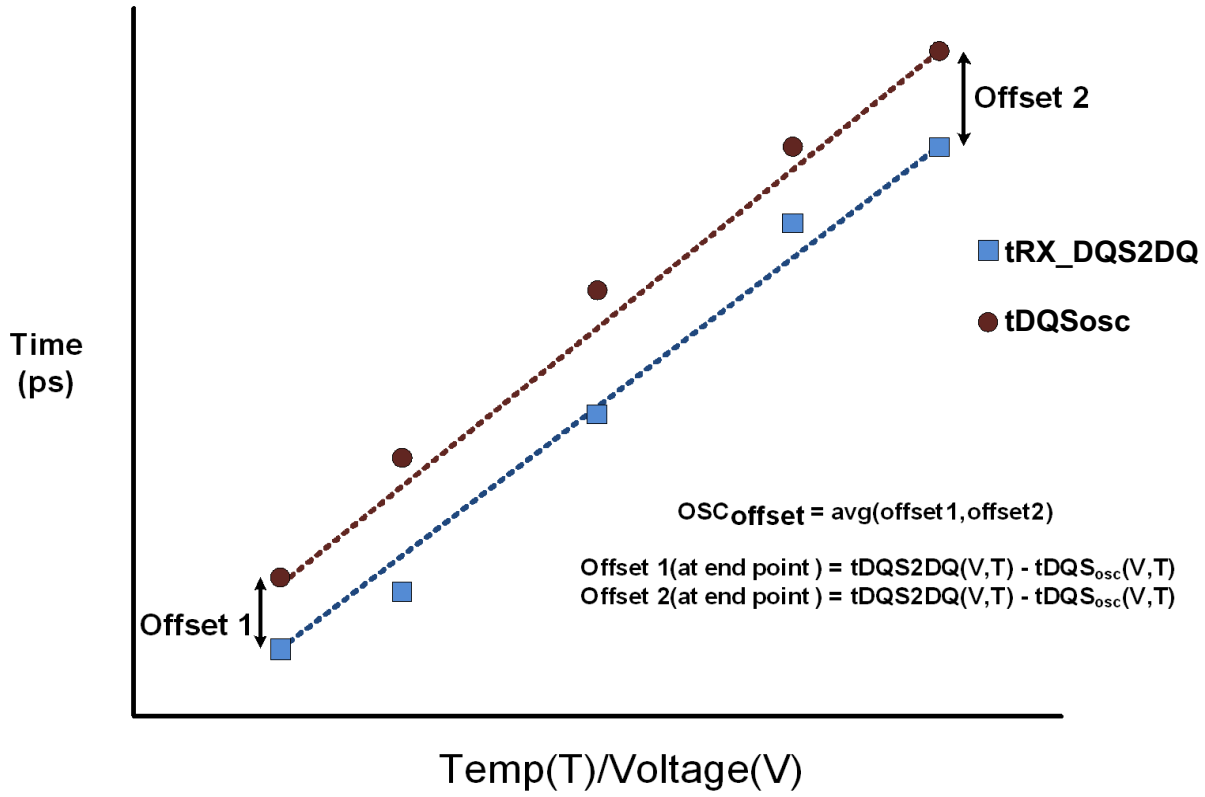


Figure 136 — Interval oscillator offset (OSC_{offset})

- OSC_{Match}:

$$OSC_{Match} = [tRX\_DQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

- $tDQS_{OSC}$:

$$tDQS_{OSC(V,T)} = \frac{Runtime}{2 * Count}$$

Table 133 — DQS Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Units	Notes
DQS Oscillator Matching Error	OSCMatch	-10	+10	ps	1,2,3,4,5,6,7,8
DQS Oscillator Offset	OSC_{offset}	-150	150	ps	2,4,6,7

Note.

1. The OSC_{Match} is the matching error per between the actual DQS and DQS interval oscillator over voltage and temp.
2. This parameter will be characterized or guaranteed by design.
3. The OSC_{Match} is defined as the following:

$$OSC_{Match} = [tRX\_DQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

Where $tRX\_DQS2DQ_{(V,T)}$, $tDQS_{OSC(V,T)}$ and $OSC_{offset(V,T)}$ are determined over the same voltage and temp conditions.

4. The runtime of the oscillator must be at least 200ns for determining $tDQS_{OSC(V,T)}$

$$tDQS_{OSC(V,T)} = \frac{Runtime}{2 * Count}$$

5. The input stimulus for tRX_DQS2DQ will be consistent over voltage and temp conditions.
6. The OSCoffset is the average difference of the endpoints across voltage and temp.
7. These parameters are defined per channel.
8. tRX_DQS2DQ(V,T) delay will be the average of DQS to DQ delay over the runtime period.
9. The matching error and offset of OSC came from DQS2DQ interval oscillator.

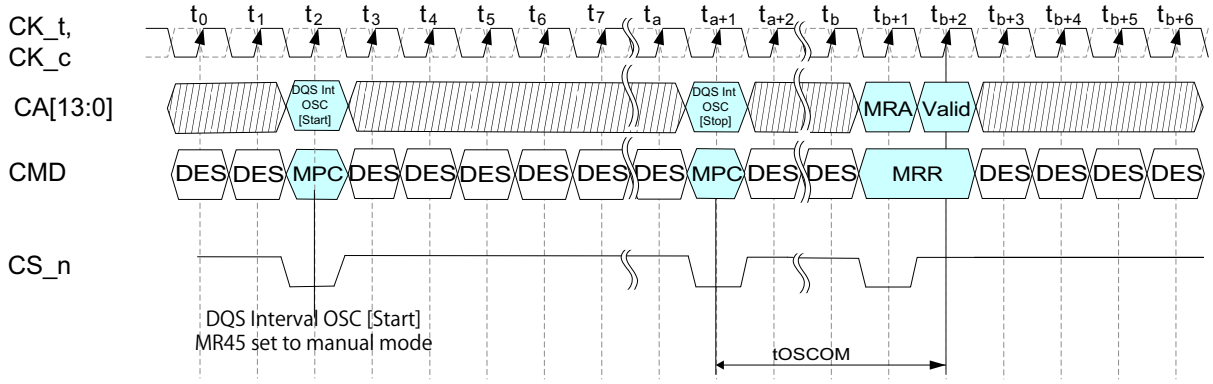
The interval oscillator count read out timing

Table 134 — DQS Interval Oscillator Read out AC Timing

Parameter	Symbol	DDR5-3200 to 4800		DDR5-5200 to 5600		Unit	Notes
		Min	Max	Min	Max		
Delay time from DQS Interval Oscillator stop to Mode Register Readout in manual mode	tOSCOM	tMPC_Delay	-	tMPC_Delay	-	nCK	
Delay time from DQS Interval Oscillator automatic mode timer expiration to Mode Register Readout	tOSCOA	tMRD	-	tMRD	-	nCK	
DQS Interval Oscillator start gap in automatic stop mode	tOSCS	tMPC_Delay + DQS Interval Timer Run Time				nCK	

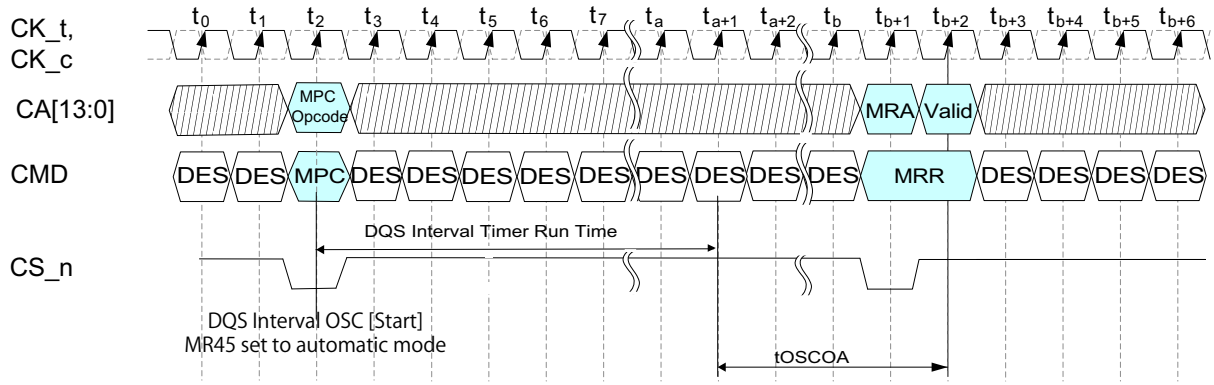
Note(s):
1. In manual stop mode, DQS osc start command should be followed by DQS osc stop command (MPC). Otherwise, DQS osc result value (MR46 & MR47) cannot be guaranteed.

Figure 137 — DQS Interval Oscillator Manual Mode Timing Diagram



Note(s):
1. DES commands are shown for erase of illustrator; other commands may be valid at these times.

Figure 138 — DQS Interval Oscillator Automatic Mode Timing Diagram



Note(s):
1. DES commands are shown for ease of illustration; other commands may be valid at these times.

4.33 tRX_DQS2DQ Offset due to Temperature and Voltage Variation

As temperature and voltage change on the SDRAM die, the DQS clock tree will shift and may require retraining. The oscillator is usually used to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The tRX_DQS2DQ offset due to temperature and voltage variation specification can be used for instances when the oscillator cannot be used to control the tRX_DQS2DQ.

Table 135 — tRX_DQS2DQ Offset Due to Temperature and Voltage Variation for DDR5-4400 to 4800

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
tRX_DQS2DQ_temp	DQS to DQ offset temperature variation	-	9.28	-	8.50	ps/10℃	1,3
tRX_DQS2DQ_volt	DQS to DQ offset voltage variation	-	39.00	-	32.00	ps/50mV	2,3

Notes:
1. tRX_DQS2DQ max delay variation as a function of temperature
2. tRX_DQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD. It includes the VDDQ and VDD AC noise impact for frequencies >20MHz and max voltage of 45mVpk-pk from DC -20MHz at a fixed temperature on the package. For tester measurement VDDQ=VDD is assumed
3. Absolute value of DQS to DQ offset

Table 136 — tRX_DQS2DQ Offset Due to Temperature and Voltage Variation for DDR5-5200 to 5600

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
tRX_DQS2DQ_temp	DQS to DQ offset temperature variation	-	7.85	-	7.29	ps/10℃	1,3
tRX_DQS2DQ_volt	DQS to DQ offset voltage variation	-	30.00	-	28.00	ps/50mV	2,3

Notes:
1. tRX_DQS2DQ max delay variation as a function of temperature
2. tRX_DQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD. It includes the VDDQ and VDD AC noise impact for frequencies >20MHz and max voltage of 45mVpk-pk from DC -20MHz at a fixed temperature on the package. For tester measurement VDDQ=VDD is assumed
3. Absolute value of DQS to DQ offset.

4.34 2N Mode

2N mode allows the system to provide more setup and hold time on the CA bus. 2N mode is enabled by default on the DDR5 SDRAM, and an MPC is used to change between 2N and 1N modes. MR2:OP[2] allows the state of the 2N Mode to be read.

DDR5 has defined two cycle commands, which requires the DRAM to capture the command differently between 1N and 2N modes. In both modes, the first half of the command is sampled on the clock that the chip select is active. In 1N mode, the second half of the command is sampled on the next clock edge. In 2N mode, the second half of the command is sampled 2 clocks after the first half. Non-target ODT signaling (on the chip select) is also delayed by a clock in 2N mode.

To the DRAM, one clock commands operate the same in 1N and 2N mode, with the command sampled on the same clock as the chip select active.

A 2-cycle or 1-cycle command can start on any clock (unlike geardown mode). Figure 139 below shows the differences between standard 1N mode with a 2-cycle read command, followed by a 1-cycle precharge command, and what it looks like when operated in 2N mode with the same commands. While in 2N mode, the host will never send two consecutive Chip Selects except during explicit cases such as exiting CATM mode.

Table 137 — MR2 Functional Modes (for reference only)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Savings Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training

OP(0-7) can be programed with either “0” or “1”.

Table 138 — 2N Mode Register Config

Function	Register Type	Operand	Data	Notes
2N Mode	R	OP[2]	0B: 2N Mode (Default) 1B: 1N Mode	1, 2

1 - To ensure training modes can be enabled and run appropriately, the default (power-on) mode for DDR5 is 2N mode. Post CA Training, the user can configure this bit to put the device into either 1N mode or 2N mode. Both 1N and 2N modes are valid operating conditions for DDR5.

2 - Since 2N Mode setting is an MPC based command, it can only be programmed via that command and its mode register is therefore read only.

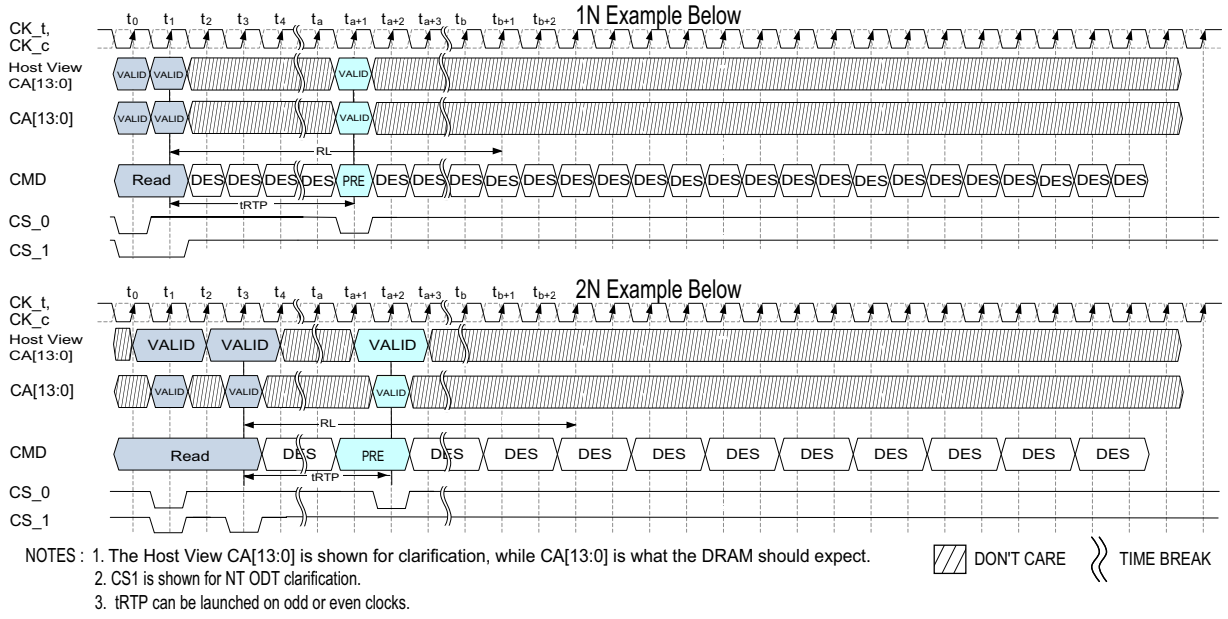


Figure 139 — Example of 1N vs 2N Mode - For reference only

4.34.1 1N / 2N Mode Clarifications

Several DDR5 SDRAM features require specific CS_n and CA bus behavior to function correctly in 1N and 2N mode. Table 139 below describes the various behaviors (additional details in the respective sections of the spec).

Table 139 — CS_n and CA Bus Required Behaviors

	CS Assertion Duration	CS_n Required Behavior for 1N	CS_n Required Behavior for 2N	CA Bus Required Behavior for Multi-Cycle CS Assertion / 2N
Cold or Warm Reset Exit	Multi (default)	NA	Static low for 3+ nCK	Static NOP for 3+ nCK
MPC (includes CSTM Exit)	Single	Single low pulse	Single low pulse	Single MPC
	Multi	Static multi-cycle low	Static multi-cycle low	Static MPC surrounding CS_n low by tMC_MPC_*
VREFCS / VREFCA	Single	Single low pulse	Single low pulse	Single VREFCS / VREFCA
	Multi	Static multi-cycle low	Static multi-cycle low	Static VREFCS / VREFCA surrounding CS_n low by tMC_VREFCS_* / tMC_VREFCA_*
CATM exit (NOP Command)	Don't care	Static low for 2+ nCK	Static low for 2+ nCK	Static NOP for the duration of tCATM_CS_Exit
PDX	Don't care	Single low pulse	Single low pulse	Single NOP
SRX (3 NOPs)	Don't care	Static low for 3+ nCK	Static low for 3+ nCK	Static NOP for 3+ nCK if CS_n held static low
		Pulsing low 3+ cycles (...0, 1, 0, 1, 0...)	Pulsing low 3+ cycles (...0, 1, 0, 1, 0...)	Static NOP for 5+ nCK if CS_n is pulsed low

Note 1 - MR2:OP[4], CS Assertion Duration, setting only applies to the MPC, VREFCS and VREFCA commands.

4.35 Write Pattern Command

Due to the significant percentage of writes that contain all zeros, this new mode is being proposed for inclusion into the DDR5 specification as a new WRITE Pattern command. When used effectively, the command can save power by not actually sending the data across the bus.

This new mode is operated very similar to a standard write command with the notable exceptions that it has its own encoded WRITE Pattern command, no data is sent on the DQ bus, no toggling of DQS is needed, and the DRAM does not turn on any internal ODT. ECC parity is based on the Write Pattern Mode data in MR48.

Upon receiving the command, the DRAM device will source the input for the memory array from the Write Pattern Mode Registers instead of from the DQ bits themselves. The DQ mapping across the burst is shown below in DQ output mapping table. The host will not send any data during this time. All timing constraints are still measured from the clocks where the write command data would have been transferred. e.g. tWR is measured from end of write burst to PRE as shown below in Figure 140. The pattern used for this mode is provided by the contents of MR48:OP[7:0]. That pattern can be all zeros, all ones, or something else, and can be changed with an MRW command to MR48. The power on default for this mode register is all zeros.

Table 140 — Write Pattern Mode Register

MR Address	WRITE Pattern	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR48	UI	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Valid

NOTES:

1. OP[7:0] can be independently programmed with either “0” or “1”.
2. Default is all zeros for OP[7:0]
3. If CRC is enabled, ALERT_n will not be issued from the DRAM during Write Pattern mode, and tCCD_S=9tCK should be satisfied..

The DQ output mapping table below describes how the pattern stored in MR48 above will be mapped into the DRAM array across the DQ bits and Burst. The pattern is described as follows:

In the case of a x4 SDRAM device, only OP[3:0] will used, with each bit of the pattern corresponding to DQ[3:0] respectively. The same OP value will be repeated over the entire burst for that bit (i.e. DQ0 store OP0 on every UI of the burst). Although OP[7:4] are not used for the x4, the original programmed MRW values will still be read during an MRR. OP[7:4] will not revert back to the default of zero.

In the case of a x8 SDRAM device, the whole pattern OP[7:0] will be used, with each bit of the pattern corresponding to DQ[7:0] respectively. The same OP value will be repeated over the entire burst for that bit. (i.e. DQ0 store OP0 on every UI of the burst)

In the case of a x16 SDRAM device, the whole pattern OP[7:0] will be used, with each bit of the pattern corresponding to DQL[7:0] respectively and then that pattern will be repeated for DQU[7:0]. The same OP value will be repeated over the entire burst for that bit. (i.e. DQ0 store OP0 on every UI of the burst)

The Burst Length (BL) supported in Write Pattern Mode is based on MR0 OP[1:0]. The Write Pattern Command (WRP) does not support On-The-Fly (OTF), resulting in the output values being either a fixed BL16 or BL32.

Table 37 - Write Pattern DQ output mapping

SDRAM CONFIG	BL16 x16	BL16 x8	BL16 x4	BL32 x4
UI	0-15	0-15	0-15	0-31
DQL0 / DQ0	OP0	OP0	OP0	OP0
DQL1 / DQ1	OP1	OP1	OP1	OP1
DQL2 / DQ2	OP2	OP2	OP2	OP2
DQL3 / DQ3	OP3	OP3	OP3	OP3
DQL4 / DQ4	OP4	OP4	-	
DQL5 / DQ5	OP5	OP5	-	
DQL6 / DQ6	OP6	OP6	-	
DQL7 / DQ7	OP7	OP7	-	
DQU0	OP0	-	-	
DQU1	OP1	-	-	
DQU2	OP2	-	-	
DQU3	OP3	-	-	
DQU4	OP4	-	-	
DQU0	OP5	-	-	
DQU6	OP6	-	-	
DQU7	OP7	-	-	
DML_n / DM_n	INVALID	INVALID	-	
DMU_n	INVALID	-	-	

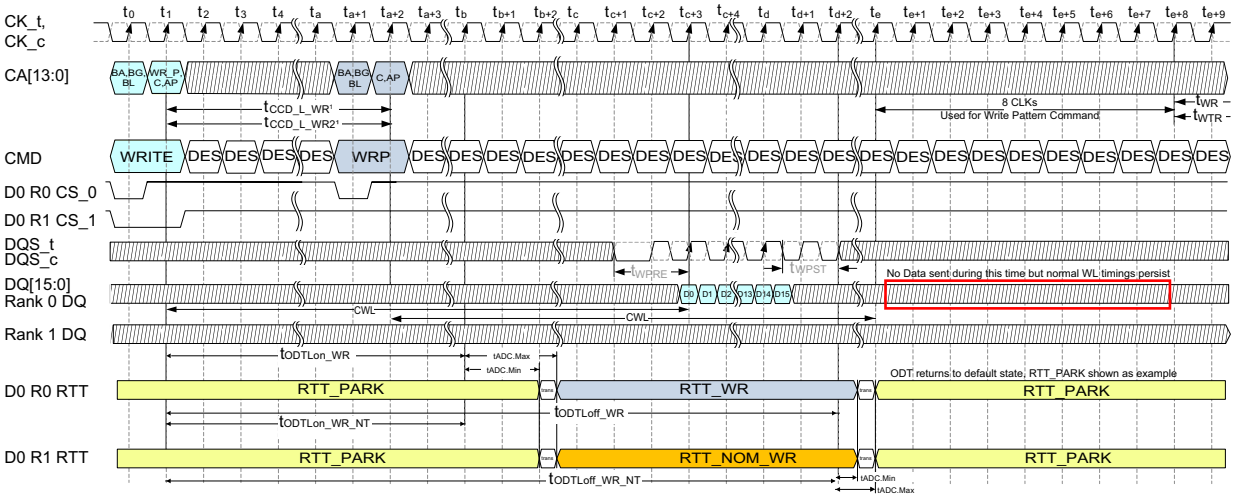


Figure 140 — Example of Write Pattern Command

Note(s):
1. Refer to Table 48, Table 49 and Table 50 to determine if the timing parameter definition for WRITE to WRP is tCCD_L_WR or tCCD_L_WR2.

4.36 On-Die ECC

DDR5 devices shall implement internal Single Error Correction (SEC) ECC to improve the data integrity within the DRAM. The DRAM shall use 128 data bits to compute the ECC code of 8 ECC Check Bits.

For a x4 DDR5 device, internal prefetch for on-die ECC is 128 bits even though a x4 is a 64-bit prefetch device. For each read or write transaction in a x4 device, an additional section of the DRAM array is accessed internally to provide the required additional 64 bits used in the 128-bit ECC computation. In other words, in a x4 device, each 8-bit ECC Check Bit word is tied to two 64-bit sections of the DRAM. In the case of a x8 device, no extra prefetch is required, as the prefetch is the same as the external transfer size. For a x16 device, two 128-bit data words and their corresponding 8 check bits are fetched from different internal banks(same external bank address). Each 128 Data bits and the corresponding 8 check bits are checked separately and in parallel.

On reads, the DRAM corrects any single-bit errors before returning the data to the memory controller. The DRAM shall not write the corrected data back to the array during a read cycle.

On writes, the DRAM computes ECC and writes data and ECC bits to the array. If the external data transfer size is smaller than the 128 data bits code word (x4 devices), then DRAM will have to perform an internal 'read-modify-write' operation. The DRAM will correct any single-bit errors that result from the internal read before merging the incoming write data and then re-compute 8 ECC Check bits before writing data and ECC bits to the array. In the case of a x8 and x16 DDR5, no internal read is required.

For a x16 device, two 136-bit code words are read from two internal banks(same external bank address), one code word is mapped to DQ[0:7] and the other code word is mapped to DQ[8:15].

4.36.1 SEC Overview

The ECC blocks show in Figure 141 are the ECC Check Bit Generator, Syndrome Generator, Syndrome Decode and Correction. The Check Bit Generator and Syndrome Generator blocks are fully specified by the H matrix.

The Syndrome Decode block executes the following function:

Zero Syndrome => No Error

Non-Zero Syndrome matches one of the columns of the H matrix => Flip Corresponding bit

Non-Zero Syndrome that does not match any of the columns in the H matrix => DUE

DUE: Detected Uncorrected

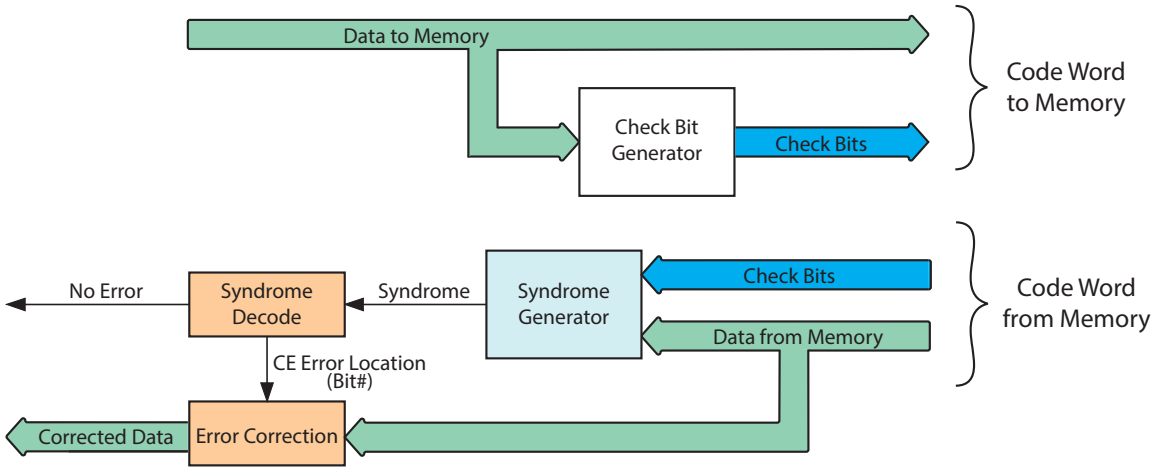


Figure 141 — On Die ECC Block Diagram

4.37 DDR5 ECC Transparency and Error Scrub

DDR5 ECC Transparency and Error Scrub incorporates an ECC Error Check and Scrub (ECS) mode with an error counting scheme for transparency. The ECS mode allows the DRAM to internally read, correct single bit errors, and write back corrected data bits to the array (scrub errors) while providing transparency to error counts. It is recommended that a full error scrub of the DRAM is performed a minimum of once every 24 hours.

There are two options for ECS mode, set via Mode Register. The Manual ECS mode (MR14:OP[7] = 1_B) allows for ECS operations via the Multi-Purpose Command. The Automatic ECS mode (MR14:OP[7] = 0_B, default setting) allows for the ECS to run internal to the DRAM.

The ECS feature is available on all device configurations.

ECS mode implements two counters to track ECC code word errors detected during operation: Error Counter (EC) and Errors per Row Counter (EpRC). The EC defaults to counting rows with errors; however, it may also be configured to count code words with errors. In row mode (default), the EC tracks the number of rows that have at least one code word error detected subject to a threshold filter. In the code word mode, the EC tracks the total number of code word errors, also subject to the threshold filter. The second counter, EpRC, tracks the error count of the row with the largest number of code word errors along with the address of that row. EpRC error reporting is also subject to a separate threshold filter. A general functional block diagram example of the ECS Mode operation is shown in Figure 142 while the ECC Error Checking and Scrub mode, Mode Register (MR14), is shown in Table 141 below.

Figure 142 — Example of an ECC Transparency and Error Scrub Functional Block Diagram

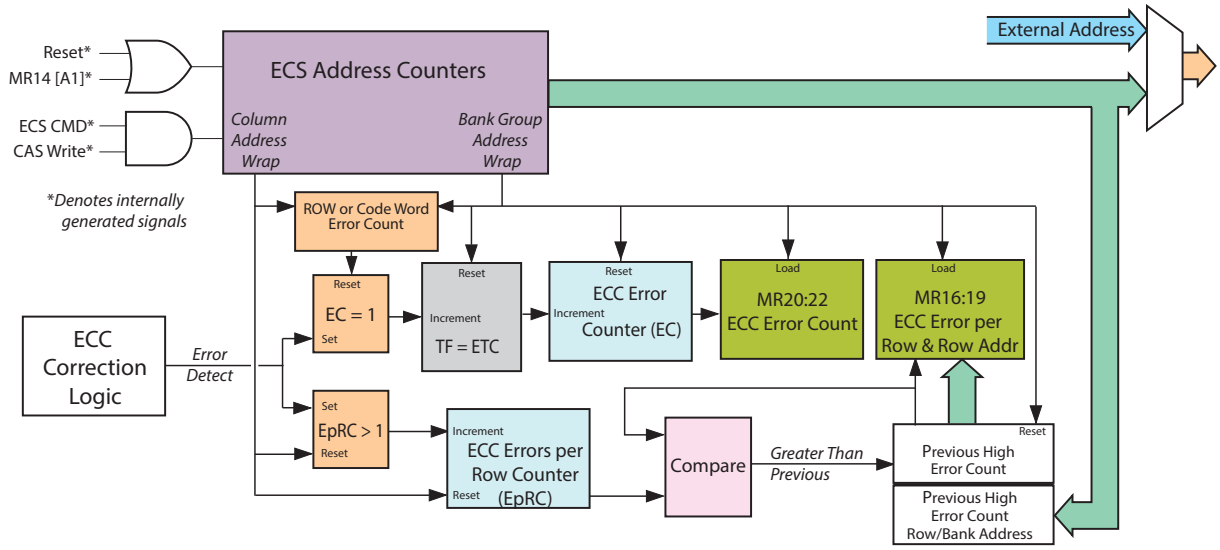


Table 141 — MR14 ECC Transparency and Error Scrub Mode Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECS Mode	Reset ECS Counter	Row Mode/ Code Word Mode	RFU	CID3	CID2	CID1	CID0

4.37.1 Mode Register and DRAM Initialization Prior to ECS Mode Operation

The ECC Transparency and Error Scrub counters are set to zero and the internal ECS Address Counters are initialized either by a RESET or by manually writing MR14 OP[6]=1_B. While MR14:OP[6]=1_B, ECS counters are reset and no additional ECS operations shall occur. If manual reset via mode register is utilized, mode register bit MR14 OP[6] shall be written back to a 0 before any subsequent ECS operations will continue or a subsequent reset can be applied.

ECS mode selections, MR15 OP[3], Automatic ECS in Self-Refresh, MR14 OP[7], Manual/Automatic ECS Mode, and MR14 OP[5], row/code word mode shall be programmed during DRAM initialization and shall not be changed once the first ECS operation occurs unless followed by issuing a RESET or ECS Reset Counters, otherwise an unknown operation could result during subsequent ECS operations.

An ECS Reset Counters operation requires setting MR14:OP[6]=1_B to reset MR16 - MR20. Setting MR14:OP[6]=0_B is then required to re-enable Manual or Automatic ECS operations.

Manual ECS mode is enabled by MR14 OP[7] = 1_B. A manual ECS operation requires an MPC command with OP[7:0]=0000 1100_B.

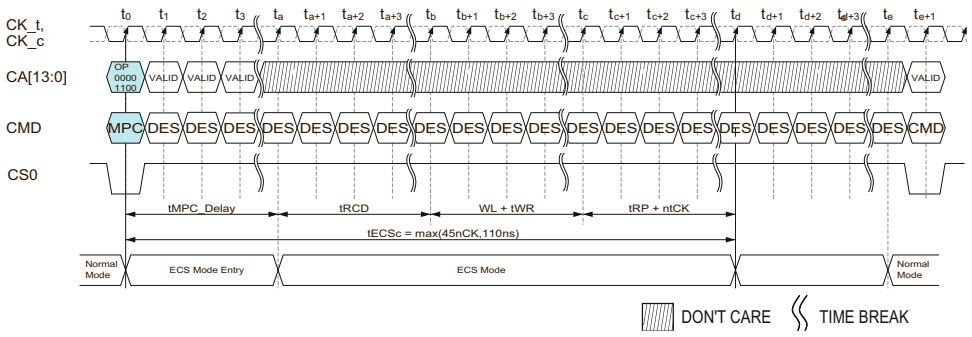
The DRAM must have all array bits written to prior to executing ECS operations to avoid generating false failures.

4.37.2 ECS Operation

All banks shall be precharged and in an idle state prior to executing a manual ECS operation.

Executing a manual ECS operation, MPC command with OP[7:0]=0000 1100_B, generates the following internally self-timed command sequence: ACT→RD→WR→PRE. ECS operation timing is shown in Figure 143.

Figure 143 — ECS Operation Timing Diagram



ECS Mode Timing Diagram

The minimum time for the ECS operation to execute is t_{ECSc} (t_{MPC_Delay} + t_{RCD} + WL + t_{WR} + t_{RP} + nt_{CK}). nt_{CK} is required to satisfy t_{ECSc}.

Table 142 — ECS Operation Timing Parameter

Parameter	Symbol	Min	Max	Unit	NOTE
ECS Operation time	t_{ECSc}	Max(176nCK, 110ns)	-	ns	

Upon executing a manual ECS operation. DQ's will remain in RTT_PARK and DQS in DQS_RTT_PARK. The only commands allowed other than DES during t_{ECSc} for a manual ECS operation are ODT NT commands, which may change the DQ and DQS termination state.

Any illegal usage of manual ECS mode (e.g. refresh or temperature violations) will result in operation not being guaranteed.

Executing a manual ECS operation by an MPC command with OP[7:0]=0000 1100_B will issue an internally timed ACT command row activation based on the internal ECS Address Counters' row address, t_{MPC_Delay} after the MPC command. The ACT command is to

be followed by a WR command t_{RCD} later. The WR command will perform an internal Read-Modify-Write cycle on the code word determined by the internal ECS Address Counters' column address.

The internal Read-Modify-Write cycle will:

1. Read the entire code word (128 data bits and 8 check bits) from the array
2. Correct a single bit error in the code word or check bits, if an error is detected
3. Write the resultant code word back to the DRAM array

The WR command is followed by a PRE command WL + t_{WR} later. The PRE command will automatically re-enable the DRAM's I/Os and address inputs, and it will return the DRAM to idle mode t_{RP} + nt_{CK} later, after t_{ECSc} is satisfied.

For each ECS operation, ECS Address Counters increment the column address after each internal ECS WR command such that the next code word and check bits are selected. Once the column counter wraps (all code words and check bits on the row have been accessed), the row counter will increment until all code words on each of the rows within a bank are accessed. When the row counter wraps (all rows within the bank have been accessed), the bank counter will increment and the next bank within a bank group will repeat the process of accessing each code word. When the bank counter wraps, the bank group counter will increment and the next bank group will repeat the process of accessing each code word, until all bank groups within the DRAM have been accessed.

After all the code words within the DRAM are read, corrected, and written once, the bank group counter will wrap and the process begins again with the next manual ECS operation. The total number of manual ECS operations required to complete one cycle of Error Check and Scrub is density and configuration dependent, as listed in Table 143 below. The DRAM controller shall track the number of manual ECS operations to complete a full scrub of that device.

Table 143 — Number of Code Words Per DRAM

Configuration	16Gb
x4, x8, x16	2^27

In order to complete a full Error Check and Scrub within the recommended 24 hours, the average periodic interval per ECS operation (t_{ECSint}) is 86,400 seconds divided by the total number of manual ECS operations to complete one full cycle of ECS. t_{ECSint} is included in Table 144.

Table 144 — Average Periodic ECS Interval (tECSint)

Configuration	16Gb
x4, x8, x16	0.644mS

In order for the DDR5 SDRAM to perform automatic ECS operations when in Automatic ECS Mode, the host needs to issue periodic REFab commands or periodically enter Self Refresh mode. The maximum spacing between REFab commands or Self Refresh entry for the DRAM to complete the automatic scrub within the recommended 24 hours is t_{ECSint}. Meeting this REFab/Self-Refresh requirement allows the DRAM to perform the automatic ECS operations without placing additional restrictions on refresh mode usage, i.e. all bank/same bank refresh or normal/FGR mode refresh, while in Automatic ECS mode. REFab commands issued in excess of required by the DRAM for automatic ECS operations (one per t_{ECSint}) may be used by the DRAM for normal refresh operation. Issuing multiple REF commands shall not exceed the total number allowed within a 1 x tREFI window, as described in the Refresh Operation Scheduling Flexibility section of the spec.

When in Automatic ECS mode, the ECS commands and timing are generated and satisfied internal to the DRAM, following the Average Periodic ECS Interval timings to ensure that the Error Check and Scrub is completed and the transparency registers (MR16-20) are updated within the recommended 24-hour period.

The DRAM is required to perform automatic ECS operations while in Self Refresh mode if Automatic ECS is enabled by MR14 OP[7]=0_B or Automatic ECS in Self-Refresh is enabled by MR15 OP[3]=1_B, to meet the Average Periodic ECS Interval timings. However, some variation in the DRAM scrubbing rate may be encountered while in Self Refresh since the DRAM will need to sync the internal operations to an internal oscillator fre-quency. Entering and exiting Self Refresh will not reset the ECS transparency counters/registers. Interval timing for the maximum spacing between REFab commands or another Self Refresh entry is allowed to restart upon Self Refresh exit.ECS Threshold Filter

The ECC Transparency and Error Scrub scheme incorporates a user programmable ECS Threshold Filter that masks error counts less than the programmed filter value. The value is set using MR15 as listed in Table below. The default MR15 setting is 256 fails per Gb of memory cells (OP[2:0] = 011B).

Table 145 — MR15 Transparency ECC Error Threshold Count per Gb of Memory Cells and Automatic ECS in Self-Refresh

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				Automatic ECS in Self-Refresh	OP[2:0]: 000_B = 4 OP[2:0]: 001_B = 16 OP[2:0]: 010_B = 64 OP[2:0]: 011B = 256 (Default) OP[2:0]: 100B = 1024 OP[2:0]: 101B = 4096 OP[2:0]: 110B = RFU OP[2:0]: 111B = RFU		

4.37.3 ECS Error Tracking

The type of error tracking provided by the ECC Transparency and Error Scrub is selectable using MR14 OP[5], which can track either the number of rows (default) or code words with errors using the Error Counter. The row or code word error count will be tracked and written to MR20 register. MR14 OP[5] is programmed during DRAM initialization and should not be changed once the first ECS command has been issued, otherwise an unknown operation could result. If MR14 OP[5] is changed without powering down, a MR14 OP[6] reset shall be issued prior to subsequent ECS commands to reinitialize the counters.

When the ECC row count mode is selected, the Error Counter (EC) increments each time a row with check bit errors is detected. After all rows, in all banks, in all bank groups have ECS operations performed, the result of the Error Counter is loaded into MR20, subject to error threshold reporting. The EC is reset after the value has been transferred to the mode register.

MR20 is shown in Table 146. EC[7:0] indicate error counts within a range. EC0 is set to "1" if $EC0_{min}$ (the ETC set by MR15) has been reached, but the fail count is less than or equal to $EC0_{max}$ = 2 * ETC * Density(Gb) - 1. Likewise, the min values of EC[7:1] are defined as $EC[x]_{min}$ = ETC * Density(Gb) * 2^x, and max values are defined as $EC[x]_{max}$ = 2 * (ETC * Density(Gb) * 2^x) - 1. The exception is $EC7_{max}$, which is unlimited. The corresponding bit will be set if the error count is within the required range.

Table 146 — MR20 Number of Rows or Code Word Errors per DRAM Die

	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
MR20	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

When the ECC code word error count mode is selected, the Error Counter (EC) increments each time a code word with check bit errors is detected. After all code words, on all rows, in all banks, in all bank groups had ECS commands performed, the result of the Error Counter is loaded into MR20, subject to error threshold reporting. The EC is reset after the value has been transferred to the mode register.

The ECC Errors per Row Counter increments the number of code words errors on a given row, after more than one error on a given row is detected. The EpRC counter is reset with each column address wrap. Each row's code word error count is compared to the previous code word error count to determine the row address with the highest error count within the DRAM die. After reading all code words on a row, the number of errors counted is compared to the number of errors from the previous row. If the previous row error count is less than the present row error count, the present larger error count is saved to the Previous High Error Count register, its associated address is saved to the Previous High Error Count Row/Bank Address/Bank Group register, and the present row error counter is cleared. If the previous row error count is greater than the present row error count, the previous row error count and register value remains unchanged, however the present row error counter is cleared.

After all rows, in all banks, in all bank groups have executed ECS operations, the result of the Previous High Error Count (address and error count) are latched into MR16:19 when the bank group counter wraps, if the Errors per Row Count(EpRC) meets or exceeds the Row Error Threshold Count(RETC) in Table 148. MR16:18 shown in Table 147 contains the information for the row with the highest number of code word errors and is allocated as A[17:0] Row Address, BA[1:0] Bank Address, BG[2:0] Bank Group Address. MR19 shown in Table 147 contains the information for the Errors per Row Count (EpRC) for the number of code word errors on the highest failing row. REC[5:0] indicates error counts within a range. REC0 is set to "1" if REC0min (the RETC defined in Table 148) has been reached, but the fail count is less than or equal to REC0max = 2 * RETC - 1. Likewise, the min values of REC[5:1] are defined as REC[*x*]min = RETC * 2^x, and max values are defined as REC[*x*]max = 2 * (RETC * 2^x) - 1. The exception is $REC5_{max}$, which is unlimited. The corresponding bit will be set if the error count is within the required range.

Table 147 — MR16-MR19 Address of Row with Max Errors and Error Count

	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
MR16	R7	R6	R5	R4	R3	R2	R1	R0
MR17	R15	R14	R13	R12	R11	R10	R9	R8
MR18	RFU	BG2	BG1	BG0	BA1	BA0	R17	R16
MR19	RFU	RFU	REC5	REC4	REC3	REC2	REC1	REC0

Table 148 — Row Error Threshold Count (RETC)

	Error Count
Row Error Threshold Count (RETC)	4

The error counters (ECC Error Counter and ECC Errors per Row Counter) reset each time the bank group counter wraps. This process will occur on the ECS operation following the ECS operation that processed the last row in the last bank in the last bank group. The MR16:20 are not cleared after being read from, they will retain the most recent written data until they are rewritten during a subsequent bank group wrap or reset by either issuing a RESET or ECS Reset Counters.

4.37.4 3DS Operation

The ECS feature supports 3DS stacking where the Chip ID, MR14 OP[3:0] (CID3:0 respectively), command bits steer the ECS command to the proper mode registers MR14-MR20 within the die stack. The CID[3:0] bits will be ignored for MRW commands to MR14 or MR15, resulting in identical transparency settings for all die in a 3DS stack. The CID[3:0] bits must be set for MRR commands to MR14-MR20 to read out the data from the target die in the 3DS stack. The CID[3:0] bits will also be used by the Manual ECS MPC command. For single die packages, the CID[3:0] bits should all be set to '0'.

Mode register configuration and readout of mode register data requires per DRAM addressing mode.

Broadcasting the Manual ECS MPC command to all die in the stack is not supported. The Manual ECS MPC command to command spacing requires waiting tECSc, even to different die in the stack. The only commands allowed during t_{ECSc} for a manual ECS operation are ODT NT commands.

4.37.5 ECS Operation with PASR support

Segments which are masked are not guaranteed to retain their data if Self Refresh is entered. If Automatic ECS (MR14:OP[7]=0B) or Automatic ECS in Self Refresh (MR15:OP[3]=1B) is enabled, ECS scrubbing will still occur in unmasked segments while in Self Refresh, but the DRAM is not required to execute the ECS on the masked segments. ECS Transparency may not produce accurate results if any mak bit is set. Additionally, upon exit of Self Refresh with masked segments, the masked segments will need to be initialized with known data and the ECS counters will need to be reset, if accurate ECS data is required during the next scrub through the full array.

4.38 CRC

4.38.1 CRC polynomial and logic equation

DDR5 supports CRC for write and read operations. Write and read CRC can be enabled by separate mode register bits. Write CRC and data mask functions are not supported at the same time and cannot be enabled together.

The CRC polynomial used by DDR5 is the ATM-8 HEC, X^8+X^2+X^1+1 that is same as used on DDR4.
A combinatorial logic block implementation of this 8-bit CRC for 64-bits of data contains TBD two-input XOR gates contained in eight 6 XOR gate deep trees.

The Table x shows error detection coverage of DDR5 CRC.

Table 149 — Error Detection Details

ERROR TYPE	DETECTION CAPABILITY
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random Multi-Bit Error within Two adjacent Transfers	100%

CRC COMBINATORIAL LOGIC EQUATIONS

```
module CRC8_D64;
// polynomial: (0 1 2 8)
// data width: 64
// convention: the first serial data bit is D[63]
// initial condition all 0 implied
function [7:0]
nextCRC8_D64;
input [63:0] Data;
reg [63:0] D;
reg [7:0] NewCRC;
begin
D = Data
;
NewCRC[0] = D[63] ^ D[60] ^
D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;
NewCRC[1] = D[63] ^ D[61] ^ D[60] ^ D[57] ^
D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[63] ^ D[62] ^ D[61] ^ D[60] ^
D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[63] ^ D[62] ^ D[61] ^ D[59] ^
D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
```

```
NewCRC[4] = D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] = D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] = D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];
nextCRC8_D64 = NewCRC;
```

4.38.2 CRC data bit mapping for x4 devices

The following figure shows detailed bit mapping for a x4 device. This bit mapping is common between write and read CRC operations.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 144 — CRC bit mapping for x4 device

4.38.3 CRC data bit mapping for x8 devices

The following figure shows detailed bit mapping for a x8 device. This bit mapping is common between write and read CRC operations. x8 devices have two DQ nibbles and each DQ nibble has its own eight CRC bits to protect 64 data bits. Therefore, a x8 device will have two identical CRC trees implemented.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 145 — CRC bit mapping for x8 device

4.38.4 CRC data bit mapping for x16 devices

The following figure shows detailed bit mapping for a x16 device. This bit mapping is common between write and read CRC operations. x16 devices have four DQ nibbles and each DQ nibble has its own eight CRC bits to protect 64 data bits. Therefore, a x16 device will have four identical CRC trees implemented.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 146 — CRC bit mapping for x16 device

4.38.5 Write CRC for x4, x8 and x16 devices

The controller generates the CRC checksum and forms the write data frames as shown in <Link>Chapter 4.38.2 to <Link>Chapter 4.38.4.

Write CRC function can be enabled or disabled per each nibble independently in x8 device. There are two separate write CRC enable MR bits (for upper and lower nibbles) defined for x8. When at least one of two write CRC enable bits is set to '1' in x8, the timings of write CRC enable mode is applied to the entire device (i.e. both nibbles). When write CRC is enable in one nibble and disabled in the other nibble in x8, then the DRAM does not check CRC errors on the disabled nibble, and hence the ALERT_n signal and any internal status bit related to CRC error is not impacted by the disabled nibble.

In case of x4 or x16, only one of two write CRC enable bit is used as defined in the MR table (figure TBD). The unused write CRC enable bit is don't care in x4 and x16, i.e., MR50 OP[2] is set to low for x4 and x16 devices.

The DRAM checks for an error in received code words per each write CRC enabled nibble by comparing the received checksum against the computed checksum and reports errors using the ALERT_n signal if there is a mismatch in any of nibbles.

DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

There is no write latency adder when write CRC is enabled.

4.38.6 Write CRC auto-disable

Write CRC auto-disable mode is enabled by programming the Write CRC auto-disable mode enable bit MR50:OP[4] to '1'. When this mode is enabled, the DDR5 SDRAM counts the number of Write CRC error occurrences per device, regardless of configuration (x4, x8 or x16). When the number of Write CRC errors exceeds the Write CRC Auto-Disable Threshold (between 0 and 127) as programmed in MR51:OP[6:0], the DDR5 SDRAM disables Write CRC error checking of all nibbles and sets the Write CRC auto-disable status bit MR50:OP[5] to '1'. To exceed the Write CRC Auto-Disable Threshold, the number of Write CRC errors must occur within the Write CRC Auto-Disable Window described below.

Unless the Write CRC auto-disable status bit is set, the Write CRC error counter is reset after the predetermined number of writes between 0 and 127, where 0 means an infinite window, as programmed in MR52:OP[6:0], so that the Write CRC error count will accumulate during each Write CRC Auto-Disable Window. Once the Write CRC auto-disable status bit is set, the write CRC error checking is not re-enabled at the end of the Write CRC Auto-Disable Window, even though the Write CRC error counter is reset below the threshold value.

Write CRC error checking can be re-enabled by resetting the Write CRC auto-disable status bit MR50:OP[5] to '0'. This will reset the Write CRC error counter and restart the Write CRC Auto-Disable Window.

Prior to changing the Write CRC Auto-Disable Threshold as programmed in MR51:OP[6:0] or the Write CRC Auto-Disable Window as programmed in MR52:OP[6:0], the host shall disable the Write CRC Auto-Disable mode, MR50:OP[4]=0. Once the updated values have been programmed in MR51 and/or MR52, Write CRC Auto-Disable mode can be (re)enabled, MR50:OP[4]=1. Disabling the Write CRC Auto-Disable mode, if enabled, will reset the DRAM's Write CRC error counter and restart the Write CRC Auto-Disable Window. However, if the Write CRC auto-disable status bit had previously been set to '1', MR50:OP[5]=1, the host is required to set MR50:OP[5]=0 to resume error counting.

Changes to the Write CRC auto-disable threshold (MR51) and window (MR52) settings are only allowed when the CRC Write auto-disable mode is disabled (MR50[4]=0).

If the CRC auto-disable threshold is reached and the DDR5 SDRAM was already driving ALERT_n to low due to the current or a previous Write CRC error, then ALERT_n may be released upon satisfying CRC_ALERT_PW_min.

When Write CRC auto-disable mode is disabled, MR50:OP[4] = 0, Write CRC error counters may remain at reset values even if Write CRC errors occur.

4.38.7 Read CRC for x4, x8 and x16 devices

The DDR5 SDRAM generates the CRC checksum and forms the read data frames as shown in <Link>Chapter 4.38.2 to <Link>Chapter 4.38.4. The controller can check for an error in received code words per nibble by comparing the received checksum against the computed checksum and if there is a mismatch in any of nibbles then controller may retry the transaction.

Read latency adder when read CRC is enabled depends on data rate as shown in the table below.

Table 150 — Read CRC Latency Adder

Data Rate (MT/s)	Read CRC Latency Adder (nCK)
1980 MT/s ≤ Data Rate ≤ 2100 MT/s	0
2933 MT/s ≤ Data Rate ≤ 6000 MT/s	0
6000 MT/s < Data Rate ≤ 6400 MT/s	2
6800 MT/s < Data Rate ≤ 8400 MT/s	4

4.38.8 CRC Burst Order

When Write CRC is enabled, the CRC bits are calculated based on the sequential burst address order of the write data for the Write command. This sequential order is '0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, and '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T,T' or '8,9,A,B,C,D,E,F,T,T,T,T,T,T,T,T' in BC8 OTF.

When Read CRC is enabled, the DDR5 SDRAM's CRC generator overrides the CA burst order bits C3 and C2 to '00', and CRC bits are calculated based on the sequential burst address order of the read data for the Read command. This sequential order is '0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, and '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T,T' or 'T,T,T,T,T,T,T,T,8,9,A,B,C,D,E,F' in BC8 OTF. The override values do not modify the actual data burst ordering, and are only used for the CRC calculations. Actual data burst follows the burst order as indicated by C3 and C2 in the Read command.

4.38.9 Write CRC error handling

When DRAM detects CRC error on received code words in any of nibbles, then it drives ALERT_n signal to ‘0’ for TBD clocks.

The latency to ALERT_n signal is defined as tCRC_ALERT in the figure below.

DRAM will set Write CRC Error Status bit in A[3] of MR50 to '1' upon detecting a CRC error. The Write CRC Error Status bit remains Group At '1' until the host clears it explicitly using an MRW command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst-case delay for ALERT_n (during init) and can back up the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than TBD clocks at the controller if there are multiple CRC errors as the ALERT_n is a daisy chain bus.

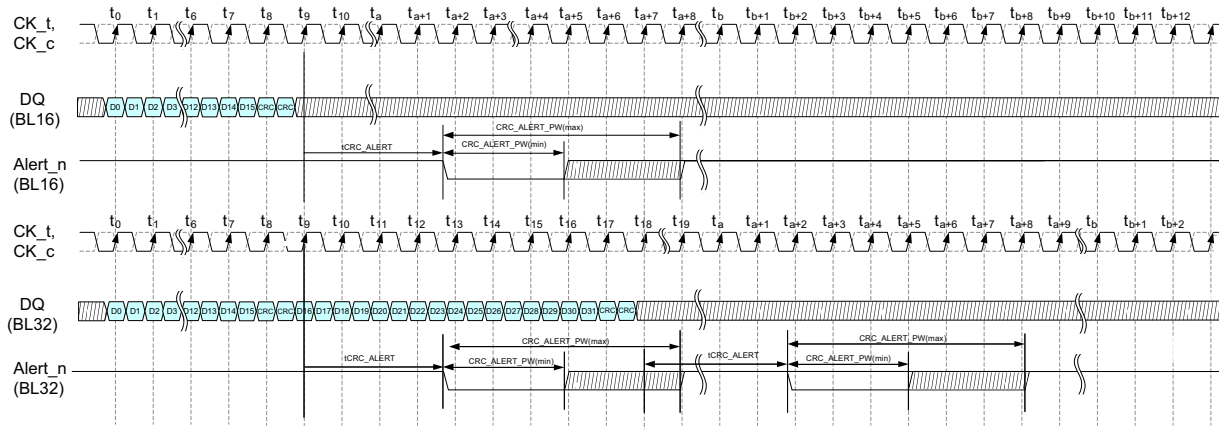


Figure 147 — CRC Error Reporting Timing diagram

Note(s):
1. CRC_ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.
2. Timing diagram applies to x4, x8 and x16 devices.

Table 151 — CRC Error Handling Timing Parameters

Symbol	Description	min	max	unit
tCRC_ALERT	CRC Alert Delay Time	3	13	ns
CRC_ALERT_PW	CRC Alert Pulse Width	12	20	nCK

4.38.10 CRC bit mapping in BC8 mode

CRC bits are always transferred on 17th and 18th UI, in BC8 mode. When read CRC is enabled during BC8 read, DQ bits are driven high and DQS is toggled by DRAM during the chopped data bursts. When write CRC is enabled during BC8 write, DQ bits must be driven high and DQS must be toggled by controller during the chopped data bursts. In BC8 mode, read CRC and write CRC bits are calculated with the inputs to the CRC engine for the chopped data bursts replaced by all '1's.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 148 — CRC bit mapping in BC8 modes for x4 device

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 149 — CRC bit mapping in BC8 modes for x8 device

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 150 — CRC bit mapping in BC8 modes for x16 device

4.38.11 CRC bit mapping in BL32 mode

In BL32 mode, CRC bits are separately calculated for the first half and the second half of the data. CRC bits for the first half of the data are transferred on 17th and 18th UI, and CRC bits for the second half of the data are transferred on 35th and 36th UI.

4.39 Loopback

With Loopback, DDR5 can feed a received signal or data back out to an external receiver for multiple purposes. Loopback allows the host (memory controller or test instrument) to monitor data that was just sent to the DRAM without having to store the data in the DRAM or use READ operations to retrieve data sent to the DRAM. Loopback in DDR5 DRAM requires that the data be sent to the Loopback path before sending it to the core so no READ/WRITE commands are required for Loopback to be operational. There are also inherent limitations when characterizing the receiver using statistical analysis methods such as Bit Error Rate (BER) analysis. At BER=$1E^{-16}$, for example, (1) there is not enough memory depth in the DRAM to store all the $1E^{+16}$ data; (2) the amount of time to perform multiple WRITE/READ commands to/from the memory is prohibitively long; (3) since the amount of time involved performing these operations is much longer than the DRAM refresh rate interval, the host or memory controller must also manage Refreshes during testing to ensure data retention; and (4) limited pattern depth means limited Inter Symbol Interference (ISI) and limited Random Jitter (Rj), and, therefore, limited errors at the receiver. Use of the Loopback feature is a necessity for characterizing the receiver without the limitations and complexities of other traditional validation methods. Loopback can also be used during “normal” operation, i.e., during training and when an operating system is loaded.

4.39.1 Loopback Output Definition

The Loopback requires two output pins (one single-ended Loopback strobe LBDQS and one single-ended Loopback data LBDQ).

The default RTT state for Loopback is RTT_OFF, designated by MR36:OP[2:0] = 000B. In this state, both the LBDQS and LBDQ outputs are disabled. If the Loopback pins of several DDR5 SDRAM devices are connected together and the “end” device needs termination, there is an RZQ/5 (48ohms) option available by setting MR36:OP[2:0] = 101B.

Selecting a Loopback Select Phase A(MR53:OP[6:5]=00_B) and Output value via MR53:OP[4:0] other than the default, Loopback Disabled(MR53:OP[4:0]=00000_B), will result in the LBDQS and LBDQ pins to transition from the RTT_OFF to a DRAM Drive State.

Before changing the Loopback Output Select from upper byte to lower byte or vice versa, host shall set Loopback Output Select to MR53:OP[4:0]=00000_B to make Loopback mode be Disabled.

The LBDQS output will transition with the differential input crossing point of DQS_t/DQS_c for x4 and x8 device configurations, plus latency. LBDQS will transition with DQSL_t/DQSL_c for x16 devices if DML or a DQL is selected for output, or with DQSU_t/DQSU_c for x16 devices if DMU or a DQU is selected for output. If an RFU output is selected, or if DMU or a DQU is selected on a x4 or x8 device where DQSU_t/DQSU_c are not valid, LBDQS will remain in a DRAM Drive State.

The LBDQ output will transition with the receiver data state of the DM or DQ pin selected by MR53:OP[4:0]. If an RFU output is selected, or if an invalid output for device configuration is selected, the LBDQ output will remain in a DRAM Drive State.

Table 152 — Loopback Output Definition

Condition	LBDQS	LBDQ	NOTE
Loopback Disabled	RTT_Loopback	RTT_Loopback	
Loopback Enabled	Selected Phase	Selected Phase and Selected DQ	1

Note 1: Selection of an unsupported DM/DQ for the device configuration may result in LBDQS toggling and the LBDQ in a driven state.

4.39.2 Loopback Phase

Due to the high data rates of the DDR5 SDRAM, Loopback may be implemented with 2-way or 4-way interleaved outputs. With a 2-way implementation, the DQS and selected DM/DQ will be sampled and output every 1 CK or 2 UI. Similarly, with a 4-way implementation, the DQS and selected DM/DQ will be sampled and output every 2 CK or 4 UI.

To be able to sample all bits with a 2-way or 4-way interleave implementation, the Loopback Select Phase programmed in MR53:OP[6:5] allow selection of the DQS/DM/DQ phase to be output. In 2-way mode, Phase A and Phase B are valid options. In 4-way mode, Phase A, Phase B, Phase C and Phase D, are valid options.

Figure 151 shows an example of a Loopback implementation for 4-way interleave x4 DRAM. This example requires a divided clock to produce DQS_0, DQS_90, DQS_180 and DQS_270. Phase A through D refers to the 4-bit naturally aligned bits in a data stream. The output of the DQ slicer runs at 1/4 the speed as received data. In a 4-way interleave design, the data is received at full speed, but internally the data is latched only at quarter speed. For example, if the input bit stream consists of A, B, C, D, then the multiplexer input “A” receives data bit A and strobe DQS_0; multiplexer input “B” receives data bit B and strobe DQS_90; multiplexer input “C” receives data bit C and strobe DQS_180; and multiplexer input “D” receives data bit D and DQS_270.

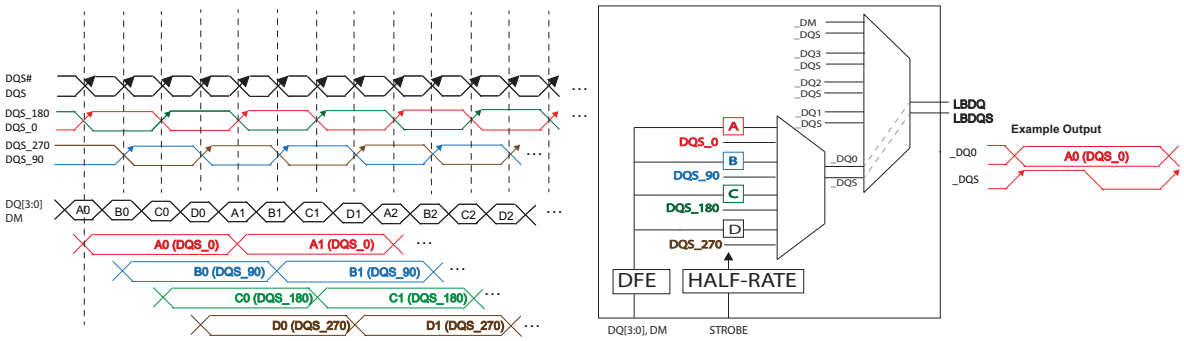


Figure 151 — Example of 4-Way Interleave Loopback Circuit on a x4 SDRAM

4.39.3 Loopback Output Mode

Loopback Output Mode selects whether to output LBDQS and LBDQ in Normal Output Mode or Write Burst Output Mode, based on MR53:OP[7]. In the default Normal Output Mode (MR53:OP[7] = 0_B), the selected DM/DQ state is captured with every DQS_t/DQS_c toggle for the selected Loopback Phase. In Write Burst Output Mode (MR53:OP[7] = 1_B), the selected DM/DQ state will be output on LBDQ when qualified by the write enable, which means data is only captured during the write burst and not during the preamble or postamble.

4.39.3.1 Loopback Normal Output Mode (Default)

In Normal Output Mode (MR53:OP[7] = 0_B), the selected DM/DQ state is captured with every DQS_t/DQS_c toggle for the selected Loopback Phase and output on LBDQ. The LBDQS output will be delayed by t_{LBDLY} from the selected DQS_t/DQS_c Loopback Phase. Phase C and D are inverted from Phase A and B, respectively. Since no Write commands are required in Normal Output Mode, MR settings pertaining to preamble, postamble, CWL are ignored by the Loopback function.

Additional requirements for Normal Output Mode:

- Loopback in Normal Output mode is not supported after completing Write Leveling training with Internal Write Timing mode set MR2:OP[7]=1.
- DQS must be driven differentially low (DQS_t low, DQS_c high) prior to entry into Normal Output Mode.
- DQS_t/DQS_c must be continuously driven during Loopback operation. (HiZ state not allowed.)
- Only DSEL and MRW commands applied at command pins during Normal Output Mode.
- RESET is required to exit Loopback Normal Output Mode.

No DFE Reset is assumed after first rising edge of DQS_t. DDR5 SDRAM array data is not guaranteed after entering Normal Output Mode.

4.39.3.2 Loopback Normal Output Mode Timing Diagrams

Loopback Normal Output Mode entry and output example timing diagrams are shown below.

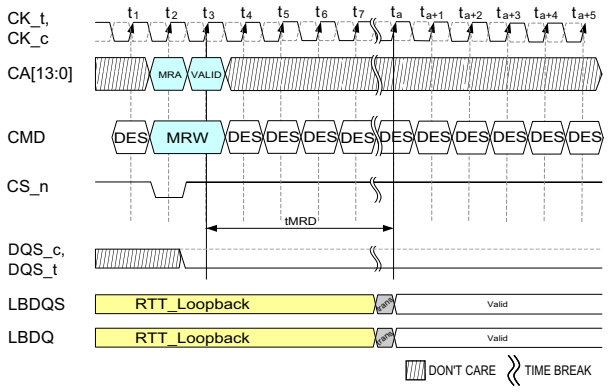


Figure 152 — Loopback Normal Output Mode Entry

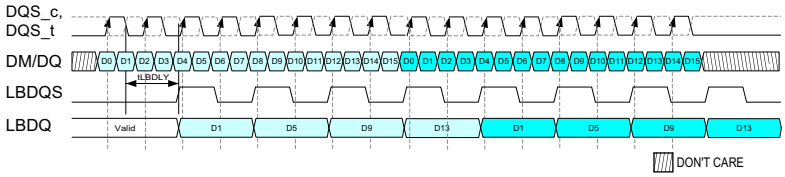


Figure 153 — Loopback Normal Output 4-Way Mode PhaseB Example

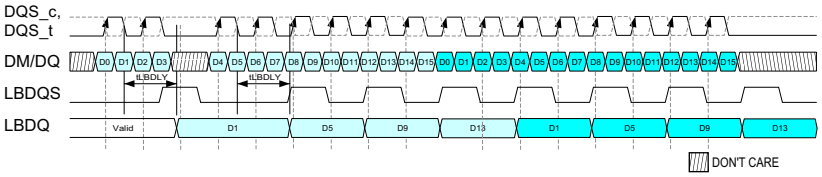


Figure 154 — Loopback Normal Output Mode 4-Way PhaseB 1CK mid Gap Example

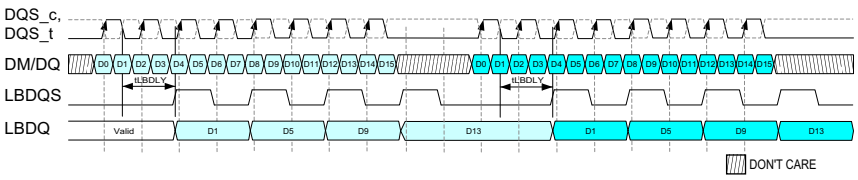


Figure 155 — Loopback Normal Output Mode 4-Way PhaseB 2CK Gap Example

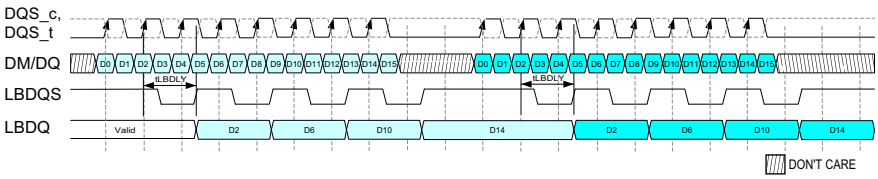


Figure 156 — Loopback Normal Output Mode 4-Way PhaseC 2CK Gap Example

4.39.3.3 Loopback Normal Mode with CRC Output Timings

Loopback Normal Output Mode with CRC, timing diagram examples are shown below.

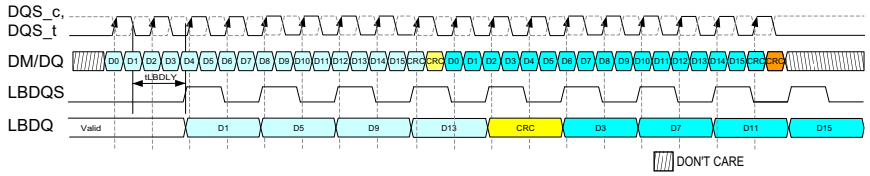


Figure 157 — Loopback Normal Output Mode 4-Way PhaseB with CRC, no Gap Example

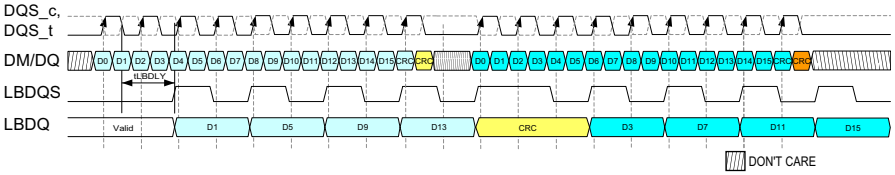


Figure 158 — Loopback Normal Output Mode 4-Way PhaseB with CRC,1CK Gap Example

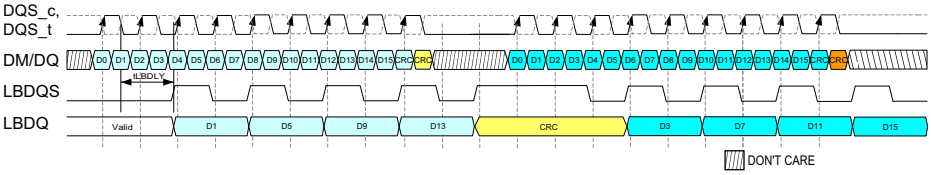


Figure 159 — Loopback Normal Output Mode 4-Way PhaseB with CRC, 2 CK Gap Example

4.39.3.4 Loopback Write Burst Output Mode

In Write Burst Output Mode (MR53:OP[7] = 1_B), Loopback data is only generated during the write burst, so it is effectively masked for the DQS toggles during the preamble or postamble. Normal Write operation for the Command, DQS and DM/DQ is assumed. MR settings pertaining to preamble, postamble, CWL apply, as they do for any Write command.

To prevent Loopback interference on the DRAM within the normal data path, the DRAM optionally may output the 2nd preamble pulse for the special case of WPRE=4CK and selection of Phase C or D for Data Burst Bit phase alignment or Phase A or B for Strobe phase alignment. With this behavior, all phases are inverted from normal behavior.

Implementation of 2-way or 4-way interleave Loopback introduces complexity in Write Burst Mode when the DQS toggle is not continuous. If the DQS toggle is continuously generated by Write commands spaced BL/2, Loopback will align the LBDQS/LBDQ output with the selected phase for all write bursts. In cases where gaps in Write commands are greater than BL/2, the phase shall be determined by the analysis of the conditions.

Table 153 — Loopback Output Phase

Write to Write Separation	Phase	NOTE
X = BL/2	Selected	
X >= BL/2	Determined via analysis of specific conditions	1

Note 1: Specific conditions include 2-way/4-way interleave implementation, selected phase, data rate, preamble, postamble and write burst gap duration.

In the case where continuous bursts are not issued in Loopback Write Burst Output Mode, selection of Phase C or D for Data Burst Bit phase alignment or Phase A or B for Strobe phase alignment may result in the last tLBQSH width of a burst that does not comply with spec.

Additional requirements for Write Burst Output Mode:

- Write Leveling training is required prior to Write Burst Loopback operation.
- All Write timing and voltage requirements must be followed. Failure to meet this requirement results in unknown data written to DRAM, and the Loopback pins may not output the captured input data as expected.

4.39.3.5 Loopback Write Burst Output Mode Timing Diagrams

Loopback Write Burst Output Mode timing diagram examples are shown below.

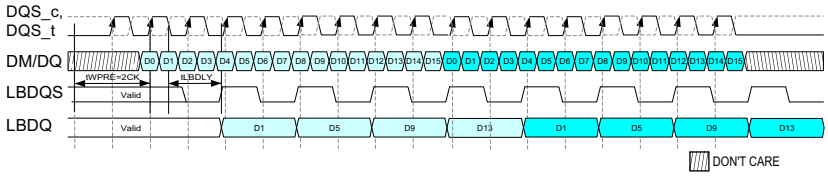


Figure 160 — Loopback Write Burst Output Mode 4-Way PhaseB WPRE=2CK Example

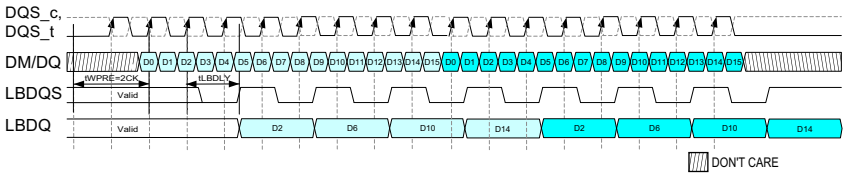


Figure 161 — Loopback Write Burst Output Mode 4-Way PhaseC WPRE=2CK Example

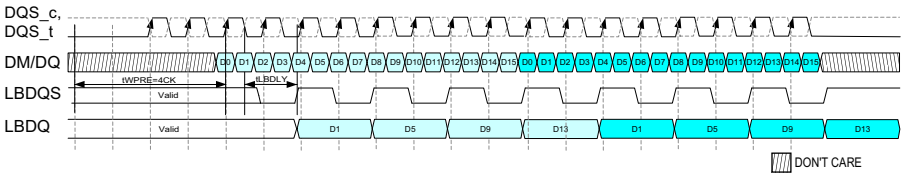


Figure 162 — Loopback Write Burst Output Mode 4-Way PhaseB Data Burst Bit and PhaseD Strobe Alignment WPRE=4CK Optional Example

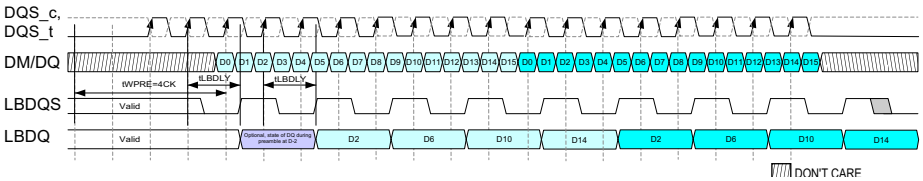


Figure 163 — Loopback Write Burst Output Mode 4-Way PhaseC Data Burst Bit and PhaseA Strobe Alignment WPRE=4CK Optional Example

4.39.3.6 Loopback Write Burst with CRC Output Mode Timing Diagrams

Loopback Write Burst Output Mode with CRC, timing diagram examples are shown below.

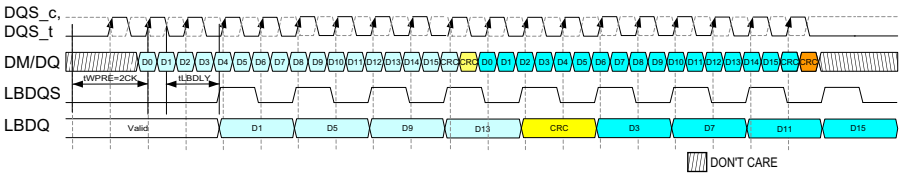


Figure 164 — Loopback Write Burst with CRC Output Mode 4-Way PhaseB with CRC, No Gap Example

4.39.4 Loopback Timing and Levels

The LBDQS output will be delayed from the selected DQS_t/DQS_c Loopback Phase. The timing parameter, *t*LBDLY, is shown in Table 154.

Table 154 — Loopback LBDQS Output Timing

Speed		DDR5-4400		DDR5-4800/5200		DDR5-5600		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing									
LBDQS Delay from Selected DQS Loopback Phase	tLBDLY	-	20	-	20	-	20	ns	

The interaction between LBDQS and LBDQ is described in section 9.10 Loopback Output Timing.

ODT for Loopback is described in Section 5.5 On-Die Termination for Loopback Signals. Output driver electrical characteristics for Loopback is described in Section 9.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ.

4.40 CA_ODT Strap Operation

With the introduction of on-die termination for CA/CS/CK on DDR5 DRAMs, the setting of the termination values per DRAM will be different depending on the configuration of DRAMs on the DIMM or system board. The CA_ODT pin enables the distinction of two “sets” of CA/CS/CK ODT settings. When the CA_ODT pin is strapped to a constant VSS setting on the DIMM or board, the CA/CS/CK ODT settings will be referred to as “Group A”. When the CA_ODT pin is strapped to a constant VDD setting on the DIMM or system board, the CA/CS/CK ODT settings will be referred to as “Group B”. Typical usage would be to apply a weak termination setting to Group A devices and a stronger termination setting to Group B devices, which would be at the end of the fly-by routing on the DIMM. To support these different settings, two sets of MPC opcodes will be used to target either Group A or Group B devices. In addition to these separate “Groups” of devices based on the CA_ODT pin, the PDA commands will also be supported. However, the correct combination of the PDA Select ID and MPC opcode must be used according to the CA_ODT pin value.

The CA_ODT pin is defined in the pinlist as follows:

Pin Name	Input/ Output	Description
CA_ODT	Input	ODT for Command and Address. Apply Group A settings if the pin is connected to VSS and apply Group B settings if the pin is connected to V_{DDQ}

MR32 is defined as follows to reflect the need to be able to read the CA_ODT strap value:

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA_ODT Strap Value	CS ODT			CK ODT		

MR33 is defined as follows:

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		DQS_RTT_PARK			CA ODT		

If the CA_ODT Strap Value for the DRAM is 0, the CK ODT, CS ODT, and CA ODT values will reflect the default settings for “Group A” ODT values, or will reflect what has been written to these mode registers via the MPC opcodes for Group A CK/CS/CA ODT settings.

If the CA_ODT Strap Value for the DRAM is 1, the CK ODT, CS ODT, and CA ODT values will reflect the default settings for “Group B” ODT values, or will reflect what has been written to these mode registers via the MPC opcodes for Group B CK/CS/CA ODT settings.

4.40.1 CA/CS/CK ODT Settings

The following MPC opcodes will be used to set the “Group A” and “Group B” RTT_CA, RTT_CS, and RTT_CK values (to be included in the MPC section)

Function	Operand	Data	Notes
Initialization and Training Modes	OP[7:0]	... 0010 0xxxB: Group A RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0010 1xxxB: Group B RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0011 0xxxB: Group A RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0011 1xxxB: Group B RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0100 0xxxB: Group A RTT_CA = xxx (See MR33:OP[2:0] for encoding) 0100 1xxxB: Group B RTT_CA = xxx (See MR33:OP[2:0] for encoding) ...	

4.41 Duty Cycle Adjuster (DCA)

DDR5 SDRAM supports a mode register adjustable DCA to allow the memory controller to adjust the DRAM internally generated DQS clock tree and DQ duty cycle to compensate for systemic duty cycle error of all DQS and DQs.
The DQS DCA is located before the DQS clock tree or equivalent place. The DCA requires a locked DLL state and will affect DQS and DQ duty cycle during the following operations.

- Read
- Read Preamble Training
- Read Training Pattern
- Mode Register Read

The controller can adjust the duty cycle through all the DCA mode registers and can determine the optimal Mode Register setting for DCA in multiple different ways.

In case of 4-phase internal clocks, for example, since QCLK(90˚)/IBCLK(180˚)/ QBCLK(270˚) are adjusted based on ICLK(0˚), the controller can first confirm that the first BL is synchronized with ICLK(0˚), and then perform the full DCA training operation which needs to have an even number of MRR(or Read) - MRR(or Read) timing to avoid confusion whether the first BL is synchronized with ICLK(0˚) or IBCLK(180˚)

4.41.1 Duty Cycle Adjuster Range

The global DCA step range is from -7 to +7, as defined in MR43 and MR44. The actual step size cannot be defined since the variation of duty cycle by changing DCA code is not linear.

Table 155 — DCA Range

Parameter	Min/Avg./Max	Value	Unit	NOTE
Duty Cycle Adjuster Range	Min	28	ps	1
	Max	56		

Note(s):
NOTE 1These values are guaranteed by design.

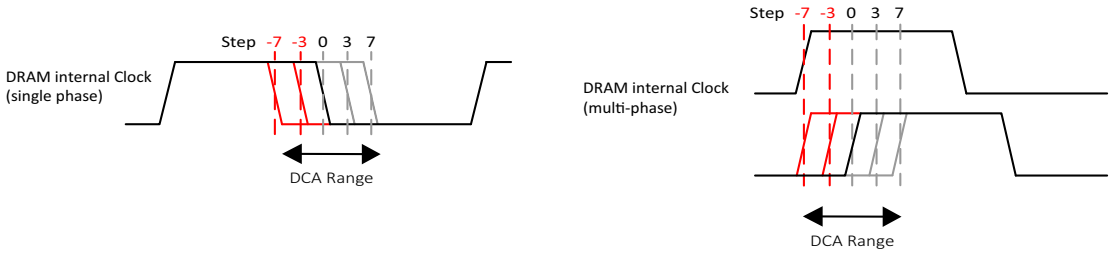


Figure 165 — Duty Cycle Adjuster Range

4.41.2 The relationship between DCA Code Change and single/two-phase internal clock(s)/DQS timing

In case of the DQS clock tree used single/two-phase clock(s) scheme, the duty-cycle ratio of all DQS per device can be adjusted directly according to the internal clock(s) controlled by the DCA code. Note that tDQSCK is not changed by DCA code change.

Using a 2-phase clock scheme, the rising edge of the 0° clock is the reference edge, while the 180° clock is adjusted based on 0° clock. The rising edge of 0° clock is for even burst bit data, and the rising edge of 180° clock is for odd burst bit data.

The global DCA adjustment uses the “DCA for single/two-phase clock(s)” mode register bits, MR43:OP[3:0]. A positive DCA adjustment results in a larger duty cycle ratio, while a negative DCA adjustment results in a smaller duty cycle ratio.

In addition to the global DCA adjustment, a per-pin DCA adjustment allows an additional step range of -3 to +3, per DQS/DQ. The 2-phase clock per-pin DCA adjustment uses the OP bits [3,1:0] of MR103 (DQSL_t), MR105 (DQSL_c), MR107 (DQSU_t), MR109 (DQSU_c), MR133 (DQL0), MR141 (DQL1), ..., MR253 (DQU7). The per-pin DCA adjustment is additive to the global DCA adjustment, as shown in the examples below:

Table 156: DCA Range Examples (not all possible combinations)

Global DCA Adjustment	Per-Pin DCA Adjustment	Total DCA Adjustment at Pin
DCA Step -3	DCA Step -2	DCA Step -5
DCA Step -2	DCA Step +2	DCA Step 0
DCA Step 0	DCA Step +1	DCA Step +1
DCA Step +2	DCA Step -3	DCA Step -1
DCA Step +4	DCA Step +3	DCA Step +7
DCA Step +7	DCA Step +2	DCA Step +9

Like the global DCA adjustment, the actual step size for the per-pin DCA adjustment cannot be defined since the variation of duty cycle by changing DCA code is not linear, however the per-pin DCA adjustment will be approximately the same as the global DCA adjustment.

Mode register OP bits associated with the IBCLK and QBCLK may not be supported on the DRAM with a 2-phase clock scheme.

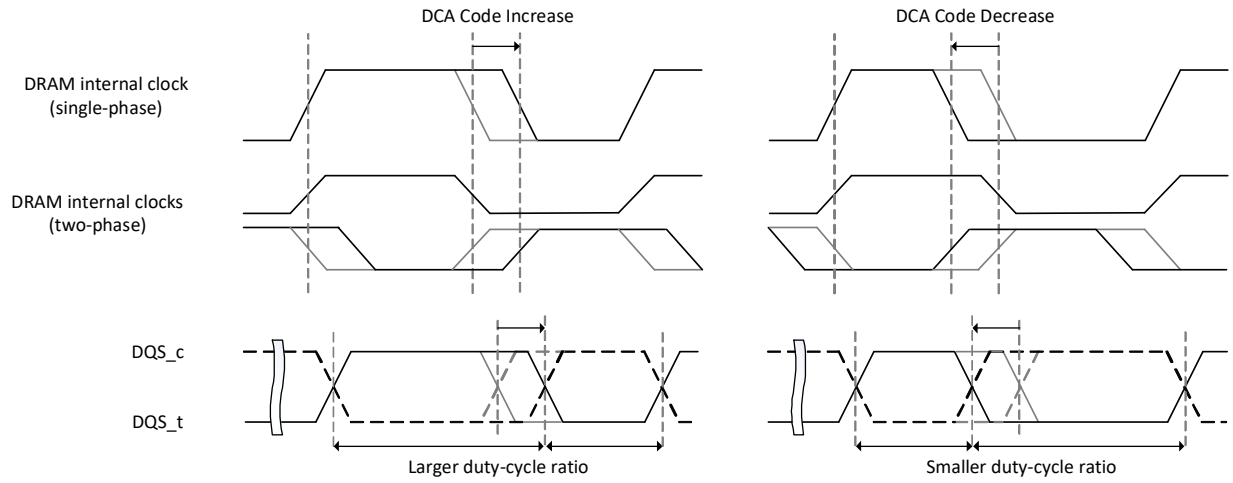


Figure 166 — Relationship between DCA code Change and the single/two-phase internal clock(s)/ DQS waveform (Example)

4.41.3 The relationship between DCA Code Change and 4-phase internal clock(s)/DQS timing

In case of the DQS clock tree used 4-phase clocks scheme, the even and odd duty-cycle ratio of all DQS per device can be respectively adjusted since the internal 4-phase clocks can be independently controlled by the DCA code.

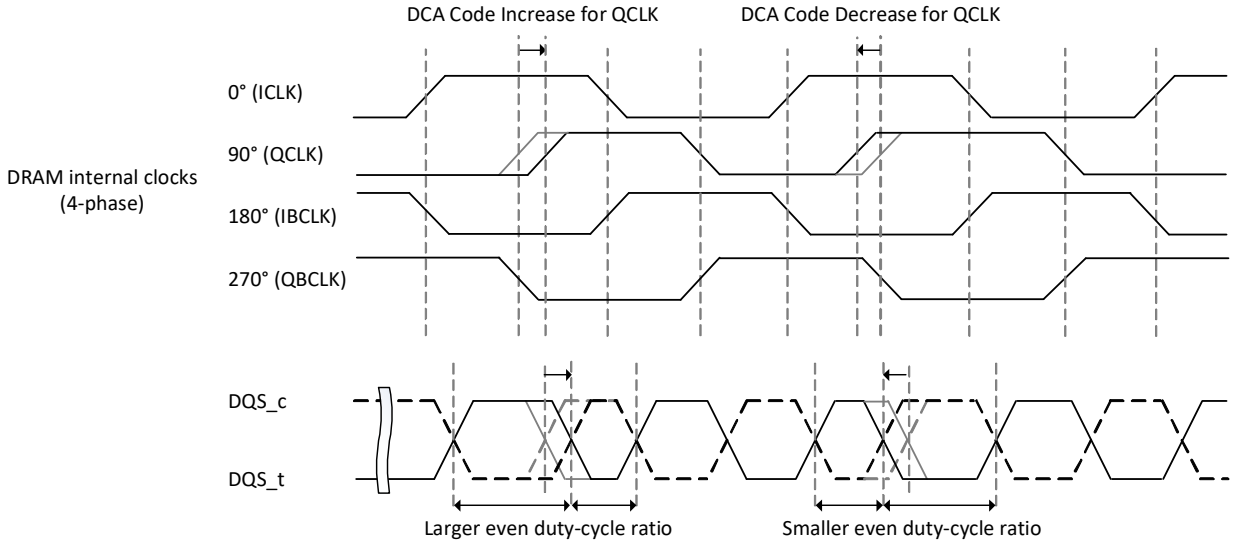


Figure 167 — Relationship between DCA Code Change for QCLK and the 4-phase internal clocks/ DQS waveform (Example)

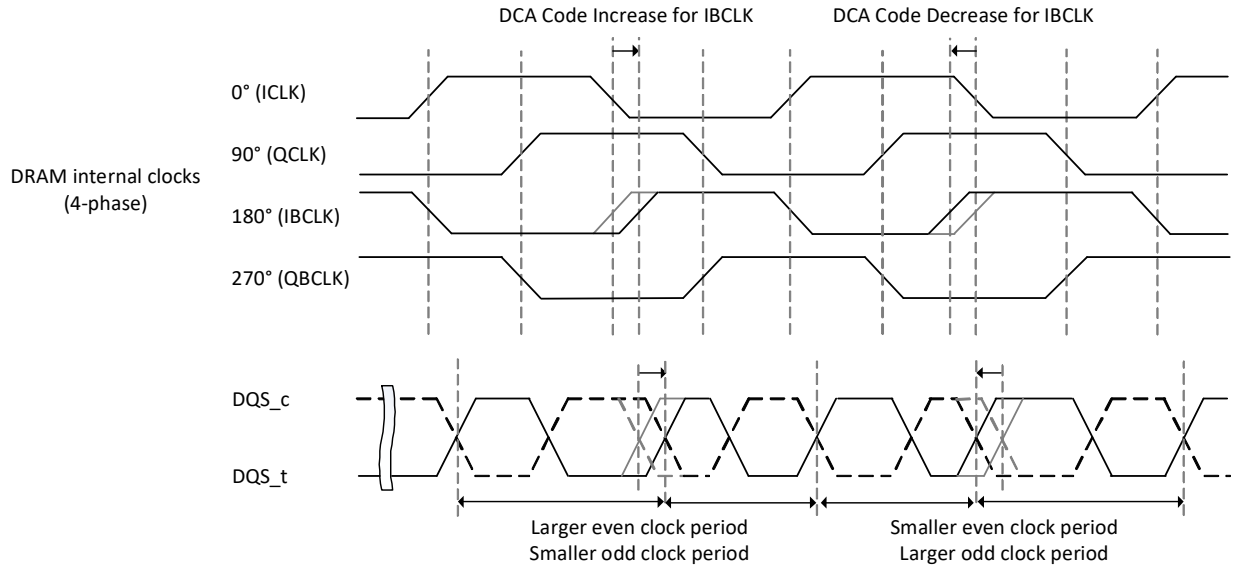


Figure 168 — Relationship between DCA Code Change for IBCLK and the 4-phase internal clocks/ DQS waveform (Example)

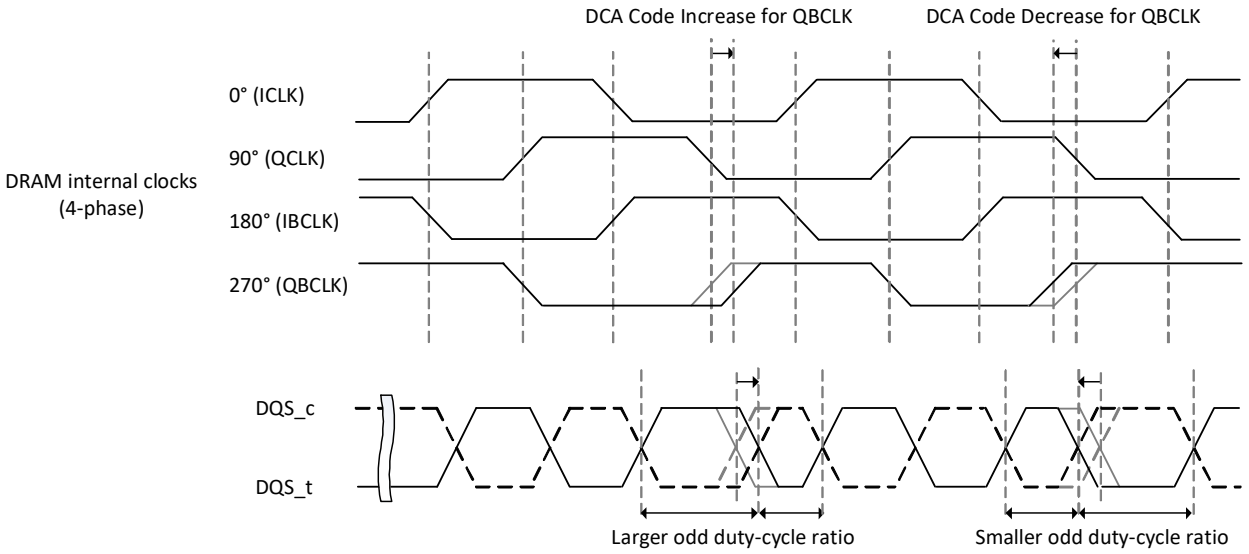


Figure 169 — Relationship between DCA Code Change for QBCLK and the 4-phase internal clocks/ DQS waveform (Example)

4.41.4 The relationship between DCA Code Change and DQs output/DQS timing

The DQS DCA code change effect to DQ Output as follows. The rising edge of DQS_t affects the even data output. The falling edge of DQS_t affects to the falling edge of the odd data output.

4.42 Refresh Management (RFM)

Periods of high DDR5 DRAM activity may require additional refresh commands to protect the integrity of the DRAM data. The DRAM will indicate the requirement for additional Refresh Management (RFM) by setting read only MR58 opcode bit 0 (Table 157). OP[0]=0 indicates no additional refresh is needed beyond the refresh required in the Refresh Operation section of the specification. OP[0]=1 indicates additional DRAM refresh management is required.

Table 157 — Mode Register definition for Refresh Management

MR58 OP[0]	Refresh Management (RFM) Requirement
0	Refresh Management (RFM) not required
1	Refresh Management (RFM) required

A suggested implementation of Refresh Management by the controller monitors ACT commands issued per bank to the DRAM. This activity can be monitored as a Rolling Accumulated ACT (RAA) count. Each ACT command will increment the RAA count by 1 for the individual bank receiving the ACT command.

When the RAA counter reaches a DRAM vendor specified Initial Management Threshold (RAAIMT), which is set by the DRAM vendor in the read only MR58 opcode bits 4:1 (Table 158), additional DRAM refresh management is needed. Executing the Refresh Management (RFM) command allows additional time for the DRAM to manage refresh internally. The RFM operation can be initiated to all banks on the DRAM with the RFMab command, or to a single bank address (BA[1:0]) in all bank groups with the RFMsb command. A DRAM with MR58 OP[0]=0 will treat the RFM command as a REF command.

Table 158 — Mode Register definition for the RAA Initial Management Threshold (RAAIMT)

MR58 OP[4:1]	RAAIMT Value Normal Refresh Mode	RAAIMT Value FGR Refresh Mode
0000_B-0011_B	RFU	RFU
0100_B	32	16
0101_B	40	20
...	...	...
1001_B	72	36
1010_B	80	40
1011_B-1111_B	RFU	RFU

The RFM command bits are the same as the REF command, except for CA9. If the Refresh Management Required bit is “0”, (MR58 OP[0]=0), CA9 is only required to be valid (“V”) for a REF command, and the DRAM will treat a RFM command as a REF command. If the Refresh Management Required bit is “1”, (MR58 OP[0]=1), CA9=”H” executes the REF command and CA9=”L” executes either an RFMab command if CA10=”L” or an RFMsb command if CA10=”H”.

The duration of the RFMab and RFMsb commands is dependent upon the DRAM being in Normal or FGR refresh mode. $t_{RFM,min}$ is equivalent to $t_{RFC,min}$. See Table 159.

Table 159 — t_{RFM} parameters

Refresh Operation	Symbol	Value	Notes
Normal Refresh Management (RFMab)	$t_{RFM1,min}$	$t_{RFC1,min}$	
Fine Granularity Refresh Management (RFMab)	$t_{RFM2,min}$	$t_{RFC2,min}$	
Same Bank Refresh Management (RFMsb)	$t_{RFMsb,min}$	$t_{RFCsb,min}$	

When an RFM command is issued to the DRAM, the RAA counter in any bank receiving the command can be decremented by the RAAIMT value, down to a minimum RAA value of 0 (no negative or “pull-in” of RFM commands is allowed). Issuing an RFMab command allows the RAA count in all banks to be decremented by the RAAIMT value. Issuing an RFMsb command with BA[1:0] allows the RAA count only with that bank address across all bank groups to be decremented by the RAAIMT value

RFM commands are allowed to accumulate or “postpone”, but the RAA counter shall never exceed a vendor specified RAA Maximum Management Threshold (RAAMMT), which is set by the DRAM vendor in the read only MR58 opcode bits 7:5 (Table 160). If the RAA counter reaches RAAMMT, no additional ACT commands are allowed to the DRAM bank until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value.

Table 160 — Mode Register definition for RAA Maximum Management Threshold (RAAMMT)

MR58 OP[7:5]	RAAMMT Value Normal Refresh Mode	RAAMMT Value FGR Refresh Mode
000_B-010_B	RFU	RFU
011_B	3x RAAIMT	6x RAAIMT
100_B	4x RAAIMT	8x RAAIMT
101_B	5x RAAIMT	10x RAAIMT
110_B	6x RAAIMT	12x RAAIMT
111_B	RFU	RFU

RFM command scheduling shall meet the same minimum separation requirements as those for the REF command (see Table 65 in the Refresh Operation section).

An RFM command does not replace the requirement for the controller to issue periodic REF commands to the DRAM, nor does a RFM command affect internal refresh counters. The RFM commands are bonus time for the DRAM to manage refresh internally. However, issuing a REF command also allows decrementing the RAA counter by the value set by MR59 OP[7:6], as shown in Table 161. Hence, any periodic REF command issued to the DRAM allows the RAA counter of the banks being refreshed to be decremented by the MR59 OP[7:6] setting. Issuing a REFab command allows the RAA count in all banks to be decremented. Issuing a REFsb command with BA[1:0] allows the RAA count only with that bank address in all bank groups to be decremented.

Table 161 — Mode Register definition for RAA Counter Decrement per REF Command

MR59 OP[7:6]	RAA Counter Decrement per REF Command
00b	RAAIMT
01b	RAAIMT * 0.5
10b	RFU
11b	RFU

No decrement to the RAA count values is allowed for entering/exiting Self Refresh. The per bank count values before Self Refresh is entered remain unchanged upon Self Refresh exit.

4.42.1 Adaptive Refresh Management (ARFM)

DDR5 supports an optional Refresh Management mode called Adaptive RFM (ARFM). Since Refresh Management settings are read only, the Adaptive RFM allows the controller flexibility to choose additional RFM threshold settings, called “RFM Levels”. The RFM Levels permit alignment of the controller-issued RFM commands with the in-DRAM management of these commands. MR59:OP[5:4} allows selection of the Adaptive RFM Level, as shown in Table 162.

Table 162 — Mode Register Definition for Adaptive RFM Levels

MR59:OP[5:4]	RFM Level	RFM Requirement	RAAIMT Normal Refresh	RAAMMT Normal Refresh	RAA Decrement per REF Command	Notes
00_B	Default	Default	Default	Default	Default	1,2
01_B	Level A	RFM Required	RAAIMT-A	RAAMMT-A	RAADEC-A	1,2,3
10_B	Level B	RFM Required	RAAIMT-B	RAAMMT-B	RAADEC-B	
11_B	Level C	RFM Required	RAAIMT-C	RAAMMT-C	RAADEC-C	

Note(s):

1. RAAIMT values for FGR are half of the normal refresh mode
2. RAAMMT values for FGR are double that of the normal refresh mode
3. RAAIMT, RAAMMT and RAADEC values for RFM Levels A-C are set by DRAM vendor

The Adaptive RFM mode inherits the RAA counting and decrement attributes of the standard RFM mode, while using the alternate RAAIMT, RAAMMT and RAADEC for the selected RFM Level. Increasing the RFM Level results in increased need for RFM commands. Level C is highest RFM Level.

Setting the MR59:OP[5:4] bits to something other than the default "00" case will enable the alternative RFM Level for the Adaptive RFM mode. The host shall decrement the Rolling Accumulated ACT (RAA) count to 0, either with RFM or pending REF commands, prior to making a change to the RFM Level.

To inform the host of the RFM settings required as the RFM Level is changed by MR59:OP[5:4], the DRAM modifies the corresponding mode register values for RAA required, RAAIMT, RAAMMT and RAADEC (MR58:OP[0], MR58:OP[4:1], MR58:OP[7:5], MR59:OP[7:6], respectively) for subsequent MRR commands. Mode register values that remain the same as the default setting indicate the default RFM threshold levels are supported at the selected ARFM level.

Adaptive RFM also allows a DRAM shipped with 'RFM not required' (MR58:OP[0]=0) to override that initial setting and enable RFM by programming a non-default RFM Level. The DRAM internally manages the change to treat the RFM command as an RFM command in this special override case, as shown in Table 163. A DRAM that supports ARFM, even if the device is shipped with 'RFM not required' (MR58:OP[0]=0), will set MR58:OP[0]=1 to indicate the chosen ARFM level is supported.

Table 163 — RFM Commands perceived by DRAM

Command	MR58:OP[0]	MR59:OP[5:4]	Command Perceived by DRAM	Notes
RFM	0_B	00_B	REF	
RFM	0_B	01_B - 11_B	REF	1
RFM	1_B	00_B	RFM	
RFM	1_B	01_B - 11_B	RFM	1,2

Note(s):
1. If the optional ARFM (MR59:OP[5:4]=01_B-11_B) is not supported on the DRAM, the command perceived by the DRAM is determined by MR58:OP[0].
2. Adaptive RFM enables a DRAM shipped with MR58:OP[0]=0 to override the initial setting and enable RFM by programming a non-default RFM Level. The DRAM will change MR58:OP[0]=1 to indicate the chosen ARFM level is supported.

4.43 Package Output Driver Test Mode (Optional)

This optional mode allows for characterization of the DRAM package by allowing the host to individually turn on the output driver of a single bit of the DRAM, while all other bits remain terminated. To use this test mode, the host sets MR61:OP[4:0] to select the target DM or DQ Output Driver. The host also sets the target driver to use the Pull-up Output Driver Impedance of 34 ohms (MR5:OP[2:1] = 00_B), while the termination for all the other DMs and DQs in the DRAM are defined by MR34:[2:0] (RTT_PARK). Note that the supportability of DM termination is decided by MR5:OP[5]

This is only a test mode, no normal functionality is assumed while in this mode or after enabling this mode without a reset to the DRAM device. Entering into this mode is done by programming any value in MR61 other than 0. Since this is an optional function, the discovery bit is located in MR5:OP[3]. A reset of the DDR5 SDRAM is required after exiting the package output driver test mode.

Even though only 5 bits of the MR are needed, the entire MR61 is blocked out to isolate it from normal operating modes.

MR5 Register - for Reference only - See Mode Register Section for details

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pull-Down Output Driver Impedance		DM Enable	TDQS Enable	PODTM Support	Pull-up Output Driver Impedance		Data Output Disable

MR61 Register - for Reference only - See Mode Register Section for details

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RSVD			Package Output Driver Test Mode				

4.44 IO features and Modes

4.44.1 Data Output Disable

The device outputs may be disabled by the Data Output Disable mode register, MR5:OP[0], as shown in the MR5 Register Definition table. For normal operation, set MR5:OP[0] = 0 (default). Setting MR5:OP[0] = 1 disables the device outputs.

4.44.2 TDQS/DM

The DDR5 SDRAM x8 configuration has a package ball that is shared between TDQS_t and DM_n. The Write Data Mask (DM) function is dependent upon Termination Data Strobe (TDQS). If TDQS is enabled, DM is disabled. If TDQS is disabled, then DM may be enabled or disabled via mode register setting, as noted in Table 164 below.

4.44.2.1 TDQS

One pair of Termination Data Strobe (TDQS) pins, TDQS_t/TDQS_c, is supported for the x8 configuration DDR5 SDRAM. The TDQS function is programmable via Mode Register bit, MR5:OP[4]. The x8 is the only configuration which supports the TDQS function. The x4 and x16 DDR5 SDRAMs do not support this function thus, for these configurations, the TDQS MR setting must be disabled, MR5:OP[4] = 0 (default).

When TDQS is enabled, MR5:OP[4] = 1, the same termination resistance function is applied to the TDQS_t/TDQS_c pins that is applied to DQS_t/DQS_c pins., except during Read commands where TDQS does not output any data and will remain at RTT_DQS_PARK.

4.44.2.2 DM

(Reference section “4.8.1 Write Data Mask” for data mask functionality.)

4.44.2.3 TDQS/DM Disable

When the TDQS is disabled, MR5:OP[4] = 0, the MR5:OP[5] bit may be used to enable or disable the DM_n pin function.

When both TDQS and DM functions are disabled, termination will be turned off and the pins will drive Hi-Z. The DM_n pin input receiver will be turned-off and does not expect any valid logic level.

Table 164 — x8 TDQS Function Matrix

TDQS (MR5:OP[4])	DM
0_B: Disabled (default)	MR5:OP[5]
1_B: Enabled	Disabled

5 On-Die Termination

5.1 On-Die Termination for DQ

ODT (On-Die Termination) is a feature of the DDR5 SDRAM that allows the DRAM to change termination resistance for each DQ, Unlike previous DDR technologies, DDR5 no longer has a physical ODT pin and all ODT based control is now command & mode register based. DQS_t, DQS_c and DM_n for x4 and x8 configuration (and TDQS_t, TDQS_c for X8 configuration), when enabled via Read (for NT ODT usage), Write Commands or Default Parking value with MR setting. For x16 configuration, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. In addition to the control capability of the DQ ODT, the DQS ODT will now be independently programmed via MR33:OP[5:3] and held static. All ODT control will be targeted for the DQs. This addition allows for adjusting the delay common in an unmatched architecture. DQS RTT offset control mode is enabled via MR39:OP[2:0].

The ODT feature is turned off and not supported in Self-Refresh mode, but does have an optional mode with in Power Down. A simple functional representation of the DRAM ODT feature is shown in Figure 170.

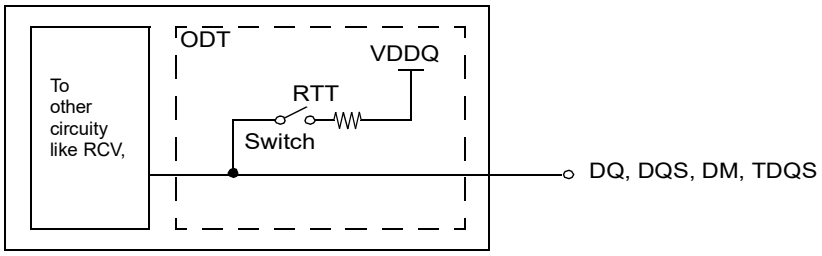


Figure 170 — Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses command decode, Mode Register Settings and other control information, see below. The value of RTT is determined by the settings of Mode Register bits.

5.2 ODT Modes, Timing Diagrams and State Table

The ODT Mode of DDR5 SDRAM has 5 states, Data Termination Disable, RTT_WR, RTT_NOM_RD, RTT_NOM_WR and RTT_PARK. The ODT Mode is enabled based on Mode Registers for each RTT listed below. In this case, the value of RTT is determined by the settings of those bits.

After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Application: Controller can control each RTT condition with WR/RD command and use of ODT Offset Control Mode Registers.

- RTT_WR: The rank that is being written to provide termination and adjusts timing based on ODT Control Mode Register settings.
- RTT_NOM_RD: DRAM turns ON RTT_NOM_RD if it sees CS asserted during the second pulse of the READ command (except when ODT is disabled by MR35:OP[5:3]).
- RTT_NOM_WR: DRAM turns ON RTT_NOM_WR if it sees a CS asserted during the second pulse of the WRITE command (except when ODT is disabled by MR35:OP[2:0])
- RTT_PARK: Default parked value set via MR34:OP[2:0] and is to be enabled when a READ or WRITE is not active.
- DQS_RTT_PARK: Default parked value set for DQS via MR33:OP[5:3] and is to be enabled when a READ is not active
- Data Termination Disable: DRAM driving data upon receiving READ command disables the termination after RL-1 and stays off for a duration of BL/2.
- Strobe Termination Disable: DRAM driving strobe upon receiving READ command disables the termination after RL-1-tRPRE and stays off for a duration of BL/2+tRPST.

Those RTT values have priority as following:
1. Data Termination Disable & Strobe Termination Disable
2. RTT_WR
3. RTT_NOM_RD
4. RTT_NOM_WR
5. RTT_PARK

which means if there is a WRITE command, then the DRAM turns on RTT_WR, not RTT_NOM_WR or RTT_NOM_RD, and also if there is a READ command, then the DRAM disables data termination and goes into Driving mode. If during the second pulse of a READ or WRITE command, a CS enable is sent, then Non-Target ODT is enabled and the appropriate RTT_NOM_RD or RTT_NOM_WR is enabled for the non-target rank. This provides additional and potentially different termination options for the other ranks on the channel.

Table 165 — Termination State Table

Command	Mode Register Configuration Settings				Results		Note
	RTT_PARK	RTT_WR	RTT_NOM_WR	RTT_NOM_RD	Target DRAM Term	Non-Target DRAM Term	
ANY	Disabled				HI-Z (ODT OFF)		3
Any Non-Term CMD	Enabled	Don't Care			RTT_PARK	RTT_PARK	4
WR	Disabled			Don't Care	HI-Z (ODT OFF)	HI-Z (ODT OFF)	
	Disabled		Enabled		HI-Z (ODT OFF)	RTT_NOM_WR	
	Disabled	Enabled	Disabled		RTT_WR	HI-Z (ODT OFF)	
	Don't Care	Enabled			RTT_WR	RTT_NOM_WR	2
	Enabled		Disabled		RTT_WR	HI-Z (ODT OFF)	2,5
	Enabled	Disabled	Enabled		RTT_PARK	RTT_NOM_WR	
	Enabled	Disabled			RTT_PARK	HI-Z (ODT OFF)	5
RD/MRR	Enabled	Don't Care		Disabled	HI-Z (ODT OFF)	HI-Z (ODT OFF)	1,5
	Don't Care			Enabled	HI-Z (ODT OFF)	RTT_NOM_RD	1

NOTE 1 - When read command is executed, DRAM termination state of target rank will be Hi-Z for defined period independent of MR setting of RTT_PARK/RTT_NOM_RD/ RTT_NOM_WR.
NOTE 2 - If RTT_WR is enabled, RTT_WR will be activated by Write command for defined period time independent of MR setting of RTT_PARK /RTT_NOM.
NOTE 3 - If all RTT configs are disabled, ODT receiver power will be turned off to save power.
NOTE 4 - If RTT_PARK is enabled, DRAM RTT_PARK termination will be enabled while WR/RD/MRR are not being executed.
NOTE 5 - When a Non-Target ODT command is executed and the RTT_NOM_WR or RTT_NOM_RD is disabled, the DRAM termination state of the non-target rank will be Hi-Z for a defined period, independent of the MR setting of RTT_PARK.

On-Die Termination effective resistance RTT is defined by MR bits.
ODT is applied to the DQ, DM, DQS_T/DQS_C and TDQS_T/TDQS_C (x8 devices only) pins.
A functional representation of the on-die termination is shown in the figure below.

$$RTT = \frac{VDDQ - Vout}{|\ I\ out\ |}$$

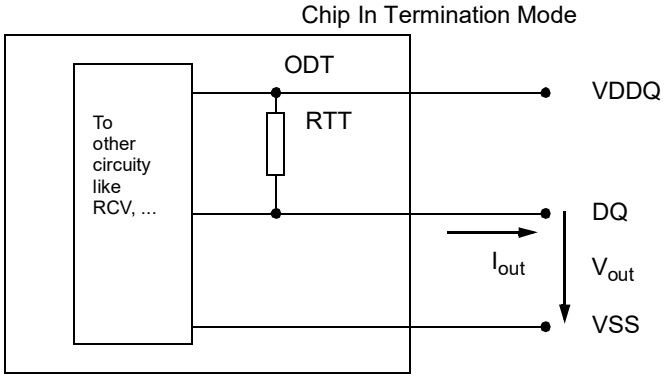


Figure 171 — On Die Termination

On die termination effective Rtt values supported are 240,120, 80, 60, 48, 40, 34 ohms.

Table 166 — ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration

RTT	Vout	Min	Nom	Max	Unit	NOTE
240Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ	1,2,3
120Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/2	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/2	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/2	1,2,3
80Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/3	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/3	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/3	1,2,3
60Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/4	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/4	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/4	1,2,3
48Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
40Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/6	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/6	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/6	1,2,3
34Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mismatch within byte	VOMdc = 0.8* VDDQ	0	-	8	%	1,2,4,5,6

NOTES:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 0.95*VDDQ.
3. The tolerance limits are specified under the condition that VDDQ=VDD and VSS=VSS
4. DQ to DQ mismatch within byte variation for a given component including DQS_T and DQS_C (characterized)
5. RTT variance range ratio to RTT Nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-DQ Mismatch in a Device} = \frac{\text{RTTMax -RTTMin}}{\text{RTTNOM}} * 100$$

6. This parameter of x16 device is specified for Upper byte and Lower byte.

5.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR5 SDRAM can be changed without issuing an MRW command. This requirement is supported by the “Dynamic ODT” feature as described as follows:

5.3.1 ODT Functional Description

The function is described as follows:

- Five RTT values are available: RTT_NOM_RD, RTT_NOM_WR, RTT_PARK, RTT_WR and DQS_RTT_PARK.
  - The value for RTT_NOM_RD is preselected via MR35:OP[5:3]
  - The value for RTT_NOM_WR is preselected via MR35:OP[2:0]
  - The value for RTT_WR is preselected via MR34:OP[5:3]
  - The value for RTT_PARK is preselected via MR34:OP[2:0] - Programmed via MPC command
  - The value for DQS_RTT_PARK is preselected via MR33:OP[5:3] - Programmed via MPC command

- During operation without commands, the termination is controlled as follows;
  - Nominal termination strength for all types (RTT_NOM_RD, RTT_NOM_WR, RTT_WR, RTT_PARK & DQS_RTT_PARK) are selected.
  - RTT_NOM_RD & RTT_NOM_WR on/off timings are controlled via the respective NT Read and Write command and latencies.
  - DQS_RTT_PARK is held static and is based on the value programmed in the MR listed above.
- When a write command (WR) is registered, the termination is controlled as follows:
  - A latency ODTLon_WR after the write command, termination strength RTT_WR is selected.
  - A latency ODTLoff_WR after the write command, termination strength RTT_WR is de-selected.

- The termination, RTT_NOM_WR, for the non-target Write command is selected and de-selected by latencies ODTLon_WR_NT and ODTLoff_WR_NT, respectively.

- When a Read command (RD) is registered, the termination is controlled as follows:
  - A latency ODTLoff_RD after the Read command, data termination is disabled. Then, ODTLon_RD after the Read command, data termination is enabled.
  - A latency ODTLoff_RD_DQS after the Read command, strobe termination is disabled. ODTLon_RD_DQS after the Read command, strobe termination is enabled.

- The termination, RTT_NOM_RD, for the non-target Read command is selected and de-selected by latencies ODTLon_RD_NT and ODTLoff_RD_NT, respectively.

The duration of a Write or Read command is a full burst cycle, BL/2. The termination select ("ODTLon_...") and de-select ("ODTLoff_...") latency settings shall not result in an ODT pulse width which violates a burst cycle (BL/2) minimum duration. The equation "ODTLoff_*X* - ODTLon_*X* >= BL/2” must be met, where *X* is the termination latency setting associated with a particular command type (WR, WR_NT, RD_NT).

To achieve the minimum write burst duration, ODTLoff_*X* and ODTLon_*X* latencies contain independent programmable mode register offsets:

- The values for the Write command ODT control offsets are preselected via MR37.
  - MR37:OP[2:0] preselects ODTLon_WR_Offset
  - MR37:OP[5:3] preselects ODTLoff_WR_Offset
- The values for the non-target Write command ODT control offsets are preselected via MR38.
  - MR38:OP[2:0] preselects ODTLon_WR_NT_Offset
  - MR38:OP[5:3] preselects ODTLoff_WR_NT_Offset
- The values for the non-target Read command ODT control offsets are preselected via MR39.
  - MR39:OP[2:0] preselects ODTLon_RD_NT_Offset
  - MR39:OP[5:3] preselects ODTLoff_RD_NT_Offset

The combination of allowable ODT offsets are shown in Table 167:

Table 167 — Allowable ODTL Offset Combinations

		ODTLon_WR_Offset, ODTLon_WR_NT_Offset, ODTLon_RD_NT_Offset Setting						
		-4	-3	-2	-1	0	1	2
ODTLoff_WR_Offset, ODTLoff_WR_NT_Offset, ODTLoff_RD_NT_Offset Setting	4	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	3	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	1	Valid	Valid	Valid	Valid	Valid	Valid	Invalid
	0	Valid	Valid	Valid	Valid	Valid	Invalid	Invalid
	-1	Valid	Valid	Valid	Valid	Invalid	Invalid	Invalid
	-2	Valid	Valid	Valid	Invalid	Invalid	Invalid	Invalid

Note 1: The offset combinations apply to the ODTLon and ODTLoff independently for each command type (e.g., ODTLon_WR_Offset and ODTLoff_WR_Offset are subject to these restrictions, but there are no restrictions on the setting of ODTLon_WR_Offset with respect to ODTLoff_WR_NT_Offset and ODTLoff_RD_NT_Offset).

Note 2: Although shown in the table, not all offset combinations may be valid for ODTL_WR, ODTL_WR_NT or ODTL_RD_NT. Reference MR37, MR38 or MR39, respectively, for valid offset settings.

See the table below for ODT latency and timing parameter details:

Table 168 — Latencies and timing parameters relevant for Dynamic ODT and CRC disabled

Name and Description	Abbr.	Defined from	Define to	DDR5 speed bins 4400 to 5600	Unit	Note
ODT Latency On from WRITE command to RTT Enable	tODTLon_WR	Registering external write command	Change RTT strength from Previous State to RTT_WR	tODTLon_WR = WL+ODTLon_WR_offset	nCK	1
ODT Latency On from NT WRITE command to RTT Enable	tODTLon_WR_NT	Registering external write command	Change RTT strength from Previous State to RTT_NOM_WR	tODTLon_WR_NT = WL+ODTLon_WR_NT_offset		1
ODT Latency Off from WRITE command to RTT Disable	tODTLoff_WR	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_NOM_RD/RTT_NOM_WR/ Hi-Z	tODTLoff_WR = WL+BL/2+ ODTLoff_WR_offset	nCK	1
ODT Latency Off from NT WRITE command to RTT Disable	tODTLoff_WR_NT	Registering external write command	Change RTT strength from RTT_NOM_WR to RTT_PARK/ RTT_NOM_RD/RTT_WR/ Hi-Z	tODTLoff_WR_NT = WL+BL/2+ ODTLoff_WR_NT_offset		1
Data Termination Disable	tODTLoff_RD	Registering external read command	Disables the termination upon driving data	Data Termination Disable = RL-1		2
Data Termination Enable	tODTLon_RD	Registering external read command	Re-enables the termination after driving data	Data Termination Enable = RL+BL/2		2
Strobe Termination Disable	tODTLoff_RD_DQS	Registering external read command	Disables the termination upon driving strobe	Strobe Termination Disable = RL-1-tRPRE-ReadDQSOffset		2
Strobe Termination Enable	tODTLon_RD_DQS	Registering external read command	Re-enables the termination after driving strobe	Strobe Termination Enable = RL+BL/2+tRPST-**0.5**-ReadDQSOffset		2
ODT Latency On from NT READ command to RTT Enable	tODTLon_RD_NT	Registering external read command	Change RTT strength from Previous State to RTT_NOM_RD	tODTLon_RD_NT = RL+ODTLon_RD_NT_offset	nCK	1
ODT Latency Off from NT READ command to RTT Disable	tODTLoff_RD_NT	Registering external read command	Change RTT strength from RTT_NOM_RD to RTT_PARK/ RTT_NOM_WR/RTT_WR/ HI-Z	tODTLoff_RD_NT = RL+BL/2+ ODTLoff_RD_NT_offset		1
RTT change skew	tADC	Transitioning from one RTT State to the next RTT State	RTT valid	tADC(min) = 0.2 tADC(max) = 0.8	tCK(avg)	3

Note(s):

1 - All "_offset" parameters refer to the ODT Configuration Mode Registers settings in MR37 to MR39.

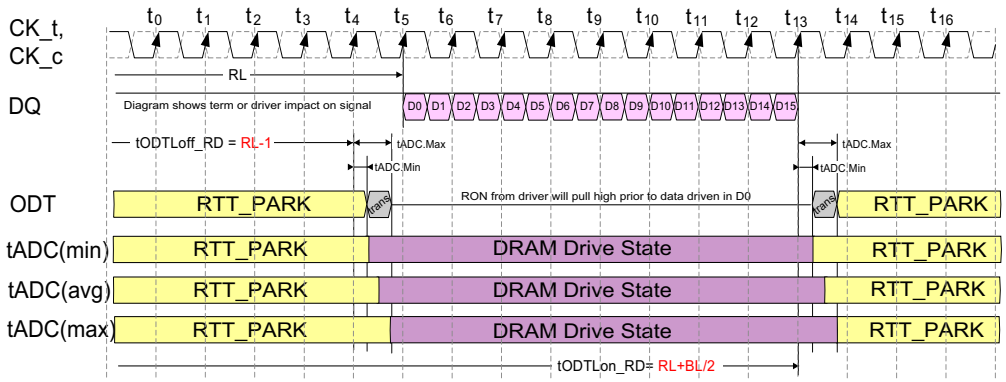
2 - For simplicity, Reads are assigned the same type of timing parameter; however, unlike others, it is a fixed timing and does not have an offset mode register to control it. To indicate this, it was named Data (or Strobe) Termination Disable and Enable.

3 - When transitioning from a value of RTT equal to RA, to a value of RTT equal to RB, the RTT termination resistance during the transition must be constrained for the minimum of (RA,RB) to the maximum of (RA, RB).

5.3.2 ODT tADC Clarifications

tADC is defined as the time it takes for the DRAM to transition from one RTT state to the next RTT state, in case of the read, it's the time from the RTT state to the DRAM Drive state. Unless the RTT is specifically disabled, no High-Z state shall be allowed during tADC. During DRAM Drive state, the DRAM RON shall keep the DQ signal high prior to the first DQ transition. The DFE should assume that 4UI prior to D0 the signal is HIGH.

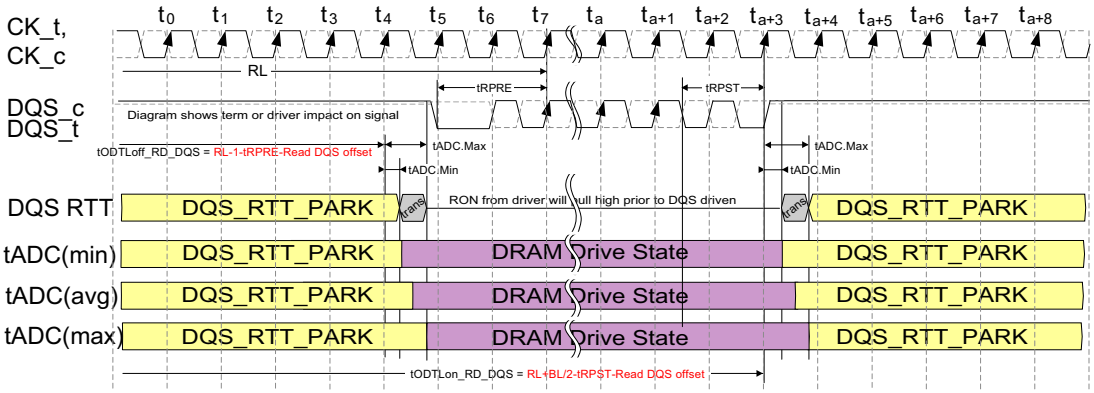
Below are examples showing the tADC(min), tADC(avg) and tADC(max) with respect to the RTT status and effects on the DQ lines prior to the burst.



Note(s):
1. The follow diagram shows a transition from RTT_PARK to Read DRAM Drive state. When tADC transitions from RTT to Read Drive state, the DRAM RON from the driver will keep the DQ signal high prior to the data driven in D0. No High-Z time during tADC is allowed in this example.
2. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
3. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Figure 172 — tADC Clarification - Example 1 - DQ RTT Park to Read

Below is an example showing the tADC(min), tADC(avg) and tADC(max) with respect to the RTT status and effects on the DQS lines prior to the burst.



Note(s):
1. The follow diagram shows a transition from DQS_RTT_PARK to Read DRAM Drive state. When tADC transitions from RTT to Read Drive state, the DRAM RON from the driver will keep the DQS signal high prior to the DQS driven at t5. No High-Z time during tADC is allowed in this example.

Figure 173 — tADC Clarification - Example 2 - DQS RTT Park to Read

5.3.3 ODT Timing Diagrams

The following pages provide examples of ODT utilization timing diagrams. Examples of write to write, read to write and read to read are provided for clarification only. Implementations may vary, including termination on other DIMMS.

It is the controller's responsibility to manage command spacing and the programmable aspect of tODLon/off times to ensure that preambles and postambles are included in the RTT ON time.

When there is a 1 tCK ODT control gap for any ODT operation (such as shown in Figure 181), the said gap's RTT value will be the same or smaller (stronger termination) than RTT_PARK.

All timings noted in the figures below are just used as reference.

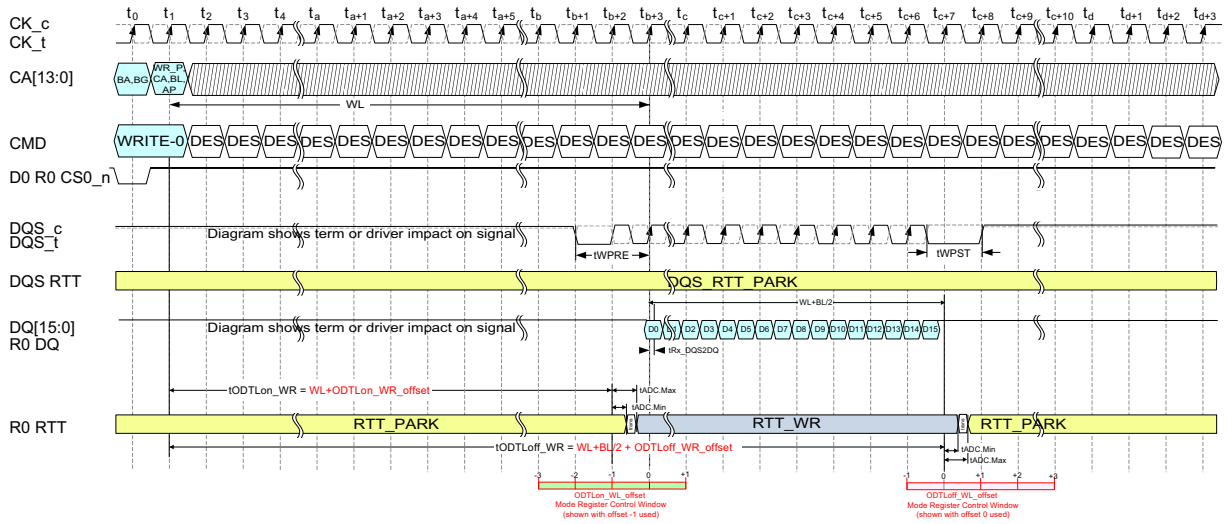


Figure 174 — Example 1 of Burst Write Operation ODT Latencies and Control Diagrams

Note(s):
1. The entire range of ODTL control is not shown for simplicity.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 0.5UI tRX_DQS2DQ, ODTLon_WL_offset configured for -1, ODTLoff_WL_offset configured for 0. Example shows how the host may aggressively adjust the offset of the tODTLon_WR timing to give tADC the min time to settle before data.
3. System designs & margins may vary requiring larger RTT_WR windows.

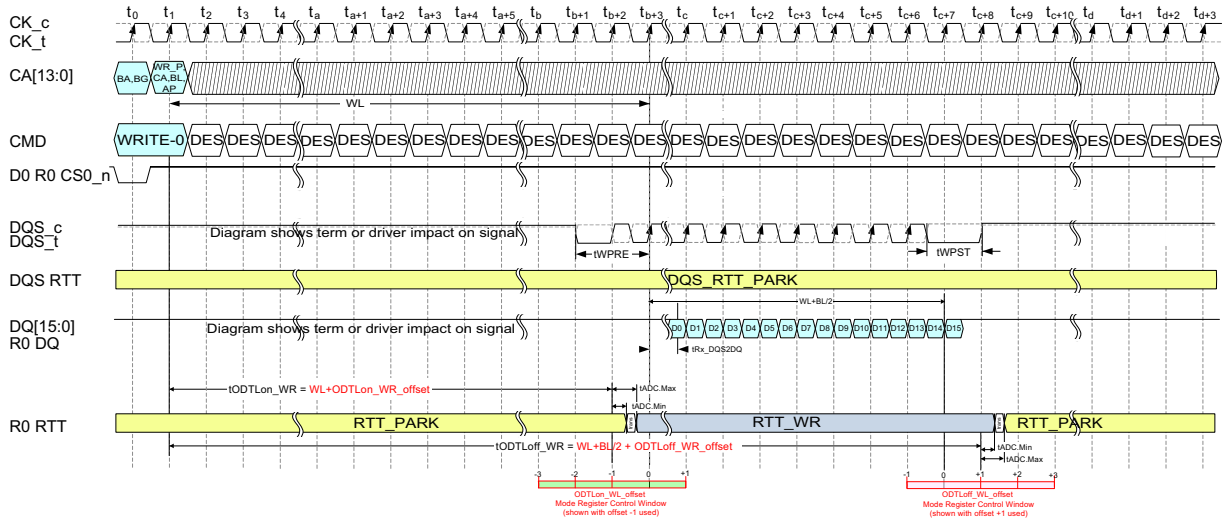


Figure 175 — Example 2 of Burst Write Operation ODT Latencies and Control Diagrams

Note(s):
1. The entire range of ODTL control is not shown for simplicity.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 1.5UI tRX_DQS2DQ, ODTLon_WL_offset configured for -1, ODTLoff_WL_offset configured for +1. Example shows how host may want to add an offset to the tODTLoff_WR time so that RTT_WR stays on for the actual burst.
3. System designs & margins may vary requiring larger RTT_WR windows.

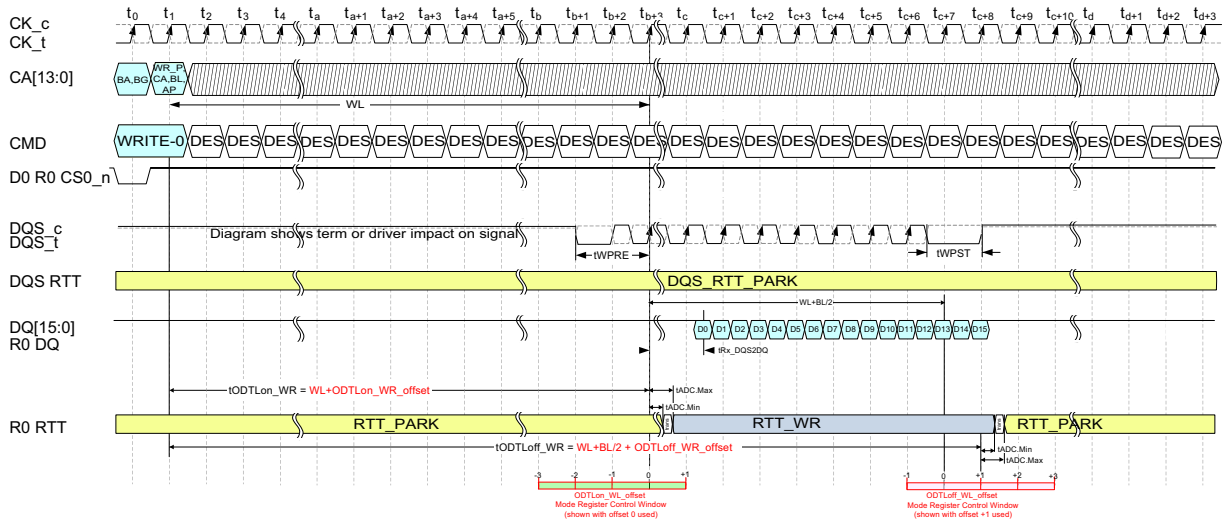


Figure 176 — Example 3 of Burst Write Operation ODT Latencies and Control Diagrams

Note(s):
1. The entire range of ODTL control is now shown for simplicity.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 3UI tRX_DQS2DQ, ODTLon_WL_offset configured for 0, ODTLoff_WL_offset configured for +1. Example shows how host could leave the RTT_WR on time to default values with no offset and may want to add an offset to the tODTLoff_WR time so that RTT_WR stays on for the actual burst.
3. System designs & margins may vary requiring larger RTT_WR windows.

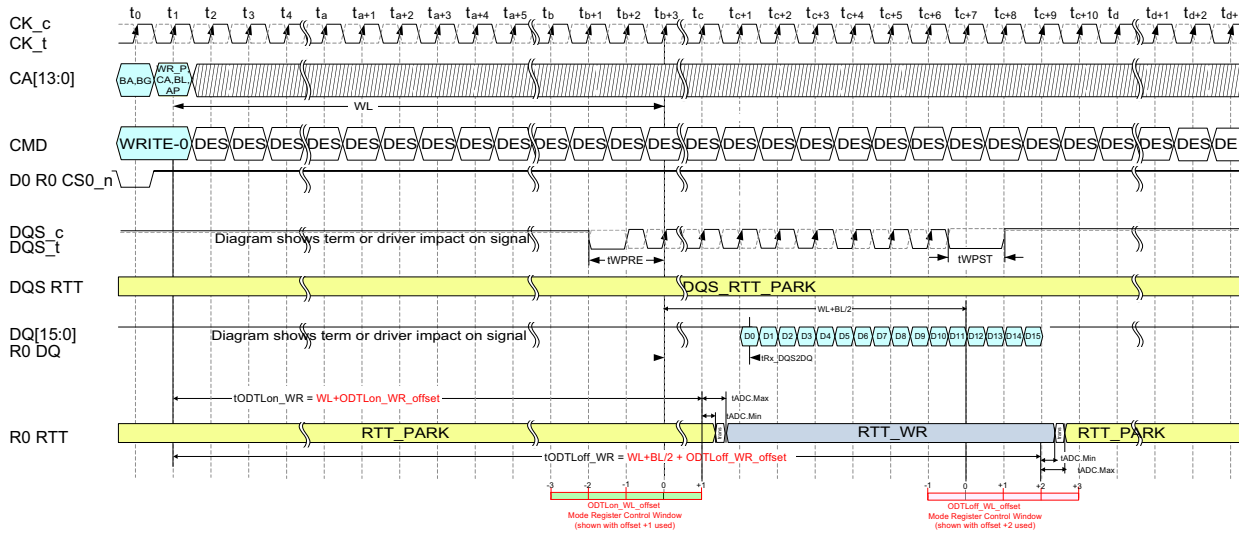


Figure 177 — Example 4 of Burst Write Operation ODT Latencies and Control Diagrams

Note(s):
1. The entire range of ODTL control is not shown for simplicity.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 5UI tRX_DQS2DQ, ODTLon_WL_offset configured for +1, ODTLoff_WL_offset configured for +2. Example shows an extreme case where data is significantly delayed from DQS and how the host may want to add an offset to the tODTLon_WR time so that RTT_WR doesn't turn on too early and how the host may want to delay the tODTLoff_WR time so that it says on for the burst.
3. System designs & margins may vary requiring larger RTT_WR windows.

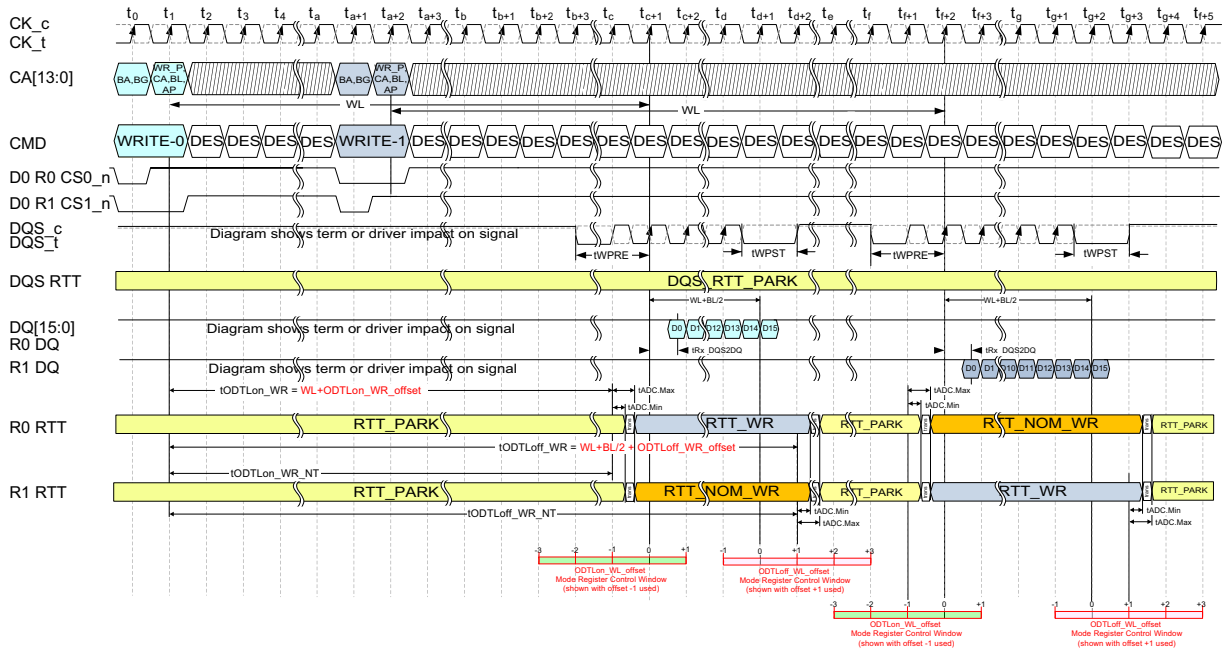


Figure 178 — Example of Write to Write turn around, Different Ranks

Note(s):
1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on Mode Register settings that can push out or pull in the RTT enable and disable time.
2. The entire range of ODTL control is not shown for simplicity.

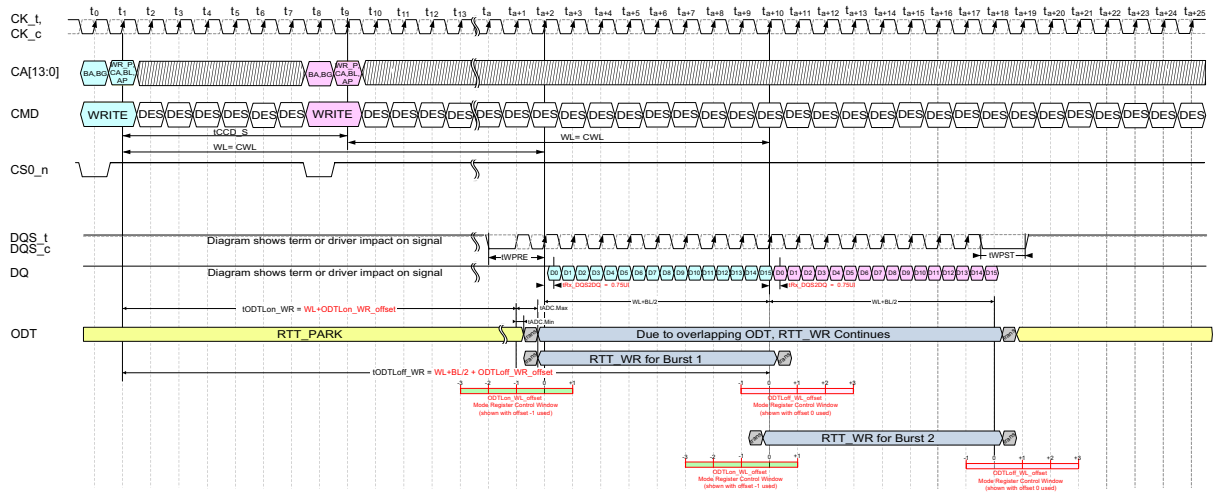


Figure 179 — WRITE (BL16) to WRITE (BL16), Different Bank, Seamless Bursts

Note(s):
1. BL=16, Preamble=2tCK - 0010 pattern, Postamble=1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Figure shown with ODTLon_WR_offset=-1, ODTLoff_WR_offset=0, tRX_DQS2DQ=1UI
4. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
5. The DFE should assume that 4UI prior to D0 the signal is HIGH.

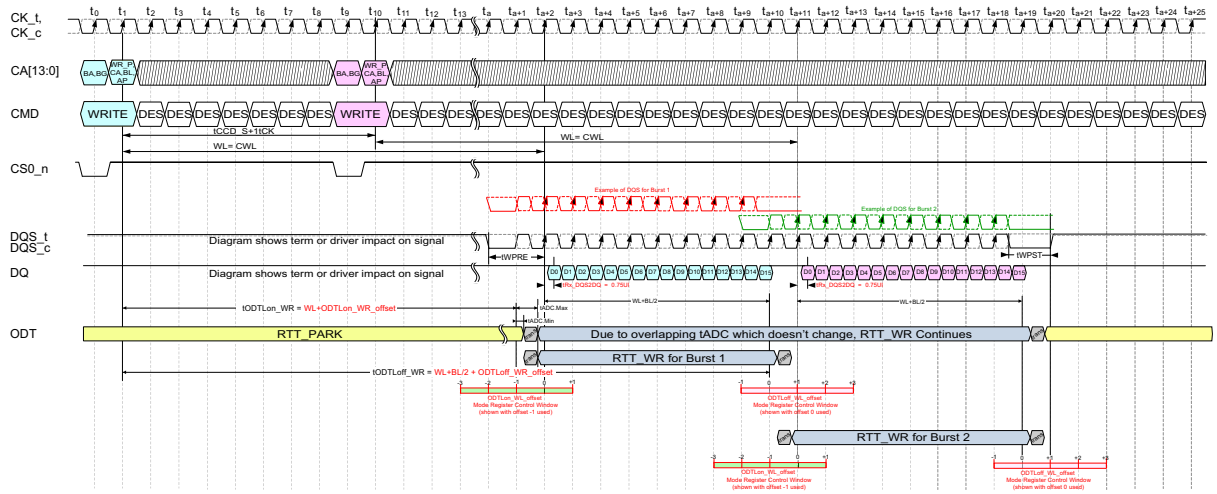


Figure 180 — WRITE (BL16) to WRITE (BL16), Different Bank, 1 tCK Gap

Note(s):
1. BL=16, Preamble=2tCK - 0010 pattern, Postamble=1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Figure shown with ODTLon_WR_offset=-1, ODTLoff_WR_offset=0, tRX_DQS2DQ=1UI
4. Read and Green DQS bursts are shown just for clarification purposes and are not part of an actual signal.
5. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.

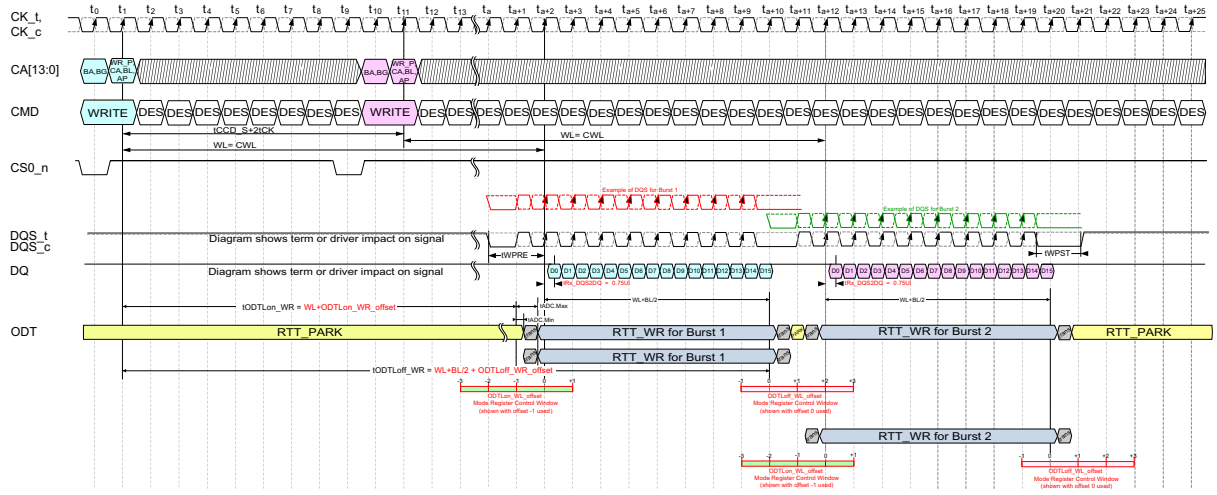


Figure 181 — WRITE (BL16) to WRITE (BL16), Different Bank, 2 tCK Gap

Note(s):
1. BL=16, Preamble=2tCK - 0010 pattern, Postamble=1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Figure shown with ODTLon_WR_offset=-1, ODTLoff_WR_offset=0, tRX_DQS2DQ=1UI
4. Read and Green DQS bursts are shown just for clarification purposes and are not part of an actual signal.
5. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.
7. When there is a 1 tCK ODT control gap for any ODT operation (such as shown in Figure 181), the said gap's RTT value will be the same or smaller (stronger termination) than RTT_PARK.

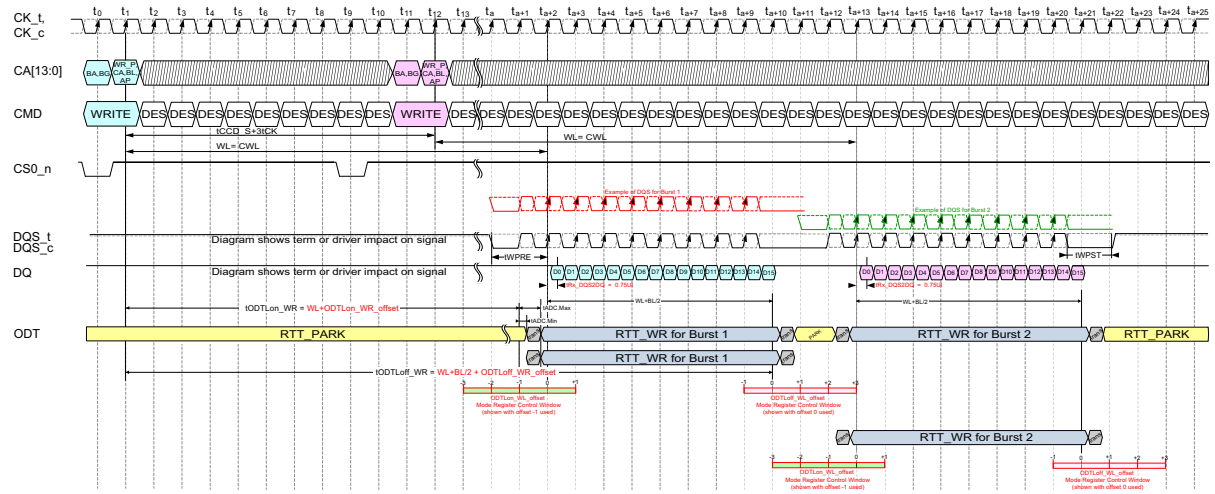


Figure 182 — WRITE (BL16) to WRITE (BL16), Different Bank, 3 tCK Gap

Note(s):
1. BL=16, Preamble=2tCK - 0010 pattern, Postamble=1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Figure shown with ODTLon_WR_offset=-1, ODTLoff_WR_offset=0, tRX_DQS2DQ=1UI
4. Read and Green DQS bursts are shown just for clarification purposes and are not part of an actual signal.
5. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.

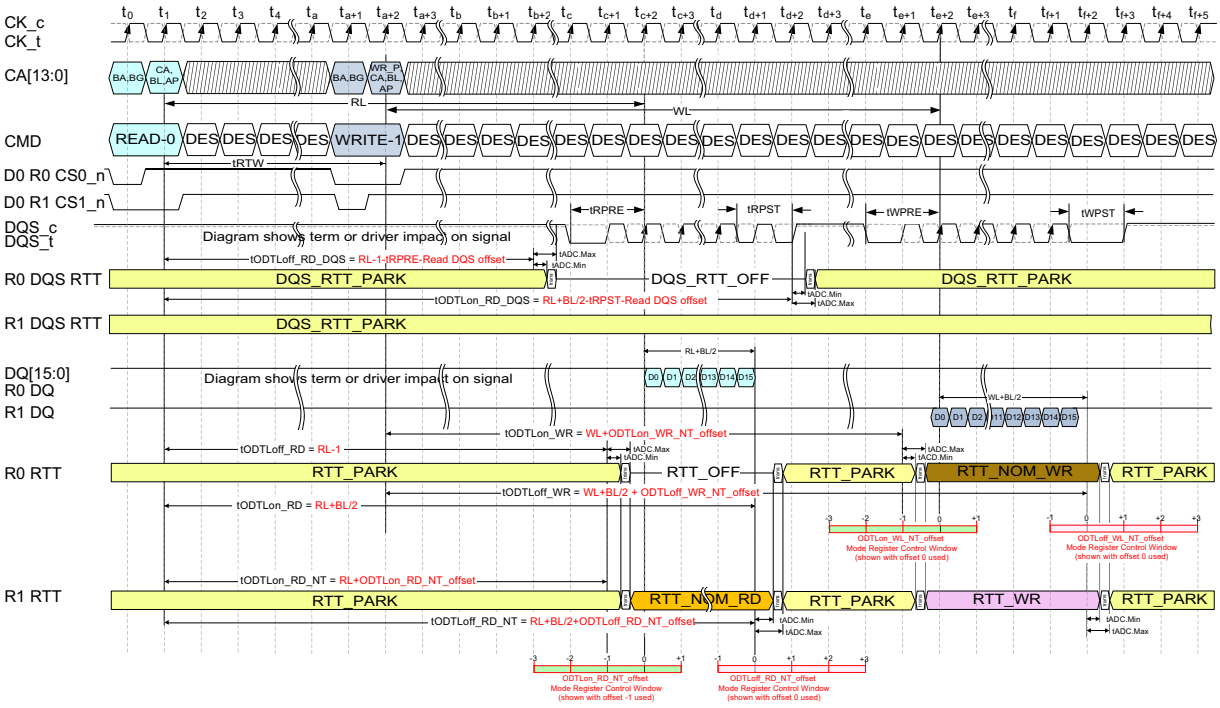


Figure 183 — Example of Read to Write turn around, Different Ranks

Note(s):
1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on Mode Register settings that can push out or pull in the RTT enable and disable time.
2. ODTLon_RD_NT and ODTLoff_RD_NT are based on Mode Register settings that can push out or pull in the RTT enable and disable time.
3. ODTLon_WR_offset and ODTLoff_WR_offset not shown for simplicity.
4. Example shown with near ideal timings for termination settings, exact offset configurations will vary based on system designs.

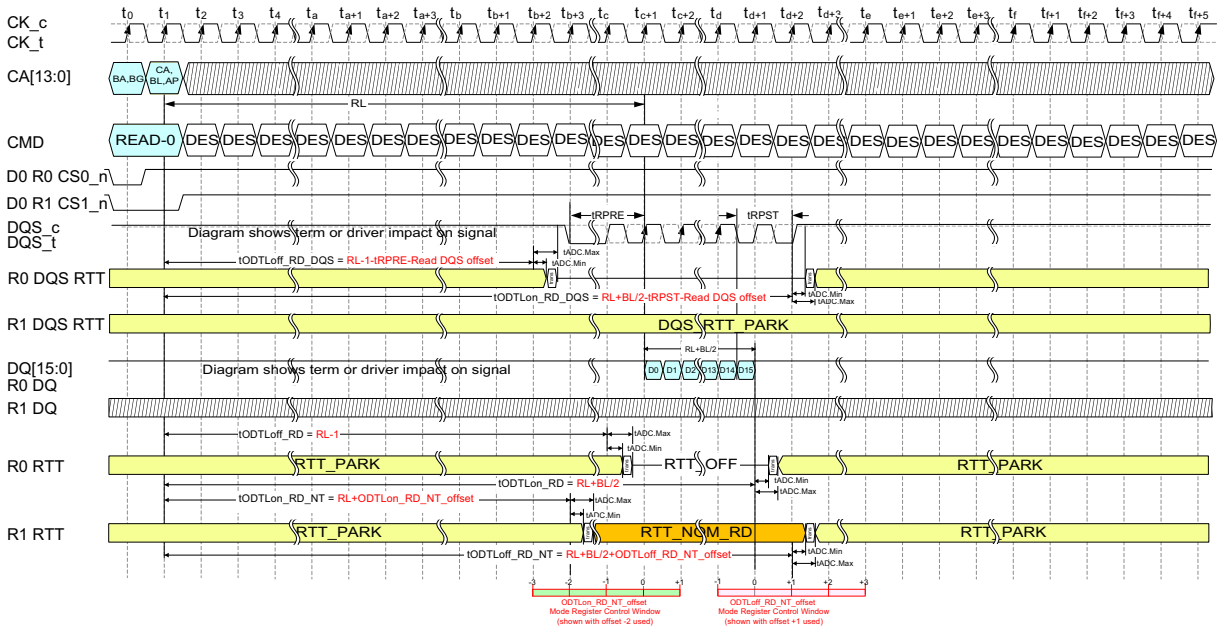


Figure 184 — Example of Burst Read Operation ODT Latencies and Control Diagrams

Note(s):

1. The entire range of ODTL control is now shown for simplicity.
2. Example shown with NT_ODT overlapping normal read disable by 1tCK on both sides (ODTLon_RD_NT_offset = -2 & ODTLoff_RD_NT_offset = +1)

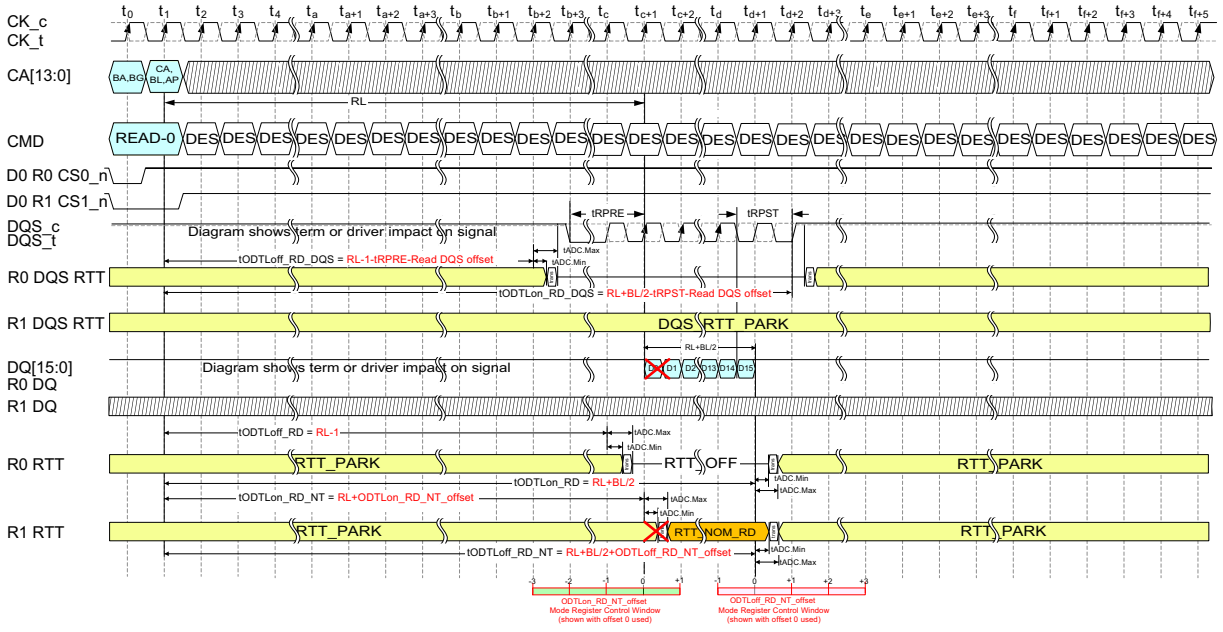


Figure 185 — Example of Burst Read Operation with ODTLon_RD_NT_offset set incorrectly

Note(s):

1. The entire range of ODTL control is now shown for simplicity.
2. Since the ODTLon_RD_NT_Offset was left at zero offset and tADC still had to be considered, the NT RTT turned on too late for the non-target device. tADC is not instantaneous.
3. Since the tODTLoff_RD_NT is referenced from the RL, it is not affected by the offset used for the 'on' time and would turn off 1 clock earlier than the read disable RTT if programed to zero offset. tODTLon_RD_NT and tODTLoff_RD_NT are independently set and calculated from RL.

5.4 On-Die Termination for CA, CS, CK_t, CK_c

The DDR5 DRAM includes ODT (On-Die Termination) termination resistance for CK_t, CK_c, CS and CA signals.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via MR setting.

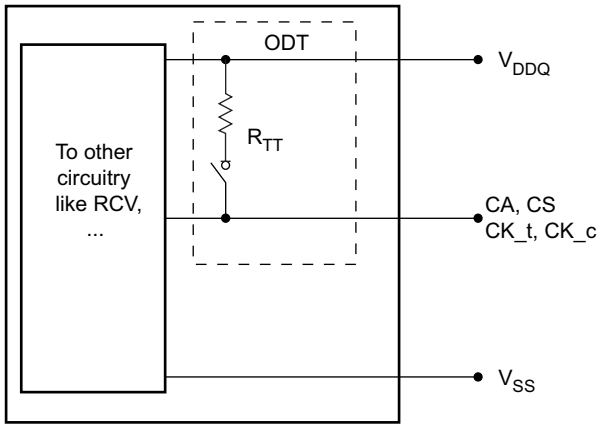


Figure 186 — A simple functional representation of the DRAM CA ODT feature

The ODT termination resistance during power up will be set to the default values based on MR32 and MR33. The ODT resistance values can be configured by those same registers.

On-Die Termination effective resistance RTT is define by MRS bits.
ODT is applied to CK_t, CK_c, CS and CA pins

$$RTT = \frac{VDDQ\text{-}Vout}{|\ I\ out\ |}$$

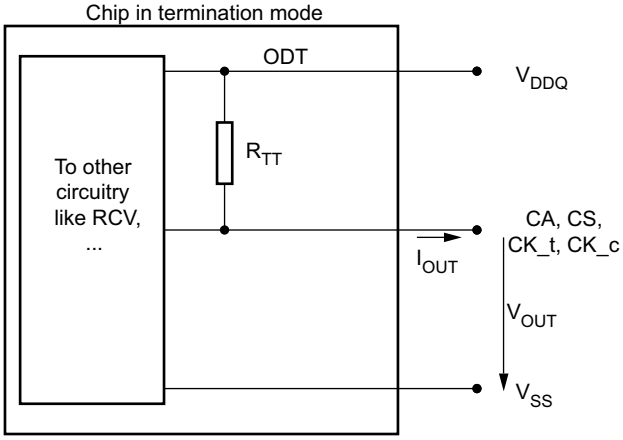


Figure 187 — A functional representation of the on-die termination

5.4.1 Supported On-Die Termination Values

On-die termination effective Rtt values supported are 480, 240,120, 80, 60, 40 ohms

Table 169 — ODT Electrical ChaCharacteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration; VDD=VDDQ

MR	RTT	Vout	Min	Nom	Max	Unit	Note
MR32 for CK & CS MR33 for CA	480Ω	V_{OLdc}= 0.5* VDDQ	0.7	1	1.4	R_{ZQ}*2	1,2,3,5
		V_{OMdc}= 0.8* VDDQ	0.7	1	1.3	R_{ZQ}*2	1,2,3,5
		V_{OHdc}= 0.95* VDDQ	0.6	1	1.3	R_{ZQ}*2	1,2,3,5
MR32 for CK & CS MR33 for CA	240Ω	V_{OLdc}= 0.5* VDDQ	0.9	1	1.25	R_{ZQ}	1,2,3,5
		V_{OMdc}= 0.8* VDDQ	0.9	1	1.1	R_{ZQ}	1,2,3,5
		V_{OHdc}= 0.95* VDDQ	0.8	1	1.1	R_{ZQ}	1,2,3,5
MR32 for CK & CS MR33 for CA	120Ω	V_{OLdc}= 0.5* VDD	0.9	1	1.25	R_{ZQ}/2	1,2,3,5
		V_{OMdc}= 0.8* VDD	0.9	1	1.1	R_{ZQ}/2	1,2,3,5
		V_{OHdc}= 0.95* VDD	0.8	1	1.1	R_{ZQ}/2	1,2,3,5
MR32 for CK & CS MR33 for CA	80Ω	V_{OLdc}= 0.5* VDDQ	0.9	1	1.25	R_{ZQ}/3	1,2,3,5
		V_{OMdc}= 0.8* VDDQ	0.9	1	1.1	R_{ZQ}/3	1,2,3,5
		V_{OHdc}= 0.95* VDDQ	0.8	1	1.1	R_{ZQ}/3	1,2,3,5
MR32 for CK & CS MR33 for CA	60Ω	V_{OLdc}= 0.5* VDDQ	0.9	1	1.25	R_{ZQ}/4	1,2,3,5
		V_{OMdc}= 0.8* VDDQ	0.9	1	1.1	R_{ZQ}/4	1,2,3,5
		V_{OHdc}= 0.95* VDDQ	0.8	1	1.1	R_{ZQ}/4	1,2,3,5
MR32 for CK & CS MR33 for CA	40Ω	V_{OLdc}= 0.5* VDDQ	0.9	1	1.25	R_{ZQ}/6	1,2,3,5
		V_{OMdc}= 0.8* VDDQ	0.9	1	1.1	R_{ZQ}/6	1,2,3,5
		V_{OHdc}= 0.95* VDDQ	0.8	1	1.1	R_{ZQ}/6	1,2,3,5
Mismatch CA-CA within Device		0.8* VDDQ	0		10	%	1,2,4,5

Note(s):
1 - The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2 - Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 0.95*VDDQ.
3 - Measurement definition for RTT:tbd
4 - CA to CA mismatch within device variation for a given component including CS, CK_t and CK_c (characterized)

$$\text{CA-CA Mismatch in a Device} = \left(\frac{RTTMax - RTTMin}{RTTNOM}\right) \times 100$$

5 - Without ZQ calibration ODT effective RTT values have an increased tolerance of +/- 30%

5.5 On-Die Termination for Loopback Signals

The DDR5 DRAM includes ODT (On-Die Termination) termination resistance for the Loopback signals LBDQS and LBDQ.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via MR setting.

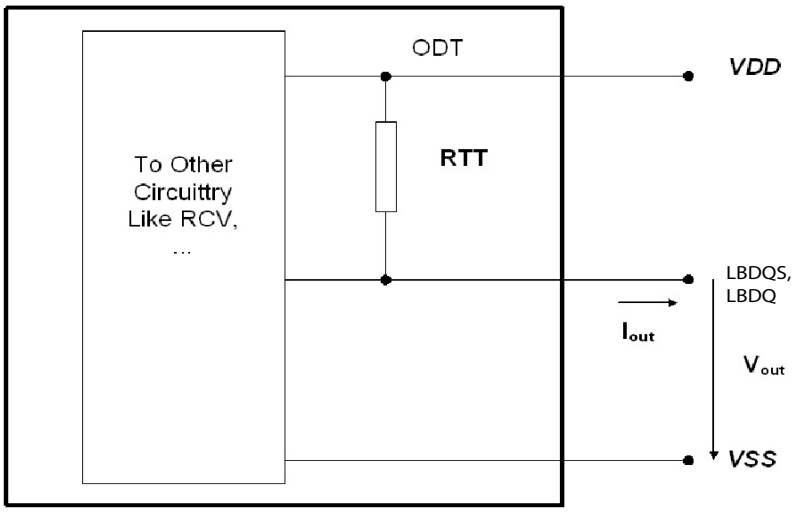


Figure 188 — Functional Representation of Loopback ODT

The ODT termination resistance during power up will be set to the default values based on TBD. The ODT resistance values can be configured by MR TBD.

On-Die Termination effective resistance RTT is defined by MR bits TBD.

ODT is applied to Loopback signals LBDQS and LBDQ. On die termination effective Rtt values supported for the Loopback pins is 48 ohms.

$$RTT = \frac{VDDQ - Vout}{|\ Iout\ |}$$

Table 170 — ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration; VDD=VDDQ

RTT	Vout	Min	Nom	Max	Unit	NOTE
48 ohms	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
Mismatch LBDQS - LBDQ within device	VOMdc = 0.8* VDDQ	0		8	%	1,2,3,4

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 0.95*VDDQ.
3. Measurement definition for RTT:tbd
4. Loopback ODT mismatch within device variation for a given component including LBDQS and LBDQ

$$LBDQS\text{-}LBDQ\ Mismatch\ in\ a\ Device = \left(\frac{RTTMax - RTTMin}{RTTNOM}\right) \times 100$$

6 AC & DC Operating Conditions

6.1 Absolute Maximum Ratings

Table 171 — Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.4	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.4	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.4	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Note(s):

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

6.2 DC Operating Conditions

Table 172 — DC Operating Conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz		Notes
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit	
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	10	mOhm	20	mOhm	3

Note(s):

1. VDD must be within 66mv of VDDQ
2. AC parameters are measured with VDD and VDDQ tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball.
4. Z(f) is defined for all pins per voltage domain. Z(f) does not include the DRAM package and silicon die.

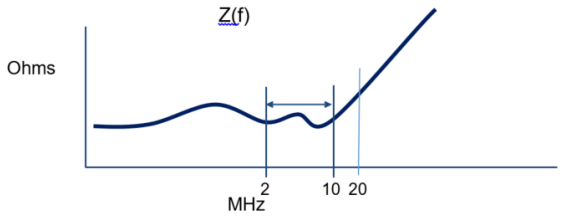


Figure 189 — Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component)

A simplified electrical system load model for Z(F) with the general frequency response is shown in the figure below. The resistance and inductance can be scaled to generalize the spec response to the DRAM pin.

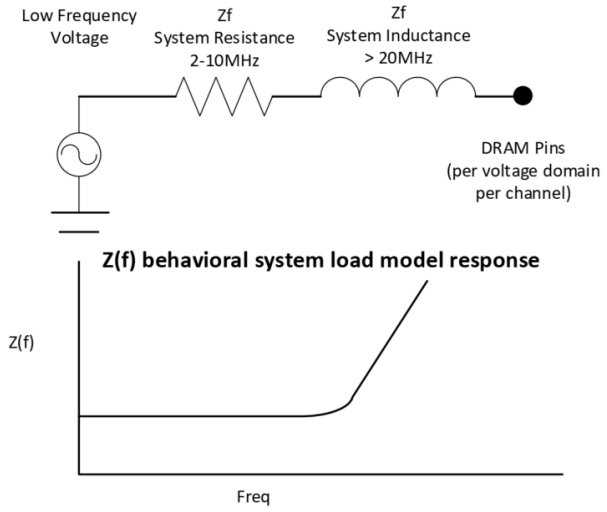


Figure 190 — Simplified Z(f) electrical model and frequency response of PDN at the DRAM pin without the DRAM component

6.3 DRAM Component Operating Temperature Range

Table 173 — DC Operating Temperature Range

Symbol	Parameter	Temperature Range (Unit: °C)		Grade	Notes
		Min	Max		
T_{oper_normal}	Normal Operating Temperature	0	85	NT	1,2,3,4
$T_{oper\_extended}$	Extended Operating Temperature	0	95	XT	1,2,3,4,5

Note(s):

1. All operating temperature symbols, ranges, acronyms are referred from JESD402-1.
2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. All DDR5 SDRDAMs are required to operate in NT and XT temperature ranges.
4. When operating above 85°C, the host shall provide appropriate Refresh mode controls associated with the increased temperature range. The full description of these settings are defined in Table 68 in section 4.13.5
5. Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: $[T_{OPER} - (2.5°C \times \log_2 N)]$, where N is the number of the stacked dies.

7 AC & DC Global Definitions

7.1 Transmitter (Tx), Receiver (Rx) and Channel Definitions - No Ballot

TBD

7.2 Bit Error Rate

7.2.1 Introduction

This section provides an overview of the Bit Error Rate (BER) and the desired Statistical Level of Confidence.

7.2.2 General Equation

$$n = \left(\frac{1}{BER}\right)\left[-\ln(1-SLC) + \ln\left(\sum_{k=0}^{N}\frac{(n\cdot BER)^k}{k!}\right)\right]$$

Where:

n = number of bits in a trial
SLC = statistical level of confidence
BER = Bit Error Rate
k = intermediate number of specific errors found in trial
N = number of errors recorded during trial

If no, errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left(\frac{1}{BER}\right)[-\ln(1-SLC)]$$

JEDEC recommends testing to 99.5% confidence levels; however, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or N=0), using BER=E^{-9} and confidence level SLC=99.5%, the result is n=(1/BER)(-ln(1-0.995) =5.298x10^9.

Results for commonly used confidence levels of 99.5% down to 70% are shown in **Table 7.2.3**.

Table 174 — Estimated Number of Transmitted Bits (n) for the confidence level of 70% to 99.5%

Number Errors	n = -ln(1-SLC)/BER							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/BER	4.61/BER	2.99/BER	2.3/BER	1.90/BER	1.61/BER	1.39/BER	1.20/BER

7.2.3 Minimum Bit Error Rate (BER) Requirements

Table 175 specifies the UIavg and Bit Error Rate requirements over which certain receiver and transmitter timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=E^{-9}.

Table 175 — Minimum BER Requirements for Rx/Tx Timing and Voltage Tests for DDR5-4400 to 5600

Parameter	Symbol	DDR5-4400-4800			DDR5 5200-5600			Unit	Notes
		Min	Nom	Max	Min	Nom	Max		
Average UI	UI_{AVG}	0.999* nominal	1000/f	1.001* nominal	0.999* nominal	1000/f	1.001* nominal	ps	1
Number of UI (min)	$N_{Min\_UI\_Validation}$	$5.3x10^9$	-	-	$5.3x10^9$	-	-	UI	2
Bit Error Rate	BER_{Lane}	-	-	E^{-16}	-	-	E^{-16}	Events	3,4,5

NOTES:
1. Average UI size, “f” is data rate
2. # of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=E^{-9}.
3. This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link layer based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver, therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
4. Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
5. This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx DQ Stressed Eye, Tx DQS Jitter, Tx DQ Jitter, and Tx DQ Stressed EH/EW specifications.

7.3 Unit Interval and Jitter Definitions

This document describes the UI and NUI Jitter definitions associated with the Jitter parameters specified in Rx Stressed Eye, Tx DQS Jitter, Tx DQ Jitter and Input Clock Jitter specifications.

7.3.1 Unit Interval (UI)

The times at which the differential crossing points of the clock occur are defined at t1, t2, …, tn-1, tn,..., tK. The UI at index "n" is defined as shown in **Figure 191** (with n=1,2,…) from an arbitrary time in steady state, where n=0 is chosen as the starting crossing point.

Mathematical definition of UI is shown in **Figure 191** and **Figure 192**.

$$UI_n = t_n - t_{n-1}$$

Figure 191 — UI Definition in Terms of Adjacent Edge Timings

For the Single-Ended data, the unit interval time starts when the signal crosses a pre-specified reference voltage. For the differential clock, the unit interval time starts when the CK_t and CK_c intersect (see **Figure 192**).

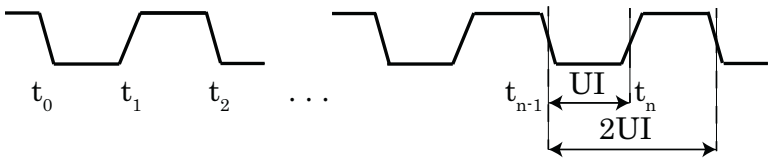


Figure 192 — UI Definition Using Clock Waveforms

7.3.2 UI Jitter Definition

If a number of UI edges are computed or measured at times t1, t2, …, tn-1, tn,..., tK, where K is the maximum number of samples, then the UI jitter at any instance "n" is defined in **Figure 193**, where T = the ideal UI size.

$$UI(jit)_n = (t_n - t_{n-1}) - T, \quad n=1,2,3,...,K$$

Figure 193 — UI Jitter for "nth" UI Definition (in terms of ideal UI)

In a large sample with random Gaussian-like jitter (therefore very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described in **Figure 193** assumes starting from an instant steady state, where n=0 is chosen as the starting point.
1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded strobe. Example: For 6.4 GT/s signaling, the forwarded strobe frequency is 3.2 GHz, or 1 UI = 156.25 ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (BER) for the link.

7.3.3 UI-UI Jitter Definition

UI-UI (read as “UI to UI”) jitter is defined to be the jitter between two consecutive UI as shown in **Figure 194**.

$$\Delta UI_n = UI_n - UI_{n-1} \qquad n=2,3,...,K$$

Figure 194 — UI-UI Jitter Definitions

7.3.4 Accumulated Jitter (Over “N” UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive “N” UI as shown in **Figure 195**.

$$T_{acc}^{N} = \sum_{p=m}^{m+N-1}(UI_p - \overline{UI}) \qquad m=1,2,...,K-N$$

Figure 195 — Definition of Accumulated Jitter (over “N” UI)

where $\overline{UI}$ is defined in the equation shown in **Figure 196**.

$$\overline{UI} = \frac{\sum_{p=1}^{K} UI_p}{K} \qquad p=1,2,...,N,...,K$$

Figure 196 — Definition of $\overline{UI}$

8 AC & DC Input Measurement Levels

8.1 Overshoot and Undershoot specifications for CAC - No Ballot

8.2 CA Rx voltage and timings

Note: The following draft assumes internal CA VREF. If the VREF is external, the specs will be modified accordingly.

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

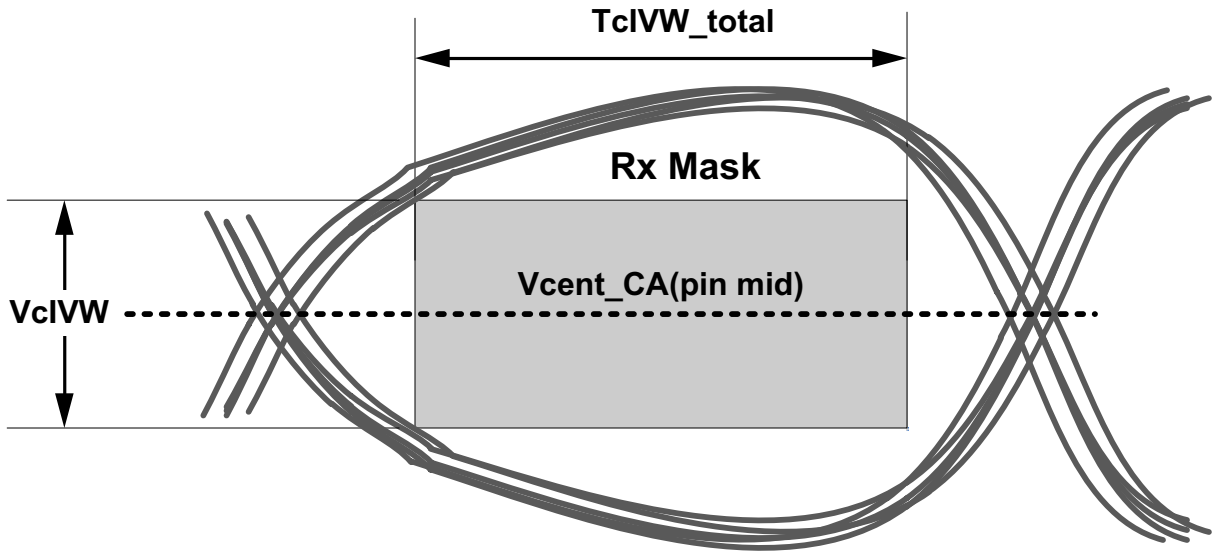


Figure 197 — CA Receiver (Rx) mask

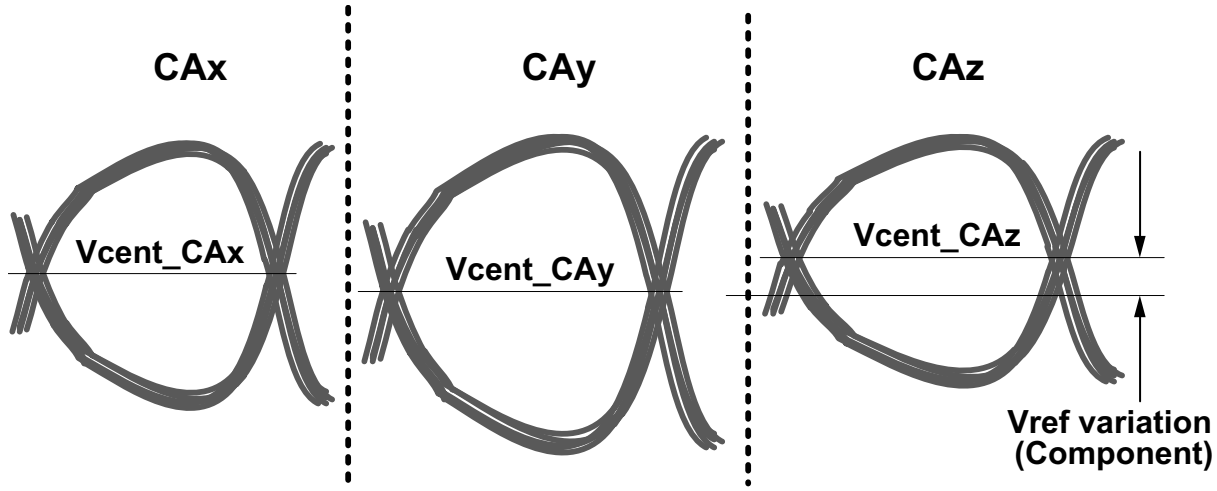
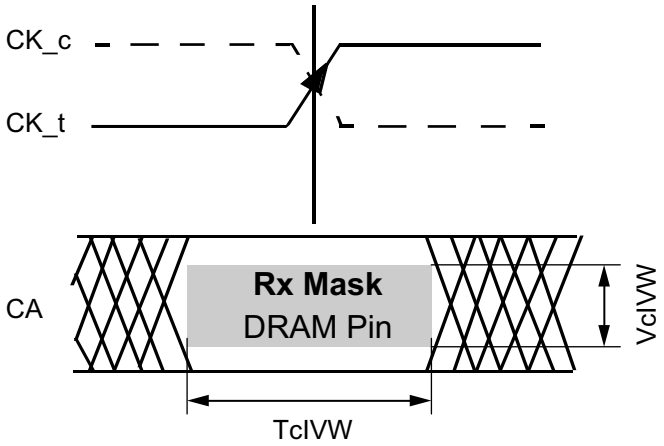


Figure 198 — Across pin V_{REF}CA voltage variation

Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 199. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{REF} will be set by the system to account for Ron and ODT settings.

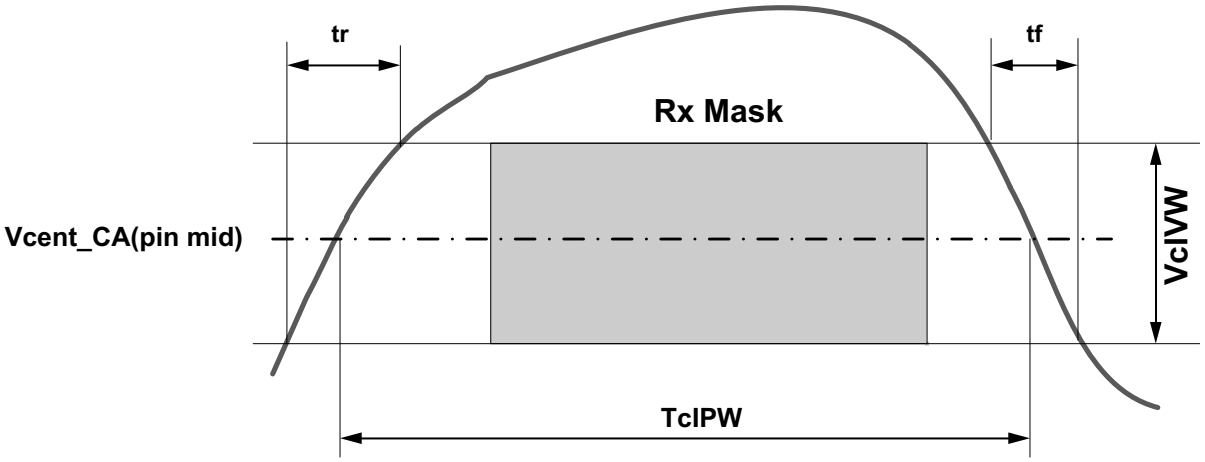
CK_t, CK_c, CA Eye at DRAM Pin

Optimally centered Rx mask



TcIVW is not necessarily center aligned on CK_t/CK_c crossing at the DRAM pin, but is assumed to be center aligned at the DRAM Latch.

Figure 199 — CA Timings at the DRAM Pins



Note
1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 200 — CA TcIPW and SRIN_cIVW definition (for each input pulse)

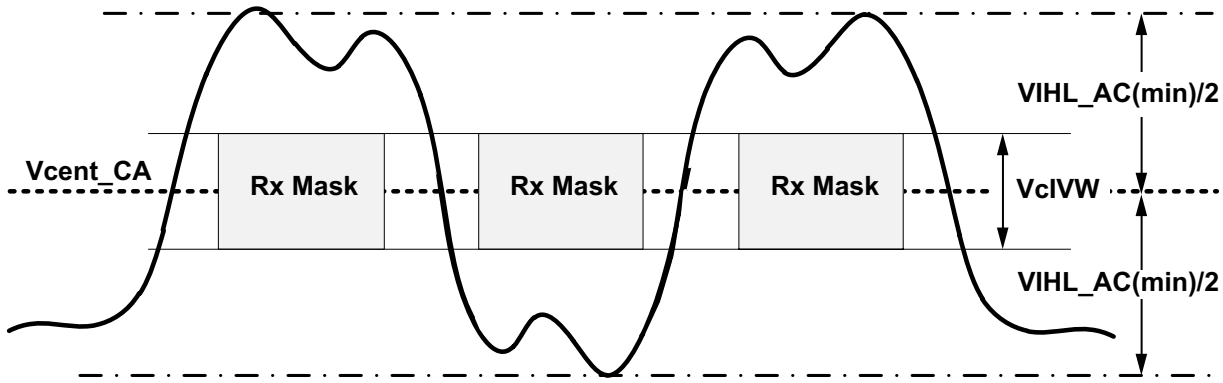


Figure 201 — CA VIHL_AC definition (for each input pulse)

Table 176 — DRAM CA, CS Parametric values for DDR5-4400 to 4800

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	-	130	-	130	mV	1,2,4
Rx Timing Window	TcIVW	-	0.2	-	0.2	UI*	1,2,3,4,8
CA Input Pulse Amplitude	VIHL_AC	150		150		mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		UI*	5,8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	V/ns	6

Note(s):
1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.
8. *** UI=tCK(avg)min**

Table 177 — DRAM CA, CS Parametric values for DDR5-5200 to 5600

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	-	100	-	100	-	TBD	-	TBD	mV	1,2,4
Rx Timing Window	TcIVW	-	0.2	-	0.2	-	TBD	-	TBD	UI*	1,2,3,4,8
CA Input Pulse Amplitude	VIHL_AC	115	TBD	115	TBD	TBD	-	TBD	-	mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		TBD		TBD		UI*	5,8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	V/ns	6

Note(s):
1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.
8. * UI=tck(avg)min

8.3 Input Clock Jitter Specification

8.3.1 Overview

The clock is being driven to the DRAM either by the RCD for L/RDIMM modules, or by the host for U/SODIMM modules (**Figure 202**).

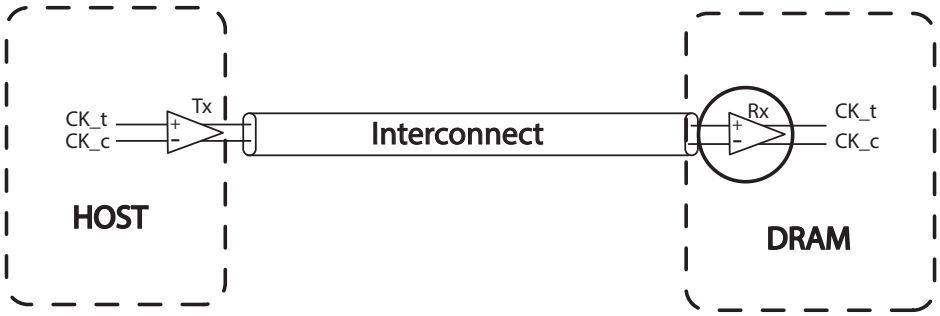


Figure 202 — HOST driving clock signals to the DRAM

8.3.2 Specification for DRAM Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5 SDRAM device.

Table 178 — DRAM Input Clock Jitter Specifications for DDR5-4400 to 4800

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	MHz	1,11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05		0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.030	-	0.030	UI	3,6,11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	UI	3,6,11
Rj RMS value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.0040	-	0.0040	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.074	-	0.074	UI	3,7,11
Tj value of N-UI Jitter, where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	UI	3,10,11,12
Tj value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	UI	3,10,11,12

Note(s):

1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600
2. Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

Table 179 — DRAM Input Clock Jitter Specifications for DDR5-5200 to 5600

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	MHz	1,11
Duty Cycle Error	tCK_Duty_UI_Error	-	TBD	-	TBD	UI	1,4,11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	TBD	-	TBD	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	TBD	-	TBD	UI	3,6,11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	TBD	-	TBD	UI	3,6,11
Rj RMS value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	TBD	-	TBD	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	TBD	-	TBD	UI	3,7,11
Tj value of N-UI Jitter, where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	TBD	-	TBD	UI	3,8,11
Rj RMS value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	UI	3,10,11,12
Tj value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	UI	3,10,11,12

NOTE(S):

1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600
2. Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

8.4 Differential Input Clock (CK_t, CK_c) Cross Point Voltage (VIX)

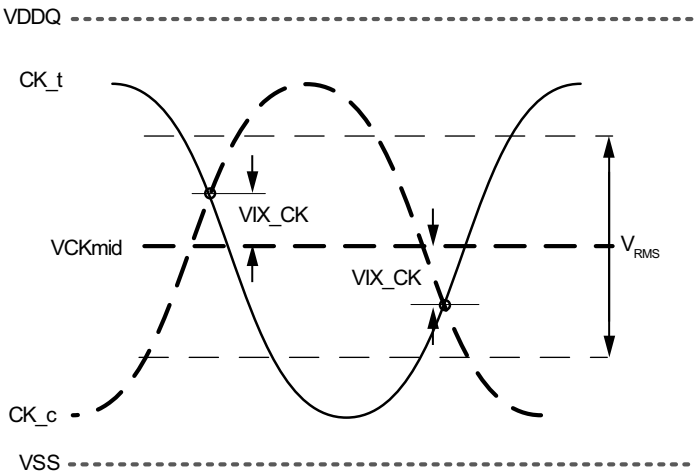


Figure 139 - VIX Definition (CK)

Table 181 — Crosspoint Voltage (VIX) for Differential Input Clock

Parameter	Symbol	DDR5-4400 - 4800		DDR5-5200 - 5600		Unit	Notes
		Min	Max	Min	Max		
Clock differential input crosspoint voltage ratio	VIX_CK_Ratio	-	50	-	50	%	1,2,3

Note(s):
1. The VIX_CK voltage is referenced to VCKmid(mean) = (CK_t voltage + CK_c voltage) /2, where the mean is over 8 UI
2. VIX_CK_Ratio = (|VIX_CK| / |V_{RMS}|)*100%, where V_{RMS} = RMS(CK_t voltage - CK_c voltage)
3. Only applies when both CK_t and CK_c are transitioning

8.5 Differential Input Clock Voltage Sensitivity - Q3'18 Ballot#1858.04

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the Rx voltage sensitivity requirement. The system input swing to the DRAM must be larger than the DRAM Rx at the specified BER

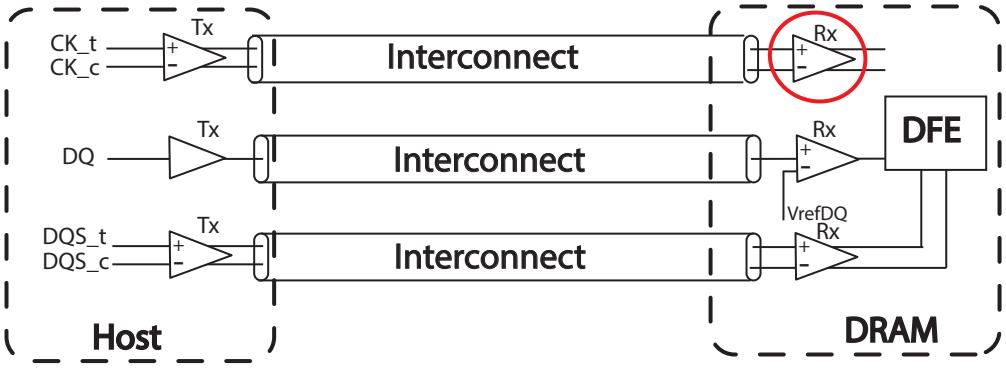


Figure 203 — Example of DDR5 Memory Interconnect

8.5.1 Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

Table 182 — Differential Input Clock Voltage Sensitivity Parameter for DDR5-4400 to 4800

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	180	-	160	mV	1,2

NOTE(S):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)

Table 183 — Differential Input Clock Voltage Sensitivity Parameter for DDR5-5200 to 5600

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	140	-	120	mV	1,2

NOTE(S):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)

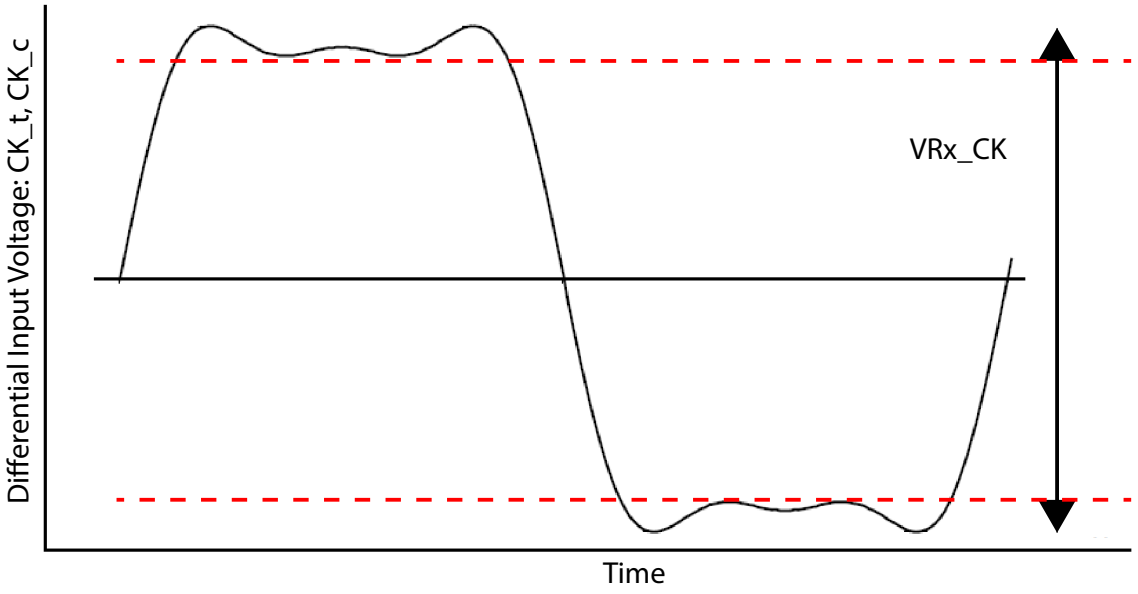


Figure 204 — VRx_CK

8.5.2 Differential Input Voltage Levels for Clock - Q2'19 Ballot #1848.48

Table 185 — Differential Clock (CK_t, CK_c) Input Levels for DDR5-4400 to DDR5-5600

From	Parameter	DDR5 4400-5600	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK_t, CK_c)	0.75 x $V_{diffpk-pk}$	1,2
$V_{ILdiff}CK$	Differential input low measurement level (CK_t, CK_c)	0.25 x $V_{diffpk-pk}$	1,2

Note(s):
1. $V_{diffpk-pk}$ defined in **Figure 205**
2. Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
3. All parameters are defined over the entire clock common mode range

8.5.3 Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below.

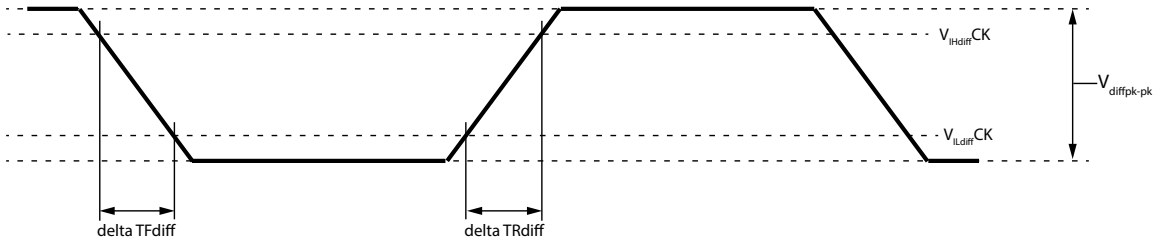


Figure 205 — Differential Input Slew Rate Definition for CK_t, CK_c

Table 186 — Differential Input Slew Rate Definition for CK_t, CK_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (CK_t - CK_c)	$VIL_{diff}CK$	$VIH_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTRdiff	
Differential Input slew rate for falling edge (CK_t - CK_c)	$VIH_{diff}CK$	$VIL_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTFdiff	

Note(s):

Table 187 — Differential Input Slew Rate for CK_t, CK_c for DDR5-4400 to DDR5-4800

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	14	2	14	V/ns	

Note(s):

Table 188 — Differential Input Slew Rate for CK_t, CK_c for DDR5-5200 to DDR5-5600

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	TBD	TBD	TBD	TBD	V/ns	

Note(s):

8.6 Rx DQS Jitter Sensitivity

The receiver DQS jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no cross-talk nor ISI is applied, and must pass through the combination of applied DCD and Rj.

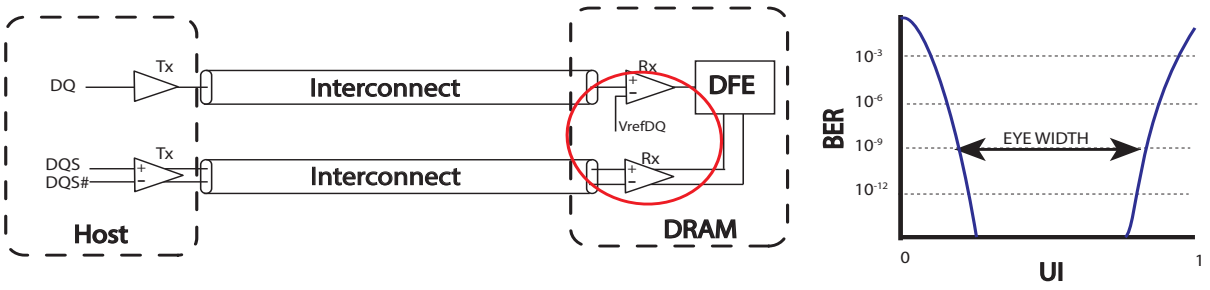


Figure 206 — SDRAM's Rx Forwarded Strobes for Jitter Sensitivity Testing

8.6.1 Rx DQS Jitter Sensitivity Specification

The following table provides Rx DQS Jitter Sensitivity Specification for the DDR5 DRAM receivers when operating at various possible transfer rates. These parameters are tested on the CTC2 card without Rx Equalization set. Additive DFE Gain Bias can be set.

Table 191 — Rx DQS Jitter Sensitivity Specification for DDR5-4400 to 4800

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
DQ Timing Width	tRx_DQ_tMargin	0.825	-	0.825	-	UI	1,2,3,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD	-	0.06	-	0.06	UI	1,4,8,9,10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_Rj	-	0.09	-	0.09	UI	1,5,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD_Rj	-	0.15	-	0.15	UI	1,2,6,8,9,10
Delay of any data lane relative to the DQS_t/ DQS_c crossing	tRx_DQS2DQ	1	3.25	1	3.5	UI	1,7,8,9,10

Note(s):

1. Validation methodology will be defined in future ballots. 2UI is defined as 1tCK for this parameter
2. Each of ΔtRx_DQ_tMargin_DQS_DCD, ΔtRx_DQ_tMargin_DQS_Rj, and ΔtRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more
3. DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 "1s" and 3 "0s"
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
7. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
8. All measurements at BER=E-9
9. This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing

10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

Table 192 — Rx DQS Jitter Sensitivity Specification for DDR5-5200 to 5600

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
DQ Timing Width	tRx_DQ_tMargin	0.835	-	0.835	-	UI	1,2,3,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD	-	0.06	-	0.06	UI	1,4,8,9,10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_Rj	-	0.09	-	0.09	UI	1,5,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD_Rj	-	0.15	-	0.15	UI	1,2,6,8,9,10
Delay of any data lane relative to the DQS_t/ DQS_c crossing	tRx_DQS2DQ	1	3.75	1	4.0	UI	1,7,8,9,10

Note(s):

1. Validation methodology will be defined in future ballots. 2UI is defined as 1tCK for this parameter
2. Each of ΔtRx_DQ_tMargin_DQS_DCD, ΔtRx_DQ_tMargin_DQS_Rj, and ΔtRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more
3. DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
7. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
8. All measurements at BER=E-9
9. This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing
10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

8.6.2 Test Conditions for Rx DQS Jitter Sensitivity Tests

Table 2 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx DQS Jitter Sensitivity parameters specified in **Table 191** and **Table 192**.

Table 193 — Test Conditions for Rx DQS Jitter Sensitivity Testing for DDR5-4400 to 4800

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	UI	1,2,3,6,7,10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	UI (RMS)	1,2,,4,6,8,10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	UI	1,2,5,6,7,9, 10

Note(s):

1. While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2. The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin
3. Various DCD values should be tested, complying within the maximum limits
4. Various Rj values should be tested, complying within the maximum limits
5. Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table
6. Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7. Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)
8. RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
9. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

Table 194 — Test Conditions for Rx DQS Jitter Sensitivity Testing for DDR5-5200 to 5600

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD					UI	1,2,3,6,7,10
Applied Rj RMS to the DQS	tRx_DQS_Rj					UI (RMS)	1,2,4,6,8,10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj					UI	1,2,5,6,7,9,10

Note(s):

1. While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2. The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin
3. Various DCD values should be tested, complying within the maximum limits
4. Various Rj values should be tested, complying within the maximum limits
5. Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table
6. Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7. Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)
8. RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
9. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

8.7 Rx DQS Voltage Sensitivity

8.7.1 Overview

The receiver DQS (strobe) input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

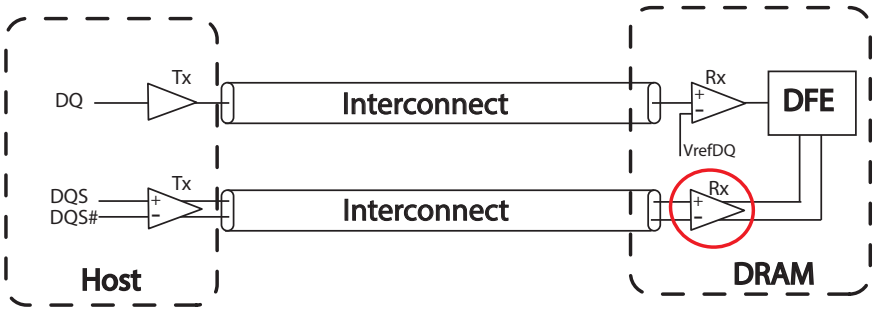


Figure 207 — Example of DDR5 Memory Interconnect

8.7.2 Receiver DQS Voltage Sensitivity Parameter

Input differential (DQS_t, DQS_c) VRx_DQS is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 197 — Rx DQS Input Voltage Sensitivity Parameter for DDR5-4400 to 4800

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	100	-	100	mV	1,2,3

Note(s):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)
3. Test using clock like pattern of repeating 3 "1s" and 3 "0s"

Table 198 — Rx DQS Input Voltage Sensitivity Parameter for DDR5-5200 to 5600

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	90	-	90	mV	1,2,3

Note(s):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)
3. Test using clock like pattern of repeating 3 "1s" and 3 "0s"

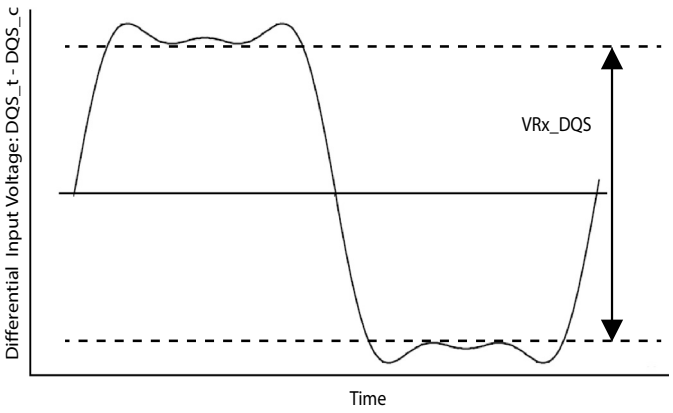


Figure 208 — VRx_DQS

8.8 Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (VIX)

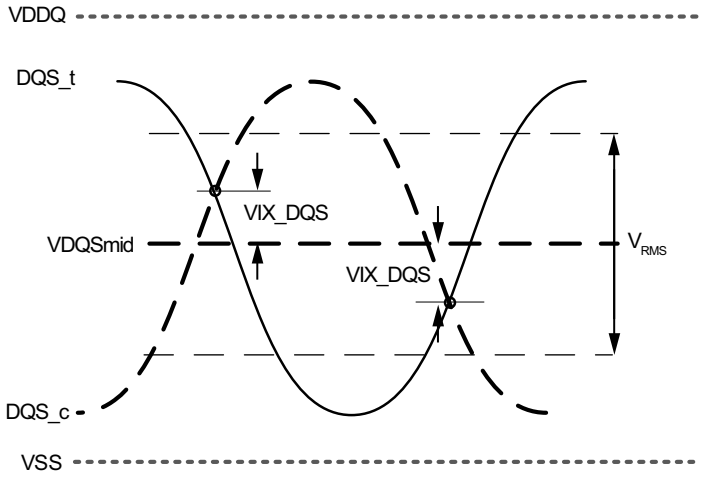


Figure 209 — VIX Definition (DQS)

Table 200 — Crosspoint Voltage (VIX) for DQS Differential Input Signals

Parameter	Symbol	DDR5-4400 - 4800		DDR5-5200 - 5600		Unit	Notes
		Min	Max	Min	Max		
DQS differential input crosspoint voltage ratio	VIX_DQS_Ratio	-	50	-	50	%	1,2,3

Note(s):
1. The VIX_DQS voltage is referenced to VDQSmid(mean) = (DQS_t voltage + DQS_c voltage) /2, where the mean is over 8 UI
2. VIX_DQS_Ratio = (|VIX_DQS| / |V_{RMS}|)*100%, where V_{RMS} = RMS(DQS_t voltage - DQS_c voltage)
3. Only applies when both DQS_t and DQS_c are transitioning (including preamble)

8.9 Rx DQ Voltage Sensitivity

8.9.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

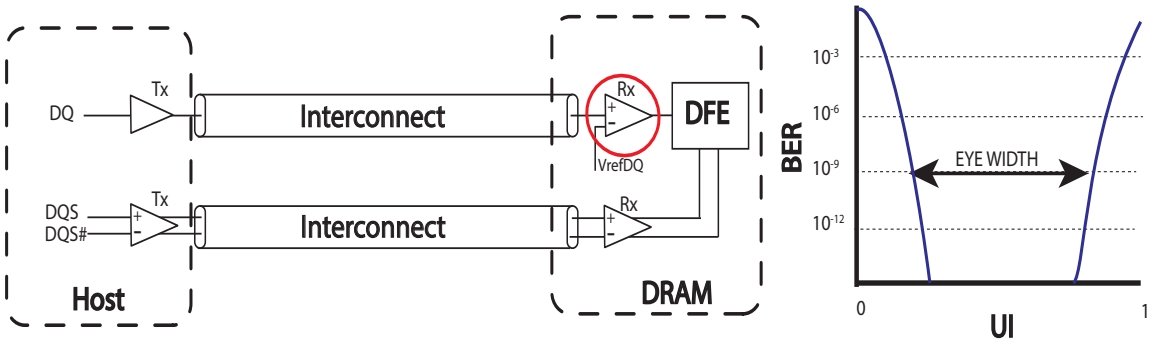


Figure 210 — Example of DDR5 Memory Interconnect

8.9.2 Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended VRx_DQ is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 201 — Rx DQ Input Voltage Sensitivity Parameters for DDR5-4400 to 4800

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	65	-	65	mV	1,2,3

NOTE(S):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)
3. Recommend testing using clock like pattern such as repeating 3 "1s" and 3 "0s"

Table 202 — Rx DQ Input Voltage Sensitivity Parameters for DDR5-5200 to 5600

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	60	-	60	mV	1,2,3

NOTE(S):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)
3. Recommend testing using clock like pattern such as repeating 3 "1s" and 3 "0s"

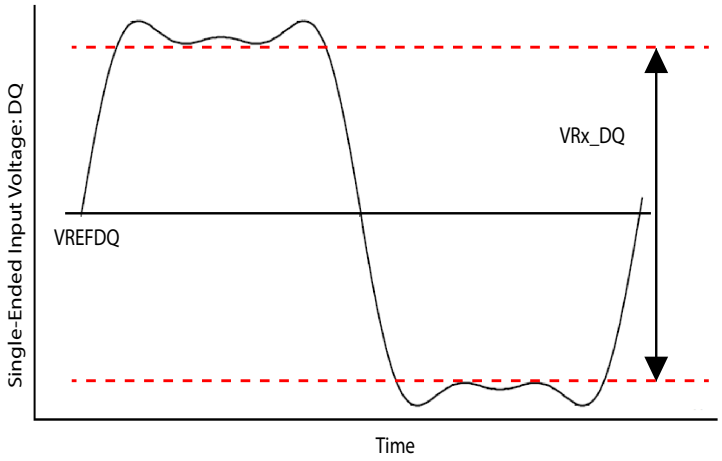


Figure 211 — VRx_DQ

8.9.3 Differential Input Levels for DQS

Table 204 — Differential Input Levels for DQS (DQS_t, DQS_c) for DDR5-4400 to DDR5-5600

From	Parameter	DDR5 4400-5600	Note
$V_{IHdiff}DQS$	Differential input high measurement level (DQS_t, DQS_c)	0.75 x $V_{diffpk-pk}$	1,2,3
$V_{ILdiff}DQS$	Differential input low measurement level (DQS_t, DQS_c)	0.25 x $V_{diffpk-pk}$	1,2,3

Note(s):
1. Vdiffpk-pk defined in **Figure 212**
2. Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
3. All parameters are defined over the entire clock common mode range

8.9.4 Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals are defined and measured as shown below.

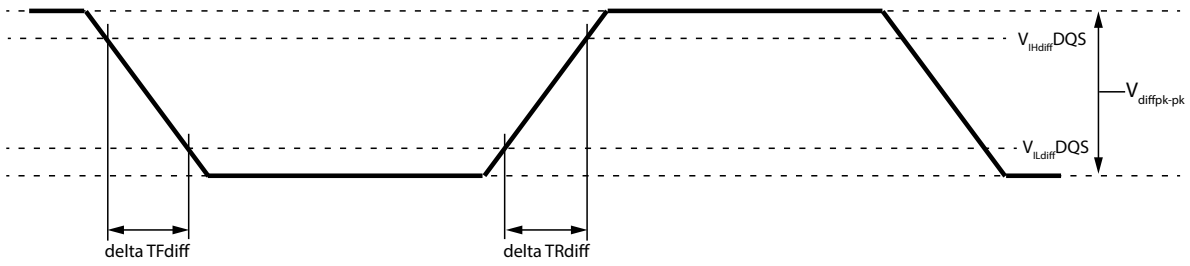


Figure 212 — Differential Input Slew Rate Definition for DQS_t, DQS_c

Table 205 — Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (DQS_t, DQS_c)	$V_{ILdiff}DQS$	$V_{IHdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) /deltaTRdiff	1,2,3
Differential Input slew rate for falling edge (DQS_t, DQS_c)	$V_{IHdiff}DQS$	$V_{ILdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) /deltaTFdiff	1,2,3

Note(s):

Table 206 — Differential Input Slew Rate for DQS_t, DQS_c for DDR5-4400 to 4800

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	TBD	TBD	TBD	TBD	V/ns	1

Note(s):
1. Only applies when both DQS_t and DQS_c are transitioning.

Table 207 — Differential Input Slew Rate for DQS_t, DQS_c for DDR5-5200 to 5600

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	TBD	TBD	TBD	TBD	V/ns	1

Note(s):
1. Only applies when both DQS_t and DQS_c are transitioning.

8.10 Rx Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

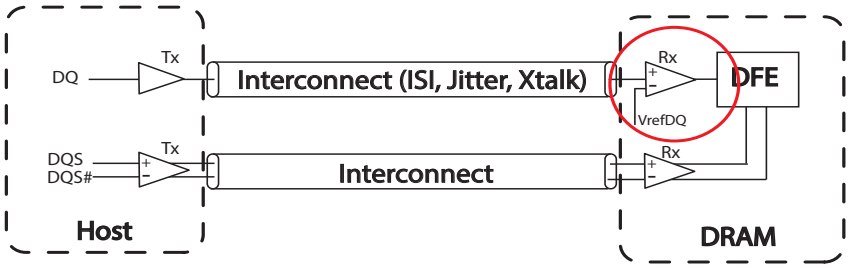


Figure 213 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

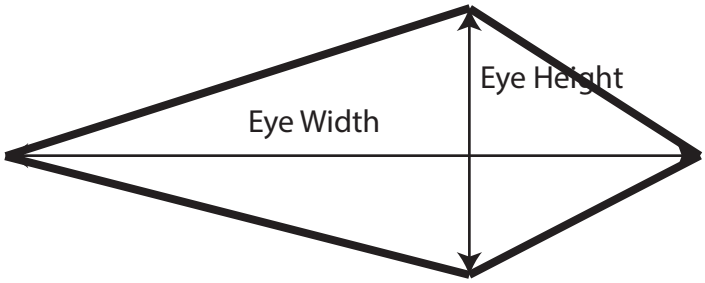


Figure 214 — Example of Rx Stressed Eye Height and Eye Width

8.10.1 Parameters for DDR5 Rx Stressed Eye Tests

Table 210 — Test Conditions for Rx Stressed Eye Tests for DDR5-4400 to 4800

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	75	-	70	mV	1,2,3,4,5,6,7,8,9,10
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.25	-	0.25	UI	1,2,3,4,5,6,7,8,9,10
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	mV	1.2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	UI p-p	1,2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	mV p-p	1,2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics					dB	3

Note(s):

1. Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E^{-16}.
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE Tap 1-4 Bias settings that give the best eye margin are used and referring to Table 132, Min/Max Ranges for the DFE Tap Coefficients. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV) after the tap multiflier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions
7. The stressed eye is to be assumed to have a diamond shape
8. The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.
10. The Rx stressed eye spec applies at DDR5-2933 and faster data rates.

Table 211 — Test Conditions for Rx Stressed Eye Tests for DDR5-5200 to 5600

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	65	-	60	mV	1,2,3, 4,5,6, 7,8,9,10
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	.0.235	-	0.235	UI	1,2,3, 4,5,6, 7,8,9,10
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	mV	1.2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	-	0.45	-	0.45	UI p-p	1,2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	mV p-p	1,2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics					dB	3

Note(s):

1. Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E^{-16}.
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV).
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions
7. The stressed eye is to be assumed to have a diamond shape
8. The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.
10. EH/WE are measured at the slicer of the receiver.

8.11 Connectivity Test Mode - Input level and Timing Requirement

During CT Mode, input levels are defined below.
TEN pin: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ
CS_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
Test Input pins: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
RESET_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR5 memory device will enter into the CT mode after time tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on, after RESET_n has de-asserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting clocks (CK_t, CK_c).

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR5 memory device are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

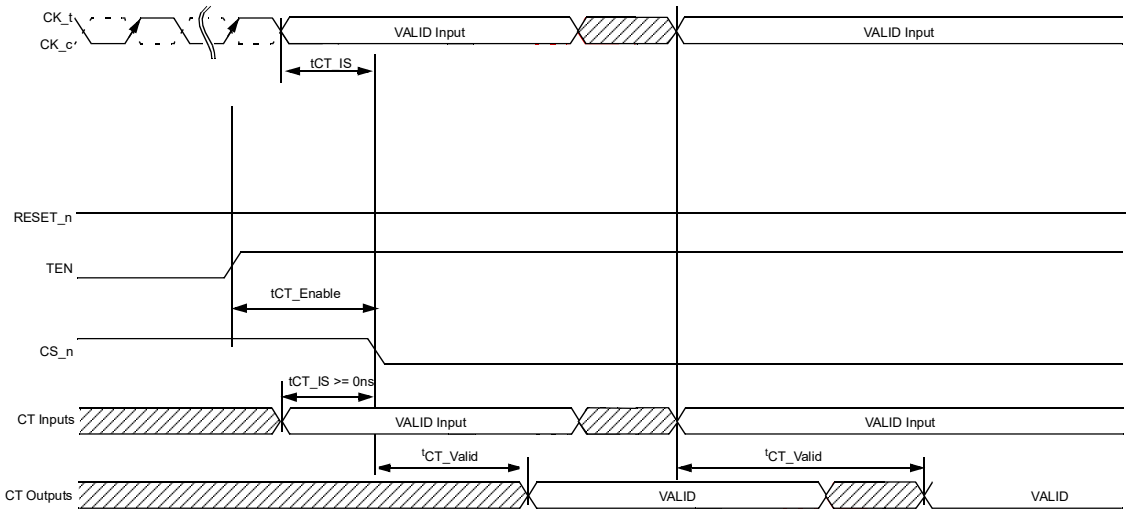


Figure 215 — Timing Diagram for Connectivity Test (CT) Mode

Table 213 — AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

8.11.1 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR5 SDRAM Input Signals during Connectivity Test Mode.

Table 214 — CMOS rail to rail Input Levels for TEN, CS_n and Test inputs

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDDQ	VDDQ	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDDQ	VDDQ	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDDQ	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDDQ	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

Note(s):
1. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
2. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

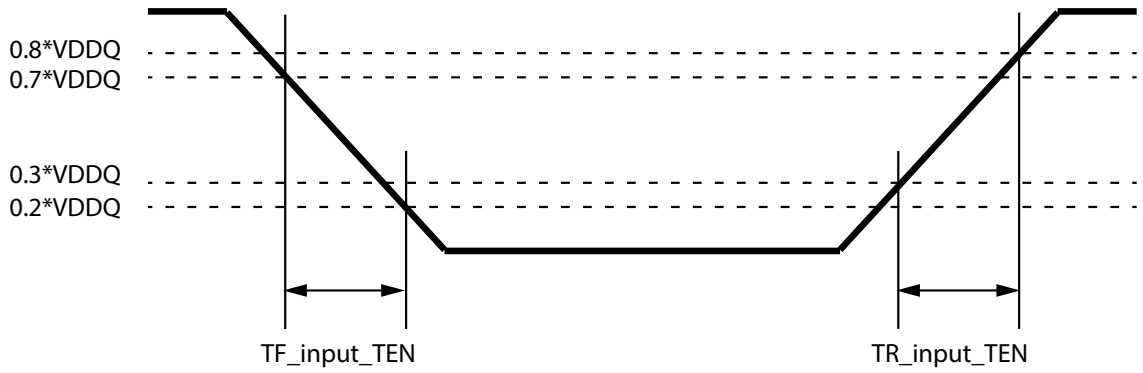


Figure 216 — TEN Input Slew Rate Definition

8.11.2 CMOS rail to rail Input Levels for RESET_n

Table 215 — CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDDQ	VDDQ	V	5
DC Input High Voltage	VIH(DC)_RESET	0.7*VDDQ	VDDQ	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDDQ	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDDQ	V	6
Rising time	TR_RESET	-	1.0	us	
RESET pulse width	tPW_RESET	1.0	-	us	3,4

Note(s):

1.After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. This definition is applied only for “Reset Procedure at Power Stable”.
5. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
6. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

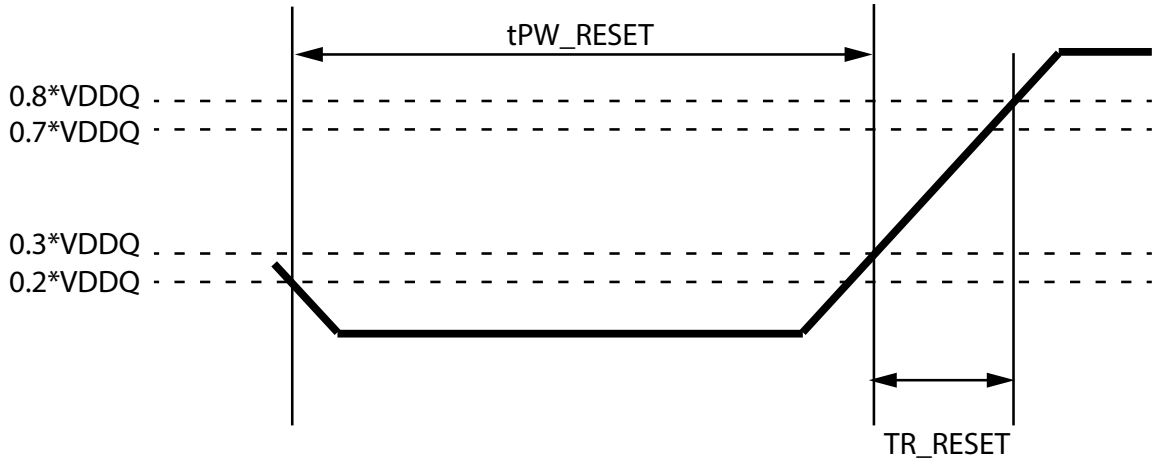


Figure 217 — RESET_n Input Slew Rate Definition

9 AC & DC Output Measurement Levels and Timing

9.1 Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below.

Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

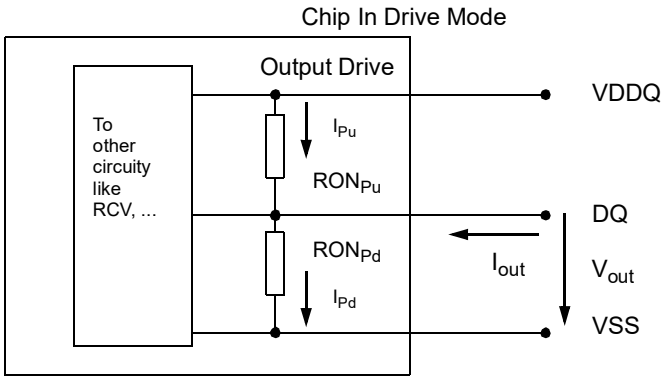


Table 216 — Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5. This parameter of x16 device is specified for Upper byte and Lower byte.

9.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

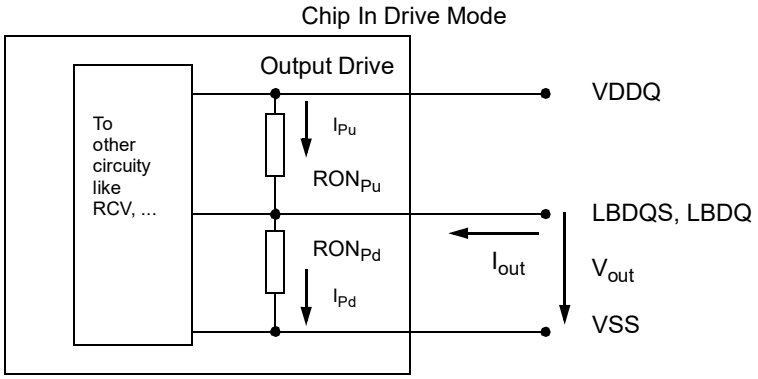


Figure 218 — Output Driver for Loopback Signals

Table 217 — Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch LBDQS-LBDQ within device variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch LBDQS-LBDQ within device variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including LBDQS and LBDQ.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

9.3 Loopback Output Timing

Loopback strobe LBDQS to Loopback data LBDQ relationship is illustrated in **Figure 219**.

- tLBQSH describes the single-ended LBDQS strobe high pulse width
- tLBQSL describes the single-ended LBDQS strobe low pulse width
- tLBDQSQ describes the latest valid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBQH describes the earliest invalid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBDVW describes the data valid window per device per UI and is derived from (tLBQH-tLBDQSQ) of each UI on a given DRAM

Table 218 — Loopback Output Timing Parameters for DDR5-4400 to 4800

Speed		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Loopback Timing							
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	0.2	-	0.2	-	tCK/2	1
Loopback LBDQ Output Time from LBDQS	tLBQH	3.6	-	3.6	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	3.4	-	3.4	-	tCK/2	1

Note(s):

1: Based on Loopback 4-way interleave setting (see MR53)

Table 219 — Loopback Output Timing Parameters for DDR5-5200 to 5600

Speed		DDR5-5200		DDR5-5600		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Loopback Timing							
Loopback LBDQS Output Low Time	tLBQSL	TBD	-	TBD	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	TBD	-	TBD	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	TBD	-	TBD	-	tCK/2	1
Loopback LBDQ Output Time from LBDQS	tLBQH	TBD	-	TBD	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	TBD	-	TBD	-	tCK/2	1

Note(s):

1: Based on Loopback 4-way interleave setting (see MR53)

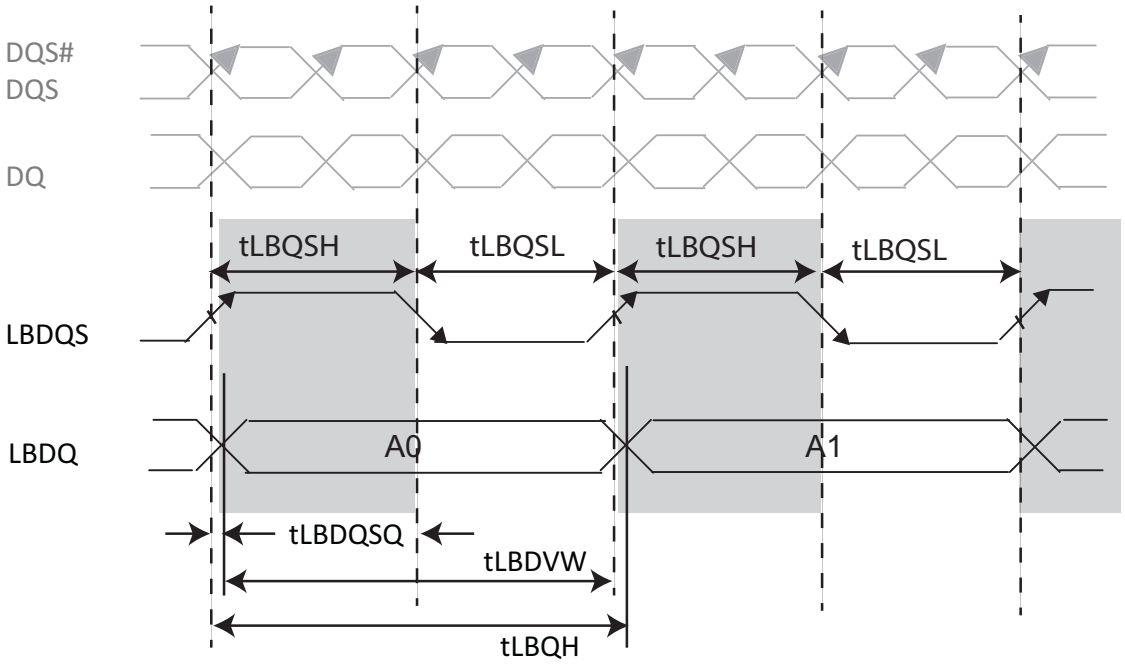
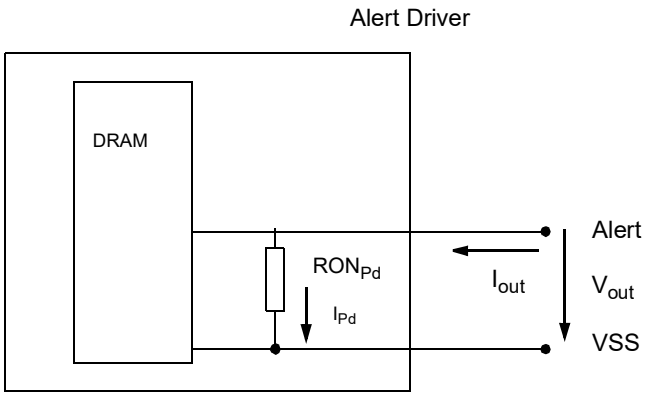


Figure 219 — Loopback Strobe to Data Relationship

9.3.1 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$



Resistor	Vout	Min	Max	Unit	NOTE
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.1	$R_{ZQ}/7$	
	V_{OMdc} = 0.8* VDDQ	0.4	1.1	$R_{ZQ}/7$	
	V_{OHdc} = 0.95* VDDQ	0.4	1.25	$R_{ZQ}/7$	

Note(s):

9.3.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied to the Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

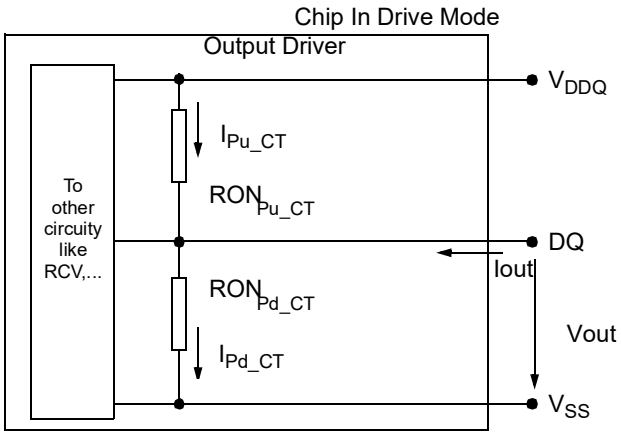


Figure 220 — Output Driver

RONNOM_CT	Resistor	Vout	Max	Units	NOTE
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2
	RONPu_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2

Note(s):
1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.
2. Uncalibrated drive strength tolerance is specified at +/- 30%

9.4 Single-ended Output Levels - VOL/VOH

Table 221 — Single-ended Output levels for DDR5-4400 to DDR5-5600

Symbol	Parameter	DDR5-4400-5600	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

Note(s):
1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

9.5 Single-Ended Output Levels - VOL/VOH for Loopback Signals

Table 222 — Single-ended Output levels for Loopback Signals DDR5-4400 to DDR5-5600

Symbol	Parameter	DDR5-4400-5600	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

Note(s):
1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

9.6 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single ended signals as shown in Table 223 and Figure 221.

Table 223 — Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}	V_{OH}	[V_{OH}-V_{OL}] / delta TRse
Single ended output slew rate for falling edge	V_{OH}	V_{OL}	[V_{OH}-V_{OL}] / delta TFse

Note(s):
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

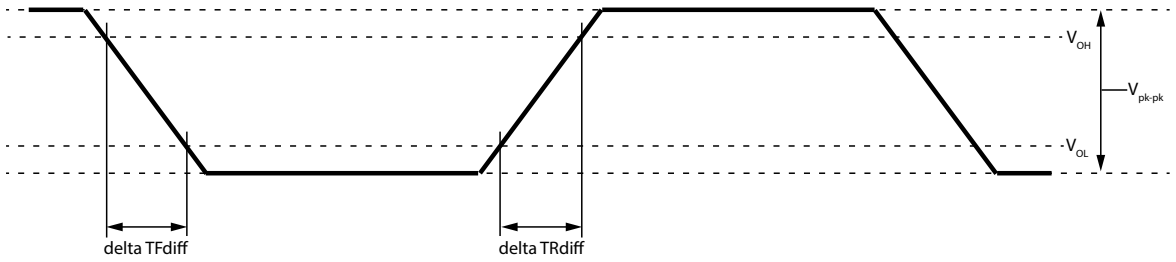


Figure 221 — Single-ended Output Slew Rate Definition

Table 224 — Single-ended Output Slew Rate for DDR5-4400 to DDR5-4800

Speed		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	8	24	8	24	V/ns	

Note(s):

Table 225 — Single-ended Output Slew Rate for DDR5-5200 to DDR5-5600

Speed		DDR5-5200		DDR5-5600		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	12	24	12	24	V/ns	

Note(s):

9.7 Differential Output Levels

Table 226 — Differential Output levels for DDR5-4400 to DDR5-5600

Symbol	Parameter	DDR5-4400-5600	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1

Note(s):
1. $V_{diffpk-pk}$is the mean high voltage minus the mean low voltage over TBD samples.

9.8 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL-diff}$ and V_{OHdiff} for differential signals as shown in Table 227 and Figure 222

Table 227 — Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}	V_{OHdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}	V_{OLdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TFdiff

Note(s):
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

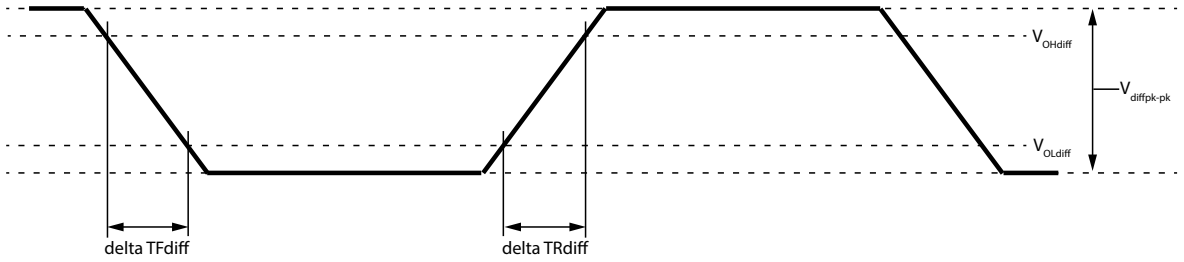


Figure 222 — Differential Output Slew Rate Definition

Table 228 — Differential Output Slew Rate for DDR5-4400 to DDR5-4800

Speed		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	16	48	16	48	V/ns	

Note(s):

Table 229 — Differential Output Slew Rate for DDR5-5200 to DDR5-5600

Speed		DDR5-5200		DDR5-5600		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	24	48	24	48	V/ns	

Note(s):

9.9 Tx DQS Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in **Table 235**.

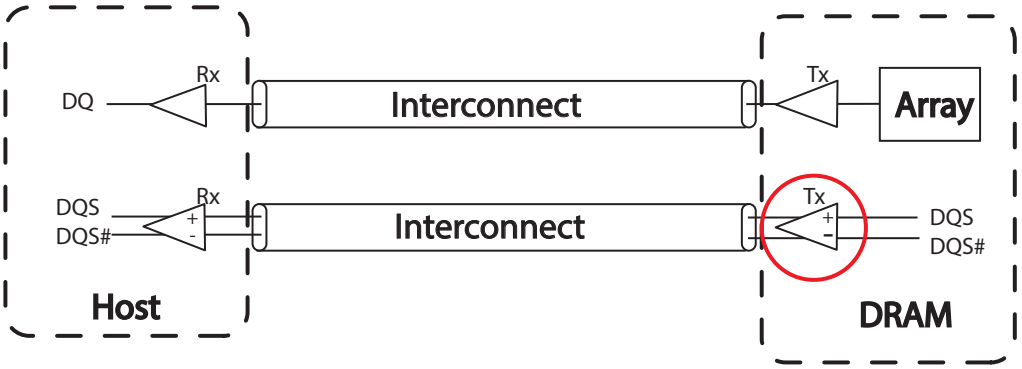


Table 235 — Tx DQS Jitter Parameters for DDR5-4400 to 4800

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,4, 5,6,7,8,9, 10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.150	-	0.150	UI	1,2,3,5,6,7,8,9,10,11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,5,6,7,8,9,10,11,12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.150	-	0.150	UI	1,2,3,5,6,7,8,9,10,11

Note(s)

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5. See Section 7.2 for details on the minimum BER requirements
6. See Section 7.3 for details on UI, NUI and Jitter definitions
7. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test
8. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44, and the Mode Registers for the Per Pin DCA of DQS are MR103 - MR110.
9. Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test
10. These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
11. Tested on the CTC2 card only
12. The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6mUI RMS

Table 236 — Tx DQS Jitter Parameters for DDR5-5200 to 5600

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,4,5,6,7,8,9,10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.130	-	0.130	UI	1,2,3,5,6,7,8,9,10,11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,5,6,7,8,9,10,11,12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.130	-	0.130	UI	1,2,3,5,6,7,8,9,10,11

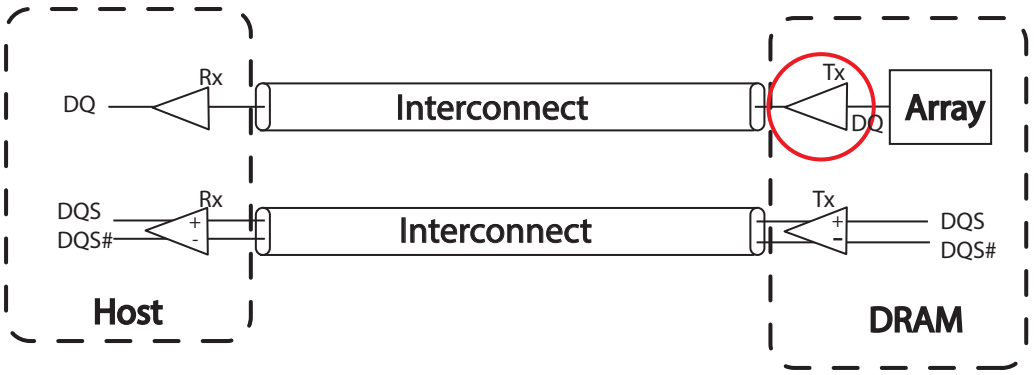
Note(s)

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5. See Section 7.2 for details on the minimum BER requirements
6. See Section 7.3 for details on UI, NUI and Jitter definitions
7. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test
8. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44, the Mode Register for the Per Pin DCA of DQS are MR103 - MR110.
9. Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test
10. These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
11. Tested on the CTC2 card only
12. The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6mUI RMS

9.10 Tx DQ Jitter

9.10.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in **Table 238**.



9.10.2 Tx DQ Jitter Parameters

Table 238 — **Tx DQ Jitter Parameters for DDR5-4400 to 4800**

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_No BUJ	-	tCK_ 1UI_Rj_ NoBUJ + 0.002	-	tCK_ 1UI_Rj_ NoBUJ + 0.002	UI (RMS)	1,3,4,5,7,8,9,10, 11, 12,13,14
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_No BUJ	-	0.150	-	0.150	UI	3,5,7, 8,9,10, 11,12,13
Rj RMS of N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_No BUJ	-	tCK_ NUI_Rj_ NoBUJ + 0.002	-	tCK_ NUI_Rj_ NoBUJ + 0.002	UI (RMS)	3,5,7, 8,9,10, 11,12,13,14
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Dj_No BUJ	-	0.150	-	0.150	UI	3,6,7, 8,9,10, 11,12,13
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	UI	3,5,6,7,9,10, 11,12,13

Note(s):

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5. Delay of any data lane relative to strobe lane, as measured at Tx output
6. Vref noise level to DQ jitter should be adjusted to minimize DCD
7. See **Chapter 7** for details on the minimum BER requirements
8. See **Chapter 7** for details on UI, NUI and Jitter definitions
9. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
10. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
11. Spread Spectrum Clocking (SSC) must be disabled while running this test
12. These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
13. Tested on the CTC2 card only
14. The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6mUI RMS

Table 239 — Tx DQ Jitter Parameters for DDR5-5200 to 5600

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_No BUJ	-	tCK_ 1UI_Rj_ NoBUJ + 0.002	-	tCK_ 1UI_Rj_ NoBUJ + 0.002	UI (RMS)	1,3,4,5,7,8,9,10,11, 12,13,14,
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_No BUJ	-	0.130	-	0.130	UI	3,5,7,8,9,10,11,12,1 3,
Rj RMS of N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_No BUJ	-	tCK_ NUI_Rj_ NoBUJ + 0.002	-	tCK_ NUI_Rj_ NoBUJ + 0.002	UI (RMS)	3,5,7,8,9,10,11,12,1 3,14,
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Dj_No BUJ	-	0.130	-	0.130	UI	3,6,7,8,9,10,11, 12,13
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	UI	3,5,6,7,9,10,11,12,1 3

Note(s):

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5. Delay of any data lane relative to strobe lane, as measured at Tx output
6. Vref noise level to DQ jitter should be adjusted to minimize DCD
7. See **Chapter 7** for details on the minimum BER requirements
8. See **Chapter 7** for details on UI, NUI and Jitter definitions
9. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
10. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
11. Spread Spectrum Clocking (SSC) must be disabled while running this test
12. These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
13. Tested on the CTC2 card only
14. The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6mUI RMS

9.11 Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E^{-9} and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40 OP[3:0]).

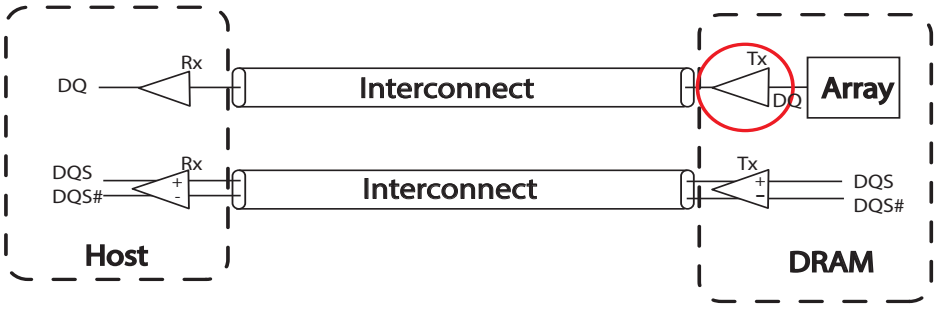


Figure 223 — Example of DDR5 Memory Interconnect

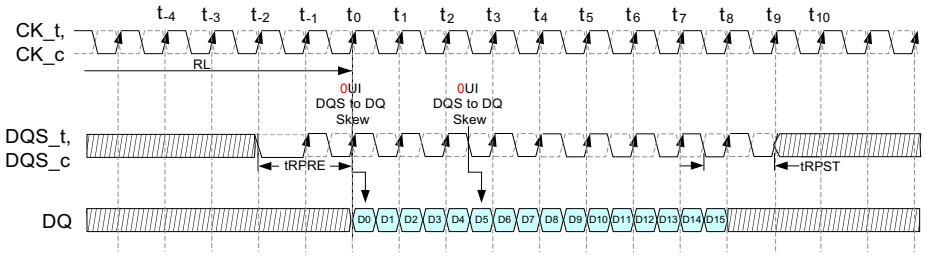


Figure 224 — Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 0 UI skew

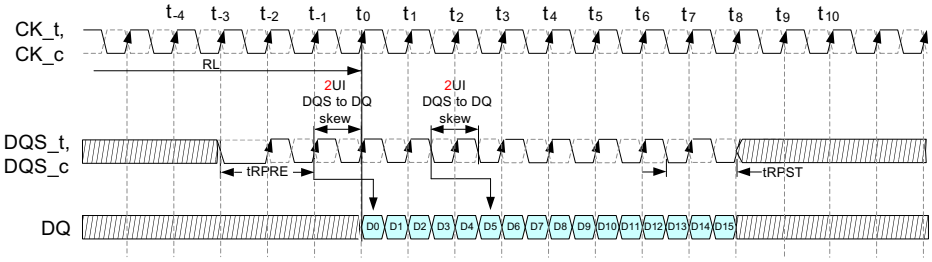


Figure 225 — Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 2 UI skew with Read DQS Offset Timing set to 1 Clock (2UI)

9.11.1 Tx DQ Stressed Eye Parameters

Table 241 — Tx DQ Stressed Eye Parameters for DDR5-4400 to 4800

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Eye Height specified at the transmitter with a skew between DQ and DQS of 1UI	TxEH_DQ_SES_1UI	TBD	-	TBD	-	mV	1,2,3,4,6, 7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.72	-	0.72	-	UI	1,2,3,4,6, 7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 2UI	TxEH_DQ_SES_2UI	TBD	-	TBD	-	mV	1,2,3,4,6, 7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.72	-	0.72	-	UI	1,2,3,4,6, 7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 3UI	TxEH_DQ_SES_3UI	TBD	-	TBD	-	mV	1,2,3,4,6, 7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.72	-	0.72	-	UI	1,2,3,4,6, 7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 4UI	TxEH_DQ_SES_4UI	TBD	-	TBD	-	mV	1,2,3,4,5, 6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	TBD	-	TBD	-	UI	1,2,3,4,5, 6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 5UI	TxEH_DQ_SES_5UI	TBD	-	TBD	-	mV	1,2,3,4,5, 6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	TxEW_DQ_SES_5UI	TBD	-	TBD	-	UI	1,2,3,4,5, 6,7,8,9,10

Note(s):

1. Minimum BER E^{-9} and Confidence Level of 99.5% per pin
2. Refer to the minimum Bit Error Rate (BER) requirements for DDR5
3. The validation methodology for these parameters will be covered in future ballot(s)
4. Mismatch is defined as DQS to DQ mismatch, in UI increments
5. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable
6. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
7. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
8. Spread Spectrum Clocking (SSC) must be disabled while running this test
9. These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.
10. Tested on the CTC2 card only
11. Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye.

Table 242 — Tx DQ Stressed Eye Parameters for DDR5-5200 to 5600

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate]

Parameter	Symbol	DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max		
Eye Height specified at the transmitter with a skew between DQ and DQS of 1UI	TxEH_DQ_SES_1UI	-	TBD	-	TBD	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	-	0.74	-	0.74	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 2UI	TxEH_DQ_SES_2UI	-	TBD	-	TBD	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	-	0.74	-	0.74	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 3UI	TxEH_DQ_SES_3UI	-	TBD	-	TBD	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	-	0.74	-	0.74	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 4UI	TxEH_DQ_SES_4UI	-	TBD	-	TBD	mV	1,2,3,4,5,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	-	0.74	-	0.74	UI	1,2,3,4,5,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 5UI	TxEH_DQ_SES_5UI	-	TBD	-	TBD	mV	1,2,3,4,5,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	TxEW_DQ_SES_5UI	-	TBD	-	TBD	UI	1,2,3,4,5,6,7,8,9,10

Note(s):

1. Minimum BER E^{-9} and Confidence Level of 99.5% per pin
2. Refer to the minimum Bit Error Rate (BER) requirements for DDR5
3. The validation methodology for these parameters will be covered in future ballot(s)
4. Mismatch is defined as DQS to DQ mismatch, in UI increments
5. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable
6. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
7. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$
8. Spread Spectrum Clocking (SSC) must be disabled while running this test
9. These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.
10. Tested on the CTC2 card only

10 Speed Bins

10.1 DDR5-4400 Speed Bins and Operations

Table 244 — DDR5-4400 Speed Bins and Operations

Speed Bin					DDR5-4400AN		DDR5-4400B		DDR5-4400BN		DDR5-4400C		Unit	NOTE
CL-nRCD-nRP					32-32-32		36-36-36		36-36-36		40-39-39			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	14.545	22.222	16.000	22.222	16.363	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Row Precharge Time				tRP	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.545	-	48.000	-	48.363	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED								ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
Supported CL					22,24,26,28,30,32,36,40		22,26,28,30,32,36,40		22,28,30,32,36,40		22,28,32,36,40		nCK	

10.5 DDR5-4800 Speed Bins and Operations

Table 248 — DDR5-4800 Speed Bins and Operations

Speed Bin					DDR5-4800AN		DDR5-4800B		DDR5-4800BN		DDR5-4800C		Unit	NOTE
CL-nRCD-nRP					34-34-34		40-39-39		40-40-40		42-42-42			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	14.166	22.222	16.000	22.222	16.666	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Row Precharge Time				tRP	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.166	-	48.000	-	48.666	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
Supported CL					22,24,26,28,30,32,34,36,40,42		22,26,28,30,32,36,40,42		22,28,30,32,36,40,42		22,28,32,36,40,42		nCK	

10.6 DDR5-5200 Speed Bins and Operations

Table 249 — DDR5-5200 Speed Bins and Operations

Speed Bin					DDR5-5200AN		DDR5-5200B		DDR5-5200BN		DDR5-5200C		Unit	NOTE
CL-nRCD-nRP					38-38-38		42-42-42		42-42-42		46-46-46			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	14.615	22.222	16.000	22.222	16.153	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.615	-	16.000	-	16.153	-	17.500	-	ns	7
Row Precharge Time				tRP	14.615	-	16.000	-	16.153	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.615	-	48.000	-	48.153	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED								ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED								ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED								ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
Supported CL					22,24,26,28,30,32,36,38,40,42,46		22,26,28,30,32,36,40,42,46		22,26,28,30,32,36,40,42,46		22,28,32,36,40,42,46		nCK	

10.7 DDR5-5600 Speed Bins and Operations

Table 250 — 5600 Speed Bins and Operations

Speed Bin					DDR5-5600AN		DDR5-5600B		DDR5-5600BN		DDR5-5600C		Unit	NOTE
CL-nRCD-nRP					40-40-40		46-45-45		46-46-46		50-49-49			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	14.285	22.222	16.000	22.222	16.428	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.285	-	16.000	-	16.428	-	17.500	-	ns	7
Row Precharge Time				tRP	14.285	-	16.000	-	16.428	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.285	-	48.000	-	48.428	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED								ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
Supported CL					22,24,26,28,30,32,36,38,40,42,46,50		22,26,28,30,32,36,40,42,46,50		22,28,30,32,36,40,42,46,50		22,28,32,36,40,42,46,50		nCK	

DDR5 Speed Bin Table Note(s)

1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2. The translation of all timing parameters from ns values to nCK values shall follow the Rounding Algorithm. The translation of tAA to CL shall follow the explicit combinations listed in the Speed Bin Tables.
3. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When selecting tCK(avg), requirements from the CL setting as well as requirements from the CWL setting shall be fulfilled.
4. 'Reserved' settings are not allowed. The user shall program a different value.
5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm, depending on the specific speed bin and down clock frequency combination.
6. DDR5-3200 AC timings apply if the DRAM operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7. Parameters apply from tCK(avg)min to tCK(avg)max.
8. tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithms, nRC(min) shall always be greater than or equal to nRAS(min) + nRP(min).
9. tCK(avg).max of 1.010 ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
10. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC standard. The JEDEC standard does not require support for all speed bins within a given speed. The JEDEC standard requires meeting the parameters for a least one of the listed speed bins.
11. Any speed bin also supports functional operation at slower frequencies as shown in the table which are not subject to Production Tests but are verified by Design/Characterization.
12. The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the Speed Bin Tables. The CL Algorithm calculates supported CAS Latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting tCK(AVG)min, and the bin target timings, the CL Algorithm then uses the Rounding Algorithm to calculate the valid CAS Latency. Because the DDR5 SDRAM specification only supports even CAS Latencies, odd CAS Latencies are rounded up to the next even CAS Latency. The 1980-2100 MT/s data rate always uses CL22. If tAA(corrected) or tRCDtRP(corrected) are violated, the CL Algorithm uses a slower combination of tAA(target) and tRCDtRP(target) to return slower valid CAS Latencies. The DDR5 SDRAM can support up to four valid CAS Latencies, CL(AN), CL(B), CL(BN), and CL(C), for a given frequency. tAA(corrected) and tRCDtRP(corrected) are calculated by reducing tAA(min), tRCD(min), and tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin Tables, or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information.

```
// Variables already defined in other areas of the DDR5 SDRAM specification
CorrFact       = 0.30                                          // (%)   Rounding Algorithm correction factor
ScaledCorrFact = 997                                           //       Scaled correction factor (1000*(1-0.30%))
tCKreal        =1011-952, 682-238                              // (ps)  Real application tCK(AVG) (1980-2100MT/s, 2933-8400MT/s)
tAAmin         MONO=14000-17500, 3DS=16000-20000               // (ps)  From Speed Bin Tables and DIMM SPD bytes 30-31
tRCDtRPmin     MONO=14000-17500, 3DS=14000-17500               // (ps)  From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
tAAcorr        = TRUNC(tAAmin*ScaledCorrFactor/1000)           // (ps)  Corrected tAA(min) per the Rounding Algorithm rules
tRCDtRPcorr    = TRUNC(tRCDtRPmin*ScaledCorrFactor/1000)       // (ps)  Corrected tRCD(min), tRP(min) per the Rounding Algorithm
FUNC[RA(targ)] = TRUNC((targ*ScaledCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK
// Round tCKreal down to the next faster standard frequency (tCK in ps)
IF (TRUNC(2000000/(2000*99%))>=TRUNC(tCKreal)>=TRUNC(2000000/(2000*105%)))             // Check for  1980-2100 nominal data rates
   tCKstd=TRUNC(2000000/2000)                                                          // Assign standard 2000 tCK (ps)
ELSE IF (TRUNC(2000000/(2000+7*(133+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200))       // Check for  2933-3200 nominal data rates
   tCKstd=TRUNC(2000000/3200)                                                          // Assign standard 3200 tCK (ps)
ELSE
   FOR (DataRateNom=3200; DataRateNom<=8000; DataRateNom=DataRateNom+400)              // Check for >3200-8400 nominal data rates
      IF (TRUNC(2000000/DataRateNom)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
         tCKstd=TRUNC(2000000/(DataRateNom+400))                                       // Assign standard 3600-8400 tCK (ps)
      ELSE
         tCKstd=RESERVED                                                               // No valid data rate found

// Timing targets (ps) that have been used to define the Speed Bin Tables
// MONO targets              3DS targets
   BinAN_tAAtarg     = 14000 BinAN_tAAtarg     = 16000         // tAA target for AN bins
   BinB__tAAtarg     = 16000 BinB__tAAtarg     = 18500         // tAA target for AN, B bins
   BinBN_tAAtarg     = 16000 BinBN_tAAtarg     = 18500         // tAA target for AN, B, BN bins
   BinC__tAAtarg     = 17500 BinC__tAAtarg     = 20000         // tAA target for AN, B, BN, C bins
   BinAN_tRCDtRPtarg = 14000 BinAN_tRCDtRPtarg = 14000         // tRCD, tRP target for AN bins
   BinBN_tRCDtRPtarg = 16000 BinBN_tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B, BN bins
   BinC__tRCDtRPtarg = 17500 BinC__tRCDtRPtarg = 17500         // tRCD, tRP target for AN, B, BN, C bins
IF (TRUNC(2000000/3600)>tCKstd)                                // tRCD, tRP target for B bins is frequency dependent
   BinB__tRCDtRPtarg = 16000 BinB__tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B bins data rates faster than 3600
ELSE
   // 16250=(2000000/3200)*EVEN(TRUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
   BinB__tRCDtRPtarg = 16250 BinB__tRCDtRPtarg = 16250         // tRCD, tRP target for AN, B bins for data rates 3600 and slower

// CL Algorithm using variables defined above
// Up to four valid CL's can be returned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
// The B and BN bins return the same CL
// Only even CL's (not odd CL's) are valid per the DDR5 SDRAM specification
// nRCD, nRP are only even at standard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
```

```
// nRCD, nRP may be even or odd at standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
IF (TRUNC(2000000/2000)=tCKstd)                                  // CL22 is the only valid CL for 1980-2100 data rates
   CL(AN)=22                                                     // Valid even CL for AN bins
   CL(B )=22                                                     // Valid even CL for AN, B, bins
   CL(BN)=22                                                     // Valid even CL for AN, B, BN bins
   CL(C )=22                                                     // Valid even CL for AN, B, BN, C bins
ELSE IF (TRUNC(2000000/3200)>=tCKstd>=TRUNC(2000000/8400))      // Valid CL for 2933-8400 data rates
   IF      ((EVEN(RA(BinAN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinAN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=EVEN(RA(BinAN_tAAtarg))                             // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                             // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                             // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                             // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinB__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinB__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                            // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                             // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                             // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                             // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinBN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinBN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=RESERVED                                            // Valid even CL for AN bins
      CL(B )=RESERVED                                            // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                             // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                             // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinC__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinC__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                            // Valid even CL for AN bins
      CL(B )=RESERVED                                            // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                            // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                             // Valid even CL for AN, B, BN, C bins
   ELSE                                                          // No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
      CL(AN)=RESERVED                                            // Valid even CL for AN bins
      CL(B )=RESERVED                                            // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                            // Valid even CL for AN, B, BN bins
      CL(C )=RESERVED                                            // Valid even CL for AN, B, BN, C bins
ELSE                                                             // No valid data rate found
   CL(AN)=RESERVED                                               // Valid even CL for AN bins
   CL(B )=RESERVED                                               // Valid even CL for AN, B bins
   CL(BN)=RESERVED                                               // Valid even CL for AN, B, BN bins
   CL(C )=RESERVED                                               // Valid even CL for AN, B, BN, C bins
```

10.18 3DS DDR5-4400 Speed Bins and Operations

Table 261 — 3DS DDR5-4400 Speed Bins and Operations

Speed Bin					DDR5-4400AN 3DS		DDR5-4400B 3DS		DDR5-4400BN 3DS		DDR5-4400C 3DS		Unit	NOTE
CL-nRCD-nRP					36-32-32		42-36-36		42-36-36		44-39-39			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	16.363	22.222	18.750	22.222	19.090	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Row Precharge Time				tRP	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.545	-	48.000	-	48.363	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	RESERVED				ns	
3600AN	16.666	14.444	30	tCK(AVG)	RESERVED								ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
Supported CL					22,30,32,34,36,38,40,42,44		22,30,32,34,36,38,40,42,44		22,32,36,40,42,44		22,32,36,40,44		nCK	

10.19 3DS DDR5-4800 Speed Bins and Operations

Table 262 — 3DS DDR5-4800 Speed Bins and Operations

Speed Bin					DDR5-4800AN 3DS		DDR5-4800B 3DS		DDR5-4800BN 3DS		DDR5-4800C 3DS		Unit	NOTE
CL-nRCD-nRP					40-34-34		46-39-39		46-40-40		48-42-42			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	16.666	22.222	18.750	22.222	19.166	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Row Precharge Time				tRP	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.166	-	48.000	-	48.666	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	RESERVED				ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED								ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	0.416	<0.454	RESERVED						ns	
Supported CL					22,30,32,34,36,38,40,42,44,46,48		22,30,32,34,36,38,40,42,44,46,48		22,32,36,40,44,46,48		22,32,36,40,44,48		nCK	

10.20 3DS DDR5-5200 Speed Bins and Operations

Table 263 — 3DS DDR5-5200 Speed Bins and Operations

Speed Bin					DDR5-5200AN 3DS		DDR5-5200B 3DS		DDR5-5200BN 3DS		DDR5-5200C 3DS		Unit	NOTE
CL-nRCD-nRP					42-38-38		50-42-42		50-42-42		52-46-46			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	16.153	22.222	18.750	22.222	19.230	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.615	-	16.000	-	16.153	-	17.500	-	ns	7
Row Precharge Time				tRP	14.615	-	16.000	-	16.153	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.615	-	48.000	-	48.153	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	RESERVED				ns	
3600AN	16.666	14.444	30	tCK(AVG)	RESERVED								ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED								ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED								ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	16.153	14.615	42	tCK(AVG)	0.384	<0.416	RESERVED						ns	
Supported CL					22,26,30,32,34,36,38,40,42,44,46,48,50,52		22,30,32,34,36,38,40,42,44,46,48,50,52		22,32,36,40,44,48,50,52		22,32,36,40,44,48,52		nCK	

10.21 3DS DDR5-5600 Speed Bins and Operations

Table 264 — 3DS DDR5-5600 Speed Bins and Operations

Speed Bin					DDR5-5600AN 3DS		DDR5-5600B 3DS		DDR5-5600BN 3DS		DDR5-5600C 3DS		Unit	NOTE
CL-nRCD-nRP					46-40-40		52-45-45		52-46-46		56-49-49			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	16.428	22.222	18.571	22.222	18.571	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.285	-	16.000	-	16.428	-	17.500	-	ns	7
Row Precharge Time				tRP	14.285	-	16.000	-	16.4228	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.285	-	48.000	-	48.428	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED								ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED								ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	16.153	14.615	42	tCK(AVG)	RESERVED								ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	0.357	<0.384	RESERVED						ns	
Supported CL					22,30,32,34,36,38,40,42,44,46,48,50,52,56		22,30,32,34,36,38,40,42,44,46,48,50,52,56		22,32,34,36,40,44,46,48,52,56		22,32,36,40,44,48,52,56		nCK	

DDR5 Speed Bin Table Note(s)

1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2. The translation of all timing parameters from ns values to nCK values shall follow the Rounding Algorithm. The translation of tAA to CL shall follow the explicit combinations listed in the Speed Bin Tables.
3. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When selecting tCK(avg), requirements from the CL setting as well as requirements from the CWL setting shall be fulfilled.
4. 'Reserved' settings are not allowed. The user shall program a different value.
5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm, depending on the specific speed bin and down clock frequency combination.
6. DDR5-3200 AC timings apply if the DRAM operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7. Parameters apply from tCK(avg)min to tCK(avg)max.
8. tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithms, nRC(min) shall always be greater than or equal to nRAS(min) + nRP(min).
9. tCK(avg).max of 1.010 ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000MT/s according to JESD404-1.
10. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC standard. The JEDEC standard does not require support for all speed bins within a given speed. The JEDEC standard requires meeting the parameters for a least one of the listed speed bins.
11. Any speed bin also supports functional operation at slower frequencies as shown in the table which are not subject to Production Tests but are verified by Design/Characterization.
12. The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the Speed Bin Tables. The CL Algorithm calculates supported CAS Latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting tCK(AVG)min, and the bin target timings, the CL Algorithm then uses the Rounding Algorithm to calculate the valid CAS Latency. Because the DDR5 SDRAM specification only supports even CAS Latencies, odd CAS Latencies are rounded up to the next even CAS Latency. The 1980-2100 MT/s data rate always uses CL22. If tAA(corrected) or tRCDtRP(corrected) are violated, the CL Algorithm uses a slower combination of tAA(target) and tRCDtRP(target) to return slower valid CAS Latencies. The DDR5 SDRAM can support up to four valid CAS Latencies, CL(AN), CL(B), CL(BN), and CL(C), for a given frequency. tAA(corrected) and tRCDtRP(corrected) are calculated by reducing tAA(min), tRCD(min), and tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin Tables, or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information.

```
// Variables already defined in other areas of the DDR5 SDRAM specification
CorrFact       = 0.30                                          // (%)   Rounding Algorithm correction factor
ScaledCorrFact = 997                                           //       Scaled correction factor (1000*(1-0.30%))
tCKreal        =1011-952, 682-238                              // (ps)  Real application tCK(AVG) (1980-2100MT/s, 2933-8400MT/s)
tAAmin         MONO=14000-17500, 3DS=16000-20000               // (ps)  From Speed Bin Tables and DIMM SPD bytes 30-31
tRCDtRPmin     MONO=14000-17500, 3DS=14000-17500               // (ps)  From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
tAAcorr        = TRUNC(tAAmin*ScaledCorrFactor/1000)           // (ps)  Corrected tAA(min) per the Rounding Algorithm rules
tRCDtRPcorr    = TRUNC(tRCDtRPmin*ScaledCorrFactor/1000)       // (ps)  Corrected tRCD(min), tRP(min) per the Rounding Algorithm
FUNC[RA(targ)] = TRUNC((targ*ScaledCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK
// Round tCKreal down to the next faster standard frequency (tCK in ps)
IF (TRUNC(2000000/(2000*99%))>=TRUNC(tCKreal)>=TRUNC(2000000/(2000*105%)))             // Check for  1980-2100 nominal data rates
   tCKstd=TRUNC(2000000/2000)                                                          // Assign standard 2000 tCK (ps)
ELSE IF (TRUNC(2000000/(2000+7*(133+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200))       // Check for  2933-3200 nominal data rates
   tCKstd=TRUNC(2000000/3200)                                                          // Assign standard 3200 tCK (ps)
ELSE
   FOR (DataRateNom=3200; DataRateNom<=8000; DataRateNom=DataRateNom+400)              // Check for >3200-8400 nominal data rates
      IF (TRUNC(2000000/DataRateNom)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
         tCKstd=TRUNC(2000000/(DataRateNom+400))                                       // Assign standard 3600-8400 tCK (ps)
      ELSE
         tCKstd=RESERVED                                                               // No valid data rate found

// Timing targets (ps) that have been used to define the Speed Bin Tables
// MONO targets              3DS targets
   BinAN_tAAtarg     = 14000 BinAN_tAAtarg     = 16000         // tAA target for AN bins
   BinB__tAAtarg     = 16000 BinB__tAAtarg     = 18500         // tAA target for AN, B bins
   BinBN_tAAtarg     = 16000 BinBN_tAAtarg     = 18500         // tAA target for AN, B, BN bins
   BinC__tAAtarg     = 17500 BinC__tAAtarg     = 20000         // tAA target for AN, B, BN, C bins
   BinAN_tRCDtRPtarg = 14000 BinAN_tRCDtRPtarg = 14000         // tRCD, tRP target for AN bins
   BinBN_tRCDtRPtarg = 16000 BinBN_tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B, BN bins
   BinC__tRCDtRPtarg = 17500 BinC__tRCDtRPtarg = 17500         // tRCD, tRP target for AN, B, BN, C bins
IF (TRUNC(2000000/3600)>tCKstd)                                // tRCD, tRP target for B bins is frequency dependent
   BinB__tRCDtRPtarg = 16000 BinB__tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B bins data rates faster than 3600
ELSE
   // 16250=(2000000/3200)*EVEN(TRUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
   BinB__tRCDtRPtarg = 16250 BinB__tRCDtRPtarg = 16250         // tRCD, tRP target for AN, B bins for data rates 3600 and slower

// CL Algorithm using variables defined above
// Up to four valid CL's can be returned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
// The B and BN bins return the same CL
// Only even CL's (not odd CL's) are valid per the DDR5 SDRAM specification
// nRCD, nRP are only even at standard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
```

```
// nRCD, nRP may be even or odd at standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
IF (TRUNC(2000000/2000)=tCKstd)                                  // CL22 is the only valid CL for 1980-2100 data rates
   CL(AN)=22                                                     // Valid even CL for AN bins
   CL(B )=22                                                     // Valid even CL for AN, B, bins
   CL(BN)=22                                                     // Valid even CL for AN, B, BN bins
   CL(C )=22                                                     // Valid even CL for AN, B, BN, C bins
ELSE IF (TRUNC(2000000/3200)>=tCKstd>=TRUNC(2000000/8400))      // Valid CL for 2933-8400 data rates
   IF      ((EVEN(RA(BinAN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinAN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=EVEN(RA(BinAN_tAAtarg))                             // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                             // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                             // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                             // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinB__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinB__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                            // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                             // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                             // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                             // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinBN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinBN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=RESERVED                                            // Valid even CL for AN bins
      CL(B )=RESERVED                                            // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                             // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                             // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinC__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinC__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                            // Valid even CL for AN bins
      CL(B )=RESERVED                                            // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                            // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                             // Valid even CL for AN, B, BN, C bins
   ELSE                                                          // No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
      CL(AN)=RESERVED                                            // Valid even CL for AN bins
      CL(B )=RESERVED                                            // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                            // Valid even CL for AN, B, BN bins
      CL(C )=RESERVED                                            // Valid even CL for AN, B, BN, C bins
ELSE                                                             // No valid data rate found
   CL(AN)=RESERVED                                               // Valid even CL for AN bins
   CL(B )=RESERVED                                               // Valid even CL for AN, B bins
   CL(BN)=RESERVED                                               // Valid even CL for AN, B, BN bins
   CL(C )=RESERVED                                               // Valid even CL for AN, B, BN, C bins
```

11 IDD, IDDQ, IPP Specification Parameters and Test conditions

11.1 IDD, IPP and IDDQ Measurement Conditions

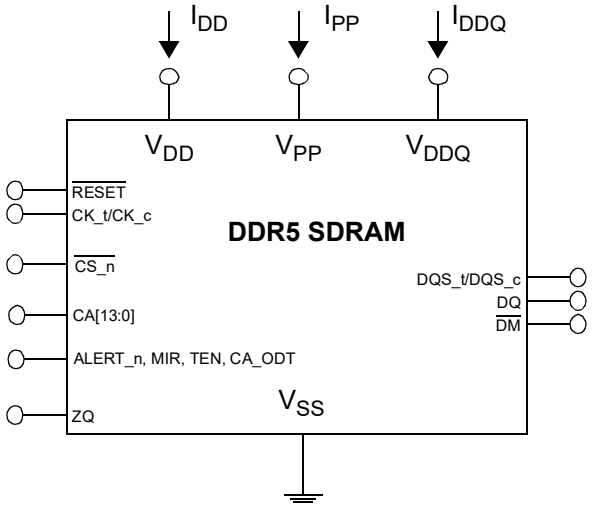
In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 226 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, IDD8, IDDQ8, IPP8 and IDD9, IDDQ9, IPP9) are measured as time-averaged currents with all VDD balls of the DDR5 SDRAM under test tied together. Any IDDQ or IPP current is not included in IDD currents.
- IDDQ currents are measured as time-averaged currents with all VDDQ balls of the DDR5 SDRAM under test tied together. Any IDD or IPP current is not included in IDDQ currents.
- IPP currents are measured as time-averaged currents with all VPP balls of the DDR5 SDRAM under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 227.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = 0.75 * VDDQ.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 272.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Chapter 11.2 through Chapter 11.11.
- IDD Measurements are done after properly initializing and training the DDR5 SDRAM. This includes but is not limited to setting
  TDQS_t disabled in MR5;
  CRC disabled in MR50;
  DM disabled in MR5;
  1N mode enabled and set CS assertion duration (MR2:OP[4]) as 1_B in MR2, unless otherwise specified in the IDD, IDDQ and IPP patterns’ conditions definitions;
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD, IDDQ or IPP measurement is started, with the exception of IDD9 which can be measured any time after the DRAM has entered MBIST mode.
- T_{CASE} defined as 0 - 95°C, unless stated in the specific condition definition table below.
- For all IDD, IDDQ and IPP measurement loop timing parameters, refer to the timing parameters defined in the spec to calculate the nCK required.



Note(s):
1. DIMM level Output test load condition may be different from above

Figure 226 — Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

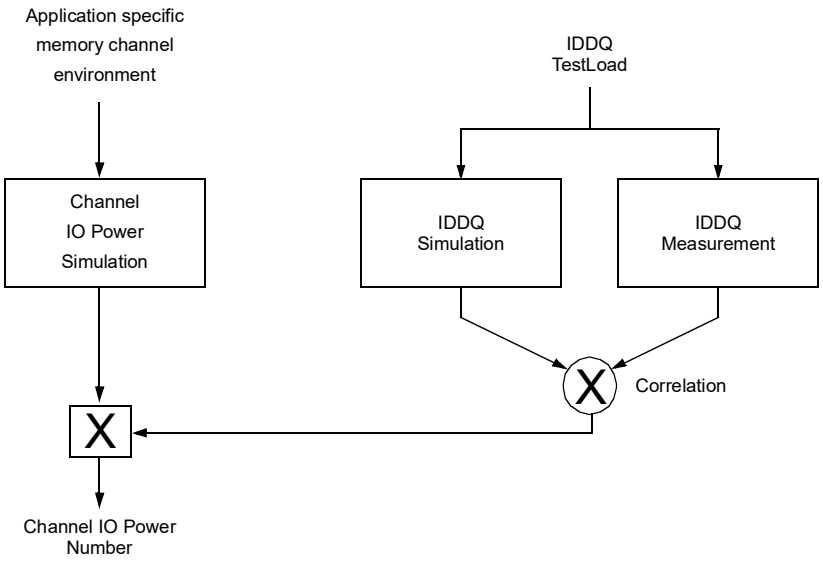


Figure 227 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

Table 272 — Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 273; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 273); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 273
IDDQ0	**Operating One Bank Active-Precharge IDDQ Current** **Same condition with IDD0,** however measuring IDDQ current instead of IDD current
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0,** however measuring IPP current instead of IDD current
IDD0F	**Operating Four Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 274; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with four bank active at a time: (see Table 274); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 274
IDDQ0F	**Operating Four Bank Active-Precharge IDDQ Current** **Same condition with IDD0F,** however measuring IDDQ current instead of IDD current
IPP0F	**Operating Four Bank Active-Precharge IPP Current** **Same condition with IDD0F,** however measuring IPP current instead of IDD current
IDD2N	**Precharge Standby Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 275; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 275
IDDQ2N	**Precharge Standby IDDQ Current** **Same condition with IDD2N,** however measuring IDDQ current instead of IDD current
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N,** however measuring IPP current instead of IDD current
IDD2NT	**Precharge Standby Non-Target Command Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between WRITE commands; **CS_n, CA Inputs:** partially toggling according to Table 276; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 276
IDDQ2NT (Optional)	**Precharge Standby Non-Target Command IDDQ Current** Same condition with IDD2NT, however measuring IDDQ current instead of IDD current

Table 272 — Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IPP2NT (Optional)	**Precharge Standby Non-Target Command IPP Current** Same condition with IDD2NT, however measuring IPP current instead of IDD current
IDD2P	**Precharge Power-Down** **Device in Precharge Power-Down, External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IDDQ current instead of IDD current
IPP2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IPP current instead of IDD current
IDD3N	**Active Standby Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 275; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 275
IDDQ3N	**Active Standby IDDQ Current** **Same condition with IDD3N,** however measuring IDDQ current instead of IDD current
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N,** however measuring IPP current instead of IDD current
IDD3P	**Active Power-Down Current** **Device in Active Power-Down, External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ3P	**Active Power-Down IDDQ Current** **Same condition with IDD3P,** however measuring IDDQ current instead of IDD current
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P,** however measuring IPP current instead of IDD current
IDD4R	**Operating Burst Read Current** **External clock:** On; **tCK, nCCD, CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between RD; **CA Inputs:** partially toggling according to Table 277; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 277; **DM_n:** stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 277); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 277
IDD4RC	**Operating Burst Read Current with Read CRC** **Read CRC enabled[4]. Other conditions:** see IDD4R
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R,** however measuring IPP current instead of IDD current
IDD4W	**Operating Burst Write Current** **External clock:** On; **tCK, nCCD, CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between WR; **CA Inputs:** partially toggling according to Table 278; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 278; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 278); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 278
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDDQ4W	**Operating Burst Write IDDQ Current** **Same condition with IDD4W,** however measuring IDDQ current instead of IDD current
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W,** however measuring IPP current instead of IDD current
IDD5B	**Burst Refresh Current (Normal Refresh Mode)** **External clock:** On; **tCK, nRFC**1: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 279; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC1 (see Table 279); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 279
IDDQ5B	**Burst Refresh IDDQ Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IDDQ current instead of IDD current
IPP5B	**Burst Refresh IPP Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IPP current instead of IDD current

Table 272 — Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IDD5F	**Burst Refresh Current (Fine Granularity Refresh Mode)** **tRFC=tRFC2, Other conditions:** see IDD5B
IDDQ5F	**Burst Refresh IDDQPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IDDQ current instead of IDD current
IPP5F	**Burst Refresh IPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IPP current instead of IDD current
IDD5C	**Burst Refresh Current (Same Bank Refresh Mode)** **External clock:** On; **tCK, nRFCsb**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 280; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFCsb (see Table 280); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 280
IDDQ5C	**Burst Refresh IDDQPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IDDQ current instead of IDD current
IPP5C	**Burst Refresh IPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IPP current instead of IDD current
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85°C; **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n#:** low; **CA, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** All ODT disabled in MR32-MR35;
IDDQ6N	**Self Refresh IDDQ Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IDDQ current instead of IDD current
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IPP current instead of IDD current
IDD6E	**SelfRefresh Current: Extended Temperature Range**) ***T*CASE:** 85 - 95°C; Extended[4]; **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** low; **CA, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]
IDDQ6E	**Self Refresh IDDQ Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IDDQ current instead of IDD current
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IPP current instead of IDD current
IDD7	**Operating Bank Interleave Read Current** **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD_S, nFAW, tCCD_S CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between ACT and RDA; **CA Inputs:** partially toggling according to Table 282; **Data IO:** read data bursts with different data between one burst and the next one according to Table 282; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 282; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 282
IDDQ7	**Operating Bank Interleave Read IDDQ Current** **Same condition with IDD7,** however measuring IDDQ current instead of IDD current
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7,** however measuring IPP current instead of IDD current
IDD8	**Maximum Power Saving Deep Power Down Current** **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n#:** low; **CA:**High**, DM_n:** stable at 1; **Bank Activity:** All banks closed and device in MPSM deep power down mode5; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Patterns Details**: same as IDD6N but MPSM is enabled in mode register.
IDDQ8	**Maximum Power Saving Deep Power Down IDDQ Current** **Same condition with IDD8,** however measuring IDDQ current instead of IDD current
IPP8	**Maximum Power Saving Deep Power Down IPP Current** **Same condition with IDD8,** however measuring IPP current instead of IDD current
IDD9 (Optional)	**MBIST Current** **Device in MBIST mode, External clock:** On; **CS_n**: Stable at 1 after MBIST entry; **CA Inputs:** stable at 1; **Data IO:** VDDQ; **Bank Activity:** MBIST operation; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ9 (Optional)	**MBIST IDDQ Current** **Same condition with IDD9,** however measuring IDDQ current instead of IDD current
IPP9 (Optional)	**MBIST IPP Current** **Same condition with IDD9,** however measuring IPP current instead of IDD current

Note(s):

1. Burst Length: BL16 fixed by MR0 OP[1:0]=00.

2. Output Buffer Enable
   - set MR5 OP[0] = 0] : Qoff = Output buffer enabled
   - set MR5 OP[2:1] = 00]: Pull-Up Output Driver Impedance Control = RZQ/7
   - set MR5 OP[7:6] = 00]: Pull-Down Output Driver Impedance Control = RZQ/7

   RTT_Nom enable
   - set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6
   RTT_WR enable
   - set MR34 OP[5:3] = 010 RTT_WR = RZQ/2
     CA/CS/CK ODT, DQS_RTT_PART, and RTT_PARK disable
   - set MR32 OP[5:0] = 000000
   - set/MR33 OP[5:0] = 000000

   - set MR34 OP[2:0] = 000

3. WRITE CRC enabled
    - set MR50 OP[2:1] = 11

4. Read CRC enabled
    - set MR50:OP[0]=1

5. MPSM Deep Power Down Mode
   - set MR2:OP[3]=1 if PDA Enumerate ID not equal to 15
   - set MR2:OP[5]=1 if PDA Enumerate ID equal to 15

11.2 IDD0, IDDQ0, IPP0 Pattern

Executes Active and PreCharge commands with tightest timing possible while exercising all Bank and Bank Group addresses. Note 2 applies to the entire table.

Table 273 — IDD0, IDDQ0, IPP0

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H	-	0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling1					Repeat sequence to satisfy tRAS(min), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling1					Repeat sequence to satisfy tRP(min), truncate if required
	4	ACT	L H	-	0x03FFF	0x0	0x00	0x0	
	5	DES	H	Toggling1					Repeat sequence to satisfy tRAS(min), truncate if required
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling1					Repeat sequence to satisfy tRP(min), truncate if required
1	8-15	Repeat sub-loop 0, use BG[2:0]=0x1 instead							
2	16-23	Repeat sub-loop 0, use BG[2:0]=0x2 instead							
3	24-31	Repeat sub-loop 0, use BG[2:0]=0x3 instead							
4	32-39	Repeat sub-loop 0, use BG[2:0]=0x4 instead							skip for x16
5	40-47	Repeat sub-loop 0, use BG[2:0]=0x5 instead							skip for x16
6	48-55	Repeat sub-loop 0, use BG[2:0]=0x6 instead							skip for x16
7	56-63	Repeat sub-loop 0, use BG[2:0]=0x7 instead							skip for x16
8-15	64-127	Repeat sub loops 0-7, use BA[1:0]=0x1 instead							
16-23	128-191	Repeat sub loops 0-7, use BA[1:0]=0x2 instead							
24-31	192-255	Repeat sub loops 0-7, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Note(s):

1. Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

11.3 IDD0F, IDDQ0F, IPP0F Pattern

Executes a rolling four bank group Active and PreCharge commands per tRC time while exercising all Bank, Bank, Group and CID addresses. Note 2 applies to the entire table.

Table 274 — IDD0F, IDDQ0F, IPP0F

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H		0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	2	ACT	L H		0x00000	0x0	0x01	0x0	
	3	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	4	ACT	L H		0x00000	0x0	0x02	0x0	
	5	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	6	ACT	L H		0x00000	0x0	0x03	0x0	
	7	DES	H	Toggling1					Repeat to satisfy tRAS(min) from Sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	14	PREpb	L			0x0	0x03	0x0	
	15	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	16	DES	H	Toggling1					Repeat for tRC(min) from Sequence 0 first ACTIVATE. This will be zero DESELECTS for speed 4000MT/s and slower.
1	17-33	Repeat sub-loop 0, use Row Address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat sub-loop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							skip for x16
4-7	68-101	Repeat sub-loops 0-3, use BA[1:0]=0x1 instead							
8-11	102-135	Repeat sub-loops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat sub-loops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Note(s):

1. Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

11.4 IDD2N, IDD3N Pattern

Executes DESELECT commands while exercising all command/address pins in a predefined pattern. All notes apply to entire table.

Table 275 — IDD2N, IDDQ2N, IPP2N, IDD3N, IDDQ3N, IPP3N

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF

Note(s):
1. Data is pulled to VDDQ
2. DQS_t and DQS_c are pulled to VDDQ
3. Command / Address ODT is disabled
4. Repeat sequence 0 through 3.
5. All banks of all logical ranks mimic the same test condition.

11.5 IDD2NT, IDDQ2NT, IPP2NT Pattern

Executes Non-Target WRITE commands simulating Rank to Rank timing while exercising all C/A bits. Notes 3-6 apply to entire table.

Table 276 — IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Instructions
0	WRITE1	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling2	Repeat sequence to meet 1*tCCD_S(min), truncate if required
2	WRITE1	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling2	Repeat sequence to meet 1*tCCD(min), truncate if required

Note(s):
1. WRITE with CS_n=L on both cycles indicated a non-target WRITE.
2. Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
3. Time between Non-Target WRITEs reflect tCCD_S (min) for ~~two~~ one rank~~s~~.
4. DQ signals are VDDQ.
5. DQS_t, DQS_c are ~~VSSQ~~ VDDQ.
6. Repeat 0 through ~~12~~ 3.

11.6 IDD4R, IDDQ4R, IPP4R Pattern

Executes READ commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses.
Notes 2-9 apply to entire table

Table 277 — IDD4R, IDDQ4R, IPP4R

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	READ	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	READ	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	READ	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with Auto Precharge = H, Burst Chop = H.
3. Row address is set to 0x0000
4. Data reflects burst length of 16.
5. Data Pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF.
6. Data Pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0x~~0~~F, 0x0, 0xF, 0x~~F~~0, 0x~~F~~0, 0xF, 0x~~0~~F, 0x0, 0xF, 0x0, 0xF, 0x0.
7 Data Pattern for x8 each beat will reflect two like nibbles (Data Pattern A = 0x00, 0xFF, 0xFF...).
8. Data Pattern for x16 each beat will reflect two like bytes (Data Pattern A = 0x0000, 0xFFFF, 0xFFFF...).
9. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state

11.7 IDD4W, IDDQ4W, IPP4W Pattern

Executes WRITE commands with tightest timing possible while exercising all Bank, Bank Group and ~~CDI~~ CID addresses. Notes 2-6 apply to entire table.

Table 278 — IDD4W, IDDQ4W, IPP4W

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	WRITE	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	WRITE	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	WRITE	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands ~~as specified~~ per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. WRITEs performed with Auto Precharge = H, Burst Chop = H.
3. Row address is set to 0x0000.
4. Data reflects burst length of 16.
5. Refer to IDD4R measurement loop table for data pattern definition.
6. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.

11.8 IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F Pattern

Executes Refresh (all Banks) command at minimum tRFC. Notes 3-6 apply to entire table.

Table 279 — IDD5B, IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sequence	Command	CS	C/A [13:0]	CA[9:8]	CID [2:0]	Special Instructions
0	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
1	DES	H	Toggling1	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
2	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
3	DES	H	Toggling1	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For IDD5B, use tRFC1(min). For IDD5F, use tRFC2(min).
3. DQ signals are VDDQ.
4. All banks of all “non-target” logical ranks are Idd2N condition.
5. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
6. Must set CA8=H on REFab commands to indicate 1X refresh rate on devices that support RIR.

11.9 IDD5C, IDDQ5C and IPP5C Patterns

Executes Refresh (Same Bank) command at minimum tRFCsb. Notes 2-5 apply to entire table.

Table 280 — IDD5C, IDDQ5C, IPP5C

Sequence	Command	CS	C/A [13:0]	CA[9:8]	BA [1:0]	CID [2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable						CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. DQ signals are VDDQ.
3. All banks of all “non-target” logical ranks are Idd2N condition.
4. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
5. All banks of all “non-target” logical ranks are Idd2N condition.

11.10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R Pattern

All notes apply to entire table.

Table 281 — IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E

Sequence	Command	Clock	CS	C/A [13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid tCKLCS(min) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy tCPDED(min), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A = H	CK_t = CK_c = H	L	0x3FFF	Repeat sequence indefinitely

Note(s):
1. Data is pulled to VDDQ
2. DQS_t and DQS_c are pulled to VDDQ
3. For 3DS, all banks of all logical ranks mimic the same test condition.

11.11 IDD7, IDDQ7 and IPP7 Patterns

Executes ACTVATE, READ/A commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-6 apply to entire table.

Table 282 — IDD7, IDD7Q, IPP7

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L H	-	0x00000	-	0x0	0x0	0x0	-	
	1	DES	H	Toggling1							Repeat sequence to satisfy tRRD_S(min)
1	2	ACT	L H	-	0x03FFF	-	0x0	0x1	0x0	-	
	3	DES	H	Toggling1							Repeat sequence to satisfy tRRD_S(min)
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead									skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead									skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead									skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead									skip for x16
8	16	RDA	L H	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
	17	ACT	L H	-	0x00000	-	0x1	0x0	0x0	-	
	18	DES	H	Toggling1							Repeat sequence to satisfy tCCD_S(min)
9	19	RDA	L H	-	-	0x000	0x0	0x1	0x0	Pattern B	
	20	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
	21	DES	H	Toggling1							Repeat sequence to satisfy tCCD_S(min)
10	22-24	Repeat sub-loop 8, use BG[2:0]=0x2 instead									
11	25-27	Repeat sub-loop 9, use BG[2:0]=0x3 instead									
12	28-30	Repeat sub-loop 8, use BG[2:0]=0x4 instead									skip for x16
13	31-33	Repeat sub-loop 9, use BG[2:0]=0x5 instead									skip for x16
14	34-36	Repeat sub-loop 8, use BG[2:0]=0x6 instead									skip for x16
15	37-39	Repeat sub-loop 9, use BG[2:0]=0x7 instead									skip for x16
16-23	40-64	Repeat sub-loops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the ACT									
24-31	65-89	Repeat sub-loops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the ACT									
32-39	90-114	Repeat sub-loops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the ACT									
...	...	Repeat sub-loops 0-18 for each 3DS logical rank, if applicable									CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with Auto Precharge = L, Burst Chop = H.
3. x8 or x16 may have different Bank or Bank Group Address.
4. Data reflects burst length of 16.
5. Refer to IDD4R measurement loop table for data pattern definition
6. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition

12 Input/Output Capacitance

Table 283 — Silicon pad I/O Capacitance DDR5-4400 to DDR5-5600

Symbol	Parameter	DDR5-4400/ 4800		DDR5-5200/5600		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance (DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c)	0.45	0.9	0.45	0.85	pF	1,2
C_{DIO}	Input/output capacitance delta (DQ, DM_c)	-0.1	0.1	-0.1	0.1	pF	1,2,8
C_{DDQS}	Input/output capacitance delta (DQS_t and DQS_c)		0.04		0.04	pF	1,2,4
C_{CK}	Input capacitance (CK_t and CK_c)	0.2	0.6	0.2	0.55	pF	1,2
C_{DCK}	Input capacitance delta (CK_t and CK_c)		0.05		0.05	pF	1,2,3
C_{I}	Input capacitance (CS_n & CA[13:0] pins only)	0.2	0.6	0.2	0.55	pF	1,2,5
$C_{DI\_CS\_n}$	Input capacitance delta (CS_n pin only)	-0.1	0.1	-0.1	0.1	pF	1,2,6
C_{DI_CA}	Input capacitance delta (CA[13:0] pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,7
C_{ALERT}	Input/output capacitance of ALERT	0.4	1.5	0.4	1.5	pF	1,2
$C_{Loopback}$	Input/output capacitance of Loopback (LBDQ, LBDQS)	0.3	1.0	0.3	1.0	pF	1,2
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,2,9
C_{ZQ}	Input capacitance of ZQ	-	5	-	5	pF	1,2,11
C_{STRAP}	Input capacitance of MIR, CAI, CA_ODT pins	-	10	-	10	pF	1,2,10

Note(s):

1. This parameter is not subject to production test. This parameter is measured by using vendor specific measurement methodology.
2. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
3. Absolute value CIO(CK_t)-CIO(CK_c)
4. Absolute value of CIO(DQS_t)-CIO(DQS_c)
5. CI applies to CS_n and CA[13:0]
6. CDI_CS_n = CI(CS_n)-0.5*(CI(CK_t)+CI(CK_c))
7. CDI_CA = CI(CA[13:0])-0.5*(CI(CK_t)+CI(CK_c))
8. CDIO = CIO(DQ,DM)-Avg(CIO(DQ,DM))
9. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.
10. MIR, CAI, and CA_ODT are strap pins used to configure module or point to point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
11. Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality / accuracy with the max capacitive load is characterized.

Table 285 — DRAM package electrical specifications (X4/X8)

Parameter	Symbol	DDR5-4400 to DDR5-4800		DDR5-5200 to DDR5-5600		Unit	NOTE
		min	max	min	max		
Input/output Zpkg	Z_{pkg_DQ}	45	75	TBD	TBD	Ω	1,2,4,5,10
Input/output Pkg Delay	$T_{pkg\_delay\_DQ}$	10	35	TBD	TBD	ps	1,3,4,5,10
DQS_t, DQS_c Zpkg	Z_{pkg_DQS}	45	75	TBD	TBD	Ω	1,2,5,10,12
DQS_t, DQS_c Pkg Delay	$T_{pkg\_delay\_DQS}$	10	35	TBD	TBD	ps	1,3,5,10,12
Delta Zpkg DQS_t, DQS_c	DZ_{pkg_DQS}	-	5	TBD	TBD	Ω	1,2,5,7,10
Delta Delay DQS_t, DQS_c	$DT_{pkg\_delay\_DQS}$	-	2	TBD	TBD	ps	1,3,5,7,10
Input- CTRL pins Zpkg	Z_{pkg_CTRL}	45	75	TBD	TBD	Ω	1,2,5,9,10
Input- CTRL pins Pkg Delay	$T_{pkg\_delay\_CTRL}$	10	35	TBD	TBD	ps	1,3,5,9,10
Input- CMD ADD pins Zpkg	Z_{pkg_CA}	45	75	TBD	TBD	Ω	1,2,5,8,10
Input- CMD ADD pins Pkg Delay	$T_{pkg\_delay\_CA}$	10	35	TBD	TBD	ps	1,3,5,8,10
CK_t & CK_c Zpkg	Z_{pkg_CK}	45	75	TBD	TBD	Ω	1,2,5,10
CK_t & CK_c Pkg Delay	$T_{pkg\_delay\_CK}$	10	30	TBD	TBD	ps	1,3,5,10
Delta Zpkg CK_t & CK_c	$DZ_{pkg\_delay\_CK}$	-	5	TBD	TBD	Ω	1,2,5,6,10
Delta Delay CK_t & CK_c	$DT_{pkg\_delay\_CK}$	-	2	TBD	TBD	ps	1,3,5,6,10
ALERT Zpkg	Z_{pkg_ALERT}	45	75	TBD	TBD	Ω	1,2,5,10
ALERT Delay	$T_{pkg\_delay\_ALERT}$	10	60	TBD	TBD	ps	1,3,5,10
Loopback Zpkg	$Z_{pkg\_Loopback}$	45	75	TBD	TBD	Ω	1,2,5,10,11
Loopback Delay	$T_{pkg\_delay\_Loopback}$	10	60	TBD	TBD	ps	1,3,5,10,11

Note(s):

1. This parameter is not subject to production test.
2. This parameter is measured by using vendor specific measurement methodology to calculate the average Z_{pkg_xx} over the interval $T_{pkg\_delay\_xx}$
3. This parameter is measured by using vendor specific measurement methodology.
4. Z_{pkg_DQ} & $T_{pkg\_delay\_DQ}$ applies to DQ, DM
5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
6. Absolute value of $Z_{pkg\_CK\_t}$ - $Z_{pkg\_CK\_c}$ for impedance(Z) or absolute value of $T_{pkg\_delay\_CK\_t}$ - $T_{pkg\_delay\_CK\_c}$ for delay (T_{pkg_delay}).
7. Absolute value of Z_{pkg}(DQS_t)-Z_{pkg}(DQS_c) for impedance(Z) or absolute value of $T_{pkg\_delay\_DQS\_t}$ - $T_{pkg\_delay\_DQS\_c}$ for delay (T_{pkg_delay})
8. Z_{pkg_CA} & $T_{pkg\_delay\_CA}$ applies to CA[13:0]
9. Z_{pkg_CTRL} & $T_{pkg\_delay\_CTRL}$ applies to CS_n
10. Package implementations shall meet spec if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11. $Z_{pkg\_Loopback}$ & $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.
12. Z_{pkg_DQS} & $T_{pkg\_delay\_DQS}$ applies to DQS_t & DQS_c, TDQS_t & TDQS_c.

Table 286 — DRAM package electrical specifications (X16)

Parameter	Symbol	DDR5-4400 to DDR5-4800		DDR5-5200 to DDR5-5600		Unit	NOTE
		min	max	min	max		
Input/output Zpkg	Z_{pkg_DQ}	45	75	TBD	TBD	Ω	1,2,4,5,10
Input/output Pkg Delay	$T_{pkg\_delay\_DQ}$	10	40	TBD	TBD	ps	1,3,4,5,10
DQS_t, DQS_c Zpkg	Z_{pkg_DQS}	45	75	TBD	TBD	Ω	1,2,5,10,12
DQS_t, DQS_c Pkg Delay	$T_{pkg\_delay\_DQS}$	10	40	TBD	TBD	ps	1,3,5,10,12
Delta Zpkg DQS_t, DQS_c	DZ_{pkg_DQS}	-	5	TBD	TBD	Ω	1,2,5,7,10
Delta Delay DQS_t, DQS_c	$DT_{pkg\_delay\_DQS}$	-	2	TBD	TBD	ps	1,3,5,7,10
Input- CTRL pins Zpkg	Z_{pkg_CTRL}	45	75	TBD	TBD	Ω	1,2,5,9,10
Input- CTRL pins Pkg Delay	$T_{pkg\_delay\_CTRL}$	10	40	TBD	TBD	ps	1,3,5,9,10
Input- CMD ADD pins Zpkg	Z_{pkg_CA}	45	75	TBD	TBD	Ω	1,2,5,8,10
Input- CMD ADD pins Pkg Delay	$T_{pkg\_delay\_CA}$	10	45	TBD	TBD	ps	1,3,5,8,10
CK_t & CK_c Zpkg	Z_{pkg_CK}	45	75	TBD	TBD	Ω	1,2,5,10
CK_t & CK_c Pkg Delay	$T_{pkg\_delay\_CK}$	10	45	TBD	TBD	ps	1,3,5,10
Delta Zpkg CK_t & CK_c	$DZ_{pkg\_delay\_CK}$	-	5	TBD	TBD	Ω	1,2,5,6,10
Delta Delay CK_t & CK_c	$DT_{pkg\_delay\_CK}$	-	2	TBD	TBD	ps	1,3,5,6,10
ALERT Zpkg	Z_{pkg_ALERT}	45	75	TBD	TBD	Ω	1,2,5,10
ALERT Delay	$T_{pkg\_delay\_ALERT}$	10	60	TBD	TBD	ps	1,3,5,10
Loopback Zpkg	$Z_{pkg\_Loopback}$	45	75	TBD	TBD	Ω	1,2,5,10,11
Loopback Delay	$T_{pkg\_delay\_Loopback}$	10	60	TBD	TBD	ps	1,3,5,10,11

Note(s):
1. This parameter is not subject to production test.
2. This parameter is measured by using vendor specific measurement methodology.
3. This parameter is measured by using vendor specific measurement methodology.
4. Z_{pkg_DQ} & $T_{pkg\_delay\_DQ}$ applies to DQ, DM.
5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
6. Absolute value of $Z_{pkg\_CK\_t}$ - $Z_{pkg\_CK\_c}$ for impedance(Z) or absolute value of $T_{pkg\_delay\_CK\_t}$ - $T_{pkg\_delay\_CK\_c}$ for delay (T_{pkg_delay}).
7. Absolute value of Z_{pkg}(DQS_t)-Z_{pkg}(DQS_c) for impedance(Z) or absolute value of $T_{pkg\_delay\_DQS\_t}$ - $T_{pkg\_delay\_DQS\_c}$ for delay (T_{pkg_delay})
8. Z_{pkg_CA} & $T_{pkg\_delay\_CA}$ applies to CA[13:0]
9. Z_{pkg_CA} & $T_{pkg\_delay\_CTRL}$ applies to CS_n

10. Package implementations shall meet spec if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11. $Z_{pkg\_Loopback}$ & $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.
12. Z_{pkg_DQS} & $T_{pkg\_delay\_DQS}$ applies to DQS_t & DQS_c, TDQS_t & TDQS_c.

12.1 Electrostatic Discharge Sensitivity Characteristics

Table 287 — Electrostatic Discharge Sensitivity Characteristics

PARAMETER [1]	SYMBOL	MIN	MAX	UNIT	NOTES
Human body model (HBM)	ESDHBM	1000	-	V	2
Charged-device model (CDM)	ESD_{CDM}	250	-	V	3

NOTE 1 State-of-the-art basic ESD control measures have to be in place when handling devices

NOTE 2 Refer to ESDA / JEDEC Joint Standard JS-001 for measurement procedures.

NOTE 3 Refer to ESDA / JEDEC Joint Standard JS-002 f for measurement procedures

13 Electrical Characteristics & AC Timing

13.1 Rounding Definitions and Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 2200 MHz (4400 MT/s) for the DDR5-4400 speed bin, which mathematically yields a clock period tCK(AVG) of 0.454545... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be used. The DDR5 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. All timing parameters specified in the time domain (ns, ps, etc.) which must then be converted to the clock domain (nCK units) shall be defined to align with these rules. The key point is, the minimum timing parameters shall generally use the same rounding rules used to define tCK(AVG)min. The resulting rounding algorithms rely on results that are within correction factors of device testing and specification to avoid losing performance due to rounding errors.
These rules are:

- Minimum timing parameter values, including tCK(AVG)min, are rounded down and to be defined to 1 ps of accuracy in the DDR5 SDRAM specification based on the non-rounded nominal tCK(AVG)min for a given speed bin. If the nominal minimum timing parameter values require more than 1 ps of accuracy, they can be rounded down (faster) to the next 1 ps according to the rounding algorithms, and the DDR5 SDRAM is responsible for absorbing this small minimum parameter extension. In other words, the DDR5 SDRAM specification only lists the nominal minimum parameter values rounded down to the next 1ps. For example, this extends the DDR5-4400 tCK(AVG)min definition to be exactly 0.454 ns which is slightly smaller (faster) than the nominal memory clock period of 0.454545... ns by less than 1 ps.
- For minimum timing parameters, other than tCK(AVG)min, to avoid losing performance due to additional erroneous nCKs and to calculate the true real minimum values, their nominal values listed in the DDR5 SDRAM specification must be reduced (faster) by the same or greater % reduction (correction factor) that was used to define tCK(AVG)min. The DDR5 SDRAM is responsible for absorbing these parameter extensions. For example, tWRmin has a nominal value of 30.000ns, however, applying the 0.30% correction factor allows a more aggressive timing (for example, 29.910ns) to be supported, which allows the intended smaller (faster) nCK value to be maintained when rounding tCK(AVG)min down to the next 1 ps. Note, parameter values defined to be 0 ps do not need to be reduced by a correction factor, and therefore don’t require these rounding algorithms.
- Using real number math, nominal minimum parameters like tWRmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time are divided by the real application memory clock period tCK(AVG)real yielding a ratio of clock units (nCK), which is reduced by a correction factor of 0.30% (multiply by 99.70%) then the result is rounded up to the next integer number of clocks:

$$nCK = ceiling\left[\frac{\text{parameter\_nominal x 0.997}}{\text{tCK(AVG)real}}\right]$$

- Round down only integer number math is commonly used in the industry to calculate nCK values. This second algorithm uses scaling by 1000 to allow use of integer math. Here, the nominal minimum parameter, in ps, is multiplied by the scaled correction factor (1000-3=997) prior to divi-

sion by the application memory clock period, and 1 scaled by 1000 added to that result effectively rounds the result up. Division by 1000 undoes the scaling effects, resulting in a simple integer number of clocks as the final answer. The caveat is, effectively adding 1 prior to rounding down is mostly equivalent to rounding up except when the result is equal to an integer (whole number) in which case the result won't be rounded down as intended, and therefore performance would be lost. To address this, the largest correction factor of 0.28% needed for 3600 MHz (7200 MT/s) operation has been increased slightly to 0.30% in these rounding algorithms. This accounts for all integer boundary conditions, except for the specific case when the nominal minimum timing parameter value is defined to be 0 ps. This round down only integer number math algorithm is not required and not optimized for 0 ps parameter values, and will result in lost performance if used for 0 ps parameter values.

$$nCK = truncate\left[\frac{\left(\frac{truncate[\text{parameter\_nominal\_in\_ps}] \times 997}{truncate[\text{tCK(AVG)\_real\_in\_ps}]}\right) + 1000}{1000}\right]$$

- The real number math rounding algorithm and the round down only integer number math rounding algorithm both yield similar results. In case of conflicting results, the round down only integer number math algorithm shall prevail.
- The real number math and round down only integer number math rounding algorithms shall be used for all minimum timing parameters when converting from the time domain (ns, ps, etc.) to the clock domain (nCK units), except for when converting tAA to CL. If these rounding algorithms are used to convert tAA to CL, they'll return invalid CL's for some cases when down clocking (and the DIMM SPD CL Mask doesn't protect against all of these cases). The proper setting of CL shall be determined by the memory controller, either by using the speed bin tables, or by using the CL algorithm, or by some other means. Refer to the Speed Bins and Operations section for more information. Note, the CL algorithm replaces the need to use the DIMM SPD CL Mask.
- If the DDR5 SDRAM supports non-standard tCK, tAA, tRCD, and tRP speed bin timings, the CL algorithm will still only return valid CL's as defined in the speed bin tables, which may not be the intended CL's for non-standard speed bins. In these cases, the rounding algorithms may need to be used to convert tAA to CL, instead of the CL algorithm. The CL returned by the rounding algorithms shall be incremented up to the next supported CL according to the DIMM SPD CL Mask. Consult the memory vendor for more information.

13.1.1 Example 1, using real number math to convert $t_{WR(min)}$ from ns to nCK:

```
// This algorithm reduces the nominal minimum timing parameter value by a 0.30% correction factor,
// and rounds nCK up to the next integer value

real TwrMin, Correction, ClockPeriod, TempTwr, TempNck
int TwrInNck;

TwrMin      = 30.000;                  // tWRmin in ns
Correction  = 0.003                    // 0.30% per the rounding algorithm
ClockPeriod = ApplicationTck;          // Clock period in ns is application specific
TempTwr     = TwrMin * (1 - Correction); // Apply correction factor
TempNck     = TempTwr / ClockPeriod;   // Initial nCK calculation
TwrInNck    = (int) ceiling(TempNck);  // Round up to next integer value
```

Table 288 — Example 1, using real number math

DDR5 Device Operating at Standard Application Frequencies Timing Parameter: *t*WR(min) = 30.000ns					
Application Speed Grade	Device *t*WR	Application *t*CK	Device tWR / Application *t*CK	Device *t*WR * (1 - Correction) / Application *t*CK	Ceiling Result
	ns	ns	nCK (real)	nCK (corrected)	nCK (integer)
3200	30.000	0.625	48.00	47.86	48
3600	30.000	0.555	54.05	53.89	54
4000	30.000	0.500	60.00	59.82	60
4400	30.000	0.454	66.08	65.88	66
4800	30.000	0.416	72.12	71.90	72

13.1.2 Example 2, using integer math to convert $t_{WR(min)}$ from ns to nCK:

```
// This algorithm reduces the nominal minimum timing parameter value by a 0.30% correction factor,
// adds 1 nCK, and rounds nCK down to the next integer value

int TwrMin, Correction, ClockPeriod, TempTwr, TempNck, TwrInNck;

TwrMin      = 30000;                          // tWRmin in ps
Correction  = 3                               // 0.30% per the rounding algorithm
ClockPeriod = ApplicationTck;                 // Clock period in ps is application specific
TempTwr     = TwrMin * (1000 - Correction);   // Apply correction factor, scaled by 1000
TempNck     = TempTwr / ClockPeriod ;         // Initial nCK calculation, scaled by 1000
TempNck     = TempNck + 1000;                 // Add 1, scaled by 1000, to effectively round up
TwrInNck    = (int)(TempNck / 1000);          // Round down to next integer
```

Table 294 — Example 2, using round down only integer number math

DDR5 Device Operating at Standard Application Frequencies Timing Parameter: *t*WR(min) = 30.000ns = 30000ps					
Application Speed Grade	Device *t*WR	Application tCK	Device tWR / Application tCK	Device tWR * (1000 - Correction) / Application tCK + 1000	Truncate Corrected nCK / 1000
	ps	ps	nCK (real)	scaled nCK (corrected)	nCK (integer)
3200	30000	625	48.00	48856	48
3600	30000	555	54.05	54891	54
4000	30000	500	60.00	60820	60
4400	30000	454	66.08	66881	66
4800	30000	416	72.12	72899	72

13.3 Timing Parameters by Speed Grade

The analog timing parameters in this section have been defined based on nominal tCA(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

13.3.1 Timing Parameters for DDR-4400 to DDR5-5200

The analog timing parameters in this section have been defined based on nominal tCK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 295 — for DDR5-4400 to DDR5-5200

Speed		DDR5-4400		DDR5-4800		DDR5-5200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Average Clock Period	tCK(avg)	0.454	-	0.416	-	0.384	-	ns	1
Command and Address Timing									
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	
Write to Write command delay for same bank group	tCCD_L_WR	max(32nCK, 20ns)	-	max(32nCK, 20ns)	-	max(32nCK, 20ns)	-	nCK,ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	nCK,ns	
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	-	8	-	8	-	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	-	8	-	8	-	nCK	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2,4,6
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	8	-	8	-	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 14.545ns)	-	Max(32nCK, 13.333ns)	-	Max(32nCK, 12.307ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 18.181ns)	-	Max(40nCK, 16.666ns)	-	Max(40nCK, 15.384ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	nCK,ns	
Precharge to Precharge command delay	tPPD	2	-	2	-	2	-	nCK	7
Write recovery time	tWR	30	-	30	-	30	-	ns	

13.3.3 Timing Parameters for DDR-5600

Analog timing parameters in this section have been defined on nominal tCK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 297 — for DDR5-5600

Speed		DDR5-5600		Units	NOTE
Parameter	Symbol	MIN	MAX		
Clock Timing					
Average Clock Period	tCK(avg)	0.357	-	ns	1
Command and Address Timing					
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	-	nCK,ns	
Write to Write command delay for same bank group	tCCD_L_WR	max(32nCK, 20ns)		nCK,ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)	-	nCK,ns	
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)		nCK,ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	-	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	-	nCK	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)		nCK,ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP		nCK,ns	2,4,6
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 11.428ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 14.285ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	-	nCK,ns	
Precharge to Precharge command delay	tPPD	2	-	nCK	7
Write recovery time	tWR	30	-	ns	

Notes:

1 - tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.

2 - tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms, nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).

3 - RBL: Read burst length associated with Read command
- RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode
- RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
- RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

4 - WBL: Write burst length associated with Write command
- WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
- WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
- WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

5 - The following is considered for tRTW equation
- 1tCK needs to be added due to tDQS2CK
- Read DQS offset timing can pull in the tRTW timing
- 1tCK needs to be added when 1.5tCK postamble

6 - CWL=CL-2

7 - tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

13.3.7 Timing Parameters for 3DS-DDR5-4400 to 3DS-DDR5-5200 x4 2H & 4H

Analog timing parameters defined in this section are to be rounded to 1 ps of accuracy. Parameter min values which scale with tCK-min are to be defined using the tCKmin in the associated data rate

Table 301 — for x4 2H & 4H 3DS-DDR5-4400 to 3DS-DDR5-4800

Speed		DDR5-4400		DDR5-4800		DDR5-5200		Units	Notes
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Average Clock Period	tCK(avg)	0.454	-	0.416	-	0.384	-	ns	1
Command and Address Timing for 3DS									
Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	~~TBD~~ Max(8nCK, 5ns)	-	nCK, ns	
Write to Write command delay for same bank group in same logical rank	tCCD_L_WR_slr	Max(32nCK ,20ns)	-	Max(32nCK ,20ns)	-	~~TBD~~ Max(32nCK ,20ns)	-	nCK, ns	
Write to Write command delay for same bank group in same logical rank, second write not RMW	tCCD_L_WR2_slr	Max(16nCK ,10ns)	-	Max(16nCK ,10ns)	-	Max(16nCK ,10ns)	-	nCK, ns	
Read to Write command delay for same bank group in same logical rank	tCCD_L_RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for same bank group in same logical rank	tCCD_L_WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK, ns	4,6
Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	8	-	8	-	8	-	nCK	
Write to Write command delay for different bank group in same logical rank	tCCD_S_WR_slr	8	-	8	-	8	-	nCK	
Read to Write command delay for different bank group in same logical rank	tCCD_S_RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for different bank group in same logical rank	tCCD_S_WTR_slr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK, ns	4,6
Write to Read with Auto Precharge command for same bank in same logic rank	tCCD_WTRA_slr	CWL + WBL/2 + tWR_slr - tRTP_slr						nCK,ns	2,4,6
Activate to Activate command delay to same bank group in the same logical rank	tRRD_L_slr(1K)	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK, ns	
Activate to Activate command delay to different bank group in the same logical rank	tRRD_S_slr(1K)	8	-	8	-	8	-	nCK	
Four activate window to the same logical rank	tFAW_slr(1K)	max(32nCK ,14.545ns)	-	max(32nCK ,13.333ns)	-	max(32nCK ,12.307ns)	-	nCK, ns	9
Read command to Precharge command delay in same logical rank	tRTP_slr	Max(12nCK ,7.5ns)	-	Max(12nCK ,7.5ns)	-	Max(12nCK ,7.5ns)	-	nCK, ns	
Precharge to Precharge delay in same logical rank	tPPD_slr	2	-	2	-	2	-	nCK	7
Write recovery time in same logical rank	tWR_slr	30	-	30	-	30	-	ns	
Read to Read command delay in different logical ranks	tCCD_dlr	Max(8nCK, 3.636ns)	-	Max(8nCK, 3.333ns)	-	Max(8nCK, 3.333ns)	-	nCK, ns	
Write to Write command delay in different logical ranks	tCCD_WR_dlr	Max(8nCK, 3.636ns)	-	Max(8nCK, 3.333ns)	-	Max(8nCK, 3.333ns)	-	nCK, ns	12
Read to Write command delay in different logical ranks	tCCD_RTW_dlr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay in different logical ranks	tCCD_WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK, ns	4,6
Activate to Activate command delay to different logical ranks	tRRD_dlr	Max(4nCK, 1.818ns)	-	Max(4nCK, 1.666ns)	-	Max(4nCK, 1.666ns)	-	nCK, ns	
Four activate window to different logical ranks	tFAW_dlr	Max(16nCK ,7.272ns)	-	Max(16nCK ,6.666ns)	-	Max(16nCK ,6.666ns)	-	nCK, ns	
Precharge to Precharge delay in different logical rank	tPPD_dlr	2	-	2	-	2	-	nCK	7
Minimum Write to Write command delay in different physical ranks	tCCD_WR_dpr	8	-	8	-	8	-	nCK	12,13
Activate window by DIMM channel	tDCAW	128	-	128	-	128	-	nCK	10,11, 13,14
DIMM Channel Activate Command Count in tDCAW	nDCAC	-	32	-	32	-	32	ACT	10,11, 13,14

13.3.8 Timing Parameters for 3DS-DDR5-5600 to 3DS-DDR5-6400 x4 2H & 4H

Analog timing parameters defined in this section are to be rounded to 1 ps of accuracy. Parameter min values which scale with tCK-min are to be defined using the tCKmin in the associated data rate

Table 302 — for x4 2H & 4H 3DS-DDR5-5600

Speed		DDR5-5600		Units	Notes
Parameter	Symbol	MIN	MAX		
Clock Timing					
Average Clock Period	tCK(avg)	0.357	-	ns	1
Command and Address Timing for 3DS					
Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(8nCK,5ns)	-	nCK, ns	
Write to Write command delay for same bank group in same logical rank	tCCD_L_ WR_slr	Max(32nCK,20ns)	-	nCK, ns	
Write to Write command delay for same bank group in same logical rank, second write not RMW	tCCD_L_ WR2_slr	Max(16nCK,10ns)	-	nCK, ns	
Read to Write command delay for same bank group in same logical rank	tCCD_L_ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3,5,6
Write to Read command delay for same bank group in same logical rank	tCCD_L_ WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)		nCK, ns	4,6
Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	8	-	nCK	
Write to Write command delay for different bank group in same logical rank	tCCD_S_ WR_slr	8	-	nCK	
Read to Write command delay for different bank group in same logical rank	tCCD_S_ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3,5,6
Write to Read command delay for different bank group in same logical rank	tCCD_S_ WTR_slr	CWL + WBL/2 + Max(4nCK,2.5ns)		nCK,ns	4,6
Write to Read with Auto Precharge command for same bank in same logic rank	tCCD_ WTRA_slr	CWL + WBL/2 + tWR_slr - tRT-P_slr		nCK,ns	2,4,6
Activate to Activate command delay to same bank group in the same logical rank	tRRD_L_ slr(1K)	Max(8nCK,5ns)	-	nCK,ns	
Activate to Activate command delay to different bank group in the same logical rank	tRRD_S_ slr(1K)	8	-	nCK	
Four activate window to the same logical rank	tFAW_ slr(1K)	max(32nCK,11.428 s)	-	nCK, ns	9
Read command to Precharge command delay in same log-ical rank	tRTP_slr	Max(12nCK,7.5ns)	-	nCK,ns	
Precharge to Precharge delay in same logical rank	tPPD_slr	2	-	nCK	7
Write recovery time in same logical rank	tWR_slr	30	-	ns	
Read to Read command delay in different logical ranks	tCCD_dlr	Max(8nCK,3.214ns)	-	nCK, ns	
Write to Write command delay in different logical ranks	tCCD_ WR_dlr	Max(8nCK,3.214ns)	-	nCK, ns	12
Read to Write command delay in different logical ranks	tCCD_ RTW_dlr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3,5,6
Write to Read command delay in different logical ranks	tCCD_ WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)		nCK, ns	4,6
Activate to Activate command delay to different logical ranks	tRRD_dlr	Max(4nCK,1.666ns)	-	nCK, ns	
Four activate window to different logical ranks	tFAW_dlr	Max(16nCK,6.666n s)	-	nCK, ns	
Precharge to Precharge delay in different logical rank	tPPD_dlr	2	-	nCK	7
Minimum Write to Write command delay in different physi-cal ranks	tCCD_ WR_dpr	8	-	nCK	12,13
Activate window by DIMM channel	tDCAW	128	-	nCK	10,11,13,14
DIMM Channel Activate Command Count in tDCAW	nDCAC	-	32	ACT	10,11,13,14

Note(s):

1 - tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.

2 - tCCD_WTRA_slr(min) shall always be greater than or equal to CWL + WBL/2 + tWR_slr(min) - tRTP_slr(min), and when using the appropriate rounding algorithms, nCCD_WTRA_slr(min) shall always be greater than or equal to CWL + WBL/2 + nWR_slr(min) - nRTP_slr(min).

3 - RBL: Read burst length associated with Read command
RBL = 32 for fixed BL32 and BL32 in BL32 OTF mode

RBL = 16 for fixed BL16 and BL16 in BL32 OTF mode
RBL = 16 for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

4 - WBL: Write burst length associated with Write command
WBL = 32 for fixed BL32 and BL32 in BL32 OTF mode
WBL = 16 for fixed BL16 and BL16 in BL32 OTF mode
WBL = 16 for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

5 - The following is considered for tRTW equation
1tCK needs to be added due to tDQS2CK
Read DQS offset timing can pull in the tRTW timing
1tCK needs to be added when 1.5tCK postamble

6 - CWL=CL-2

7 - tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

~~4~~ 8 - The~~se~~ timings contained in this table are for x4 2H and 4H 3Ds device

~~4~~ 9 - For x4 devices only. x8 device timings are TBD.

10 - Activate commands to different channels on the same DIMM may be issued on the same cycle, not requiring any stagger.

11 - Activate commands to the same channel on a DIMM are subject to tDCAW. No more than nDCAC activate commands may be issued to the same channel on a DIMM within tDCAW.

12 - tCCD_-WR_dlr and tCCD_-WR_dpr also apply to the WRITE PATTERN command.

13 - Parameter applies to dual-physical-rank (36 and 40 placement) 3DS-based DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs.

14 - Activate commands to a DIMM channel include all Activate commands to the same logical rank (SLR), all Activate commands to different logical ranks (DLR), and all Activate commands to different physical ranks (DPR)

14 DDR5 Module Rank and Channel Timings

14.1 Module Rank and Channel Limitations for DDR5 DIMMs

To achieve efficient module power supply design for JEDEC-standard DDR5 DIMMs, minimum timings as well as limitations in the number of DRAMs are provided for Refresh, and Write operations occurring on a single module. As well, since these modules are organized as two independent 36-bit or 40-bit channels (32 bits for non-ECC DIMMs), additional restrictions apply in order to limit localized power delivery noise on the module. To provide best performance, the different channels may initiate commands on the same cycle provided the rank to rank timings are met, the maximum number of DRAMs in a given activity is not exceeded, and the applicable component timings shown elsewhere in this specification are met. The timing and operational relationships for DDR5 DIMMs are shown in **Table 303** below.

Table 303 — DDR5 Module Rank and Channel Timings for DDR5 DIMMs

DIMM Configuration	Maximum number of DRAM die in simultaneous or overlapping activity			
	Refresh (All-Bank Refresh)		Write, Write-Pattern	
	Die per Physical Rank	Die per DIMM	Die per Channel	Die per DIMM
SR x16	No restriction			
DR x16	No restriction		2	4
SR x8	No restriction			
DR x8	No restriction		5	10
SR x4	No restriction			
DR x4	No restriction		10	20
DR x4 (2H 3DS)	No restriction	40	10	20
DR x4 (4H 3DS)	30	40	10	20
DR x4 (8H 3DS)	30	40	10	20
Notes	1, 2, 3, 4, 7, 8, 9		1, 5, 6, 7, 9	

NOTE(S):

1. Any combination of commands with up to the maximum of die per channel and per DIMM, per condition is allowed.
2. Refresh commands to different channels do not require stagger.
3. tRFC_dlr must be met for refresh commands to different logical ranks within a package rank on the same channel.
4. Any DRAM is considered to be in Refresh mode until tRFC time has been met.
5. tCCD parameters must be met for Write and Write-Pattern commands to different logical ranks or physical ranks within the same channel; no overlapping write data bus activity is allowed on two physical or logical ranks within the same channel.
6. Write and Write-Pattern commands to different channels do not require stagger.
7. Each rank consists of one group of DRAMs making up a 36 or 40 bit channel (32 bits for non-ECC DIMMs).
8. These restrictions only apply to explicit all-banks refresh commands (REFab) and not to self-refresh entry or exit
9. Restrictions apply to DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs

15 DDR5 System RAS Improvement

15.1 Design Guidelines for DDR5 Bounded Fault RAS Improvement

15.1.1 DDR5 Reliability Design Guidelines Overview

These DDR5 reliability design guidelines aim to bound bits impacted by certain DRAM failures. This limits the number of failure patterns seen by the memory controller such that correction of many failures can be reliably performed in DIMMs with one ECC device.

Many internal DRAM failures may impact only a portion of the data from a fetch. The likelihood of a specific component failing may also vary between process generations and DRAM vendors. These guidelines can be used by DDR5 DRAM's to bound failures from the components most likely to fail. These design guidelines can only address failures that impact a portion of the data from a 128-bit fetch. Failures that impact all the data in a 128-bit fetch from a device (e.g. device failure, bank failure) cannot be bounded as described here.

15.1.2 Reliability Design Guidelines

In a x8 device bounded failures are defined by the following qualities:

- A bounded fault will not impact more than 32 bits of data in a 128-bit fetch
- The data bits impacted by a bounded failure will be confined to at most 2 DQs (i.e. the failures will be DQ aligned)
- The DQs transmitting data impacted by the failure will both be in either the first nibble or the second nibble of a burst. That is, the impacted DQs will both be in the set of the first 4 DQs (DQ0, DQ1, DQ2, DQ3) or both in the set of the last four DQs (DQ4, DQ5, DQ6, DQ7)

Figure 229 shows examples of fault boundaries for x8 devices. Device on the left has a bounded fault in lanes DQ0 and DQ1 in the first nibble. Device on the right has a bounded fault in lanes DQ4 and DQ6 in the second nibble.

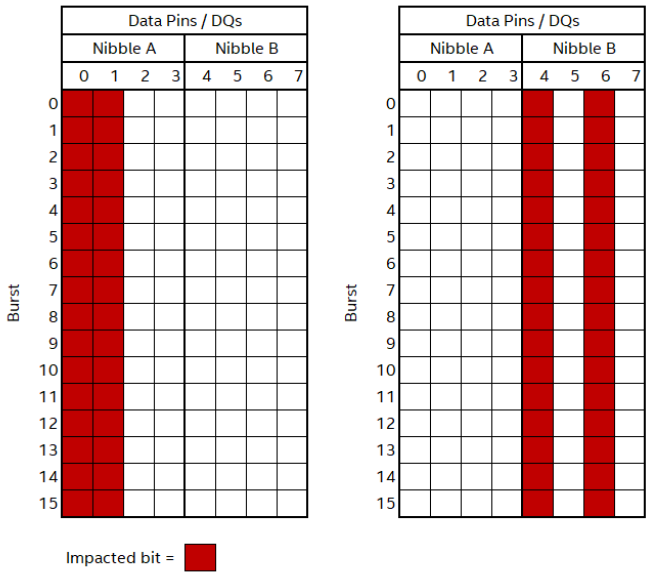


Figure 229 — Examples of x8 Fault Boundaries

A x4 device has similarly defined qualities for the failure boundaries, with the noted exception of the number of bits impacted by a bounded failure. In a DRAM device in a 9x4 configuration bounded failures should not impact more than 16 bits. However, in a 10x4 device the bounded failure may impact up to 32 bits.

In x4 devices bounded failures are defined by the following qualities:

- A bounded failure in a DRAM device in a 9x4 configuration shall not impact more than 16 bits of data in a 128-bit prefetch.
- A bounded failure in a DRAM device in a 10x4 configuration shall not impact more than 32 bits of data in a 128-bit prefetch.
- For a device in a 9x4 configuration, the data bits impacted by a bounded failure will be confined to one DQ.
- For a device in a 10x4 configuration, the data bits impacted by a bounded failure will be confined to at most two DQs.

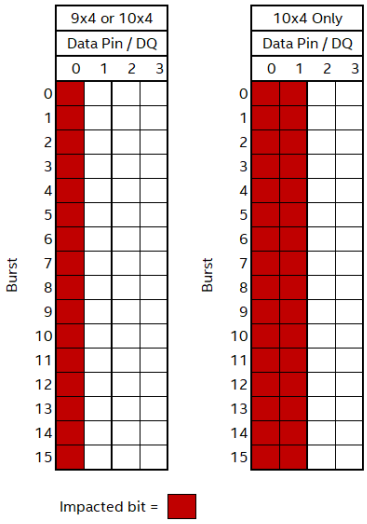


Figure 230 — Example of x4 Fault Boundary.

15.2 Single Error Correction (SEC) Code Properties

To maintain the bounded fault design guidelines, miscorrections by the on-die ECC must be restricted when a bounded fault causes a multi-bit error. In devices with bounded fault it is suggested that the DRAM vendor uses an on-die ECC code that maintains the fault boundaries. That is, if an error is contained in one boundary, then the on-die ECC should not spread the error into a second boundary by miscorrection. Note that if faults are not bounded in the device, then the on-die ECC does not need to have these properties.

To restrict miscorrection in devices following bounded fault design guidelines, the data may be divided into blocks aligned with the bounded fault and miscorrection should be restricted in the case an error is contained in a single data block. The 128 data bits used to compute a set of 8 check bits may be divided into data blocks up to 32 bits in size. These data blocks are to be determined by the memory vendor to best align with internal DRAM faults. For example, a common component fault may impact 32 bits per 128 data bits, then the vendor may choose to divide the 128 data bits into four 32-bit blocks each of which correspond to the bits impacted by one of the components failing.

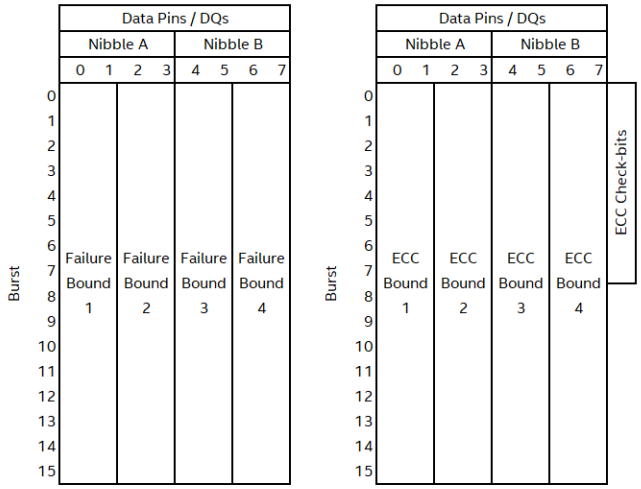


Figure 231 — Example of Fault Boundaries versus on-die ECC data blocks

If a multi-bit error occurs on a read and is limited to one data block, then the on-die ECC SEC code should do one of the following:

- Miscorrect a bit in the data block containing the error
- Miscorrect a bit in the on-die ECC check bits
- Detect the error (a SEC code may detect some multi-bit errors, but detection of these errors is not guaranteed)

The selection of block size and data blocks is determined by the vendor to best suit the device architecture and possible modes of fault.

15.3 Writeback of Data During x4 RMW and ECS Operation

The DRAM device may optionally support the suppressing of writeback for x4 devices and ECS writebacks. DRAM may implement the feature in MR9 or MR15. SPD specification will indicate if feature is supported and will also indicate whether to use MR9 or MR15 for enabling the modes.

If MR9 OP1=1 or MR15 OP7=1, then x4 DRAM's on writes will perform an internal 'read-modify-write' operation for BL16. BL32 mode does not requires an internal 'read modify write' operation. The DRAM will correct any single bit errors that result from the internal read of 128 bit data before merging the incoming 64 bit data and then re-compute 8 ECC Check bits. Note that ECC check bits are computed after merging of the incoming data with the corrected data from the array. DRAM will then write the incoming 64b data to the array along with recomputed 8 ECC Check bits. DRAM will suppress the writeback of 64 bit data that was fetched from the array irrespective of whether the 64 bit data needed any correction or not. Suppression of writeback (where applicable due to BC8 or DM usage) is not supported on x8/x16 devices; MR9:OP[1] or MR15:OP[7] must be set to "0_B". Suppression of writeback may or may not occur when BC8 mode is used on x4 devices.

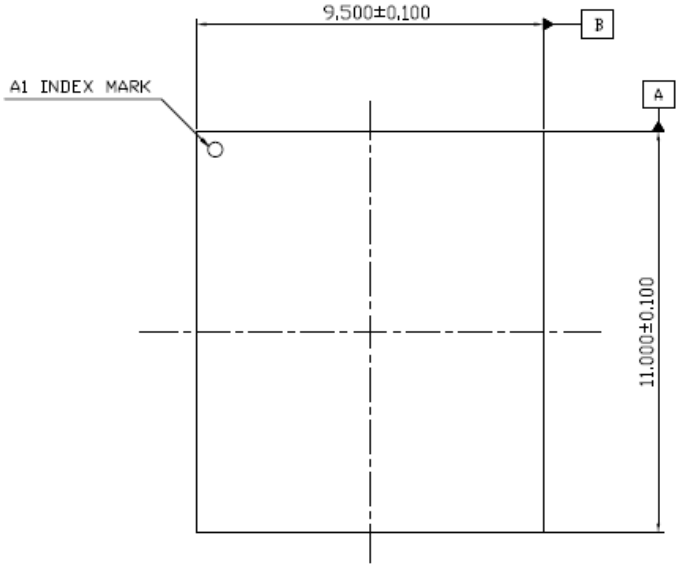
If MR9 OP0=1 or MR15 OP6=1, then DRAM will suppress writeback of data and ECC Check bits during ECS operation for x4, x8 and x16 DDR5. DRAM will continue to count errors to provide transparency.

MR9 or MR15 Register Information

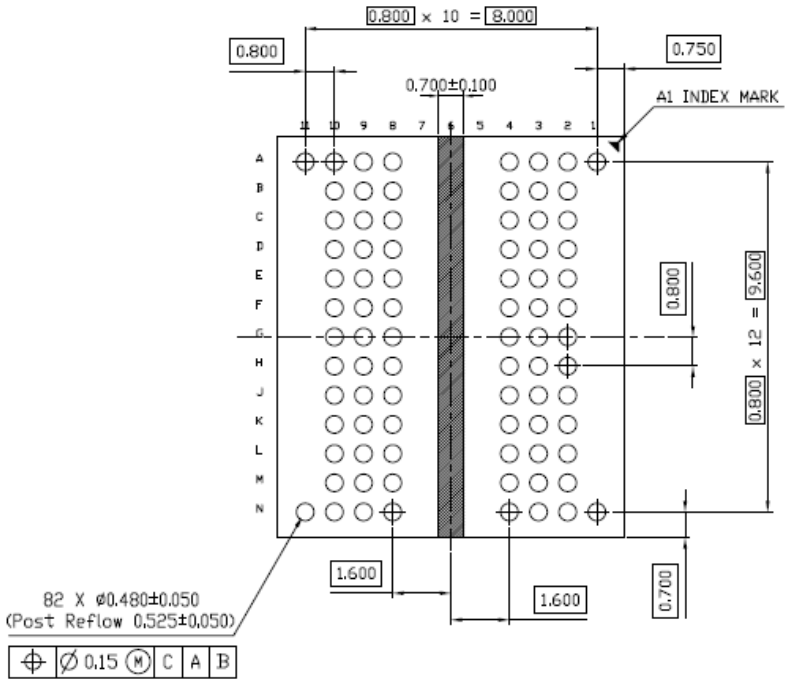
Function	Register Type	Operand	Data	Notes
x4 Writes	R/W	MR9:OP[1] or MR15:OP[7]	0B: Do not suppress writeback of Data during RMW (Default) 1B: Suppress writeback of Data during RMW (Optional)	1
ECS Write-back	R/W	MR9:OP[0] or MR15:OP[6]	0B: Do not suppress writeback of Data and ECC Check Bits (Default) 1B: Suppress writeback of Data and ECC Check Bits (Optional)	1

Note(s):
1. SPD specification will indicate if feature is supported and will also indicate whether to use MR9 or MR15 for enabling the modes.

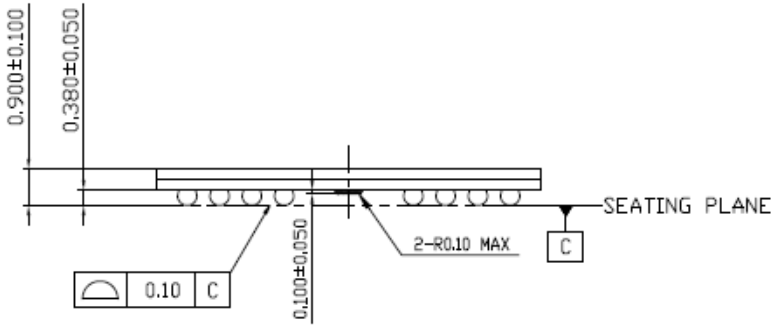
Package Dimension(x4/x8): 82Ball Fine Pitch Ball Grid Array Outline



TOP VIEW

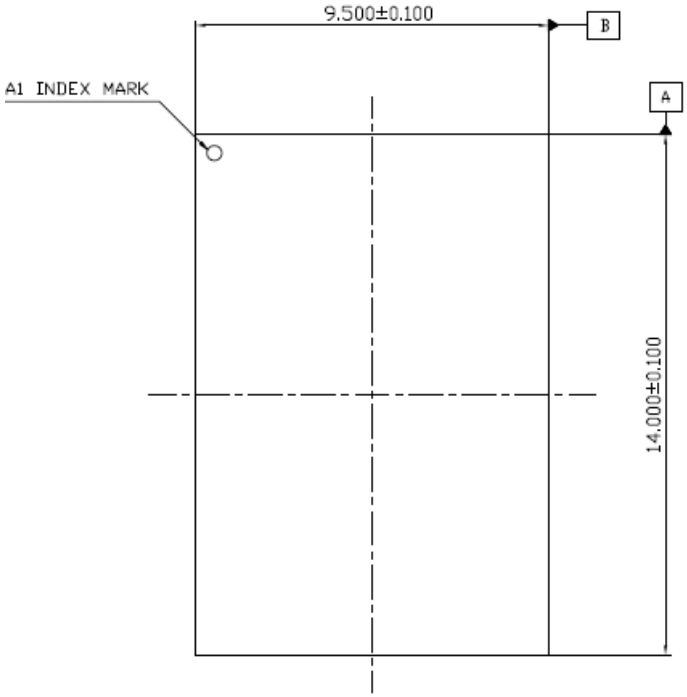


BOTTOM VIEW

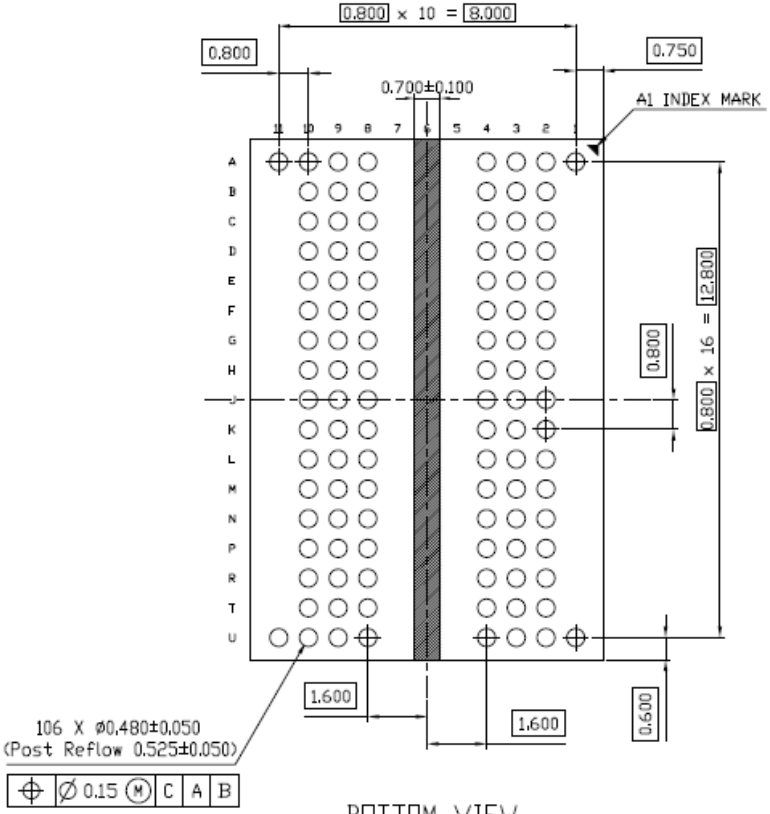


FRONT VIEW

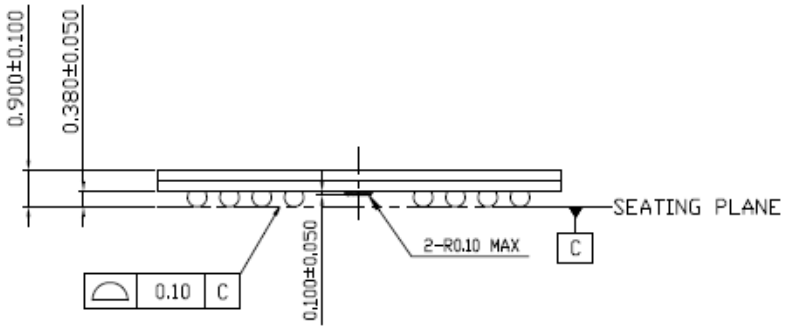
Package Dimension(x16): 106Ball Fine Pitch Ball Grid Array Outline



TOP VIEW



BOTTOM VIEW



FRONT VIEW