SAMSUNG

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K4RAH046VB
K4RAH086VB

16Gb B-die DDR5 SDRAM

82FBGA with Lead-Free & Halogen-Free (RoHS compliant)

Datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.90	- Preliminary spec	Jan.2020	Preliminary	H.S.Yoon J.Y.Lee
0.91	- Preliminary datasheet • Change bin (40-40-40 → 40-39-39).	Apr 15th.2021	Preliminary	J.W.Cho J.Y.Kim
1.0	- Final datasheet. • Update IDD and IPP values.	Jul 22th.2021	Final	J.W.Cho J.Y.Kim

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16Gb B-die DDR5 SDRAM

1.0 ORDERING INFORMATION

[Table 1] Ordering Information Table

Organization	DDR5-4800(40-39-39)[1]	Package
4Gx4	K4RAH046VB-BCQK	82 FBGA
2Gx8	K4RAH086VB-BCQK	82 FBGA

NOTE :
1) Speed bin is in order of CL-tRCD-tRP.
2) Backward compatible to lower frequency.

2.0 KEY FEATURES

[Table 2] Speed Bins

Speed	DDR5-4000	DDR5-4400	DDR5-4800	Unit
	32-32-32	36-36-36	40-39-39	
tCK(min)	0.500	0.454	0.416	ns
CAS Latency	32	36	40	nCK
tRCD(min)	16.000	16.000	16.000	ns
tRP(min)	16.000	16.000	16.000	ns
tRAS(min)	32.000	32.000	32.000	ns
tRC(min)	48.000	48.000	48.000	ns

- JEDEC standard compliant.
- VDD = VDDQ = 1.1V (1.067V(- 3%) ~ 1.166V(+6%)).
- VPP = 1.8V(1.746V(-3%) ~ 1.908V(+6%)).
- 2000MHz f_{CK} for 4000Mb/sec/pin, 2200MHz f_{CK} for 4400Mb/sec/pin, 2400MHz f_{CK} for 4800Mb/sec/pin.
- x4/8-32Banks(8 Bank Groups).
- Programmable CAS Latency (posted CAS): 26,30,32,36,40,42,46,48,52.
- Programmable Additive Latency: CL-2 clock.
- Programmable CAS Write Latency (CWL) = 32(DDR5-4000), 36(DDR5-4400), 40(DDR5-4800).
- 16-bit pre-fetch.
- Burst Length: 16 by default. 8 with tCCD=8, which does not allow gapless READ or WRITE, where BC8 and BL32 refer to CA4 BL*=L.
- Bi-directional Differential Data-Strobe.
- Internal ZQ calibration via Multi-Purpose Command(MPC) - ZQcal start and ZQcal Latch.
- On Die Termination (ODT) via Mode Register setting : RTT_PARK, RTT_WR, RTT_NOM_WR, RTT_NOM_RD.
- Average Refresh period 3.9us at lower than T_{CASE} 85°C, 1.95us at 85°C < T_{CASE} ≤ 95 °C.
- Connectivity Test Mode (TEN) is supported.
- Asynchronous Reset.
- Package: 82 balls FBGA - x4/x8.
- All of Lead-Free products are compliant for RoHS.
- All of products are Halogen-free.
- POD (Pseudo Open Drain) interface for data input/output,command and address input.
- Internal VREF for data inputs, command/address inputs and chip select.
- External VPP for DRAM activating power.
- hPPR and sPPR are supported.
- Refresh Management(RFM) is supported.
- Package Output Driver Test Mode (SNEM) is supported.
- CAI (Command Address Inversion).
- 2N Mode support.
- 4-tap Decision Feedback Equalizer(DFE) is supported.
- Loopback and Bit Error Rate Test are supported.
- On-Die ECC is supported with ECC Transparency and Error Check and Scrub(ECS).
- 2-step(external and internal) WRITE Leveling is supported.
- CRC(Cyclic Redundancy Check) for READ/WRITE data integrity.
- Command Address Inversion(CAI).

The 16Gb DDR5 SDRAM B-die is organized as a 128Mbit x 4 I/Os x 32banks or 64Mbit x8 I/Os x 32banks device.

This synchronous device achieves high speed double-data-rate transfer rates of up to 4800Mb/sec/pin (DDR5-4800) for general applications.

The chip is designed to comply with the following key DDR5 SDRAM features such as posted CAS, Programmable CWL, Internal Calibration via MPC, On Die Termination via Mode Register setting and Asynchronous Reset.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and $\overline{DQS}$) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a $\overline{RAS}/\overline{CAS}$ multiplexing style. The DDR5 device operates with 1.1V (1.067V~1.166V) and 1.8V (1.746V~1.908V) power supply.

The 16Gb DDR5 B-die device is available in 82ball FBGAs(x4/x8).

NOTE :
1) This is an abstract of full DDR5 specification and does not cover the common features which are described in "Device Operation Datasheet".
2) The functionality described and the timing specifications included in this datasheet are for the DLL Enabled mode of operation.

3.0 PACKAGE PINOUT/MECHANICAL DIMENSION & ADDRESSING

3.1 x4/8 Package Pinout (Top view): 82ball FBGA Package

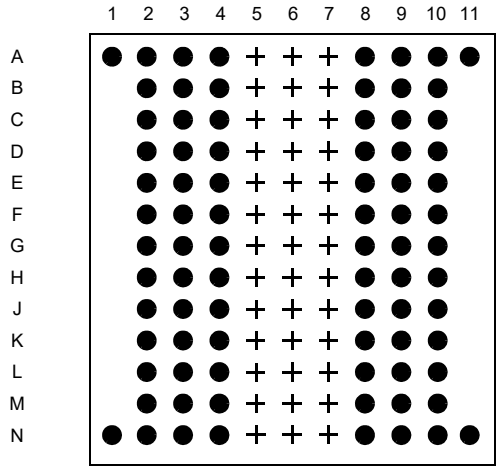
	1	2	3	4	5	6	7	8	9	10	11	
A	NC	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	NC	A
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD		B
C		VSS	DQ0	DQS_t				DM_n TDQS_t	DQ1	VSS		C
D		VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ		D
E		VDD	DQ4	DQ6				DQ7	DQ5	VDD		E
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS		F
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		G
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		H
J		VDDQ	A4	A0				A1	A5	VDDQ		J
K		VDD	A6	A2				A3	A7	VDD		K
L		VDDQ	VSS	A8				A9	VSS	VDDQ		L
M		CAI	A10	A12				A13	A11	RESET_n		M
N	NC	VDD	VSS	VDD				VPP	VSS	VDD	NC	N

NOTE :
1) DQ4-DQ7 are higher order DQ pins and are not connected for the x4 configuration.
2) TDQS_t is not valid for the x4 configuration.
3) TDQS_c is not available for the x4 configuration.
4) DM_n not valid for the x4 configuration.

Ball Locations (x4/8)

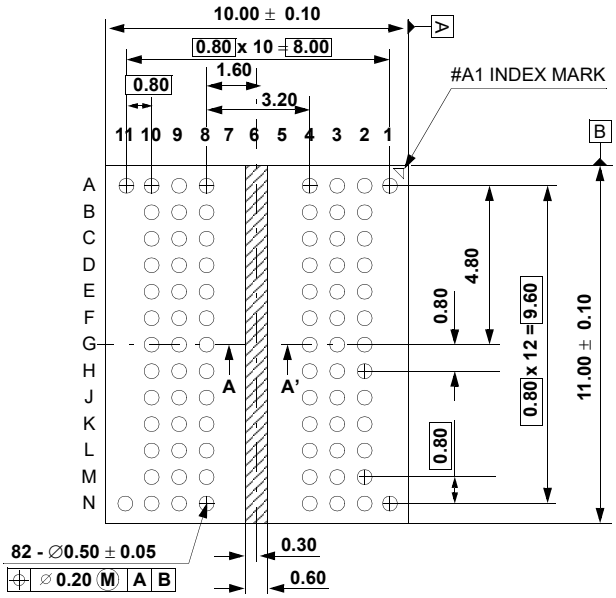
● **Populated ball**
\+ **Ball not populated**

Top view
(See the balls through the package)

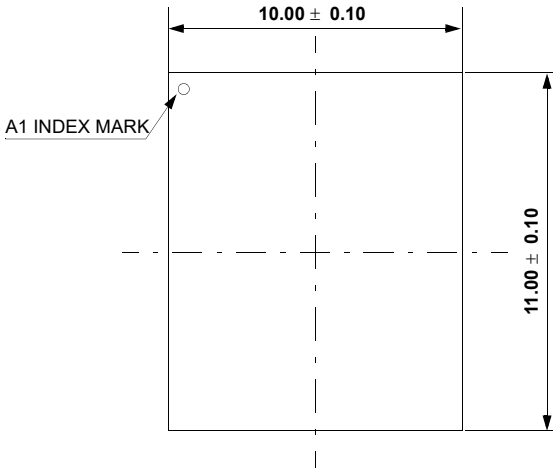


3.2 FBGA Package Dimensions (x4/x8)

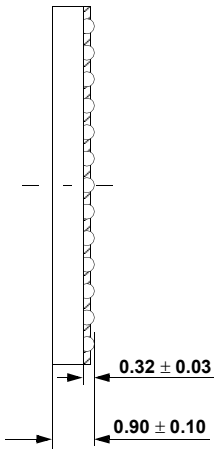
Units : mm



BOTTOM VIEW



TOP VIEW



SIDE VIEW

4.0 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

[Table 3] Input/Output Function Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DM_n, DMU_n, DML_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
CA[13:0]	Input	Command/Address Inputs:CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via MR5:OP[4]=1, the DRAM shall enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t shall provide the data mask function depending on MR5:OP[5];TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via MR5:OP[4]=0.
ALERT_n	Input/Output	Alert : If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on x4, x8 & x16 devices. HIGH in this pin shall enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
MIR	Input	Mirror: Used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSSQ if no CA mirror is required. Mirror pair examples:CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note: The CA[13] function is only relevant for certain densities(including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected to VDDQ.
CAI	Input	Command & Address Inversion: With the CAI pin connected to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSSQ if no CA inversion is required.
CA_ODT	Input	ODT for Command and Address . Apply Group A settings if the pin is connected to VSS and apply Group B settings if the pin is connected to VDDQ.
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V (1.067V ~1.166V)
VSSQ	Supply	DQ Ground

Symbol	Type	Function
VDD	Supply	Power Supply: 1.1 V (1.067V ~1.166V)
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8V (1.746V ~ 1.908V)
ZQ	Supply	Reference Pin for ZQ calibration

5.0 DDR5 SDRAM ADDRESSING

[Table 4] 16Gb Addressing Table

Configuration		4Gb x4	2Gb x8
Bank Address	BG Address	BG0~BG2	BG0~BG2
	Bank Address in a BG	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32
Row Address		R0~R15	R0~R15
Column Address		C0~C10	C0~C9
Page size		1KB	1KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H

6.0 AC & DC OPERATION CONDITIONS

6.1 Absolute Maximum Ratings

[Table 5] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.4	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.4	V	1
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.4	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :
1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6.2 DC Operating Conditions

[Table 6] DC Operating Conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz		NOTE
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit	
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	TBD	mOhm	TBD	mOhm	1,2,3
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	TBD	mOhm	TBD	mOhm	1,2,3
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	TBD	mOhm	TBD	mOhm	3

NOTE :
1) VDD must be within 66mV of VDDQ
2) AC parameters are measured with VDD and VDDQ tied together
3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball
4) Z(f) is defined for all pins per voltage domain. Z(f) does not include the DRAM package and silicon die

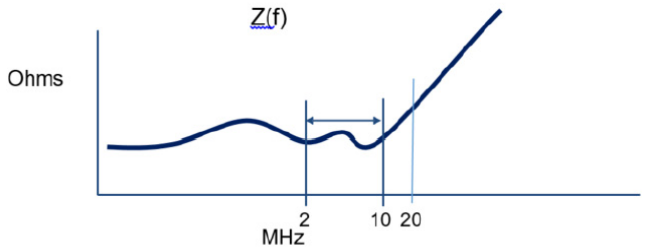


Figure 1. Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component)

A simplified electrical system load model for Z(F) with the general frequency response is shown in the figure below. The resistance and inductance can be scaled to generalize the spec response to the DRAM pin.

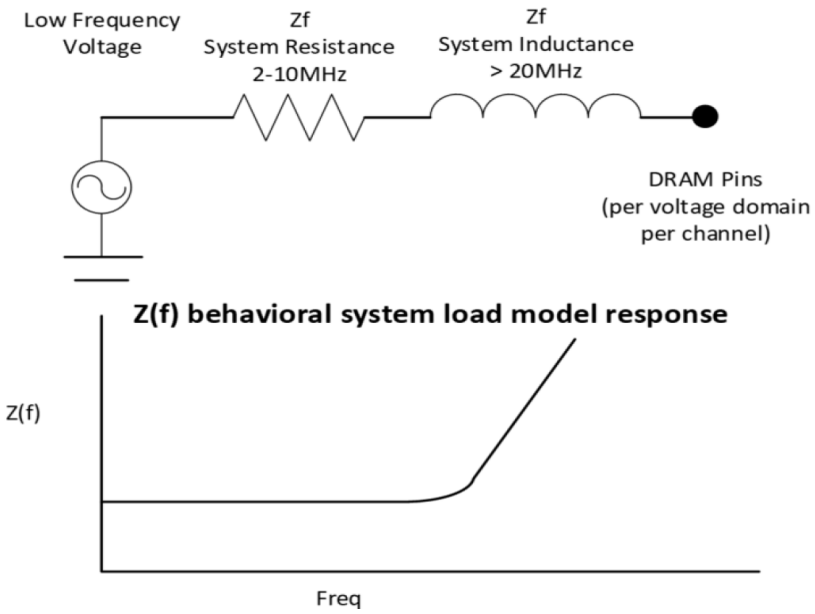


Figure 2. Simplified Z(f) electrical model and frequency response of PDN at the DRAM pin without the DRAM component

6.3 DRAM Component Operating Temperature Range

[Table 7] DC Operating Temperature Range

Symbol	Parameter	Temperature Range (Unit: ℃)		Grade	Notes
		Min	Max		
T_{oper_normal}	Normal Operating Temperature	0	85	NT	1,2,3,4
$T_{oper\_extended}$	Extended Operating Temperature	0	95	XT	1,2,3,4,5

NOTE :
1) All operating temperature symbols, ranges, acronyms are referred from JESD402-1.
2) Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3) All DDR5 SDRDAMs are required to operate in NT and XT temperature ranges.
4) When operating above 85°C, the host shall provide appropriate Refresh mode controls associated with the increased temperature range. The full description of these settings are defined in Table 68 in section 4.13.5.
5) Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [TOPER – (2.5°C × log2N)], where N is the number of the stacked dies.

7.0 AC & DC GLOBAL DEFINITIONS

7.1 Bit Error Rate

This section provides an overview of the Bit Error Rate (BER) and the desired Statistical Level of Confidence.

7.1.1 General Equation

$$n = \left(\frac{1}{BER}\right)\left[-\ln(1-SLC) + \ln\left(\sum_{k=0}^{N}\frac{(n\cdot BER)^k}{k!}\right)\right]$$

Where:

n = number of bits in a trial
SLC = statistical level of confidence
BER = Bit Error Rate
k = intermediate number of specific errors found in trial
N = number of errors recorded during trial

If no, errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left(\frac{1}{BER}\right)[-\ln(1-SLC)]$$

JEDEC recommends testing to 99.5% confidence levels; however, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or N=0), using BER=E^{-9} and confidence level SLC=99.5%, the result is n=(1/BER)(-ln(1-0.995) =5.298x10^9.
Results for commonly used confidence levels of 99.5% down to 70% are shown in Table 8.

[Table 8] Estimated Number of Transmitted Bits (n) for the confidence level of 70% to 99.5%

Number Errors	n = -ln(1-SLC)/BER							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/BER	4.61/BER	2.99/BER	2.3/BER	1.90/BER	1.61/BER	1.39/BER	1.20/BER

7.1.2 Minimum Bit Error Rate (BER) Requirements

Table 9 specifies the UIavg and Bit Error Rate requirements over which certain receiver and transmitter timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=E^{-9}.

[Table 9] Minimum BER Requirements for Rx/Tx Timing and Voltage Tests

Parameter	Symbol	DDR5-4000-4800			Unit	Notes
		Min	Nom	Max		
Average UI	UI_{AVG}	0.999* nominal	1000/f	1.001* nominal	ps	1
Number of UI (min)	$N_{Min\_UI\_Validation}$	$5.3x10^9$	-	-	UI	2
Bit Error Rate	BER_{Lane}	-	-	E^{-16}	Events	3,4,5

NOTE :
1) Average UI size, "f" is data rate
2) # of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=E^{-9}.
3) This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link layer based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver, therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
4) Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
5) This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx DQ Stressed Eye, Tx DQS Jitter, Tx DQ Jitter, and Tx DQ Stressed EH/EW specifications.

7.2 Unit Interval and Jitter Definitions

This chapter describes the UI and NUI Jitter definitions associated with the Jitter parameters specified in Rx Stressed Eye, Tx DQS Jitter, Tx DQ Jitter and Input Clock Jitter specifications.

7.2.1 Unit Interval (UI)

The times at which the differential crossing points of the clock occur are defined at t1, t2, …, tn-1, tn,..., tK. The UI at index "n" is defined as shown in Figure 3(with n=1,2,…) from an arbitrary time in steady state, where n=0 is chosen as the starting crossing point.

Mathematical definition of UI is shown in Figure 3 and Figure 4.

$$UI_n = t_n - t_{n-1}$$

Figure 3. UI Definition in Terms of Adjacent Edge Timings

For the Single-Ended data, the unit interval time starts when the signal crosses a pre-specified reference voltage. For the differential clock, the unit interval time starts when the CK_t and CK_c intersect (Figure 4).

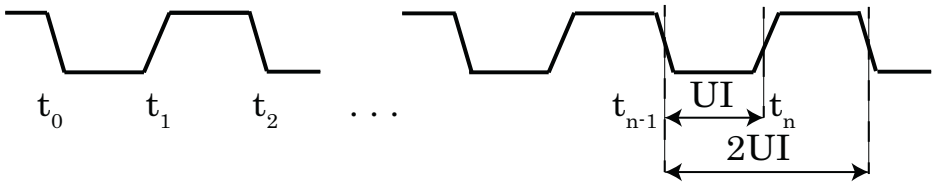


Figure 4. UI Definition Using Clock Waveforms

7.2.2 UI Jitter Definition

If a number of UI edges are computed or measured at times t1, t2, …, tn-1, tn,..., tK, where K is the maximum number of samples, then the UI jitter at any instance “n” is defined in Figure 5, where T = the ideal UI size.

$$UI(jit)_n = (t_n - t_{n-1}) - T, \quad n=1,2,3,...,K$$

Figure 5. UI Jitter for “nth” UI Definition (in terms of ideal UI)

In a large sample with random Gaussian-like jitter (therefore very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described in Figure 5 assumes starting from an instant steady state, where n=0 is chosen as the starting point.

1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded strobe.

Example: For 6.4 GT/s signaling, the forwarded strobe frequency is 3.2 GHz, or 1 UI = 156.25 ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (BER) for the link.

7.2.3 UI-UI Jitter Definition

UI-UI (read as “UI to UI”) jitter is defined to be the jitter between two consecutive UI as shown in Figure 6.

$$\Delta UI_n = UI_n - UI_{n-1} \quad n=2,3,...,K$$

Figure 6. UI-UI Jitter Definitions

7.2.4 Accumulated Jitter (Over “N” UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive “N” UI as shown in Figure 7.

$$T_{acc}^{N} = \sum_{p=m}^{m+N-1}(UI_p - \overline{UI}) \qquad m=1,2,...,K-N$$

Figure 7. Definition of Accumulated Jitter (over “N” UI)

where $\overline{UI}$ is defined in the equation shown in Figure 8.

$$\overline{UI} = \frac{\sum_{p=1}^{K} UI_p}{K} \qquad p=1,2,...,N,...,K$$

Figure 8. Definition of $\overline{UI}$

8.0 AC & DC INPUT MEASUREMENT LEVELS

8.1 CA Rx Voltage and Timings

The following draft assumes internal CA VREF. If the VREF is external, the specs will be modified accordingly.

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

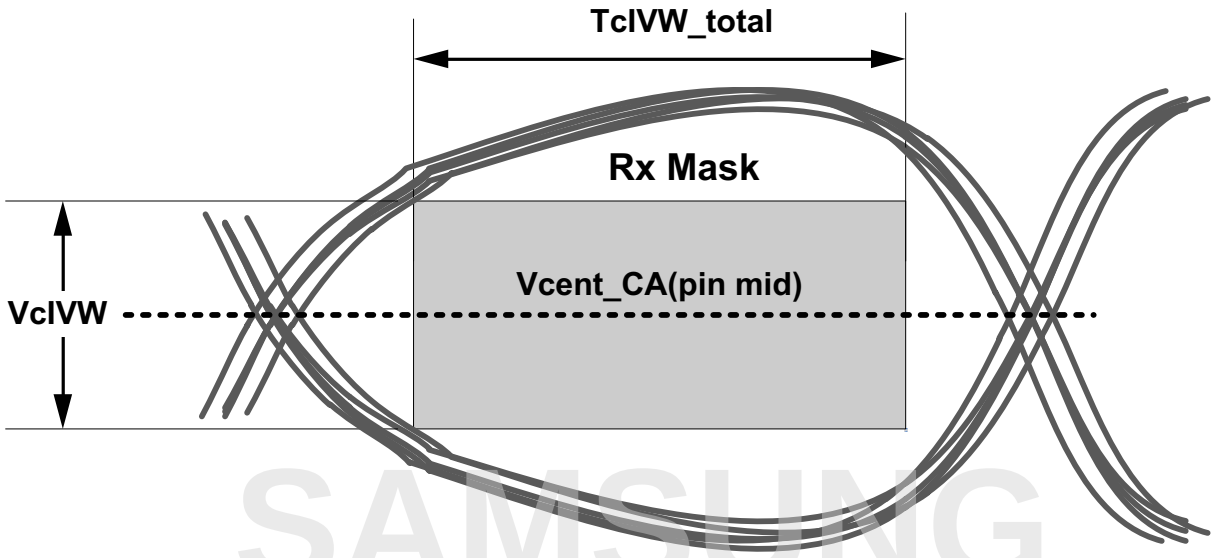


Figure 9. CA Receiver (Rx) mask

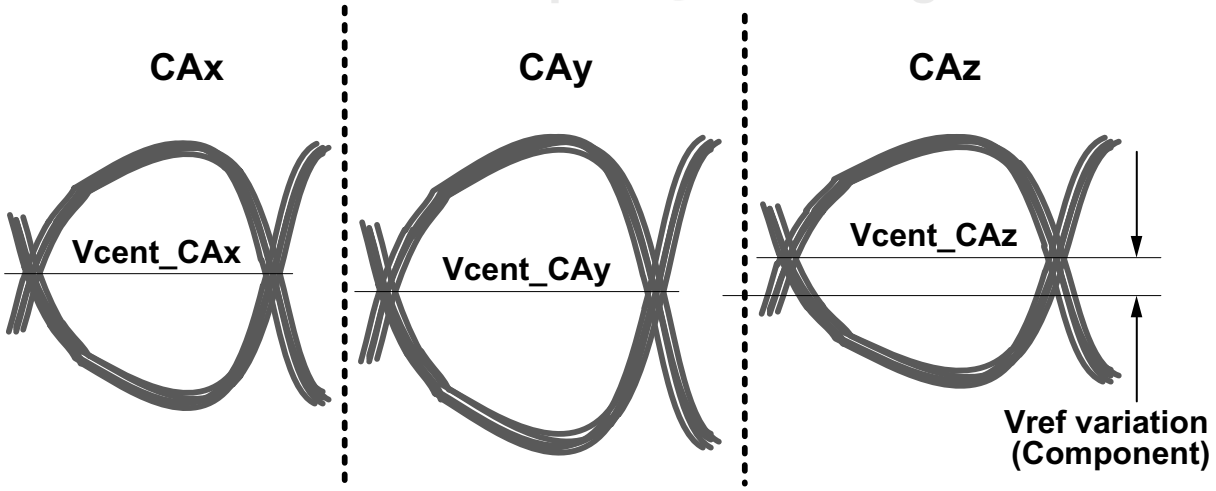


Figure 10. Across pin V_{REF}CA voltage variation

Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 10. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{REF} will be set by the system to account for Ron and ODT settings.

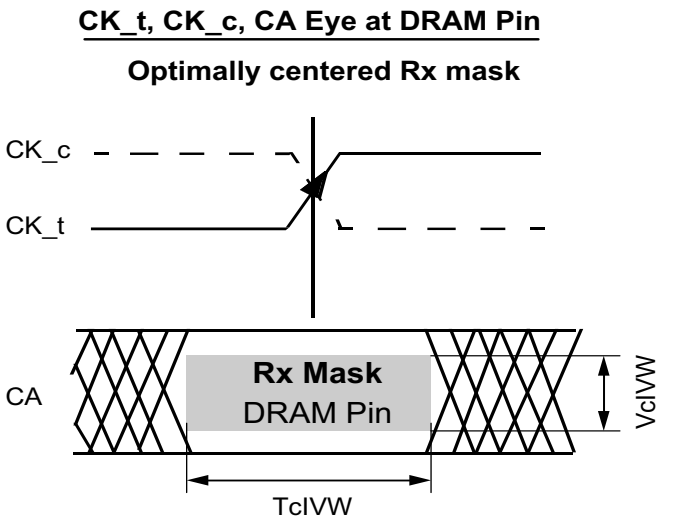
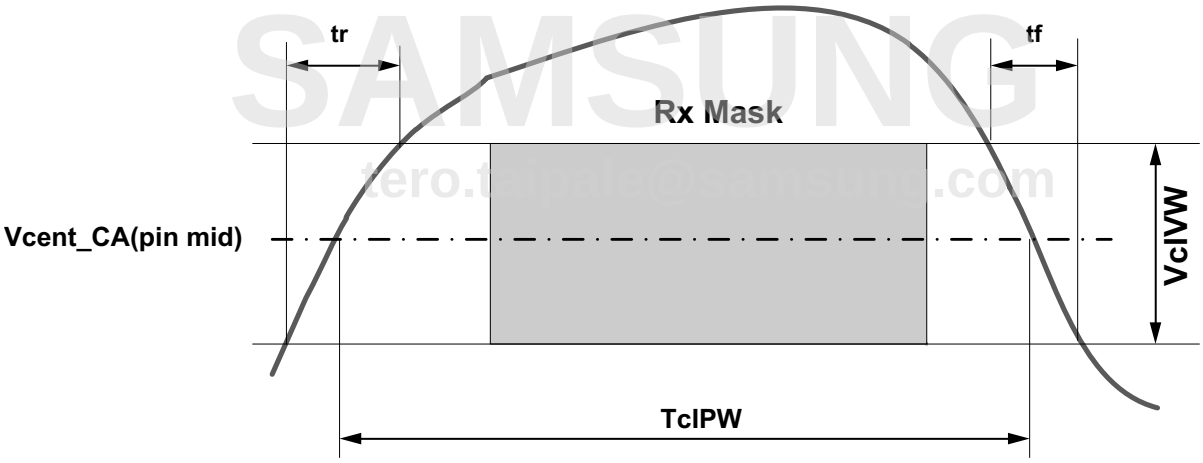


Figure 11. CA Timings at the DRAM Pins



Note
1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 12. CA TcIPW and SRIN_cIVW definition (for each input pulse)

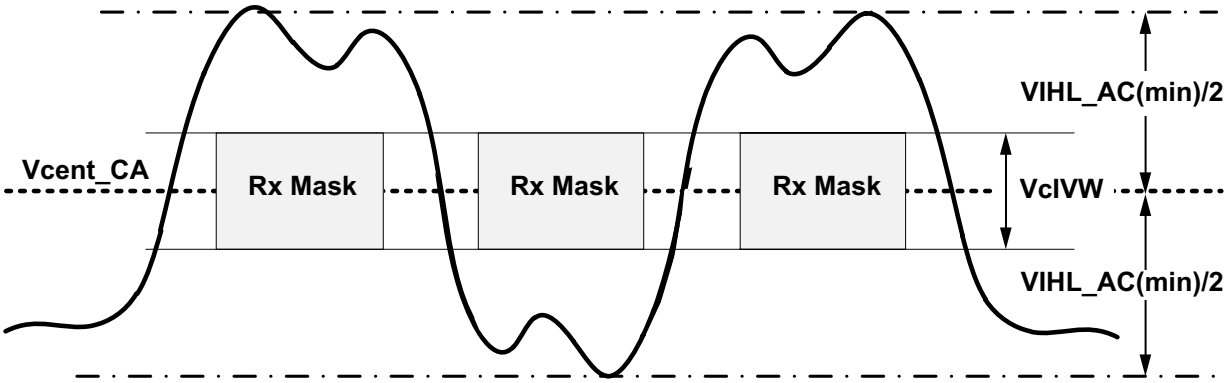


Figure 13. CA VIHL_AC definition (for each input pulse)

[Table 10] DRAM CA, CS Parametric Values

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	-	140	-	130	-	130	mV	1,2,4
Rx Timing Window	TclVW	-	0.2	-	0.2	-	0.2	UI*	1,2,3,4,8
CA Input Pulse Amplitude	VIHL_AC	160		150		150		mV	7
CA Input Pulse Width	TclPW	0.58		0.58		0.58		UI*	5,8
Input Slew Rate over VclVW	SRIN_clVW	1	7	1	7	1	7	V/ns	6

NOTE :
1) CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2) Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).
3) Rx differential CA to CK jitter total timing window at the VclVW voltage levels.
4) Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
5) CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6) Input slew rate over VclVW Mask centered at Vcent_CA(pin mid).
7) VIHL_AC does not have to be met when no transitions are occurring.
8) UI=tCK(avg)min.

8.2 Input Clock Jitter Specification

8.2.1 Overview

The clock is being driven to the DRAM either by the RCD for L/RDIMM modules, or by the host for U/SODIMM modules.

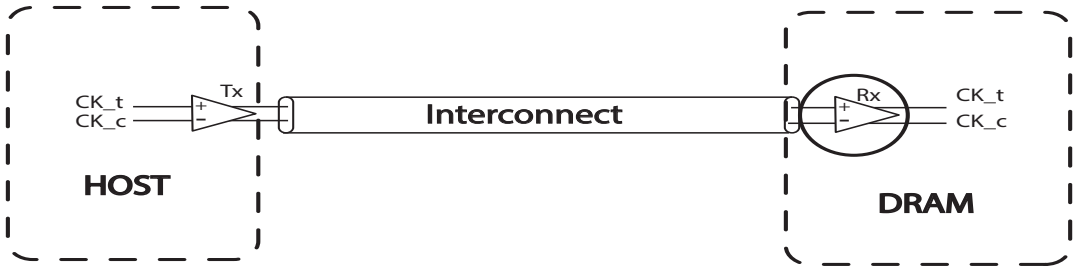


Figure 14. HOST driving clock signals to the DRAM

8.2.2 Specification for DRAM Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5 SDRAM device.

[Table 11] DRAM Input Clock Jitter Specifications

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	MHz	1,11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05	-	0.05	-	0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.030	-	0.030	-	0.030	UI	3,6,11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	-	0.090	UI	3,6,11
Rj RMS value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.0040	-	0.0040	-	0.0040	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.074	-	0.074	-	0.074	UI	3,7,11
Tj value of N-UI Jitter, where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	0.140	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI	3,10,11,12
Tj value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI	3,10,11,12

NOTE :

1) f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600.
2) Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock.
3) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4) Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5) Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD.
6) Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
7) Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD.
8) Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
9) Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD.
10) Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
11) The validation methodology for these parameters will be covered in future ballots.
12) If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$.

8.3 Differential Input Clock (CK_t, CK_c) Cross Point Voltage (VIX)

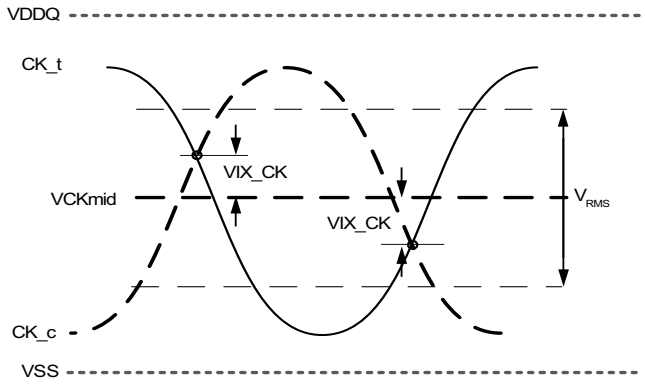


Figure 15. VIX Definition (CK)

[Table 12] Crosspoint Voltage (VIX) for Differential Input Clock

Parameter	Symbol	DDR5-4000 to 4800		Unit	Note
		min	max		
Clock differential input crosspoint voltage ratio	VIX_CK_Ratio	-	50	%	1,2,3

NOTE :
1) The VIX_CK voltage is referenced to VCKmid(mean) = (CK_t voltage + CK_c voltage) /2, where the mean is over 8 UI.
2) VIX_CK_Ratio = (|VIX_CK| / |VRMS|)*100%, where VRMS = RMS(CK_t voltage - CK_c voltage).
3) Only applies when both CK_t and CK_c are transitioning.

8.4 Differential Input Clock Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the Rx voltage sensitivity requirement. The system input swing to the DRAM must be larger than the DRAM Rx at the specified BER.

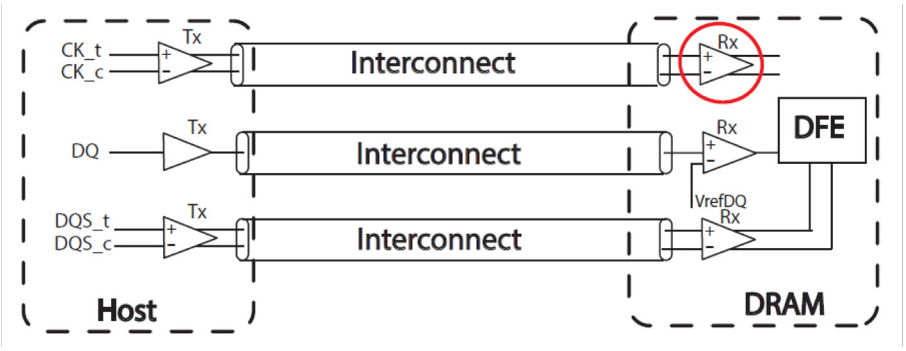


Figure 16. Example of DDR5 Memory Interconnect

8.4.1 Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

[Table 13] Differential Input Clock Voltage Sensitivity Parameter

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Note
		min	max	min	max	min	max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	180	-	180	-	160	mV	1,2

NOTE :
1) Refer to the minimum BER requirements for DDR5
2) The validation methodology is TBD

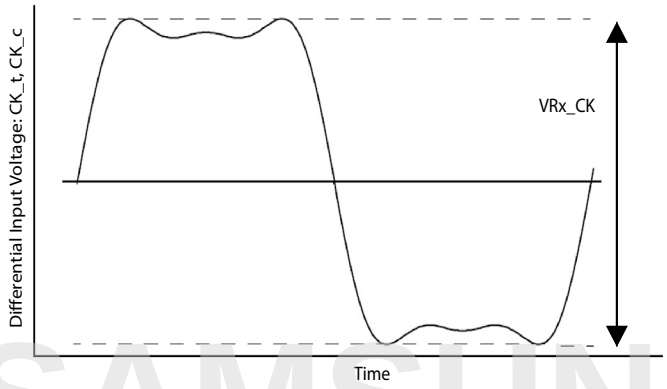


Figure 17. VRx_CK

8.4.2 Differential Input Voltage Levels for Clock

[Table 14] Differential Clock (CK_t, CK_c) Input Levels

From	Parameter	DDR5 4000 ~ 4800	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK_t, CK_c)	0.75 x Vdiffpk-pk	1,2
$V_{ILdiff}CK$	Differential input low measurement level (CK_t, CK_c)	0.25 x Vdiffpk-pk	1,2

NOTE :
1) Vdiffpk-pk defined in Figure 18.
2) Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples.
3) All parameters are defined over the entire clock common mode range.

8.4.3 Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below.

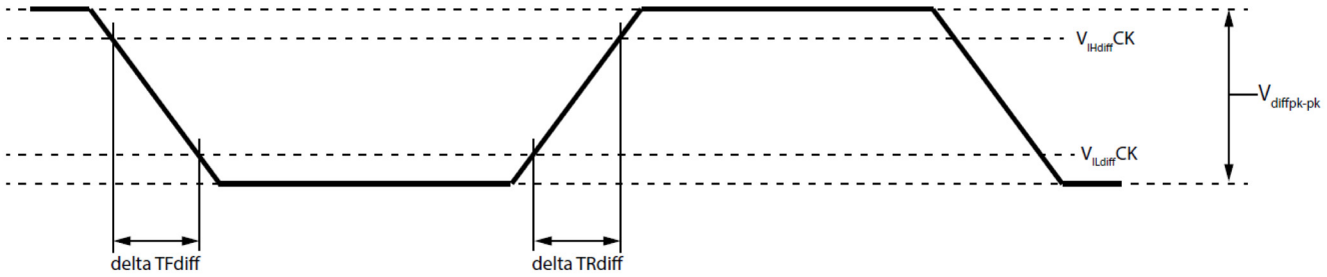


Figure 18. Differential Input Slew Rate Definition for CK_t, CK_c

[Table 15] Differential Input Slew Rate Definition for CK_t, CK_c

Parameter	Measured		Defined by	Note
	From	To		
Differential Input slew rate for rising edge (CK_t - CK_c)	$VIL_{diff}CK$	$VIH_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTRdiff	
Differential Input slew rate for falling edge (CK_t - CK_c)	$VIH_{diff}CK$	$VIL_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTFdiff	

[Table 16] Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Note
		min	max	min	max	min	max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	14	2	14	2	14	V/ns	

8.5 Rx DQS Jitter Sensitivity

The receiver DQS jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/ or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no cross-talk nor ISI is applied, and must pass through the combination of applied DCD and Rj.

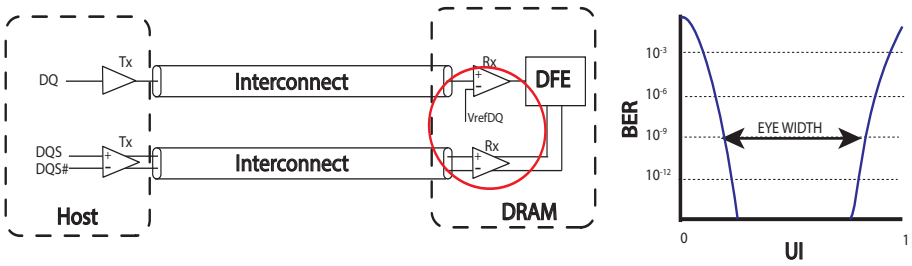


Figure 19. SDRAM's Rx Forwarded Strobes for Jitter Sensitivity Testing

8.5.1 Rx DQS Jitter Sensitivity Specification

The following table provides Rx DQS Jitter Sensitivity Specification for the DDR5 DRAM receivers when operating at various possible transfer rates. These parameters are tested on the CTC2 card without Rx Equalization set. Additive DFE Gain Bias can be set.

[Table 17] Rx DQS Jitter Sensitivity Specification

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Note
		min	max	min	max	min	max		
DQ Timing Width	tRx_DQ_tMargin	0.825	-	0.825	-	0.825	-	UI	1,2,3,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	ΔtRx_DQ_tMargin_ DQS_DCD	-	0.06	-	0.06	-	0.06	UI	1,4,8,9,10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	ΔtRx_DQ_tMargin_ DQS_Rj	-	0.09	-	0.09	-	0.09	UI	1,5,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	ΔtRx_DQ_tMargin_ DQS_DCD_Rj	-	0.15	-	0.15	-	0.15	UI	1,2,6,8,9,10
Delay of any data lane relative to the DQS_t DQS_c crossing	tRx_DQS2DQ	1	3	1	3.25	1	3.5	UI	1,7,8,9,10

NOTE :

1) Validation methodology will be defined in future JEDEC ballots. 2UI is defined as 1tCK for this parameter
2) Each of ?tRx_DQ_tMargin_DQS_DCD, ?tRx_DQ_tMargin_DQS_Rj, and ?tRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more
3) DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9
4) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 "1s" and 3 "0s"
5) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing
6) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing
7) Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx
8) All measurements at BER=E-9
9) This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing
10) The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test

8.5.2 Test Conditions for Rx DQS Jitter Sensitivity Tests

Table 17 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx DQS Jitter Sensitivity parameters specified in **Table 18**.

[Table 18] Test Conditions for Rx DQS Jitter Sensitivity Testing

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	-	0.045	UI	1,2,3,6,7,10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	1,2,4,6,8,10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	UI	1,2,5,6,7,9,10

NOTE :
1) While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2) The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin
3) Various DCD values should be tested, complying within the maximum limits
4) Various Rj values should be tested, complying within the maximum limits
5) Various combinations of DCD and Rj should be tested, complying within the maximum limits.The maximum timing margin degradation as a result of these injected jitter is specified in a separate table
6) Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7) Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)
8) RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
9) Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
10) The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

8.6 Rx DQS Voltage Sensitivity

8.6.1 Overview

The receiver DQS (strobe) input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

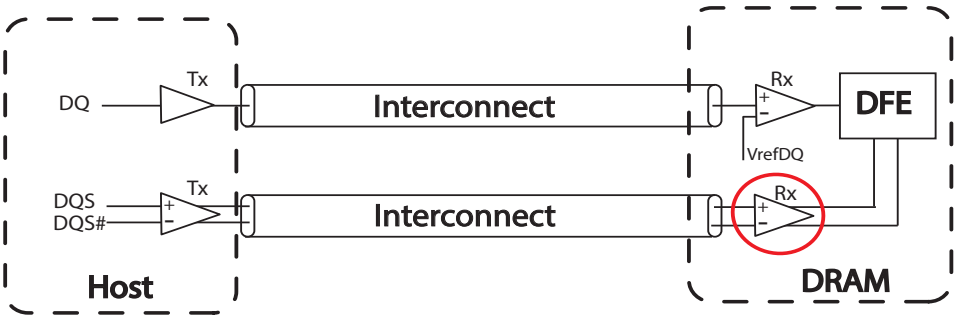


Figure 20. Example of DDR5 Memory Interconnect

8.6.2 Receiver DQS Voltage Sensitivity Parameter

Input differential (DQS_t, DQS_c) VRx_DQS is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

[Table 19] Rx DQS Input Voltage Sensitivity Parameter

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	105	-	100	-	100	mV	1,2,3

NOTE :
1) Refer to the minimum BER requirements for DDR5
2) The validation methodology for this parameter will be covered in future JEDEC ballot(s)
3) Test using clock like pattern of repeating 3 "1s" and 3 "0s"

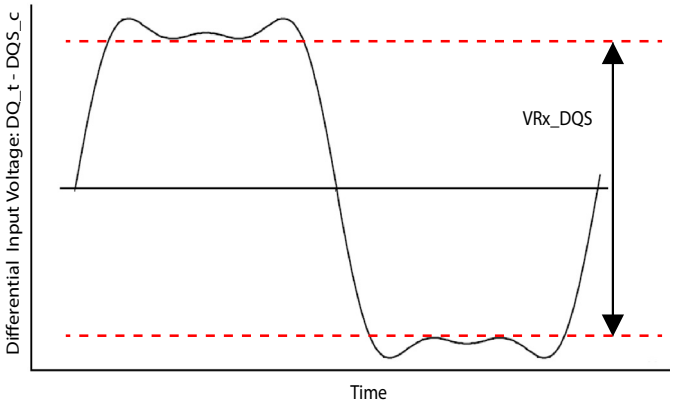


Figure 21. VRx_DQS

8.7 Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (VIX)

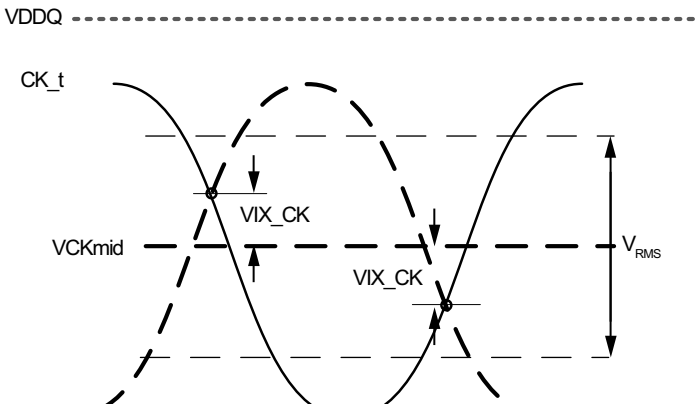


Figure 22. VIX Definition (DQS)

[Table 20] Crosspoint Voltage (VIX) for DQS Differential Input Signals

Parameter	Symbol	DDR5-4000 to4800		Unit	Notes
		Min	Max		
DQS differential input crosspoint voltage ratio	VIX_DQS_Ratio	-	50	%	1,2,3

NOTE :
1) The VIX_DQS voltage is referenced to VDQSmid(mean) = (DQS_t voltage + DQS_c voltage) /2, where the mean is over 8 UI
2) VIX_DQS_Ratio = (|VIX_DQS| / |V_{RMS}|)*100%, where V_{RMS} = RMS(DQS_t voltage - DQS_c voltage)
3) Only applies when both DQS_t and DQS_c are transitioning (including preamble)

8.8 Rx DQ Voltage Sensitivity

8.8.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

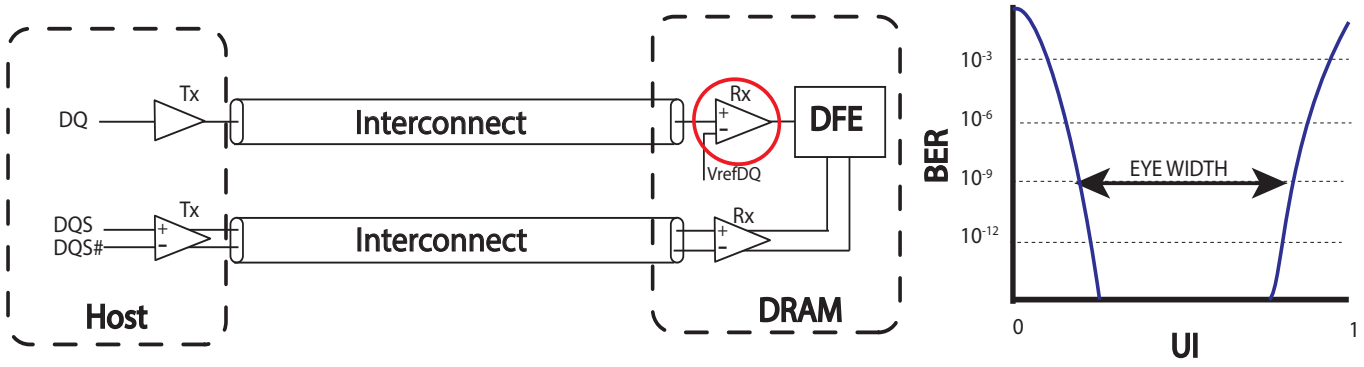


Figure 23. Example of DDR5 Memory Interconnect

8.8.2 Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended VRx_DQ is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

[Table 21] Rx DQ Input Voltage Sensitivity Parameters

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	70	-	65	-	65	mV	1,2,3

NOTE :
1) Refer to the minimum BER requirements for DDR5
2) The validation methodology for this parameter will be covered in future JEDEC ballot(s)
3) Recommend testing using clock like pattern such as repeating 3 "1s" and 3 "0s"

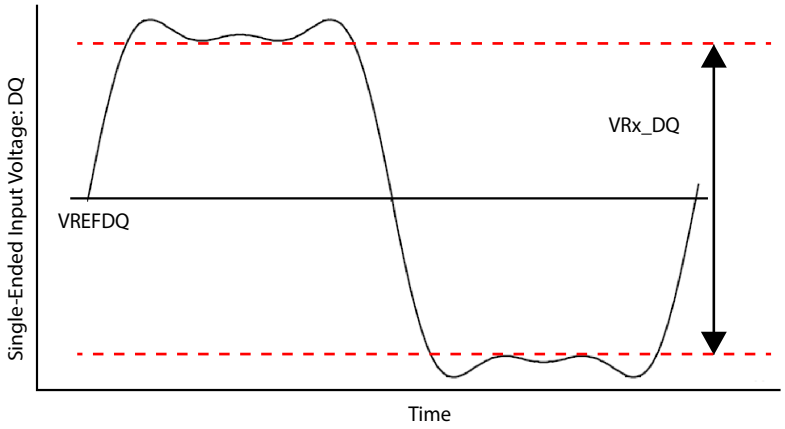


Figure 24. VRx_DQ

8.8.3 Differential Input Levels for DQS

[Table 22] Differential Input Levels for DQS (DQS_t, DQS_c)

From	Parameter	DDR5 4000 to 4800	Note
$V_{IHdiff}DQS$	Differential input high measurement level (DQS_t, DQS_c)	0.75 x $V_{diffpk-pk}$	1,2,3
$V_{ILdiff}DQS$	Differential input low measurement level (DQS_t, DQS_c)	0.25 x $V_{diffpk-pk}$	1,2,3

NOTE :
1) Vdiffpk-pk defined in **Table 15**
2) Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
3) All parameters are defined over the entire clock common mode range

8.8.4 Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals are defined and measured as shown below.

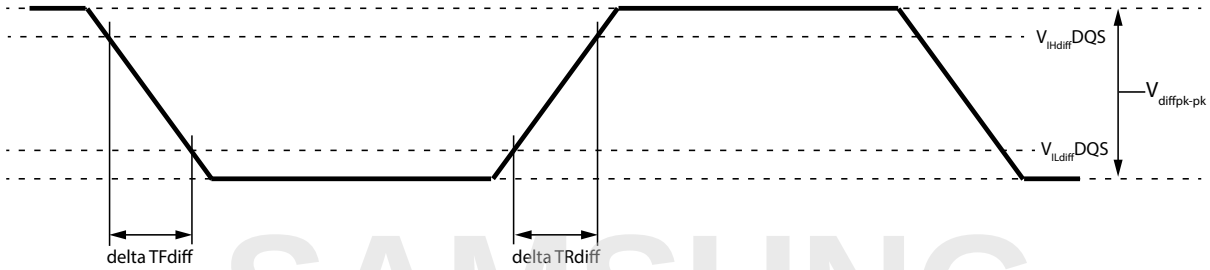


Figure 25. Differential Input Slew Rate Definition for DQS_t, DQS_c

[Table 23] Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (DQS_t, DQS_c)	$V_{ILdiff}DQS$	$V_{IHdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) / deltaTRdiff	
Differential Input slew rate for falling edge (DQS_t, DQS_c)	$V_{IHdiff}DQS$	$V_{ILdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) / deltaTFdiff	

[Table 24] Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	TBD	TBD	TBD	TBD	TBD	TBD	V/ns	1

NOTE :
1) Only applies when both DQS_t and DQS_c are transitioning.

8.9 Rx Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

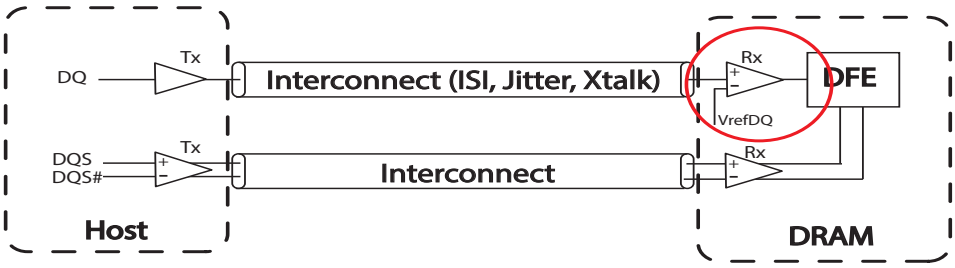


Figure 26. Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

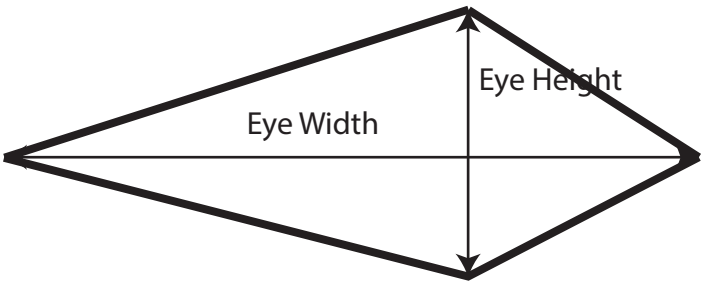


Figure 27. Example of Rx Stressed Eye Height and Eye Width

8.9.1 Parameters for DDR5 Rx Stressed Eye Tests

[Table 25] Test Conditions for Rx S3tressed Eye Tests

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	80	-	75	-	70	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.25	-	0.25	-	0.25	UI	1,2,3,4,5,6,7,8,9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	mV	1.2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.45	UI p-p	1,2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	mV p-p	1,2

NOTE :

1) Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E-^{16}.
2) These parameters are applied on the defined golden reference channel with parameters TBD.
3) DFE Tap 1-4 Bias settings that give the best eye margin are used and referring to Table 132, Min/Max Ranges for the DFE Tap Coefficients. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV) after the tap multiflier is applied.
4) Evaluated with no DC supply voltage drift.
5) Evaluated with no temperature drift.
6) Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions.
7) The stressed eye is to be assumed to have a diamond shape.
8) The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.
9) The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.
10) The Rx stressed eye spec applies at DDR5-2933 and faster data rates.

8.10 Connectivity Test Mode - Input level and Timing Requirement

During CT Mode, input levels are defined below.
TEN pin: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ
CS_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
Test Input pins: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
RESET_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR5 memory device will enter into the CT mode after time tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on, after RESET_n has de-asserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting clocks (CK_t, CK_c).

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR5 memory device are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

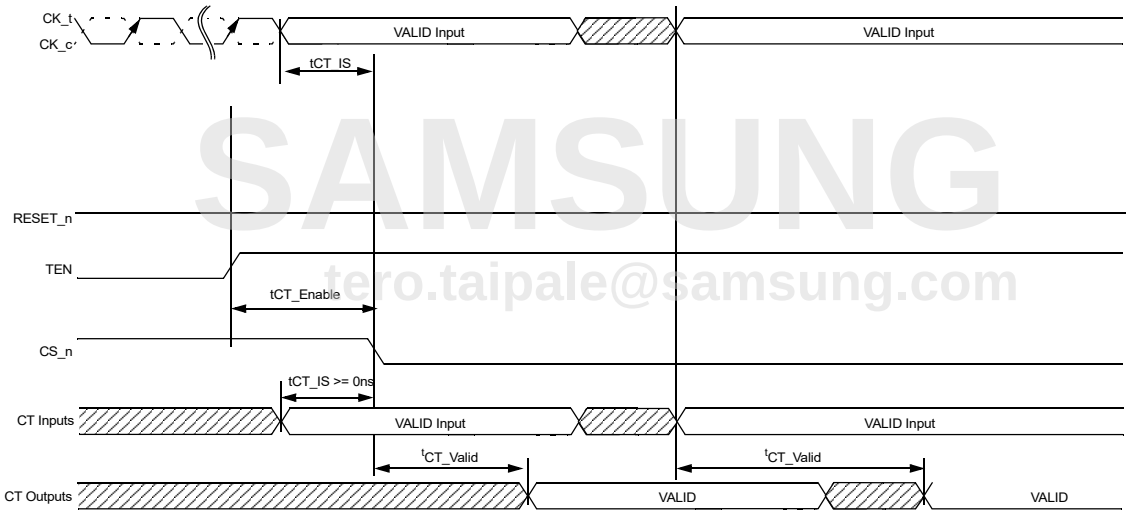


Figure 28. Timing Diagram for Connectivity Test (CT) Mode

[Table 26] AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

8.10.1 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR5 SDRAM Input Signals during Connectivity Test Mode.

[Table 27] CMOS rail to rail Input Levels for TEN, CS_n and Test inputs

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDDQ	VDDQ	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDDQ	VDDQ	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDDQ	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDDQ	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

NOTE :
1) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings
2) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

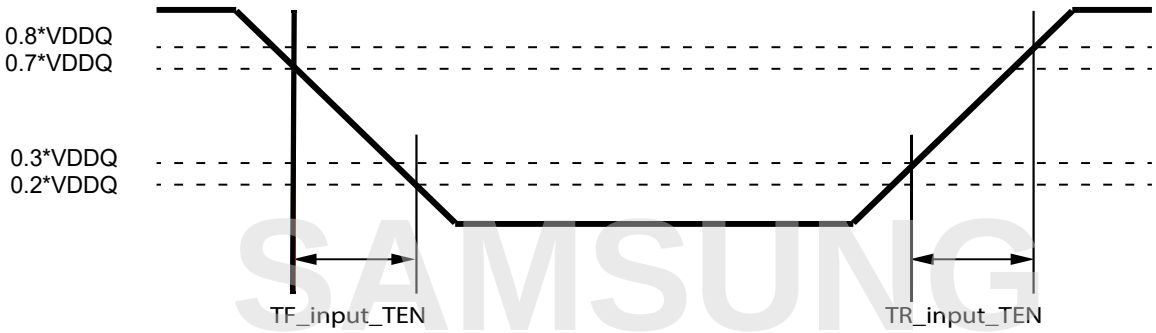


Figure 29. TEN Input Slew Rate Definition

8.10.2 CMOS rail to rail Input Levels for RESET_n

[Table 28] CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDDQ	VDDQ	V	5
DC Input High Voltage	VIH(DC)_RESET	0.7*VDDQ	VDDQ	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDDQ	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDDQ	V	6
Rising time	TR_RESET	-	1.0	us	
RESET pulse width	tPW_RESET	1.0	-	us	3,4

NOTE :
1) After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset
2) Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW
3) RESET is destructive to data contents
4) This definition is applied only for “Reset Procedure at Power Stable”
5) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings
6) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

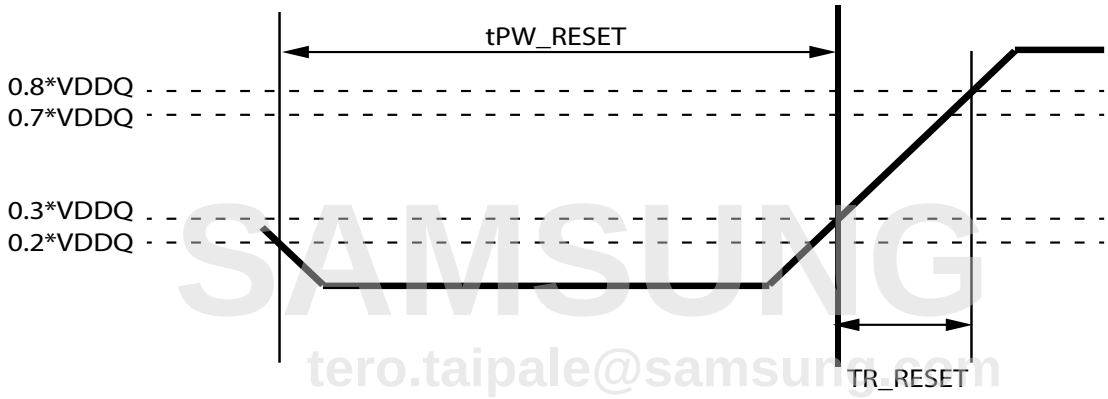


Figure 30. RESET_n Input Slew Rate Definition

9.0 AC & DC Output Measurement Levels and Timing

9.1 Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below.

Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows
:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

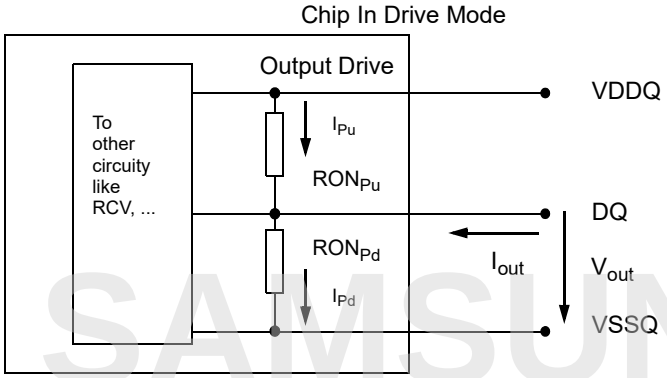


Figure 31. Output Driver Impedance Ron

[Table 29] Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	0		10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	0		10	%	1,2,4

NOTE :

1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;Ronnom is the nominal Ron value.

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4) RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5) This parameter of x16 device is specified for Upper byte and Lower byte.

9.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

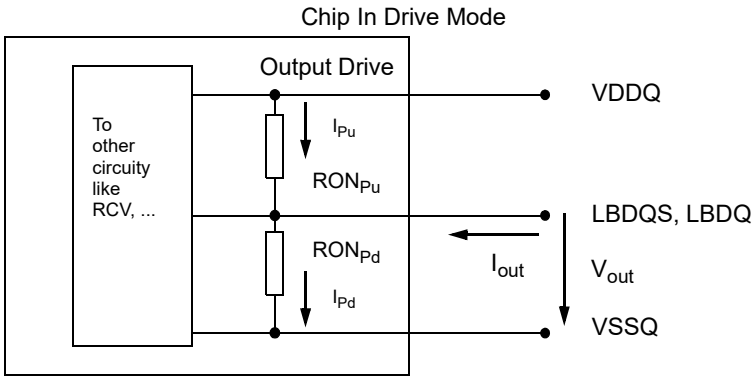


Figure 32. Output Driver for Loopback Signals

[Table 30] Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch LBDQS-LBDQ within device variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch LBDQS-LBDQ within device variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD) .
2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;Ronnom is the nominal Ron value.

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4) RON variance range ratio to RON Nominal value in a given component, including LBDQS and LBDQ.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

9.3 Loopback Output Timing

Loopback strobe LBDQS to Loopback data LBDQ relationship is illustrated in Figure 33.

- tLBQSH describes the single-ended LBDQS strobe high pulse width.
- tLBQSL describes the single-ended LBDQS strobe low pulse width.
- tLBDQSQ describes the latest valid transition of LBDQ measured at both rising and falling edges of LBDQS.
- tLBQH describes the earliest invalid transition of LBDQ measured at both rising and falling edges of LBDQS.
- tLBDVW describes the data valid window per device per UI and is derived from (tLBQH-tLBDQSQ) of each UI on a given DRAM.

[Table 31] Loopback Output Timing Parameters

Speed		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	0.2	-	0.2	-	0.2	-	tCK/2	1
Loopback LBDQ Output Time from LBDQS	tLBQH	3.6	-	3.6	-	3.6	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	3.4	-	3.4	-	3.4	-	tCK/2	1

NOTE :
1) Based on Loopback 4-way interleave setting (see MR53).

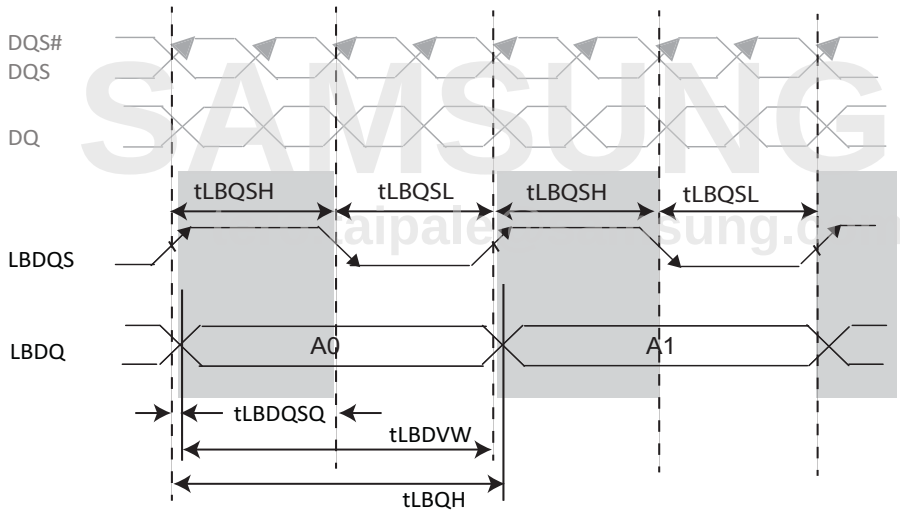


Figure 33. Loopback Strobe to Data Relationship

9.3.1 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |}$$ under the condition that RON_{Pu} is off

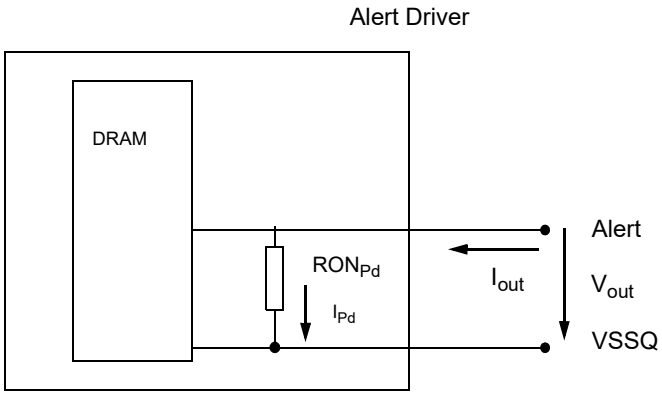


Figure 34. Alert Driver

Resistor	Vout	Min	Max	Unit	Notes
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.1	$R_{ZQ}/7$	
	V_{OMdc} = 0.8* VDDQ	0.4	1.1	$R_{ZQ}/7$	
	V_{OHdc} = 0.95* VDDQ	0.4	1.25	$R_{ZQ}/7$	

9.3.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied to the Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

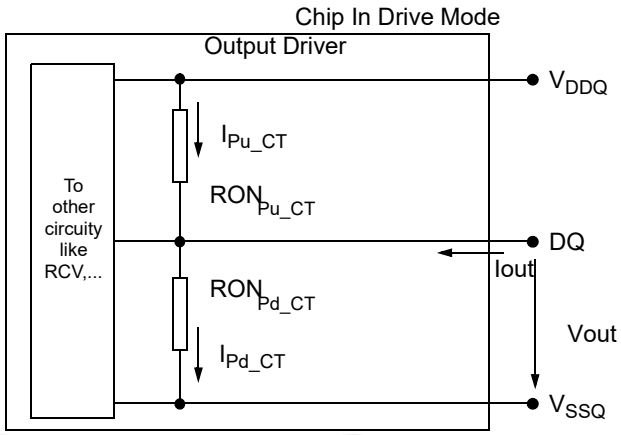


Figure 35. Output Driver

RONNOM_CT	Resistor	Vout	Max	Units	NOTE
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2
	RONPu_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2

NOTE :
1) Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.
2) Uncalibrated drive strength tolerance is specified at +/- 30%.

9.4 Single-ended Output Levels - VOL/VOH

[Table 32] Single-ended Output levels

Symbol	Parameter	DDR5-4000 to 4800	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

NOTE:
1) $V_{pk-pk}$is the mean high voltage minus the mean low voltage over TBD samples.

9.5 Single-Ended Output Levels - VOL/VOH for Loopback Signals

[Table 33] Single-ended Output levels for Loopback Signals

Symbol	Parameter	DDR5-4000 to 4800	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

NOTE :
1) $V_{pk-pk}$is the mean high voltage minus the mean low voltage over TBD samples.

9.6 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single ended signals as shown in Table 34 and Figure 36.

[Table 34] Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}	V_{OH}	[V_{OH}-V_{OL}] / delta TRse
Single ended output slew rate for falling edge	V_{OH}	V_{OL}	[V_{OH}-V_{OL}] / delta TFse

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test

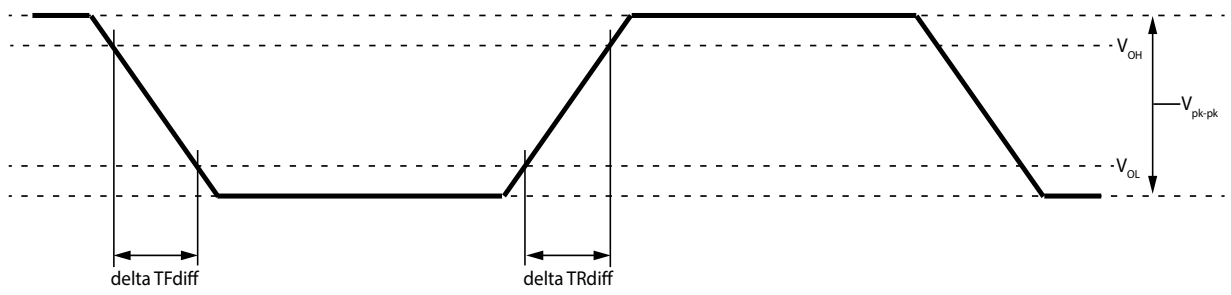


Figure 36. Single-ended Output Slew Rate Definition

[Table 35] Single-ended Output Slew Rate

Speed		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	8	24	8	24	8	24	V/ns	

9.7 Differential Output Levels

[Table 36] Differential Output levels

Symbol	Parameter	DDR5-4000 to 4800	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1

NOTE :
1) $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples.

9.8 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OLdiff} and V_{OHdiff} for differential signals as shown in Table 37 and Figure 37.

[Table 37] Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}	V_{OHdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}	V_{OLdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TFdiff

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

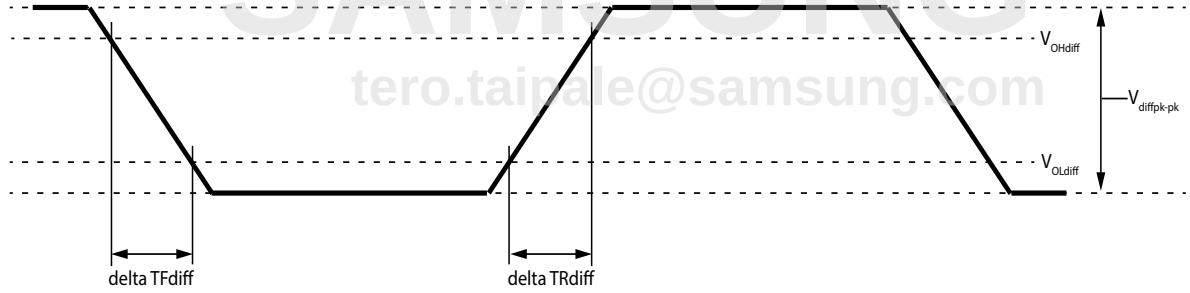


Figure 37. Differential Output Slew Rate Definition

[Table 38] Differential Output Slew Rate

Speed		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	16	48	16	48	16	48	V/ns	

9.9 Tx DQS Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 39.

[Table 39] Tx DQS Jitter Parameters
[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,4, 5,6,7,8,9, 10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	UI	1,2,3,5,6,7,8,9, 10,11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,5,6,7,8,9, 10,11,12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	UI	1,2,3,5,6,7,8,9, 10,11

NOTE :
1) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated.
When there is no socket in transmitter measurement setup, in many cases,
The contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns.
When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant.
To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC),
While the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching.
Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup,
In many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns.
When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant.
To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC),
While the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching.
Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
3) The validation methodology for these parameters will be covered in future ballots.
4) Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.
5) See Section 7.2 for details on the minimum BER requirements.
6) See Section 7.3 for details on UI, NUI and Jitter definitions.
7) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test.
8) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44, and the Mode Registers for the Per Pin DCA of DQS are MR103 - MR110.
9) Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test.
10) These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands.
The MR25 OP[3] is set to “1” to enable this feature.
11) Tested on the CTC2 card only.

9.10 Tx DQ Jitter

9.10.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 40.

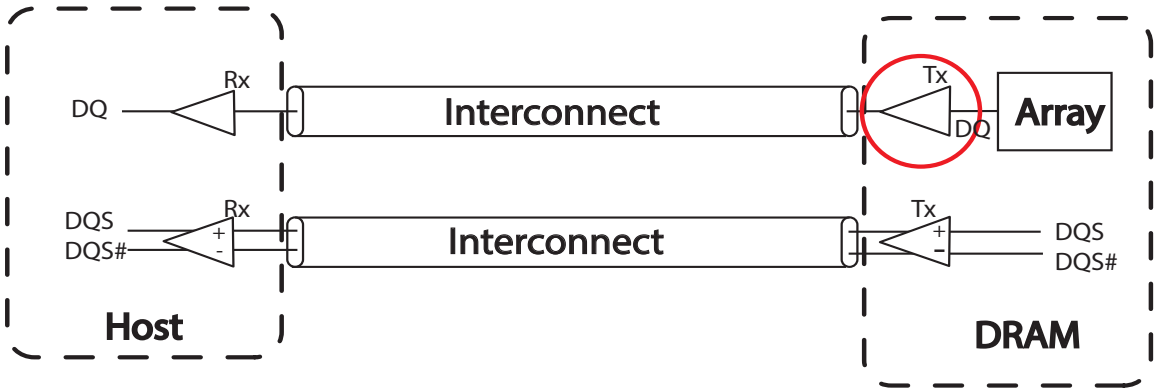


Figure 38. Tx DQ Jitter

9.10.2 Tx DQ Jitter Parameters

[Table 40] Tx DQ Jitter Parameters

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,3,4,5,7,8,9,10, 11, 12,13,14
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	UI	3,5,7,8,9,10, 11,12,13
Rj RMS of N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	3,5,7,8,9,10 ,11,12,13,14
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	UI	3,6,7,8,9,10, 11,12,13
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	-0.100	0.100	UI	3,5,6,7,9,10, 11,12,13

NOTE :

1) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
3) The validation methodology for these parameters will be covered in future JEDEC ballots
4) Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.
5) Delay of any data lane relative to strobe lane, as measured at Tx output.
6) Vref noise level to DQ jitter should be adjusted to minimize DCD.
7) See Section 7 for details on the minimum BER requirements.
8) See Section 7 for details on UI, NUI and Jitter definitions.
9) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using.
10) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44.
11) Spread Spectrum Clocking (SSC) must be disabled while running this test.
12) These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
13) Tested on the CTC2 card only.
14) The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6mUI RMS.

9.11 Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E^{-9} and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40 OP[3:0]).

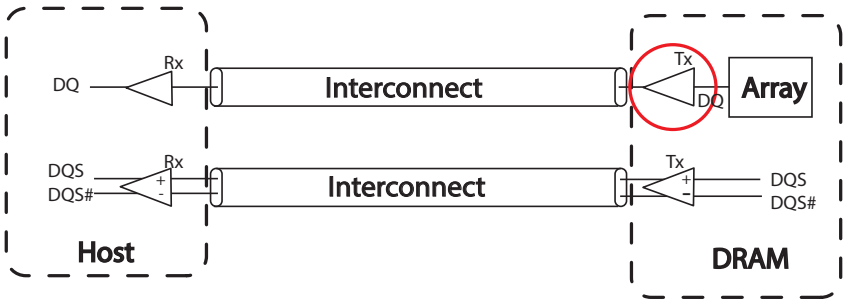


Figure 39. Example of DDR5 Memory Interconnect

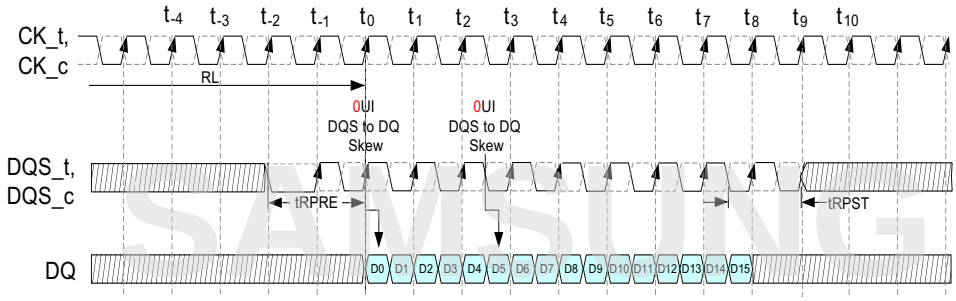


Figure 40. Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 0 UI skew

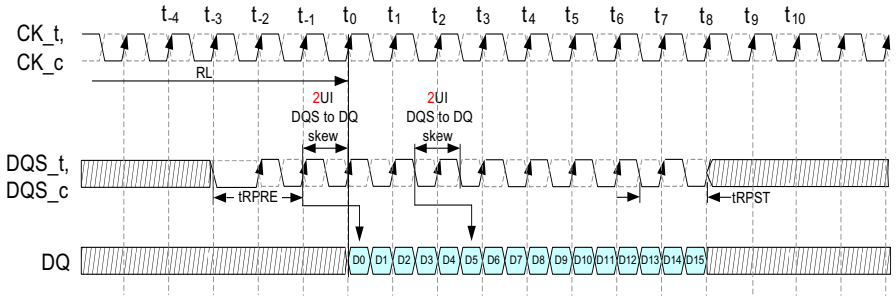


Figure 41. Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 2 UI skew with Read DQS Offset Timing set to 1 Clock (2UI)

9.11.1 Tx DQ Stressed Eye Parameters

[Table 41] Tx DQ Stressed Eye Parameters

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Parameter	Symbol	DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Eye Height specified at the transmitter with a skew between DQ and DQS of 1UI	TxEH_DQ_SES_1UI	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.72	-	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 2UI	TxEH_DQ_SES_2UI	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.72	-	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 3UI	TxEH_DQ_SES_3UI	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.72	-	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 4UI	TxEH_DQ_SES_4UI	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,5,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	TBD	-	TBD	-	TBD	-	UI	1,2,3,4,5,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 5UI	TxEH_DQ_SES_5UI	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,5,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	TxEW_DQ_SES_5UI	TBD	-	TBD	-	TBD	-	UI	1,2,3,4,5,6,7,8,9,10

NOTE :

1) Minimum BER E^{-9} and Confidence Level of 99.5% per pin.
2) Refer to the minimum Bit Error Rate (BER) requirements for DDR5.
3) The validation methodology for these parameters will be covered in future JEDEC ballot(s).
4) Mismatch is defined as DQS to DQ mismatch, in UI increments.
5) The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable.
6) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Duty Cycle Adjuster feature prior to running this test.
7) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where 0≤x≤7, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where 0≤y≤7.
8) Spread Spectrum Clocking (SSC) must be disabled while running this test.
9) These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.
10) Tested on the CTC2 card only.
11) Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye.

10.0 Speed Bins

[Table 42] DDR5-4000 Speed Bins and Operations

Speed Bin					DDR5-4000		Unit	NOTE
CL-nRCD-nRP					32-32-32			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL			nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36		nCK	

[Table 43] DDR5-4400 Speed Bins and Operations

Speed Bin					DDR5-4400		Unit	NOTE
CL-nRCD-nRP					36-36-36			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL			nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRP-min (ns)[5]	Read CL[12]	Supported Frequency Down Bins				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36,40		nCK	

[Table 44] DDR5-4800 Speed Bins and Operations

Speed Bin					DDR5-4800		Unit	NOTE
CL-nRCD-nRP					40-39-39			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL			nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRP-min (ns)[5]	Read CL[12]	Supported Frequency Down Bins				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED		ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36, 40,42		nCK	

NOTE :

1) Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2) The translation of all timing parameters from ns values to nCK values shall follow the Rounding Algorithm. The translation of tAA to CL shall follow the explicit combinations listed in the Speed Bin Tables.
3) The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When selecting tCK(avg), requirements from the CL setting as well as requirements from the CWL setting shall be fulfilled.
4) 'Reserved' settings are not allowed. The user shall program a different value.
5) This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm, depending on the specific speed bin and down clock frequency combination.
6) DDR5-3200 AC timings apply if the DRAM operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7) Parameters apply from tCK(avg)min to tCK(avg)max.
8) tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithms, nRC(min) shall always be greater than or equal to nRAS(min) + nRP(min).
9) tCK(avg).max of 1.010 ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
10) Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC standard. The JEDEC standard does not require support for all speed bins within a given speed. The JEDEC standard requires meeting the parameters for a least one of the listed speed bins.
11) Any speed bin also supports functional operation at slower frequencies as shown in the table which are not subject to Production Tests but are verified by Design/Characterization.
12) The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the Speed Bin Tables. The CL Algorithm calculates supported CAS Latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting tCK(AVG)min, and the bin target timings, the CL Algorithm then uses the Rounding Algorithm to calculate the valid CAS Latency. Because the DDR5 SDRAM specification only supports even CAS Latencies, odd CAS Latencies are rounded up to the next even CAS Latency. The 1980-2100 MT/s data rate always uses CL22. If tAA(corrected) or tRCDtRP(corrected) are violated, the CL Algorithm uses a slower combination of tAA(target) and tRCDtRP(target) to return slower valid CAS Latencies. The DDR5 SDRAM can support up to four valid CAS Latencies, CL(AN), CL(B), CL(BN), and CL(C), for a given frequency. tAA(corrected) and tRCDtRP(corrected) are calculated by reducing tAA(min), tRCD(min), and tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin Tables, or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information.

11.0 IDD, IDDQ and IPP Specification Parameters and Test Conditions

11.1 IDD, IDDQ and IPP Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. **Figure 42** shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, IDD8, IDDQ8, IPP8 and IDD9, IDDQ9, IPP9) are measured as time-averaged currents with all VDD balls of the DDR5 SDRAM under test tied together. Any IDDQ or IPP current is not included in IDD currents.
- IDDQ currents are measured as time-averaged currents with all VDDQ balls of the DDR5 SDRAM under test tied together. Any IDD or IPP current is not included in IDDQ currents.
- IPP currents are measured as time-averaged currents with all VPP balls of the DDR5 SDRAM under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in **Figure 43**.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = 0.75 * VDDQ.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in **Table 46**.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in **Table 45**.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in **Table 46** through **Table 55**.
- IDD Measurements are done after properly initializing and training the DDR5 SDRAM. This includes but is not limited to setting TDQS_t disabled in MR5; CRC disabled in MR50; DM disabled in MR5; 1N mode enabled and set CS assertion duration (MR2:OP[4]) as 1B in MR2, unless otherwise specified in the IDD, IDDQ and IPP patterns’ conditions definitions;

Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD, IDDQ or IPP measurement is started, with the exception of IDD9 which can be measured any time after the DRAM has entered MBIST mode.

- TCASE defined as 0 - 95°C, unless stated in the specific condition definition table below.
- For all IDD, IDDQ and IPP measurement loop timing parameters, refer to the timing parameters defined in the spec to calculate the nCK required.

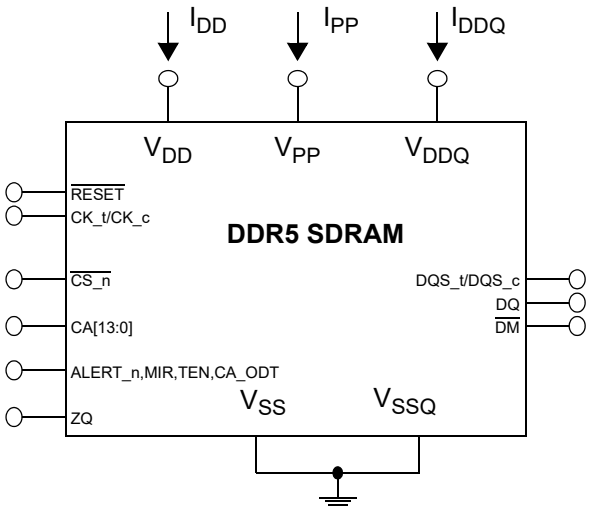


Figure 42. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

NOTE :
1) DIMM level Output test load condition may be different from above

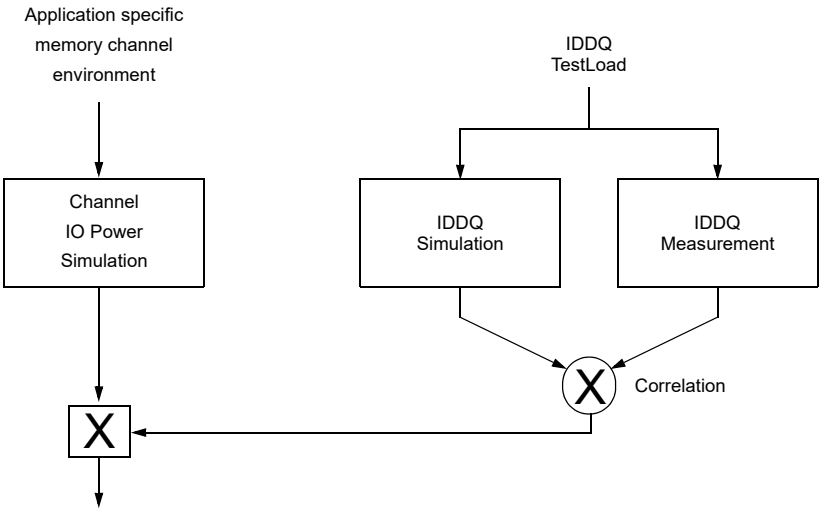


Figure 43. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

[Table 45] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current External clock: On; tCK, nRC, nRAS, nRP, nRRD: see Table 46; BL: 161; CS_n: High between ACT and PRE; CA Inputs: partially toggling according to Table 46; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 46); Output Buffer and RTT: Enabled in Mode Registers2; Pattern Details: see Table 46
IDDQ0	Operating One Bank Active-Precharge IDDQ Current Same condition with IDD0, however measuring IDDQ current instead of IDD current
IPP0	Operating One Bank Active-Precharge IPP Current Same condition with IDD0, however measuring IPP current instead of IDD current
IDD0F	Operating Four Bank Active-Precharge Current External clock: On; tCK, nRC, nRAS, nRP, nRRD: see Table 46; BL: 161; CS_n: High between ACT and PRE; CA Inputs: partially toggling according to Table 47; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with four bank active at a time: (see Table 47); Output Buffer and RTT: Enabled in Mode Registers2; Pattern Details: see Table 47
IDDQ0F	Operating Four Bank Active-Precharge IDDQ Current Same condition with IDD0F, however measuring IDDQ current instead of IDD current
IPP0F	Operating Four Bank Active-Precharge IPP Current Same condition with IDD0F, however measuring IPP current instead of IDD current
IDD2N	Precharge Standby Current External clock: On; tCK: see Table 48; CS_n: stable at 1; CA Inputs: partially toggling according to Table 46; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; Pattern Details: see Table 48
IDDQ2N	Precharge Standby IDDQ Current Same condition with IDD2N, however measuring IDDQ current instead of IDD current
IPP2N	Precharge Standby IPP Current Same condition with IDD2N, however measuring IPP current instead of IDD current
IDD2NT	Precharge Standby Non-Target Command Current External clock: On; tCK: see Table 46; BL: 161; CS_n: High between WRITE commands; CS_n, CA Inputs: partially toggling according to Table 49; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; Pattern Details: see Table 49
IDDQ2NT (Optional)	Precharge Standby Non-Target Command IDDQ Current Same condition with IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NT (Optional)	Precharge Standby Non-Target Command IPP Current Same condition with IDD2NT, however measuring IPP current instead of IDD current
IDD2P	Precharge Power-Down Device in Precharge Power-Down, External clock: On; tCK: see Table 46; CS_n: stable at 1 after Power Down Entry command; CA Inputs: stable at 1; CA11=H during the PDE command; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2;
IDDQ2P	Precharge Power-Down Same condition with IDD2P, however measuring IDDQ current instead of IDD current
IPP2P	Precharge Power-Down Same condition with IDD2P, however measuring IPP current instead of IDD current
IDD3N	Active Standby Current External clock: On; tCK: see Table 46; CS_n: stable at 1; CA Inputs: partially toggling according to Table 48; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; Pattern Details: see Table 48
IDDQ3N	Active Standby IDDQ Current Same condition with IDD3N, however measuring IDDQ current instead of IDD current
IPP3N	Active Standby IPP Current Same condition with IDD3N, however measuring IPP current instead of IDD current

Symbol	Description
IDD3P	Active Power-Down Current Device in Active Power-Down, External clock: On; tCK: see Table 46; CS_n: stable at 1 after Power Down Entry command; CA Inputs: stable at 1; CA11=H during the PDE command; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2;
IDDQ3P	Active Power-Down IDDQ Current Same condition with IDD3P, however measuring IDDQ current instead of IDD current
IPP3P	**Active Power-Down IPP Current** Same condition with IDD3P, however measuring IPP current instead of IDD current
IDD4R	**Operating Burst Read Current** External clock: On; tCK, nCCD, CL: see **Table 46**; BL: 16[1]; CS_n: High between RD; CA Inputs: partially toggling according to **Table 48**; Data IO: seamless read data burst with different data between one burst and the next one according to **Table 48**; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see **Table 48**); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see **Table 48**
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	**Operating Burst Read IPP Current** Same condition with IDD4R, however measuring IPP current instead of IDD current
IDD4W	**Operating Burst Write Current** External clock: On; tCK, nCCD, CL: see **Table 46**; BL: 16[1]; CS_n: High between WR; CA Inputs: partially toggling according to **Table 51**; Data IO: seamless write data burst with different data between one burst and the next one according to **Table 51**; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see **Table 51**); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see **Table 51**
IDD4WC	**Operating Burst Write Current with Write CRC** Write CRC enabled[3], Other conditions: see IDD4W
IDDQ4W	**Operating Burst Write IDDQ Current** Same condition with IDD4W, however measuring IDDQ current instead of IDD current
IPP4W	**Operating Burst Write IPP Current** Same condition with IDD4W, however measuring IPP current instead of IDD current
IDD5B	**Burst Refresh Current (Normal Refresh Mode)** External clock: On; tCK, nRFC1: see **Table 46**; BL: 16[1]; CS_n: High between REF; CA Inputs: partially toggling according to **Table 51**; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC1 (see **Table 51**); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see **Table 51**
IDDQ5B	**Burst Refresh IDDQ Current (Normal Refresh Mode)** Same condition with IDD5B, however measuring IDDQ current instead of IDD current
IPP5B	**Burst Refresh IPP Current (Normal Refresh Mode)** Same condition with IDD5B, however measuring IPP current instead of IDD current
IDD5F	**Burst Refresh Current (Fine Granularity Refresh Mode)** tRFC=tRFC2, Other conditions: see IDD5B
IDDQ5F	**Burst Refresh IDDQPP Current (Fine Granularity Refresh Mode)** Same condition with IDD5F, however measuring IDDQ current instead of IDD current
IPP5F	**Burst Refresh IPP Current (Fine Granularity Refresh Mode)** Same condition with IDD5F, however measuring IPP current instead of IDD current
IDD5C	**Burst Refresh Current (Same Bank Refresh Mode)** External clock: On; tCK, nRFCsb: see **Table 46**; BL: 16₁; CS_n: High between REF; CA Inputs: partially toggling according to **Table 53**; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFCsb (see **Table 53**); Output Buffer and RTT: Enabled in Mode Registers₂; Pattern Details: see **Table 53**
IDDQ5C	**Burst Refresh Write IPP Current (Same Bank Refresh Mode)** Same condition with IDD5C, however measuring IDDQ current instead of IDD current
IPP5C	**Burst Refresh Write IPP Current (Same Bank Refresh Mode)** Same condition with IDD5C, however measuring IPP current instead of IDD current

Symbol	Description
IDD6N	**Self Refresh Current: Normal Temperature Range** TCASE: 0 - 85°C; External clock: Off; CK_t and CK_c#: HIGH; tCK, nCPDED: see **Table 46**; BL: 16[1]; CS_n#: low; CA, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: All ODT disabled in MR32-MR35;
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** Same condition with IDD6N, however measuring IPP current instead of IDD current
IDD6E	**SelfRefresh Current: Extended Temperature Range** T_{CASE}: 85 - 95°C; Extended[4]; External clock: Off; CK_t and CK_c: HIGH; tCK, nCPDED: see **Table 46**; BL: 16[1]; CS_n: low; CA, Data IO: High; DM_n:stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** Same condition with IDD6E, however measuring IPP current instead of IDD current
IDD7	**Operating Bank Interleave Read Current** External clock: On; tCK, nRC, nRAS, nRCD, nRRD_S, nFAW, tCCD_S CL: see **Table 46**; BL: 16[1]; CS_n: High between ACT and RDA; CA Inputs: partially toggling according to **Table 55**; Data IO: read data bursts with different data between one burst and the next one according to **Table 55**; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see **Table 55**; Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see **Table 55**
IDDQ7	**Operating Bank Interleave Read IDDQ Current** Same condition with IDD7, however measuring IDDQ current instead of IDD current
IPP7	**Operating Bank Interleave Read IPP Current** Same condition with IDD7, however measuring IPP current instead of IDD current
IDD8	**Maximum Power Saving Deep Power Down Current** External clock: Off; CK_t and CK_c#: HIGH; tCK, nCPDED: see **Table 46**; BL: 16[1]; CS_n#: low; CA:High, DM_n: stable at 1; Bank Activity: All banks closed and device in MPSM deep power down mode5; Output Buffer and RTT: Enabled in Mode Registers[2]; Patterns Details: same as IDD6N but MPSM is enabled in mode register.
IDDQ8	**Maximum Power Saving Deep Power Down IDDQ Current** Same condition with IDD8, however measuring IDDQ current instead of IDD current
IPP8	**Maximum Power Saving Deep Power Down IPP Current** Same condition with IDD8, however measuring IPP current instead of IDD current

NOTE :

1) Burst Length: BL16 fixed by MR0 OP[1:0]=00.

2) Output Buffer Enable
- set MR5 OP[0] = 0] : Qoff = Output buffer enabled
- set MR5 OP[2:1] = 00] : Pull-Up Output Driver Impedance Control = RZQ/7
- set MR5 OP[7:6] = 00] : Pull-Down Output Driver Impedance Control = RZQ/7

RTT_Nom enable
- set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6

RTT_WR enable
- set MR34 OP[5:3] = 010 RTT_WR = RZQ/2 CA/CS/CK ODT, DQS_RTT_PART, and RTT_PARK disable
- set MR32 OP[5:0] = 000000
- set/MR33 OP[5:0] = 000000
- set MR34 OP[2:0] = 000

3) WRITE CRC enabled
- set MR50 OP[2:1] = 11

4) Read CRC enabled
- set MR50:OP[0]=1

5) MPSM Deep Power Down Mode
- set MR2:OP[3]=1 if PDA Enumerate ID not equal to 15
- set MR2:OP[5]=1 if PDA Enumerate ID equal to 15

11.2 IDD0, IDDQ0, IPP0 Pattern

Executes Active and PreCharge commands with tightest timing possible while exercising all Bank and Bank Group addresses. Note 2 applies to the entire table

[Table 46] IDD0, IDDQ0, IPP0

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H	-	0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling1					Repeat sequence to satisfy tRAS(min), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling1					Repeat sequence to satisfy tRP(min), truncate if required
	4	ACT	L H	-	0x03FFF	0x0	0x00	0x0	
	5	DES	H	Toggling1					Repeat sequence to satisfy tRAS(min), truncate if required
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling1					Repeat sequence to satisfy tRP(min), truncate if required
1	8-15	Repeat sub-loop 0, use BG[2:0]=0x1 instead							
2	16-23	Repeat sub-loop 0, use BG[2:0]=0x2 instead							
3	24-31	Repeat sub-loop 0, use BG[2:0]=0x3 instead							
4	32-39	Repeat sub-loop 0, use BG[2:0]=0x4 instead							skip for x16
5	40-47	Repeat sub-loop 0, use BG[2:0]=0x5 instead							skip for x16
6	48-55	Repeat sub-loop 0, use BG[2:0]=0x6 instead							skip for x16
7	56-63	Repeat sub-loop 0, use BG[2:0]=0x7 instead							skip for x16
8-15	64-127	Repeat sub loops 0-7, use BA[1:0]=0x1 instead							
16-23	128-191	Repeat sub loops 0-7, use BA[1:0]=0x2 instead							
24-31	192-255	Repeat sub loops 0-7, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

NOTE :

1) Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.

2) For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

11.3 IDD0F, IDDQ0F, IPP0F Pattern

Executes four Active and PreCharge commands per tRC time while exercising all Bank, Bank, Group and CID addresses. Notes 2 apply to entire table.

[Table 47] IDD0F, IDDQ0F, IPP0F

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H		0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	2	ACT	L H		0x00000	0x0	0x01	0x0	
	3	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	4	ACT	L H		0x00000	0x0	0x02	0x0	
	5	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	6	ACT	L H		0x00000	0x0	0x03	0x0	
	7	DES	H	Toggling1					Repeat to satisfy tRAS(min) from Sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	14	PREpb	L			0x0	0x03	0x0	
	15	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	16	DES	H	Toggling1					Repeat for tRC(min) from Sequence 0 first ACTIVATE. This will be zero DESELECTS for speed 4000Mbps and slower.
1	17-33	Repeat sub-loop 0, use Row Address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat sub-loop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							skip for x16
4-7	68-101	Repeat sub-loops 0-3, use BA[1:0]=0x1 instead							
8-11	102-135	Repeat sub-loops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat sub-loops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

NOTE :

1) Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2) For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

11.4 IDD2N, IDD2P, IDD3N, IDD3P Pattern

Executes DESELECT commands while exercising all command/address pins in a predefined pattern. All notes apply to entire table.

[Table 48] IDD2N, IDD2P, IDDQ2N, IDDQ2P, IPP2N, IPP2P, IDD3N, IDD3P, IDDQ3N, IDDQ3P, IPP3N, IPP3P

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x03FFF
2	DES	H	0x03FFF
3	DES	H	0x03FFF

NOTE :
1) Data is pulled to VDDQ.
2) DQS_t and DQS_c are pulled to VDDQ.
3) Command / Address ODT is disabled.
4) Repeat sequence 0 through 3.
5) All banks of all logical ranks mimic the same test condition.

11.5 IDD2NT, IDDQ2NT, IPP2NT Pattern

Executes Non-Target WRITE commands simulating Rank to Rank timing while exercising all C/A bits. Notes 3-6 apply to entire table.

[Table 49] IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Instructions
0	WRITE1	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling2	Repeat sequence to meet 1*tCCD_S(min), truncate if required
2	WRITE1	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling2	Repeat sequence to meet 1*tCCD(min), truncate if required

NOTE :
1) WRITE with CS_n=L on both cycles indicated a non-target WRITE.
2) Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
3) Time between Non-Target WRITEs reflect tCCD_S (min) for one ranks.4) DQ signals are VDDQ.
4) DQ signals are VDDQ.
5) DQS_t, DQS_c are VDDQ.
6) Repeat 0 through 3.

11.6 IDD4R, IDDQ4R, IPP4R Pattern

Executes READ commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-9 apply to entire table.

[Table 50] IDD4R, IDDQ4R, IPP4R

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	READ	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	READ	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	READ	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

NOTE :

1) Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2) READs performed with Auto Precharge = H, Burst Chop = H.
3) Row address is set to 0x0000.
4) Data reflects burst length of 16.
5) Data Pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF.
6) Data Pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0x0F, 0x0, 0xF, 0xF0, 0xF0, 0xF, 0x0F, 0x0, 0xF, 0x0, 0xF, 0x0.
7) Data Pattern for x8 each beat will reflect two like nibbles (Data Pattern A = 0x00, 0xFF, 0xFF...).
8) Data Pattern for x16 each beat will reflect two like bytes (Data Pattern A = 0x0000, 0xFFFF, 0xFFFF...).
9) Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.

11.7 IDD4W, IDDQ4W, IPP4W Pattern

Executes WRITE commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-6 apply to entire table.

[Table 51] IDD4W, IDDQ4W, IPP4W

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	WRITE	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	WRITE	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	WRITE	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2) WRITEs performed with Auto Precharge = H, Burst Chop = .
3) Row address is set to 0x0000.
4) Data reflects burst length of 16.
5) Refer to IDD4R measurement loop table for data pattern definition.
6) Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.

11.8 IDD5B, IDDQ5B and IPP5B Pattern

Executes Refresh (all Banks) commands at minimum tRFC1. Notes 3-6 apply to entire table.

[Table 52] IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sequence	Command	CS	C/A [13:0]	CA8	CID [2:0]	Special Instructions
0	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
1	DES	H	Toggling1	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
2	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
3	DES	H	Toggling1	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2) For IDD5B, use tRFC1(min). For IDD5F, use tRFC2(min).
3) DQ signals are VDDQ.
4) All banks of all “non-target” logical ranks are Idd2N condition
5) Where C/A[13:0] column is not populated, refer to command truth table, CA8, and CID columns for the C/A state.
6) Must set CA8=H on REFab commands to indicate 1X refresh rate on devices that support RIR.

11.9 IDD5C, IDDQ5C and IPP5C Pattern

Executes Refresh (Same Bank) command at minimum tRFCsb. Notes 2-5 apply to entire table.

[Table 53] IDD5C, IDDQ5C, IPP5C

Sequence	Command	CS	C/A [13:0]	CA8	BA [1:0]	CID [2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable						CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2) DQ signals are VDDQ
3) All banks of all “non-target” logical ranks are IDD2N condition.
4) Where C/A[13:0] column is not populated, refer to command truth table, CA8, and CID columns for the C/A state.
5) All banks of all “non-target” logical ranks are IDD2N condition.

11.10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R Pattern

All notes apply to entire table.

[Table 54] IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R

Sequence	Command	Clock	CS	C/A [13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid tCKLCS(min) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy tCPDED(min), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A = H	CK_t = CK_c = H	L	0x3FFF	Repeat sequence indefinitely

NOTE :
1) Data is pulled to VDDQ.
2) DQS_t and DQS_c are pulled to VDDQ.
3) For 3DS, all banks of all logical ranks mimic the same test condition.

11.11 IDD7, IDDQ7 and IPP7 Pattern

Executes ACTVATE, READ/A commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-6 apply to entire table.

[Table 55] IDD7, IDD7Q, IPP7

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L H	-	0x00000	-	0x0	0x0	0x0	-	
	1	DES	H	Toggling1							Repeat sequence to satisfy tRRD_S(min)
1	2	ACT	L H	-	0x03FFF	-	0x0	0x1	0x0	-	
	3	DES	H	Toggling1							Repeat sequence to satisfy tRRD_S(min)
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead									skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead									skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead									skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead									skip for x16
8	16	RDA	L H	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
	17	ACT	L H	-	0x00000	-	0x1	0x0	0x0	-	
	18	DES	H	Toggling1							Repeat sequence to satisfy tCCD_S(min)
9	19	RDA	L H	-	-	0x000	0x0	0x1	0x0	Pattern B	
	20	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
	21	DES	H	Toggling1							Repeat sequence to satisfy tCCD_S(min)
10	22-24	Repeat sub-loop 8, use BG[2:0]=0x2 instead									
11	25-27	Repeat sub-loop 9, use BG[2:0]=0x3 instead									
12	28-30	Repeat sub-loop 8, use BG[2:0]=0x4 instead									skip for x16
13	31-33	Repeat sub-loop 9, use BG[2:0]=0x5 instead									skip for x16
14	34-36	Repeat sub-loop 8, use BG[2:0]=0x6 instead									skip for x16
15	37-39	Repeat sub-loop 9, use BG[2:0]=0x7 instead									skip for x16
16-23	40-64	Repeat sub-loops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the ACT									
24-31	65-89	Repeat sub-loops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the ACT									
32-39	90-114	Repeat sub-loops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the ACT									
...	...	Repeat sub-loops 0-18 for each 3DS logical rank, if applicable									CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2) READs performed with Auto Precharge = H, Burst Chop = H.
3) x8 or x16 may have different Bank or Bank Group Address.
4) Data reflects burst length of 16.
5) Refer to IDD4R measurement loop table for data pattern definition.
6) For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

12.0 16Gb DDR5 SDRAM B-die IDD SPECIFICATION TABLE

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[Table 56] IDD 4800(40-39-39) Specification

Symbol	4Gx4 (K4RAH046VB)			2Gx8 (K4RAH086VB)			Unit
	DDR5-4800(40-39-39)			DDR5-4800(40-39-39)			
	IDD Max.	IDDQ Max.	IPPE Max.	IDD Max.	IDDQ Max.	IPPE Max.	
I_{DD0}	53	22	7	53	22	7	mA
I_{DD0F}	100	22	13	100	22	13	mA
I_{DD2N}	30	21	4	30	21	4	mA
I_{DD2P}	23	15	4	23	15	4	mA
I_{DD2NT}	60	23	4	60	23	4	mA
I_{DD3N}	46	21	5	46	21	5	mA
I_{DD3P}	30	13	5	30	13	5	mA
I_{DD4R}	170	125	8	190	162	8	mA
I_{DD4RC}	170	125	8	190	162	8	mA
I_{DD4W}	265	105	8	230	172	8	mA
I_{DD4WC}	265	105	8	230	172	8	mA
I_{DD5B}	230	23	56	230	23	56	mA
I_{DD5F}	220	23	56	220	23	56	mA
I_{DD5C}	95	23	25	95	23	25	mA
I_{DD6N}	62	5	12	62	5	12	mA
I_{DD6E}	80	8	16	80	8	16	mA
I_{DD7}	300	125	30	320	162	30	mA
I_{DD8}	16	6	4	16	6	4	mA

[Table 57] IDD6 Specification

Symbol	Temperature Range	4Gx4 (K4RAH046VB)			2Gx8 (K4RAH086VB)			Unit	NOTE
		DDR5-4800(40-39-39)			DDR5-4800(40-39-39)				
		IDD Max.	IDD Max.	IDD Max.	IDD Max.	IDD Max.	IDD Max.		
I_{DD6N}	0 - 85 °C	62	5	12	62	5	12	mA	1,2
I_{DD6E}	0 - 95 °C	80	8	16	80	8	16	mA	2,3

13.0 Input/Output Capacitance

[Table 58] Silicon pad I/O Capacitance

Symbol	Parameter	DDR5-4000		DDR5-4400 to 4800		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance(DQ, DM_n, DQS_t, DQS_c, TDQS_t,TDQS_c)	0.45	0.9	0.45	0.9	pF	1,2,
C_{DIO}	Input/output capacitance delta(DQ, DM_c)	-0.1	0.1	-0.1	0.1	pF	1,2,8
C_{DDQS}	Input/output capacitance delta (DQS_t and DQS_c)		0.04		0.04	pF	1,2,4
C_{CK}	Input capacitance(CK_t and CK_c)	0.2	0.7	0.2	0.6	pF	1,2
C_{DCK}	Input capacitance delta(CK_t and CK_c)		0.05		0.05	pF	1,2,3
C_{I}	Input capacitance(CS_n & CA[13:0] pins only)	0.2	0.7	0.2	0.6	pF	1,2,5
$C_{DI\_CS\_n}$	Input capacitance delta(CS_n pin only)	-0.1	0.1	-0.1	0.1	pF	1,2,6
C_{DI_CA}	Input capacitance delta(CA[13:0] pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,7
C_{ALERT}	Input/output capacitance of ALERT	0.4	1.5	0.4	1.5	pF	1,2
$C_{Loopback}$	Input/output capacitance of Loopback(LBDQ, LBDQS)	0.3	1.0	0.3	1.0	pF	1,2
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,2,9
C_{ZQ}	Input capacitance of ZQ		5	-	5	pF	1,2,11
C_{STRAP}	Input capacitance of MIR, CAI, CA_ODT pins		10	-	10	pF	1,2,10

NOTE :

1) This parameter is not subject to production test. This parameter is measured by using vendor specific measurement methodology.
2) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
3) Absolute value CIO(CK_t)-CIO(CK_c).
4) Absolute value of CIO(DQS_t)-CIO(DQS_c).
5) CI applies to CS_n and CA[13:0].
6) CDI_CS_n = CI(CS_n)-0.5*(CI(CK_t)+CI(CK_c)).
7) CDI_CA = CI(CA[13:0])-0.5*(CI(CK_t)+CI(CK_c)).
8) CDIO = CIO(DQ,DM)-Avg(CIO(DQ,DM)).
9) TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.
10) MIR, CAI, and CA_ODT are strap pins used to configure module or point to point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
11) Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality / accuracy with the max capacitive load is characterized.

[Table 59] DRAM package electrical specifications (X4/X8)

Parameter	Symbol	4000 to 4800		Unit	NOTE
		min	max		
Input/output Zpkg	Zpkg_DQ	45	75	W	1,2,4,5,10,
Input/output Pkg Delay	Tpkg_delay_DQ	10	35	ps	1,3,4,5,10
DQS_t, DQS_c Zpkg	Zpkg_DQS	45	75	W	1,2,5,10,12
DQS_t, DQS_c Pkg Delay	Tpkg_delay_DQS	10	35	ps	1,3,5,10,12
Delta Zpkg DQS_t, DQS_c	DZpkg_DQS	-	5	W	1,2,5,7,10
Delta Delay DQS_t, DQS_c	DTpkg_delay_DQS	-	2	pF	1,3,5,7,10
Input- CTRL pins Zpkg	Zpkg_CTRL	45	75	W	1,2,5,9,10
Input- CTRL pins Pkg Delay	Tpkg_delay_CTRL	10	35	ps	1,3,5,9,10
Input- CMD ADD pins Zpkg	Zpkg_CA	45	75	W	1,2,5,8,10
Input- CMD ADD pins Pkg Delay	Tpkg_delay_CA	10	35	ps	1,3,5,8,10
CK_t & CK_c Zpkg	Zpkg_CK	45	75	W	1,2,5,10
CK_t & CK_c Pkg Delay	Tpkg_delay_CK	10	30	ps	1,3,5,10
Delta Zpkg CK_t & CK_c	DZpkg_delay_CK	-	5	W	1,2,5,6,10
Delta Delay CK_t & CK_c	DTpkg_delay_CK	-	2	ps	1,3,5,6,10
ALERT Zpkg	Zpkg_ALERT	45	75	W	1,2,5,10
ALERT Delay	Tpkg_delay_ALERT	10	60	ps	1,3,5,10
Loopback Zpkg	Zpkg_Loopback	45	75	W	1,2,5,10,11
Loopback Delay	Tpkg_delay_Loopback	10	60	ps	1,3,5,10,11

NOTE :

1) This parameter is not subject to production test.
2) This parameter is measured by using vendor specific measurement methodology to calculate the average Z_{pkg_xx} over the interval $T_{pkg\_delay\_xx}$.
3) This parameter is measured by using vendor specific measurement methodology.
4) Z_{pkg_DQ} & $T_{pkg\_delay\_DQ}$ applies to DQ, DM.
5) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
6) Absolute value of $Z_{pkg\_CK\_t}$ - $Z_{pkg\_CK\_c}$ for impedance(Z) or absolute value of $T_{pkg\_delay\_CK\_t}$ - $T_{pkg\_delay\_CK\_c}$ for delay (T_{pkg_delay}).
7) Absolute value of Z_{pkg}(DQS_t)-Z_{pkg}(DQS_c) for impedance(Z) or absolute value of $T_{pkg\_delay\_DQS\_t}$ - $T_{pkg\_delay\_DQS\_c}$ for delay (T_{pkg_delay})
8) Z_{pkg_CA} & $T_{pkg\_delay\_CA}$ applies to CA[13:0].
9) Z_{pkg_CTRL} & $T_{pkg\_delay\_CTRL}$ applies to CS_n.
10) Package implementations shall meet spec if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11) $Z_{pkg\_Loopback}$ & $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.
12) Z_{pkg_DQS} & $T_{pkg\_delay\_DQS}$ applies to DQS_t & DQS_c, TDQS_t & TDQS_c.

13.1 Electrostatic Discharge Sensitivity Characteristics

[Table 60] Electrostatic Discharge Sensitivity Characteristics

Parameter	Symbol	min	max	Unit	NOTE
Human body model (HBM)	ESD_{HBM}	1000	-	V	2
Charged-device model(CDM)	ESD_{CDM}	250	-	V	3

NOTE :
1) State-of-the-art basic ESD control measures have to be in place when handling devices.
2) Refer to ESDA / JEDEC Joint Standard JS-001 for measurement procedures.
3) Refer to ESDA / JEDEC Joint Standard JS-002 for measurement procedures.

14.0 Electrical Characteristics & AC Timing

14.1 Rounding Definitions and Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 2200 MHz (4400 MT/s) for the DDR5-4400 speed bin, which mathematically yields a clock period tCK(AVG) of 0.454545... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be used.
The DDR5 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. All timing parameters specified in the time domain (ns, ps, etc.) which must then be converted to the clock domain (nCK units) shall be defined to align with these rules. The key point is, the minimum
timing parameters shall generally use the same rounding rules used to define tCK(AVG)min. The resulting rounding algorithms rely on results that are within correction factors of device testing and specification to avoid losing performance due to rounding errors.
These rules are :

- Minimum timing parameter values, including tCK(AVG)min, are rounded down and be defined to 1 ps of accuracy in the DDR5 SDRAM specification based on the non-rounded nominal tCK(AVG)min for a given speed bin. If the nominal minimum timing parameter values require more than 1 ps of accuracy, they can be rounded down (faster) to the next 1 ps according to the rounding algorithms, and the DDR5 SDRAM is responsible for absorbing this small minimum parameter extension. In other words, the DDR5 SDRAM specification only lists the nominal minimum parameter values rounded down to the next 1ps. For example, this extends the DDR5-4400 tCK(AVG)min definition to be exactly 0.454 ns which is slightly smaller (faster) than the nominal memory clock period of 0.454545... ns by less than 1 ps.

- For minimum timing parameters, other than tCK(AVG)min, to avoid losing performance due to additional erroneous nCKs and to calculate the true real minimum values, their nominal values listed in the DDR5 SDRAM specification must be reduced (faster) by the same or greater % reduction (correction factor) that was used to define tCK(AVG)min. The DDR5 SDRAM is responsible for absorbing these parameter extensions.
For example, tWRmin has a nominal value of 30.000ns, however, applying the 0.30% correction factor allows a more aggressive timing (for example, 29.910ns) to be supported, which allows the intended smaller (faster) nCK value to be maintained when rounding tCK(AVG)min down to the next 1 ps.
Note, parameter values defined to be 0 ps do not need to be reduced by a correction factor, and therefore don't require these rounding algorithms.

- Using real number math, nominal minimum parameters like tWRmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time are divided by the real application memory clock period tCK(AVG)real yielding a ratio of clock units (nCK), which is reduced by a correction factor of 0.30% (multiply by 99.70%) then the result is rounded up to the next integer number of clocks:

$$nCK = ceiling\left[\frac{parameter\_nominal \times 0.997}{tCK(AVG)real}\right]$$

- Round down only integer number math is commonly used in the industry to calculate nCK values. This second algorithm uses scaling by 1000 to allow use of integer math. Here, the nominal minimum parameter, in ps, is multiplied by the scaled correction factor (1000-3=997) prior to division by the application memory clock period, and 1 scaled by 1000 added to that result effectively rounds the result up. Division by 1000 undoes the scaling effects, resulting in a simple integer number of clocks as the final answer. The caveat is, effectively adding 1 prior to rounding down is mostly equivalent to rounding up except when the result is equal to an integer (whole number) in which case the result won't be rounded down as intended, and therefore performance would be lost. To address this, the largest correction factor of 0.28% needed for 3600 MHz (7200 MT/s) operation has been increased slightly to 0.30% in these rounding algorithms. This accounts for all integer boundary conditions, except for the specific case when the nominal minimum timing parameter value is defined to be 0 ps. This round down only integer number math algorithm is not for 0 ps parameter values, and will result in lost performance if used for 0 ps parameter values.

$$nCK = truncate\left[\frac{\left(\frac{truncate[\text{parameter\_nominal\_in\_ps} \times 1000] \times 997}{truncate[\text{tCK(AVG)\_real\_in\_ps}]}\right) + 1000}{1000}\right]$$

- The real number math rounding algorithm and the round down only integer number math rounding algorithm both yield similar results. In case of conflicting results, the round down only integer number math algorithm shall prevail.

- The real number math and round down only integer number math rounding algorithms shall be used for all minimum timing parameters when converting from the time domain (ns, ps, etc.) to the clock domain (nCK units), except for when converting tAA to CL. If these rounding algorithms are used to convert tAA to CL, they'll return invalid CL's for some cases when down clocking (and the DIMM SPD CL Mask doesn't protect against all of these cases). The proper setting of CL shall be determined by the memory controller, either by using the speed bin tables, or by using the CL algorithm, or by some other means. Refer to the Speed Bins and Operations section for more information. Note, the CL algorithm replaces the need to use the DIMM SPD CL Mask.

- If the DDR5 SDRAM supports non-standard tCK, tAA, tRCD, and tRP speed bin timings, the CL algorithm will still only return valid CL's as defined in the speed bin tables, which may not be the intended CL's for non-standard speed bins. In these cases, the rounding algorithms may need to be used to convert tAA to CL, instead of the CL algorithm. The CL returned by the rounding algorithms shall be incremented up to the next supported CL according to the DIMM SPD CL Mask. Consult the memory vendor for more information.

14.1.1 Example 1, using integer math to convert tAA(min) from ns to nCK:

// This algorithm reduces the nominal minimum timing parameter value by a 0.30% correction factor,
// and rounds nCK up to the next integer value.

```
real TwrMin, Correction, ClockPeriod, TempTwr, TempNck
int TwrInNck;

TwrMin = 30.000;                        // tWRmin in ns
Correction = 0.003                      // 0.30% per the rounding algorithm
ClockPeriod = ApplicationTck;           // Clock period in ns is application specific
TempTwr = TwrMin * (1 - Correction);    // Apply correction factor
TempNck = TempTwr / ClockPeriod;        // Initial nCK calculation
TwrInNck = (int) ceiling(TempNck);      // Round up to next integer value
```

[Table 61] Example 1, using real number math

DDR5 Device Operating at Standard Application Frequencies Timing Parameter: *t*WR(min) = 30.000ns					
Application Speed Grade	Device *t*WR	Application *t*CK	Device tWR / Application *t*CK	Device *t*WR * (1 - Correction) / Application *t*CK	Ceiling Result
	ns	ns	nCK (real)	nCK (corrected)	nCK (integer)
3200	30.000	0.625	48.00	47.86	48
3600	30.000	0.555	54.05	53.89	54
4000	30.000	0.500	60.00	59.82	60
4400	30.000	0.454	66.08	65.88	66
4800	30.000	0.416	72.12	71.90	72

14.1.2 Example 2, using integer math to convert tWR(min) from ns to nCK:

```
// This algorithm reduces the nominal minimum timing parameter value by a 0.30% correction factor,
// adds 1 nCK, and rounds nCK down to the next integer value

int TwrMin, Correction, ClockPeriod, TempTwr, TempNck, TwrInNck;

TwrMin      = 30000;                        // tWRmin in ps
Correction  = 3                             // 0.30% per the rounding algorithm
ClockPeriod = ApplicationTck;               // Clock period in ps is application specific
TempTwr     = TwrMin * (1000 - Correction); // Apply correction factor, scaled by 1000
TempNck     = TempTwr / ClockPeriod ;       // Initial nCK calculation, scaled by 1000
TempNck     = TempNck + 1000;               // Add 1, scaled by 1000, to effectively round up
TwrInNck    = (int)(TempNck / 1000);        // Round down to next integer
```

[Table 62] Example 2, using round down only integer number math

DDR5 Device Operating at Standard Application Frequencies Timing Parameter: *t*WR(min) = 30.000ns = 30000ps					
Application Speed Grade	Device *t*WR	Application tCK	Device tWR / Application tCK	Device tWR * (1000 - Correction) / Application tCK + 1000	Truncate Corrected nCK / 1000
	ps	ps	nCK (real)	scaled nCK (corrected)	nCK (integer)
3200	30000	625	48.00	48856	48
3600	30000	555	54.05	54891	54
4000	30000	500	60.00	60820	60
4400	30000	454	66.08	66881	66
4800	30000	416	72.12	72899	72

14.2 AC Timings

The analog timing parameters in this section have been defined based on nominal tCA(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section. .

[Table 63] Timing Parameters

Speed		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Average Clock Period	tCK(avg)	0.500	-	0.454	-	0.416	-	ns	1
Command and Address Timing									
Read to Read command delay for same bank group	tCCD_L	Max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	
Write to Write command delay for same bank group	tCCD_L_WR	Max(32nCK, 20ns)	-	max(32nCK, 20ns)	-	max(32nCK, 20ns)	-	nCK,ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	nCK,ns	
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	-	8	-	8	-	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	-	8	-	8	-	nCK	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2,4,6
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	8	-	8	-	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 16.000ns)	-	Max(32nCK, 14.545ns)	-	Max(32nCK, 12.307ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 20.000ns)	-	Max(40nCK, 18.181ns)	-	Max(40nCK, 15.384ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	nCK,ns	
Precharge to Precharge command delay	tPPD	2	-	2	-	2	-	nCK	7
Write recovery time	tWR	30	-	30	-	30	-	ns	

NOTE :

1) tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
2) tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms, nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).
3) - RBL: Read burst length associated with Read command.
   RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode.
   RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode.
   RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.
4) WBL: Write burst length associated with Write command.
   WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode.
   WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode.
   WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.
5) The following is considered for tRTW equation.
   1tCK needs to be added due to tDQS2CK.
   Read DQS offset timing can pull in the tRTW timing.
   1tCK needs to be added when 1.5tCK postamble.
6) CWL=CL-2.
7) tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

14.3 DDR5 Function Matrix

DDR5 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

[Table 64] Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	x4	x8	NOTE
Write Leveling	V	V	
Temperature controlled Refresh	V	V	
Fine Granularity Refresh	V	V	
Same Bank Refresh	V	V	
Refresh for Management			
Data Mask		V	
Command Address Inversion	V	V	
TDQS		V	
ZQ calibration	V	V	
DQ Vref Training	V	V	
Per DRAM Addressability	V	V	
Mode Register Readout	V	V	
WRITE CRC	V	V	
READ CRC	V	V	
CA Parity			
Programmable Preamble/Postamble	V	V	
Maximum Power Saving Mode	V	V	
Connectivity Test Mode	V	V	
Bit Error Rate Test	V	V	
Package Output Driver Test Mode	V	V	
3DS	V		
CA Training Mode	V	V	
CS Training Mode	V	V	
DQS interval Oscillator	V	V	
ECC Transparency and Error Scrub	V	V	
Lookback	V	V	
Duty Cycle Adjuster	V	V	