366ball FBGA Specification

16Gb LPDDR4 (x16, 4 Channel)

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

Revision History

Version	Description	Date	Remark
0.8	- Initial version	Jan. 2014	Preliminary
0.81	- Editorial changes	Jan. 2014	Preliminary
0.82	- Package height changed	May 2014	Preliminary
0.9	- Updated IDD specification	Jul. 2014	Preliminary
1.0	Final Version - Updated IDD specification	Aug. 2014	

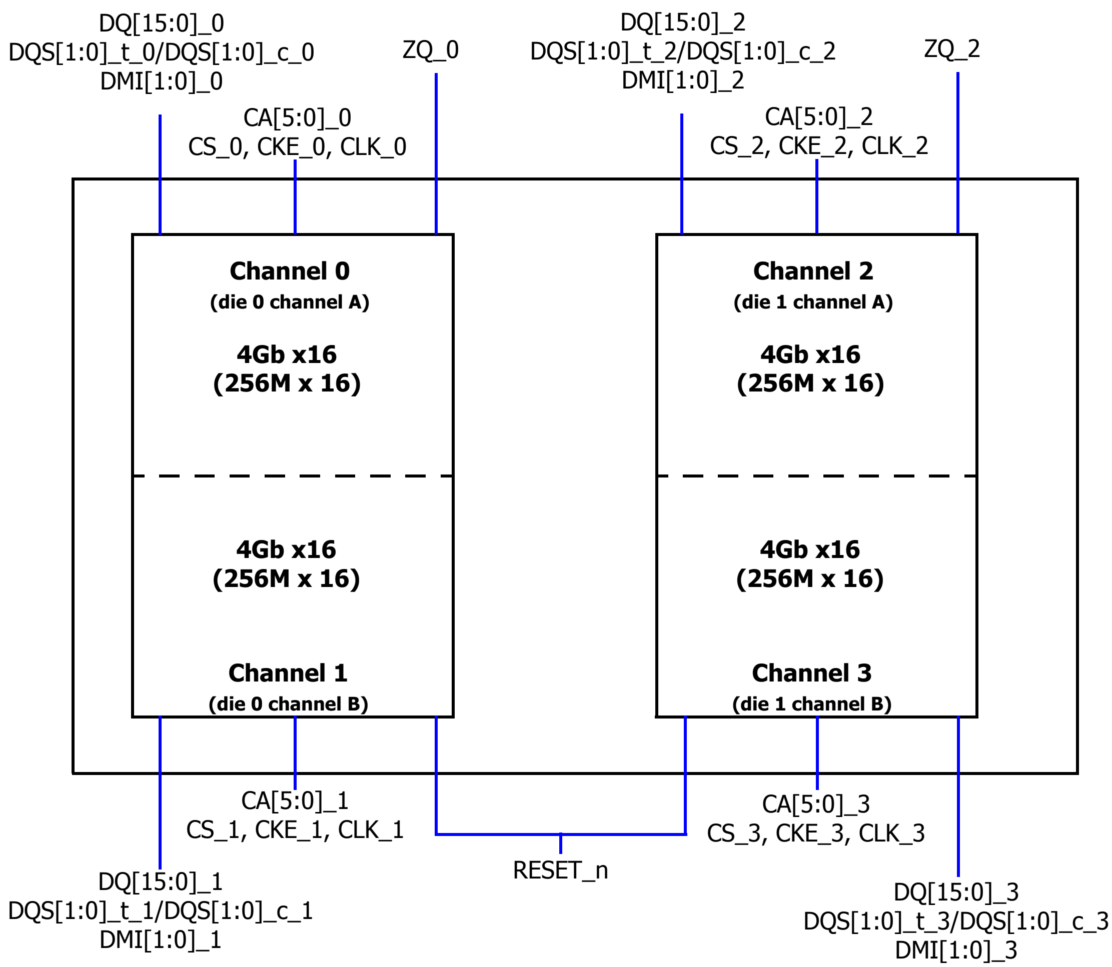
Ordering Information

Part Number	Mode	Operation Voltage	Density	Speed	Package	Operating Temperature
H9HKNNNBTUMUBR-NLM	LPDDR4	1.8V/1.1/1.1	16Gb (x16, 4 Channel)	DDR4 3200	366Ball FBGA (Lead & Halogen Free)	-25°C ~ 85°C
H9HKNNNBTUMUBR-NLH	LPDDR4	1.8V/1.1/1.1	16Gb (x16, 4 Channel)	DDR4 3200	366Ball FBGA (Lead & Halogen Free)	-25°C ~ 105°C

H 9 H K N N N B T U M U B R - N * *

- H: SK Hynix Memory
- 9: PoP
- H: Product Mode : LPDDR4
- K N: Density, Stack, Block Size & Page Buffer for NVM[1] : None
- N: Voltage & I/O for NVM : None
- N B: Density, Stack, CH & CS for DRAM : 16Gb, DDP, 4Ch 1CS
- T: Voltage, I/O & Option for DRAM : 1.1v/1.1, x16, LPDDR4
- U: Generation : 1st
- M U: Package Type : FBGA 366 Ball 15x15
- B R: Package Material : Lead & Halogen Free
- N: NAND Speed : none
- *: DRAM Speed
- *: Operating Temperature

Functional Block Diagram



1. FEATURES

[LPDDR4]

· VDD1 = 1.8V (1.7V to 1.95V)

· VDD2, VDDCA and VDDQ = 1.1V (1.06 to 1.17)

· VSSQ terminated DQ signals (DQ, DQS_t, DQS_c, DMI)

· Single data rate architecture for command and address;
- all control and address latched at rising edge of the clock

· Double data rate architecture for data Bus;
- two data accesses per clock cycle

· Differential clock inputs (CK_t, CK_c)

· Bi-directional differential data strobe (DQS_t, DQS_c)
  - Source synchronous data transaction aligned to bi-directional differential data strobe (DQS_t, DQS_c)

· DMI pin support for write data masking and DBIdc functionality

· Programmable RL (Read Latency) and WL (Write Latency)

· Burst length: 16 (default), 32 and On-the-fly
  - On the fly mode is enabled by MRS

· Auto refresh and self refresh supported
· All bank auto refresh and directed per bank auto refresh supported

· Auto TCSR (Temperature Compensated Self Refresh)

· PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask

· Background ZQ Calibration

2. Package Information

2.1. Package ballout

2.1.1. 366 balls, 15x15mm^2, 0.5mm pitch

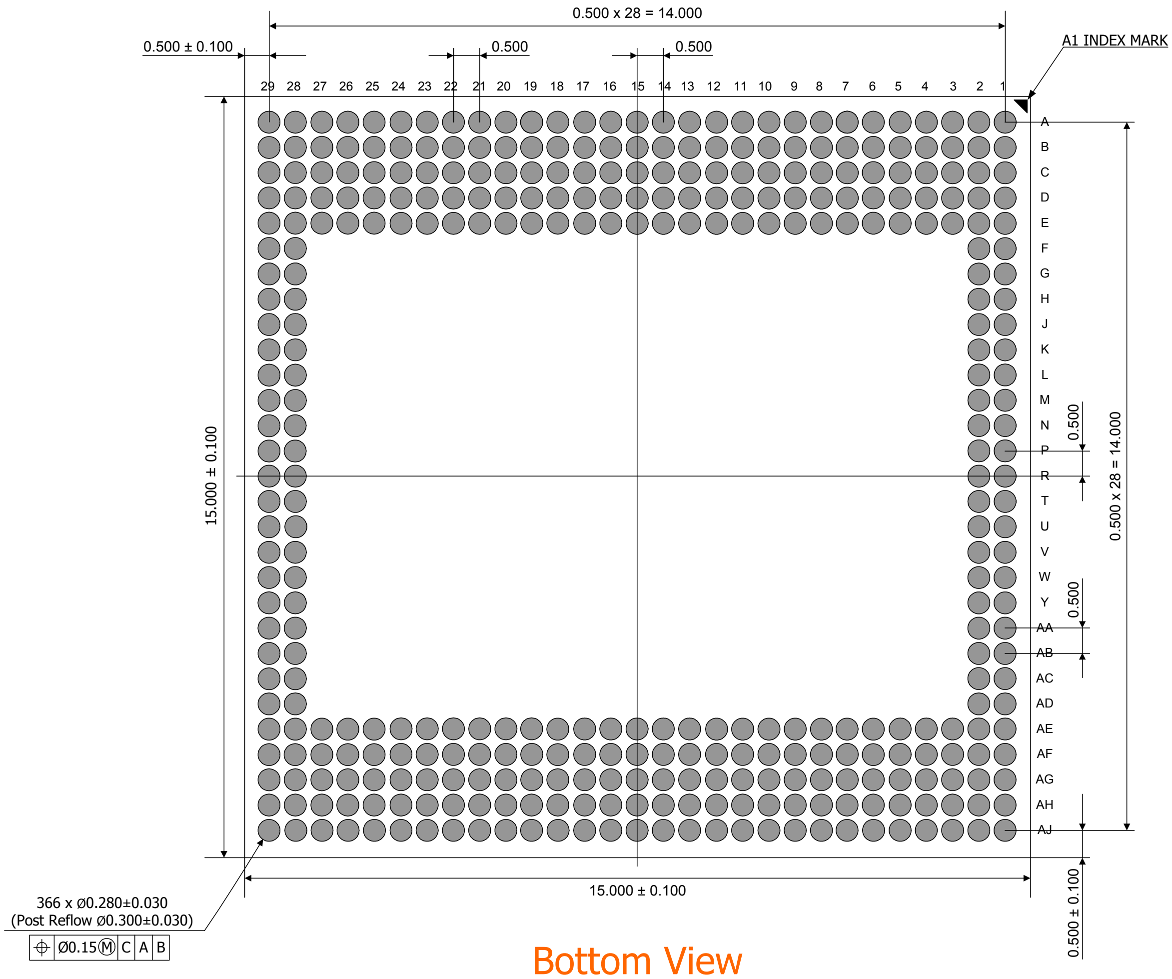
Top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	NC	VDD2	VSS	VDDQ	VDD1	VDD2	CS0_0	VDD2	VSS	VDD2	VDDQ	VSS	VDDQ	VDD2	VSS	VDD2	VDDQ	VSS	VDDQ	VDD1	VDD2	CS0_2	VDD2	VSS	VDD2	VDDQ	VSS	VDD2	NC
B	VDD1	DQ2_0	DQS0_t_0	DQ4_0	VSS	CA0_0	CS1_0	CK_t_0	CA3_0	VDD1	DQ13_0	DQS1_t_0	DQ11_0	VDD1	ZQ1_2	VDD1	DQ2_2	DQS0_t_2	DQ4_2	VSS	CA0_2	CS1_2	CK_t_2	CA3_2	VDD1	DQ13_2	DQS1_t_2	DQ11_2	VDD1
C	DQ0_0	VSS	DQS0_c_0	VSS	DQ6_0	VSS	VDD2	CK_c_0	VDD2	DQ15_0	VSS	DQS1_c_0	VSS	DQ9_0	ZQ0_2	DQ0_2	VSS	DQS0_c_2	VSS	DQ6_2	VSS	VDD2	CK_c_2	VDD2	DQ15_2	VSS	DQS1_c_2	VSS	DQ9_2
D	VDDQ	DQ3_0	VDDQ	DQ5_0	VDDQ	CA1_0	CKE0_0	VSS	CA4_0	VDDQ	DQ12_0	VDDQ	DQ10_0	VDDQ	ZQ1_0	VDDQ	DQ3_2	VDDQ	DQ5_2	VDDQ	CA1_2	CKE0_2	VSS	CA4_2	VDDQ	DQ12_2	VDDQ	DQ10_2	VDDQ
E	DQ1_0	VSS	DMI0_0	VSS	DQ7_0	ODT(ca)_0	CKE1_0	CA2_0	CA5_0	DQ14_0	VSS	DMI1_0	VSS	DQ8_0	ZQ0_0	DQ1_2	VSS	DMI0_2	VSS	DQ7_2	ODT(ca)_2	CKE1_2	CA2_2	CA5_2	DQ14_2	VSS	DMI1_2	VSS	DQ8_2
F	VSS	VSS																										VSS	VSS
G	VSS	VSS																										VSS	VSS
H	VSS	VSS																										VSS	VSS
J	VSS	VSS																										VSS	VSS
K	VSS	VSS																										VSS	VSS
L	VSS	VSS																										VSS	VSS
M	VSS	VSS																										VSS	VSS
N	VSS	VSS																										VSS	VSS
P	VSS	VSS																										VSS	VSS
R	VSS	VSS																										VSS	VSS
T	VSS	VSS																										VSS	VSS
U	VSS	VSS																										VSS	VSS
V	VSS	VSS																										VSS	VSS
W	VSS	VSS																										VSS	VSS
Y	VSS	VSS																										VSS	VSS
AA	VSS	VSS																										VSS	VSS
AB	VSS	VSS																										VSS	VSS
AC	VSS	VSS																										VSS	VSS
AD	VSS	VSS																										VSS	VSS
AE	DQ1_1	VSS	DMI0_1	VSS	DQ7_1	ODT(ca)_1	CKE1_1	CA2_1	CA5_1	DQ14_1	VSS	DMI1_1	VSS	DQ8_1	RESET_n	DQ1_3	VSS	DMI0_3	VSS	DQ7_3	ODT(ca)_3	CKE1_3	CA2_3	CA5_3	DQ14_3	VSS	DMI1_3	VSS	DQ8_3
AF	VDDQ	DQ3_1	VDDQ	DQ5_1	VDDQ	CA1_1	CKE0_1	VSS	CA4_1	VDDQ	DQ12_1	VDDQ	DQ10_1	VDDQ	RFU	VDDQ	DQ3_3	VDDQ	DQ5_3	VDDQ	CA1_3	CKE0_3	VSS	CA4_3	VDDQ	DQ12_3	VDDQ	DQ10_3	VDDQ
AG	DQ0_1	VSS	DQS0_c_1	VSS	DQ6_1	VSS	VDD2	CK_c_1	VDD2	DQ15_1	VSS	DQS1_c_1	VSS	DQ9_1	RFU	DQ0_3	VSS	DQS0_c_3	VSS	DQ6_3	VSS	VDD2	CK_c_3	VDD2	DQ15_3	VSS	DQS1_c_3	VSS	DQ9_3
AH	VDD1	DQ2_1	DQS0_t_1	DQ4_1	VSS	CA0_1	CS1_1	CK_t_1	CA3_1	VDD1	DQ13_1	DQS1_t_1	DQ11_1	VDD1	RFU	VDD1	DQ2_3	DQS0_t_3	DQ4_3	VSS	CA0_3	CS1_3	CK_t_3	CA3_3	VDD1	DQ13_3	DQS1_t_3	DQ11_3	VDD1
AJ	NC	VDD2	VSS	VDDQ	VDD1	VDD2	CS0_1	VDD2	VSS	VDD2	VDDQ	VSS	VDDQ	VDD2	VSS	VDD2	VDDQ	VSS	VDDQ	VDD1	VDD2	CS0_3	VDD2	VSS	VDD2	VDDQ	VSS	VDD2	NC

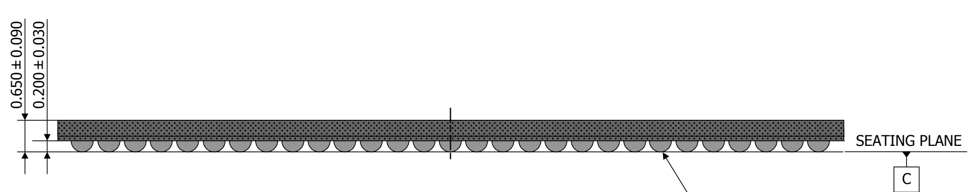
Notes:
1. Package Channel 0 and Channel 2 shall be assigned to die Channel A of different LPDDR4 die.
2. ODT(ca) for Rank 0 of each channel is wired to the respective ODT(ca) ball. ODT(ca) for other ranks (if present) is disabled in the DRAM package.
3. ZQ0_0 ball is wired to Rank 0 of the die supporting Channel 0. ZQ0_2 ball is wired to Rank 0 of the die supporting Channel 2. ZQ1_x balls are wired in the same manner to Rank 1 (if present)

2.2. Mechanical specification

366 Ball 0.50mm pitch 15.00mm x 15.00mm FBGA *[t = 0.74mm max]*



Bottom View



Front View

Notes:

1. The statistical maximum package height excluding the warpage is 0.70mm

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

2.3. Pin Description

Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A CS_B	Input	**Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A, CA[5 0]_B	Input	**Command/Address Inputs:** Provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data Input/Output** : Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Read Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and is center aligned with Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals.
ZQ	Reference	**Calibration Referce:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240-Ω ± 1% resistor.
VDD1, VDD2, VDDQ	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS	GND	**Ground Reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET pin resets both channels of the die.

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

3. Functional Description

LPDDR4-SDRAM is a high-speed synchronous DRAM device internally configured as an 2-channel memory with 8-bank memory per each channel.

These devices contain the following number of bits per die:
4Gb has 4,294,967,296 bits
6Gb has 6,442,450,944 bits
8Gb has 8,589,934,592 bits
12Gb has 12,884,901,888 bits
16Gb has 17,179,869,184 bits
24Gb has 25,769,803,776 bits
32Gb has 34,359,738,368 bits

LPDDR4 devices use multi cycle of single data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address and bank information. Each command uses two clock cycles, during which command information is transferred on positive edge of the corresponding clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4 SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and sixteen corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR4 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation

3.1. LPDDR4 SDRAM Addressing

Memory Density (per Die)	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**
Memory Density (per channel)	2Gb	3Gb	4Gb	6Gb	8Gb
Configuration	16 Mb x 16 DQ x 8 banks x 2 channels	24 Mb x 16 DQ x 8 banks x 2 channels	32 Mb x 16 DQ x 8 banks x 2 channels	48Mb x 16DQ x 8 banks x 2 channels	64 Mb x 16 DQ x 8 banks x 2 channels
Number of Channels per die	2	2	2	2	2
Number of Banks per Channel	8	8	8	8	8
Array Pre-fetch (bits, per channel)	256	256	256	256	256
Number of Rows per Channel	16,384	24,576	32,768	49,152	65,536
Number of Columns (fetch boundaries)	64	64	64	64	64
Page Size (Bytes)	2048	2048	2048	2048	2048
Channel Density (Bits per channel)	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592
Total Density (Bits per die)	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2
x16 Row Addresses	R0 - R13	R0 – R14 (R13=0 when R14=1)	R0 - R14	R0 – R15 (R14=0 when R15=1)	R0 - R15
x16 Column Addresses	C0 - C9	C0 - C9	C0 - C9	C0 - C9	C0 - C9
Burst Starting Address Boundary	64-bit	64-bit	64-bit	64-bit	64-bit

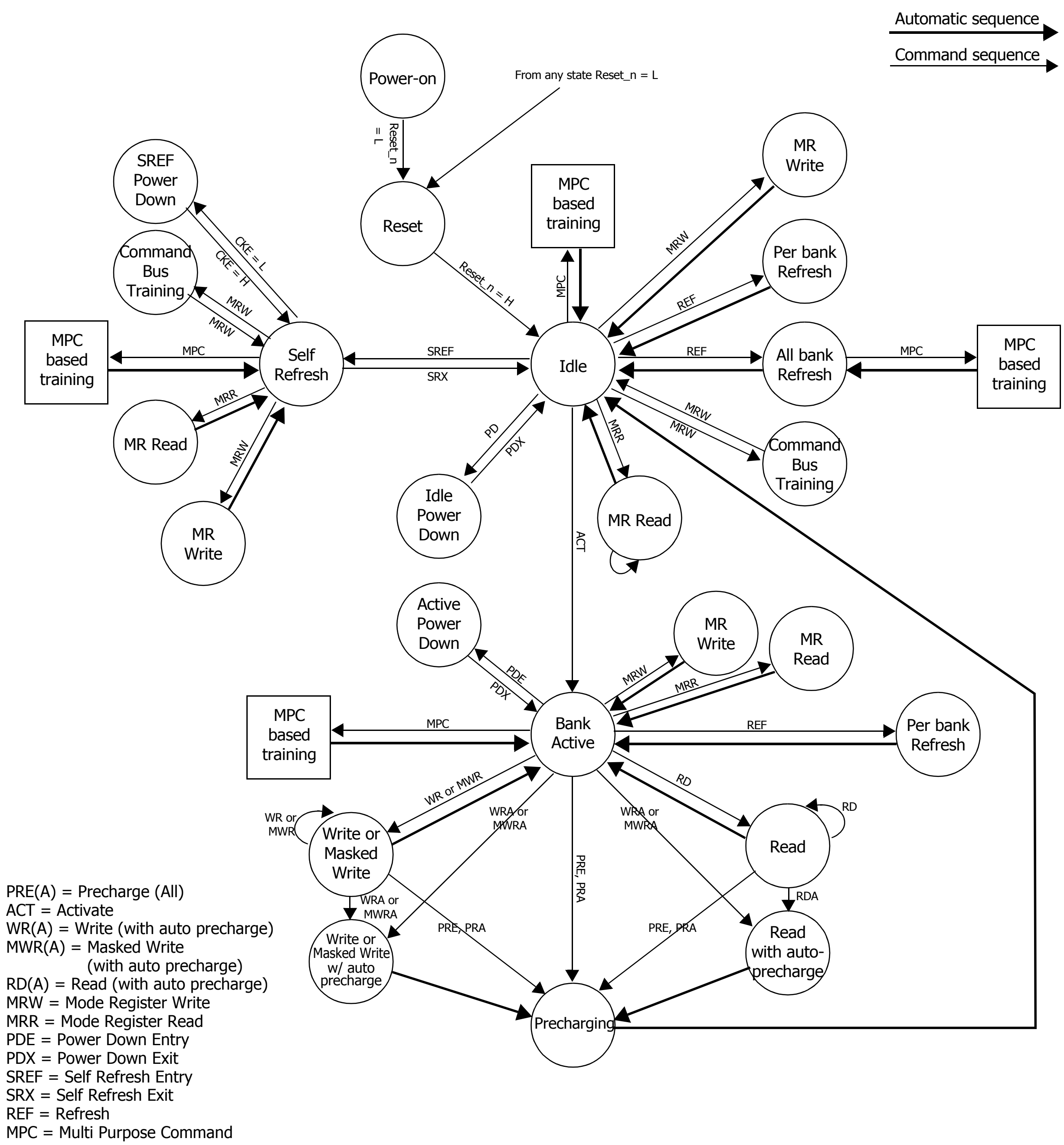
1. The lower two column addresses (C0-C1) are assumed to be "zero" and are not transmitted on the CA bus.
2. Row and Column address values on the CA bus that are not used for a particular density are "don't care."
3. For non-binary memory densities, only half of the row address space is valid. When the MSB address bit is "HIGH", then the MSB-1 address bit must be "LOW".

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

3.2. Simplified State Diagram

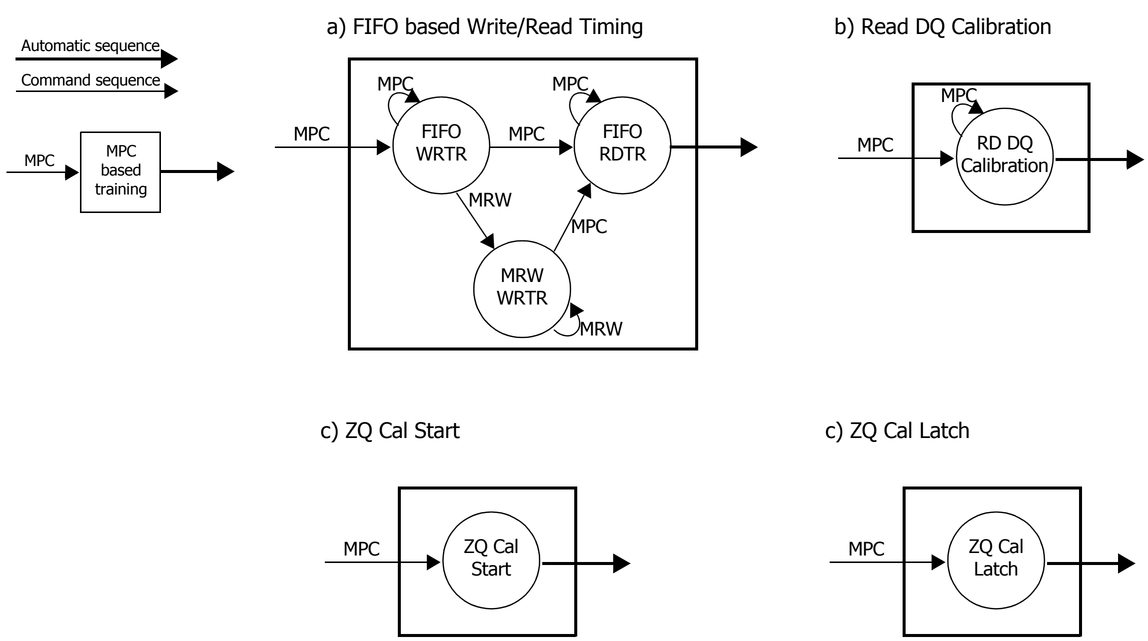
The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the Commands and Timing section.

Figure - Simplified State Diagram



Notes:
1. From the self refresh state, the device can enter power-down, MRR, MRW, or any of the training modes initiated with the MPC command. See the Self Refresh section.
2. All banks are precharged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
5. This diagram is intended to provide an overview of the possible state transitions and commands to control them; however, it does not contain the details necessary to operate the device. In particular, situations involving more than one bank are not captured in complete detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the re- set state. The diagram shows RESET applied from the power-on and idle states as an ex- ample, but this should not be construed as a restriction on RESET.
8. MRW commands from the active state cannot change operating parameters of the de- vice that affect timing. Mode register fields which may be changed via MRW from the active state include: MR1-OP[3:0], MR1-OP[7], MR3-OP[7:6], MR10-OP[7:0], MR11-OP[7:0], MR13-OP[5], MR15-OP[7:0], MR16-OP[7:0], MR17-OP[7:0], MR20-OP[7:0], and MR22-OP[4:0].

Figure - Simplified Bus Interface State Diagram



Notes:
1. From the self refresh state, the device can enter power-down, MRR, MRW, or MPC states. See the Self Refresh section.
2. All banks are precharged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
5. This diagram is intended to provide an overview of the possible state transitions and commands to control them; however, it does not contain the details necessary to oper- ate the device. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in complete detail.

6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET_n pin can be asserted from any state and will cause the device to enter the re- set state. The diagram shows RESET_n applied from the power-on state as an example, but this should not be construed as a restriction on RESET_n.
8. During all bank refresh (tRFCab), MRW is not allowed.

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

3.2.1. Power-up and Initialization

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as following table.

Table - MRS defaults settings

Item	MRS	Default setting	Description
FSP-OP/WR	MR13 OP[7:6]	00B	FS-OP/WR[0] are enabled
WLS	MR2 OP[6]	0B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000B	WL = 4
RL	MR2 OP[2:0]	000B	RL = 6, nRTP = 8
nWR	MR1 OP[6:4]	000B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000B	DQ ODT is disabled
Vref(ca) Setting	MR12 OP[6]	1B	Vref(ca) Range[1] enabled
Vref(ca) value	MR12 OP[5:0]	001101B	Range1: 27.2% of VDDQ
Vref(DQ) Setting	MR14 OP[6]	1B	Vref(DQ) Range[1] enabled
Vref(DQ) Value	MR14 OP[5:0]	001101B	Range1: 27.2% of VDDQ

3.2.1.1. Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x VDD2) and all inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table "Voltage Ramp Conditions". VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table - Voltage Ramp Conditions

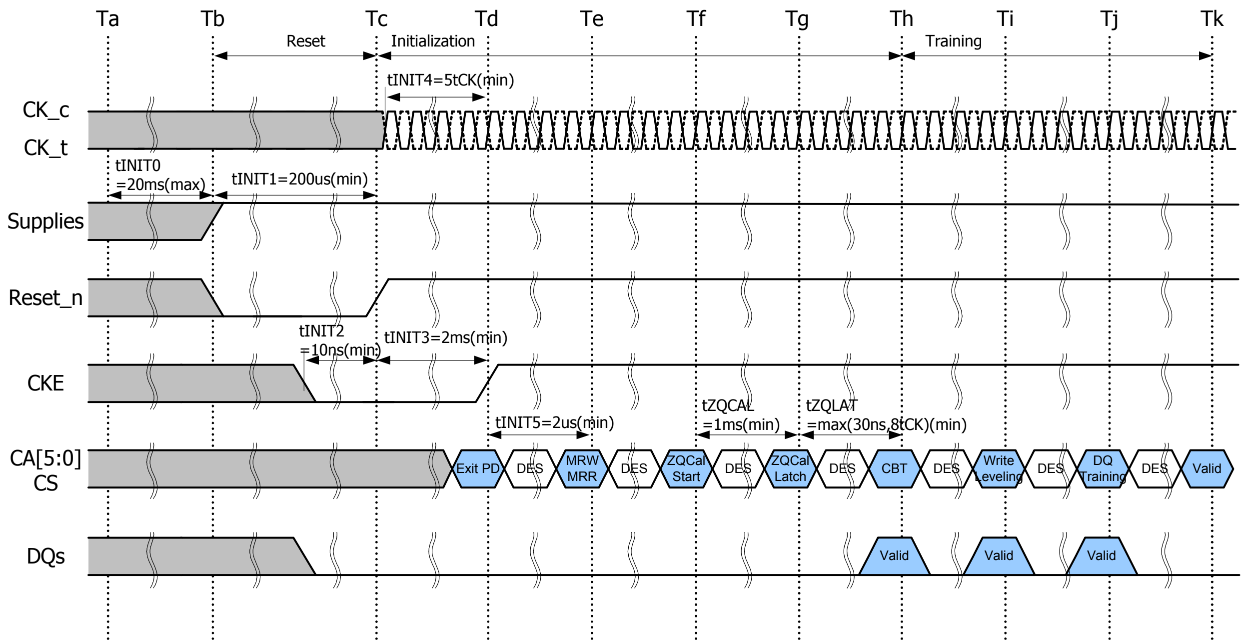
After...	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

Note:
1. Ta is the point when any power supply first reaches 300mV.
2. Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined ranges.
4. Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
5. The voltage difference between any of VSS and VSSQ pins must not excess 100mV.

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between Vssq and Vddq during voltage ramp to avoid latch-up. CKE, CK_t, CK_c, CS_n and CA input levels must be between Vss and VDD2 during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

Figure - Power Ramp and Initialization Sequence



Note
1. Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch(Th, Sequence7~9) in the above figure, is simplified recommendation and actual training sequence may vary depending on systems.

4. After RESET_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. Clock(CK_t,CK_c) is required to be started and stabilized for tINIT4 before CKE goes active(Td). CS is required to be maintained LOW when controller activates CKE.

5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands(Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory(Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th) the command bus (internal VREF(ca), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed operations, and VREF(ca) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.
The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high(Ti). See write leveling section for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS_t/_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal VREF(dq), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust VREF(dq)(Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and VREF(dq) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

10. At Tk the LPDDR4 device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

Table - Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0		20	ms	Maximum Voltage Ramp Time
tINIT1	200		us	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10		ns	Minimum CKE LOW time before RESET_n goes HIGH
tINIT3	2		ms	Minimum CKE LOW time after RESET_n goes HIGH
tINIT4	5		tCK	Minimum stable clock before first CKE HIGH
tINIT5	2		us	Minimum idle time before first MRW/MRR command
tCKb	Note 1, 2	Note 1, 2	ns	Clock cycle time during boot

Notes
1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent

3.2.1.2. Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 x VDD2 anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET_n.

2. Repeat steps 4 to 10 in "Voltage Ramp and Device Initialization" section.

Table - Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RESET	100	-	ns	Minimum RESET_n low time for Reset Initialization with stable power

3.2.2. Power-off Sequence

3.2.2.1. Controlled Power-off

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (≤0.2 X VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. RESET_n, CK_t, CK_c, CS and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.
Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After TZ, the device is powered off.

Table - Power Supply Conditions for Power-off

Between...	Applicable Conditions
TX and TZ	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

Note: The voltage difference between any of VSS, VSSQ pins must not exceed 100mV

3.2.2.2. Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5V/μs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table - Timing Parameters for Power-off

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF		2	s	Maximum Power-off ramp time

3.3. Mode Register Definition

Table below shows the mode registers for LPDDR4 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table. Mode Register Assignment

MR#	MA <5:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Information	R	CATR	RFU		RZQI		RFU		Refresh Mode	MR0
1	01H	Device Feature 1	W	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL		MR1
2	02H	Device Feature 2	W	WR Lev	WLS	WL			RL			MR2
3	03H	IO Configuration 1	W	DBI-WR	DBI-RD	PDDS			RFU	WR-PST	PU-CAL	MR3
4	04H	Refresh Rate	R/W	TUF	RFU		PPRE	RFU	Refresh Rate			MR4
5	05H	Basic Configuration 1	R	LPDDR4 Manufacturer ID								MR5
6	06H	Basic Configuration 2	R	Revision ID-1								MR6
7	07H	Basic Configuration 3	R	Revision ID-2								MR7
8	08H	Basic Configuration 4	R	IO Width		Density				Type		MR8
9	09H	Test Mode	W	Vendor Specific Test Mode								MR9
10	0AH	ZQ Reset	W	RFU							ZQ Reset	MR10
11	0BH	ODT Feature	W	RFU	CA ODT			RFU	DQ ODT			MR11
12	0CH	VREF(ca) R0	R/W	RFU	VR-CA	VREF(ca)						MR12
13	0DH	Functional options	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT	MR13
14	0EH	VREF(dq)	R/W	RFU	VR(dq)	VREF(dq)						MR14
15	0FH	Invert Register 0	W	Lower Byte Invert for DQ Calibration								MR15
16	10H	PASR Bank	W	PASR Bank Mask								MR16
17	11H	PASR Segment	W	PASR Segment Mask								MR17
18	12H	DQS Oscillator 1	R	DQS Oscillator Count - LSB								MR18
19	13H	DQS Oscillator 2	R	DQS Oscillator Count - MSB								MR19
20	14H	Invert Register 1	W	Upper Byte Invert for DQ Calibration								MR20
21	15H	Vendor Specific	N/A	Vendor Specific Mode Registor								MR21
22	16H	SOC ODT Feature	W	RFU		ODTD-CA	ODTE-CS	ODTE-CK	CODT			MR22
23	17H	DQS Oscillator Run Time	W	DQS Oscillator Run Time Setting								MR23
24	18H	TRR	R/W	TRR	TRR Bank Address			U-MAC	MAC Value			MR24
25	19H	PPR Resource	R	Post Package Repair Resources								MR25
26:31	1AH:1FH	RFU	N/A	Reserved for Future Use								
32	20H	DQ Calibration - Pattern A	W	See "DQ Calibration" section								MR32
33:39	21H:27H	DNU	N/A	Do Not Use								
40	28H	DQ Calibration - Pattern B	W	See "DQ Calibration" section								MR40
41:47	29H:2FH	DNU	N/A	Do Not Use								
48:63	30H:3FH	RFU	N/A	Reserved for Future Use								

1. RFU bits should be set to '0' during mode register writes
2. RFU bits should be read as '0' during mode register reads

3. All mode registers that are specified as RFU or Write-only shall return undefined data when read and DQS_t/DQS_c shall be toggled
4. All mode registers that are specified as RFU shall not be written
5. See vendor device datasheet for details on vendor-specific mode registers
6. Writes to Read-only registers shall have no effect on the functionality of the device

3.3.1. MR0 Register Information (MA[7:0] = 00H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CATR	RFU		RZQI		RFU		Refresh Mode

Function	Register Type	Operand	Data	Notes
Refresh Mode	Read-only	OP[0]	0B: Both legacy & modified refresh mode supported 1B: Only modified refresh mode supported	
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	00B: RZQ Self-Test Not Supported 01B: ZQ pin may connect to VSS or float 10B: ZQ-pin may short to VDDQ 11B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to VDD2 or float, nor short to VSS)	1,2,3,4
CATR (CA Terminating Rank)		OP[7]	0B: CA for this rank is not terminated 1B: CA for this rank is terminated	

Notes:
1. RZQI, if supported, will be set upon the completion of the MRW ZQ Initialization Calibration command.
2. If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01B or OP[4:3] = 10B might indicate might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error, the LPDDR4-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.
4. If ZQ Self-Test returns OP[4:3] = 11B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).
5. OP[7] is set at power-up, according to the state of the CA-ODT pad on the die AND the state of MR11 OP[7]. If the CAODT pad is tied LOW, then the die will not terminate the CA bus and MR12 OP[7]=0B, regardless of the state of ODTECA (MR11 OP[7]). If the CA-ODT pad is tied HIGH AND ODTE-CA is enabled (MR11 OP[7]=1B), then this bit will be set (MR0 OP[7]=1B) and the die will terminate the CA bus.

3.3.2. MR1 Register Information (MA[7:0] = 01H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

Function	Register Type	Operand	Data	Notes
BL (Burst Length)	Write-only	OP[1:0]	00B: BL=16 Sequential (default) 01B: BL=32 Sequential 10B: BL=16 or 32 Sequential (on-the-fly) All Others: Reserved	1,5,6
WR-PRE (WR Pre-amble Length)		OP[2]	0B: Reserved 1B: WR Pre-amble = 2nCK (default)	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	0B: RD Pre-amble = Static (default) 1B: RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto Precharge commands)		OP[6:4]	000B: nWR = 6 (default) 001B: nWR = 10 010B: nWR = 16 011B: nWR = 20 100B: nWR = 24 101B: nWR = 30 110B: nWR = 34 111B: nWR = 40	2,5,6
RPST (RD Post-amble Length)		OP[7]	0B: RD Post-amble = 0.5*tCK (default) 1B: RD Post-amble = 1.5*tCK	4,5,6

1. Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the "BL" bit in the command operands. See the Command Truth Table.
2. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled. See Table, "Frequency Ranges for RL, WL, and nWR Settings" later in this section
3. For Read operations this bit must be set to select between a "toggling" pre-amble and a "Non-toggling" pre-amble. See the pre-amble section for a drawing of each type of pre-amble.
4. OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

3.3.2.1. Burst Sequence

Table - Burst Sequence for Read

Burst Length	Burst Type	C4	C3	C2	C1	Co	Burst Cycle Number and Burst Address Sequence																														
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
		V	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
		V	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
		V	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Table - Burst Sequence for Write

Burst Length	Burst Type	C4	C3	C2	C1	Co	Burst Cycle Number and Burst Address Sequence																														
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

1. C1:C0 input is not present on CA bus. It is implied zero.
2. The starting burst address is on 64-bit (4n) boundaries.
3. C2-C3 for BL16 and C2-C4 for BL32 shall be set to '0' for all Write operations.

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

3.3.3. MR2 Register Information (MA[7:0] = 02H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WR Lev	WLS	WL			RL		

Function	Register Type	Operand	Data	Notes
RL (Read latency)	Write only	OP[2:0]	**DBI Disable (MR3 OP[6]=0B)** 000B: RL= 6 & nRTP = 8 (Default) 001B: RL= 10 & nRTP = 8 010B: RL= 14 & nRTP = 8 011B: RL= 20 & nRTP = 8 100B: RL= 24 & nRTP = 10 101B: RL= 28 & nRTP = 12 110B: RL= 32 & nRTP = 14 111B: RL= 36 & nRTP = 16 **DBI Enable (MR3 OP[6]=1B)** 000B: RL= 6 & nRTP = 8 001B: RL= 12 & nRTP = 8 010B: RL= 16 & nRTP = 8 011B: RL= 22 & nRTP = 8 100B: RL= 28 & nRTP = 10 101B: RL= 32 & nRTP = 12 110B: RL= 36 & nRTP = 14 111B: RL= 40 & nRTP = 16	1,3,4
WL (Write latency)		OP[5:3]	**Set "A" (MR2 OP[6]=0B)** 000B: WL=4 (Default) 001B: WL=6 010B: WL=8 011B: WL=10 100B: WL=12 101B: WL=14 110B: WL=16 111B: WL=18 **Set "B" (MR2 OP[6]=1B)** 000B: WL=4 001B: WL=8 010B: WL=12 011B: WL=18 100B: WL=22 101B: WL=26 110B: WL=30 111B: WL=34	1,3,4
WLS (Write latency set)		OP[6]	0B: WL Set "A" (default) 1B: WL Set "B"	1,3,4
WR Lev (Write Leveling)		OP[7]	0B: Disabled (default) 1B: Enabled	2

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

1. See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR/nRTP.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the LPDDR4-SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR operand, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4. There are two physical registers assigned to each bit of this MR operand, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.3.3.1. Frequency Ranges for RL, WL, and nWR Settings

Read Latency		Write Latency		nWR	nRTP	Freq. limit (Greater than)	Freq. limit (Same or less than)	Notes
No DBI	w/ DBI	Set "A"	Set "B"					
6	6	4	4	6	8	10	266	1,2,3,4,5,6
10	12	6	8	10	8	266	533	
14	16	8	12	16	8	533	800	
20	22	10	18	20	8	800	1066	
24	28	12	22	24	10	1066	1333	
28	32	14	26	30	12	1333	1600	
32	36	16	30	34	14	1600	1866	
36	40	18	34	40	16	1866	2133	
nCK	*nCK*	*nCK*	*nCK*	*nCK*	*nCK*	*MHz*	*MHz*	

Notes:
1. The LPDDR4-SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3-OP[6]. When MR3-OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3-OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set "A" and Set "B" is determined by MR2-OP[6]. When MR2-OP[6]=0, then Write Latency Set "A" should be used. When MR2-OP[6]=1, then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled. It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Read burst with AP (auto-pre-charge) enabled. It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a pre-charge.

3.3.4. MR3 Register Information (MA[7:0] = 03H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBI-WR	DBI-RD	PDDS			RFU	WR-PST	PU-CAL

Function	Register Type	Operand	Data	Notes
PU-CAL (Pull-up Calibration Point)		OP[0]	0B: VDDQ/2.5 1B: VDDQ/3 (default)	1,4
WR-PST (Write Post-amble length)		OP[1]	0B: WR Post-amble = 0.5*tCK (default) 1B: WR Post-amble = 1.5*tCK (Vendor Specific)	2,3,5
PDDS (Pull-down Drive Strength)	Write only	OP[5:3]	000B: RFU 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 (default) 111B: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	0B: Disabled (default) 1B: Enabled	2,3
DBI-WR (DBI-WR Enable)		OP[7]	0B: Disabled (default) 1B: Enabled	2,3

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. PU-CAL setting is required as the same value for both Ch.A and Ch.B before ZQCAL start command.
5. SK hynix 8Gb LPDDR4 doesn't require 1.5*tCK apply => 1.6GHz clock.

3.3.5. MR4 Register Information (MA[7:0] = 04H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	RFU		PPRE	RFU	Refresh Rate		

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	000B: SDRAM Low temperature operating limit exceeded 001B: 4x refresh 010B: 2x refresh 011B: 1x refresh (default) 100B: 0.5x refresh 101B: 0.25x refresh, no-rating 110B: 0.25x refresh, with de-rating 111B: SDRAM High temperature operating limit exceeded	1,2,3,4, 7,8,9
Self Refresh Abort	Write	OP[3]	0B: Disabled (default) 1B: Enabled	9,11

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

Function	Register Type	Operand	Data	Notes
PPRE (Post-package repair entry/ exit)	Write	OP[4]	0B: Exit PPR mode (default) 1B: Enter PPR mode	5,9
Thermal Offset (Vendor Specific Function)	Write	OP[6:5]	00B: No offset, 0-5^{o}C gradient (default) 01B: 5^{o}C offset, 5-10^{o}C gradient 10B: 10^{o}C offset, 10-15^{o}C gradient 11B: Reserved	10
TUF (Temperature Update Flag)	Read	OP[7]	0B: No change in OP[2:0] since last MR4 read (default) 1B: Change in OP[2:0] since last MR4 read	6,7,8

1. The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. If OP[2]=0B, the device temperature is less or equal to 85'C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1, the device temperature is greater than 85'C.
2. At higher temperatures (>85'C), AC timing de-rating may be required. If de-rating is required the LPDDR4-SDRAM will set OP[2:0]=110B. See de-rating timing requirements in the AC Timing section.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]=000B or 111B.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
7. OP[7]=0 at power-up. OP[2:0] bits are undefined at power-up.
8. See the section on "Temperature Sensor" for information on the recommended frequency of reading MR4.
9. OP[6:3] bits are that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register
10. Refer to the supplier data sheet for vendor specific function.
11. Self Refresh Abort feature is available for higher density devices starting with 12Gb device.

3.3.6. MR5 Register Information (MA[7:0] = 05H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LPDDR4 Manufacturer ID							

Function	Register Type	Operand	Data	Notes
LPDDR4 Manufacturer ID	Read-only	OP[7:0]	00000110B : SK hynix	

3.3.7. MR6 Register Information (MA[7:0] = 06H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

Function	Register Type	Operand	Data	Notes
LPDDR4 Revision ID-1	Read-only	OP[7:0]	00000000B: A-version 00000001B: B-version	1

1. Please contact SK hynix office for MR6 code for this device.

3.3.8. MR7 Register Information (MA[7:0] = 07H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

Function	Register Type	Operand	Data	Notes
LPDDR4 Revision ID-1	Read-only	OP[7:0]	00000000B: A-version 00000001B: B-version	1

1. Please contact SK hynix office for MR6 code for this device.

3.3.9. MR8 Register Information (MA[7:0] = 08H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO Width		Density				Type	

Function	Register Type	Operand	Data	Notes
Type	Read-only	OP[1:0]	00B: S16 SDRAM (16n pre-fetch) All Others: Reserved	
Density		OP[5:2]	0000B: 4Gb per die (2Gb per channel) 0001B: 6Gb per die (3Gb per channel) 0010B: 8Gb per die (4Gb per channel) 0011B: 12Gb per die (6Gb per channel) 0100B: 16Gb per die (8Gb per channel) 0101B: 24Gb per die (12Gb per channel) 0110B: 32Gb per die (16Gb per channel) All Others: Reserved	
IO Width		OP[7:6]	00B: x16 (per channel) All Others: Reserved	

3.3.10. MR9 Register Information (MA[7:0] = 09H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Test Register							

1. Only 00H should be written to this register.

3.3.11. MR10 Register Information (MA[7:0] = 0AH)

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							ZQ Reset

Function	Register Type	Operand	Data	Notes
ZQ Reset	Write-only	OP[0]	OB: Normal Operation (Default) 1B: ZQ Reset	1,2

1. See the AC Timing tables for calibration latency and timing
2. If the ZQ-pin is connected to VDDQ through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to VSS, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

3.3.12. MR11 Register Information (MA[7:0] = 0BH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA ODT			RFU	DQ ODT		

Function	Register Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3
CA ODT (CA Bus Receiver On-Die-Termination)		OP[6:4]	0000B: Disable (Default) 0001B: RZQ/1 0010B: RZQ/2 0011B: RZQ/3 0100B: RZQ/4 0101B: RZQ/5 0110B: RZQ/6 0111B: RFU	1,2,3

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

3.3.13. MR12 Register Information (MA[7:0] = 0CH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR-CA	VREF(ca)					

Function	Register Type	Operand	Data	Notes
VREF(ca) (VREF(ca) Setting)	Read/Write	OP[5:0]	000000B: -- Thru – 110010B: See table below All Others: Reserved	1,2,3,5,6
VREF(ca) Range		OP[6]	0B: VREF(ca) Range[0] enabled 1B: VREF(ca) Range[1] enabled (default)	1,2,4,5,6

1. This register controls the VREF(ca) levels for Frequency-Set-Point[1:0]. Values from either VR(ca)[0] or VR(ca)[1] may be selected by setting OP[6] appropriately.
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(ca) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(ca) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(ca) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal VREF(ca) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(ca) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table - VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
VREF Settings for MR12	OP[5:0]	000000B: 10.0%	011010B: 20.4%	000000B: 22.0%	011010B: 32.4%	1,2,3
		000001B: 10.4%	011011B: 20.8%	000001B: 22.4%	011011B: 32.8%	
		000010B: 10.8%	011100B: 21.2%	000010B: 22.8%	011100B: 33.2%	
		000011B: 11.2%	011101B: 21.6%	000011B: 23.2%	011101B: 33.6%	
		000100B: 11.6%	011110B: 22.0%	000100B: 23.6%	011110B: 34.0%	
		000101B: 12.0%	011111B: 22.4%	000101B: 24.0%	011111B: 34.4%	
		000110B: 12.4%	100000B: 22.8%	000110B: 24.4%	100000B: 34.8%	
		000111B: 12.8%	100001B: 23.2%	000111B: 24.8%	100001B: 35.2%	
		001000B: 13.2%	100010B: 23.6%	001000B: 25.2%	100010B: 35.6%	
		001001B: 13.6%	100011B: 24.0%	001001B: 25.6%	100011B: 36.0%	
		001010B: 14.0%	100100B: 24.4%	001010B: 26.0%	100100B: 36.4%	
		001011B: 14.4%	100101B: 24.8%	001011B: 26.4%	100101B: 36.8%	
		001100B: 14.8%	100110B: 25.2%	001100B: 26.8%	100110B: 37.2%	
		001101B: 15.2%	100111B: 25.6%	001101B: 27.2% (Default)	100111B: 37.6%	
		001110B: 15.6%	101000B: 26.0%	001110B: 27.6%	101000B: 38.0%	
		001111B: 16.0%	101001B: 26.4%	001111B: 28.0%	101001B: 38.4%	
		010000B: 16.4%	101010B: 26.8%	010000B: 28.4%	101010B: 38.8%	
		010001B: 16.8%	101011B: 27.2%	010001B: 28.8%	101011B: 39.2%	
		010010B: 17.2%	101100B: 27.6%	010010B: 29.2%	101100B: 39.6%	
		010011B: 17.6%	101101B: 28.0%	010011B: 29.6%	101101B: 40.0%	
		010100B: 18.0%	101110B: 28.4%	010100B: 30.0%	101110B: 40.4%	
		010101B: 18.4%	101111B: 28.8%	010101B: 30.4%	101111B: 40.8%	
		010110B: 18.8%	110000B: 29.2%	010110B: 30.8%	110000B: 41.2%	
		010111B: 19.2%	110001B: 29.6%	010111B: 31.2%	110001B: 41.6%	
		011000B: 19.6%	110010B: 30.0%	011000B: 31.6%	110010B: 42.0%	
		011001B: 20.0%	All Others: Reserved	011001B: 32.0%	All Others: Reserved	

1. These values may be used for MR12 OP[5:0] to set the VREF(ca) levels in the LPDDR4-SDRAM.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

3.3.14. MR13 Register Information (MA[7:0] = 0DH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	DME	RFU	VRCG	VRO	RPRE-TR	CBT

Function	Register Type	Operand	Data	Notes
CBT (Command Bus Training)	Write	OP[0]	0B: Normal Operation (default) 1B: Command Bus Training mode enabled	1
RPRE-TR (Read Preamble Training)		OP[1]	0B: Normal Operation (default) 1B: Read Preamble Training mode enabled	
VRO (Vref Output)		OP[2]	0B: Normal Operation (default) 1B: Output the Vref(ca) value on DQ[0] and the Vref(dq) value on DQ[1]	2
VRCG (VREF Current Generator)		OP[3]	0B: Normal Operation (default) 1B: VREF Fast Response (high current) mode	3
RRO (Refresh Rate Option)		OP[4]	0B: Disable MR4 OP[2:0] (default) 1B: Enable MR4 OP[2:0]	4,5
DMD (Data Mask Disable)		OP[5]	0B: Data Mask Operation Enabled (default) 1B: Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write Enable)		OP[6]	0B: Frequency-Set-Point[0] (default) 1B: Frequency-Set-Point[1]	7
FSP-OP (Frequency Set Point Oper-ation Mode)		OP[7]	0B: Frequency-Set-Point[0] (default) 1B: Frequency-Set-Point[1]	8

1. A write to set OP[0]=1 causes the LPDDR4-SDRAM to enter the VREF(ca) training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the VREF(ca) training section for more information.
2. When set, the LPDDR4-SDRAM will output the VREF(ca) voltage on DQ[0] and the VREF(dq) voltage on DQ[1]. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels.
3. When OP[3]=1, the VREF circuit uses a high-current mode to improve VREF settling time.
4. MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4 devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), Masked Write Command is not allowed and it is illegal. See the Data Mask section for more information.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions: Vref(CA) Setting, Vref(CA) Range, Vref(DQ) Setting, Vref(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following func-tions: Vref(CA) Setting, Vref(CA) Range, Vref(DQ) Setting, Vref(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.

3.3.15. MR14 Register Information (MA[7:0] = 0EH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR(dq)	VREF(dq)					

Function	Register Type	Operand	Data	Notes
VREF(dq) Setting for Set Point[0]	Read / Write	OP[5:0]	000000B: -- Thru – 110010B: See table below All Others: Reserved	1,2,3,4,5,6
VREF(dq) Range		OP[6]	0B: VREF(dq) Range[0] enabled 1B: VREF(dq) Range[1] enabled (default)	1,2,3,4,5,6

1. This register controls the VREF(dq) levels for Frequency-Set-Point[1:0]. Values from either VR(dq)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(dq) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(dq) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(dq) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal VREF(dq) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(dq) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

Table - VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
VREF Settings for MR14	OP[5:0]	000000B: 10.0%	011010B: 20.4%	000000B: 22.0%	011010B: 32.4%	1,2,3
		000001B: 10.4%	011011B: 20.8%	000001B: 22.4%	011011B: 32.8%	
		000010B: 10.8%	011100B: 21.2%	000010B: 22.8%	011100B: 33.2%	
		000011B: 11.2%	011101B: 21.6%	000011B: 23.2%	011101B: 33.6%	
		000100B: 11.6%	011110B: 22.0%	000100B: 23.6%	011110B: 34.0%	
		000101B: 12.0%	011111B: 22.4%	000101B: 24.0%	011111B: 34.4%	
		000110B: 12.4%	100000B: 22.8%	000110B: 24.4%	100000B: 34.8%	
		000111B: 12.8%	100001B: 23.2%	000111B: 24.8%	100001B: 35.2%	
		001000B: 13.2%	100010B: 23.6%	001000B: 25.2%	100010B: 35.6%	
		001001B: 13.6%	100011B: 24.0%	001001B: 25.6%	100011B: 36.0%	
		001010B: 14.0%	100100B: 24.4%	001010B: 26.0%	100100B: 36.4%	
		001011B: 14.4%	100101B: 24.8%	001011B: 26.4%	100101B: 36.8%	
		001100B: 14.8%	100110B: 25.2%	001100B: 26.8%	100110B: 37.2%	
		001101B: 15.2%	100111B: 25.6%	001101B: 27.2% (Default)	100111B: 37.6%	
		001110B: 15.6%	101000B: 26.0%	001110B: 27.6%	101000B: 38.0%	
		001111B: 16.0%	101001B: 26.4%	001111B: 28.0%	101001B: 38.4%	
		010000B: 16.4%	101010B: 26.8%	010000B: 28.4%	101010B: 38.8%	
		010001B: 16.8%	101011B: 27.2%	010001B: 28.8%	101011B: 39.2%	
		010010B: 17.2%	101100B: 27.6%	010010B: 29.2%	101100B: 39.6%	
		010011B: 17.6%	101101B: 28.0%	010011B: 29.6%	101101B: 40.0%	
		010100B: 18.0%	101110B: 28.4%	010100B: 30.0%	101110B: 40.4%	
		010101B: 18.4%	101111B: 28.8%	010101B: 30.4%	101111B: 40.8%	
		010110B: 18.8%	110000B: 29.2%	010110B: 30.8%	110000B: 41.2%	
		010111B: 19.2%	110001B: 29.6%	010111B: 31.2%	110001B: 41.6%	
		011000B: 19.6%	110010B: 30.0%	011000B: 31.6%	110010B: 42.0%	
		011001B: 20.0%	All Others: Reserved	011001B: 32.0%	All Others: Reserved	

1. These values may be used for MR14 OP[5:0] to set the VREF(dq) levels in the LPDDR4-SDRAM.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

3.3.16. MR15 Register Information (MA[7:0] = 0FH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Lower Byte Invert for DQ Calibration	Write	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55H	1

Notes:

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table - MR15 Invert Register Pin Mapping

Pin	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	No-invert	OP4	OP5	OP6	OP7

3.3.17. MR16 Register Information (MA[7:0] = 10H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Bank Mask							

Function	Register Type	Operand	Data	Notes
Bank[7:0] Mask	Write-only	OP[7:0]	0B: Bank Refresh enabled (default) : Unmasked 1B: Bank Refresh disabled : Masked	1

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank masking is on a per channel basis. The two channels on the die may have different bank masking.

3.3.18. MR17 Register Information (MA[7:0] = 11H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	Write-only	OP[7:0]	0B: Segment Refresh enabled (default) 1B: Segment Refresh disabled	1

Segment	OP[n]	Segment Mask	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	TBD	TBD
0	0	xxxxxxx1	000B						
1	1	xxxxxx1x	001B						
2	2	xxxxx1xx	010B						
3	3	xxxx1xxx	011B						
4	4	xxx1xxxx	100B						
5	5	xx1xxxxx	101B						
6	6	x1xxxxxx	110B	Not Allowed	110B	Not Allowed	110B	Not Allowed	110B
7	7	1xxxxxxx	111B		111B		111B		111B

1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking.
3. For 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00B).

3.3.19. MR18 Register Information (MA[7:0] = 12H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0:255 LSB DRAM DQS Oscillator Count	1,2,3

1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

3.3.20. MR19 Register Information (MA[7:0] = 13H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0:255 MSB DRAM DQS Oscillator Count	1,2

1. MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

3.3.21. MR20 Register Information (MA[7:0] = 14H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Upper Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Upper Byte Invert for DQ Calibration	Write	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55H	1,2

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
2. DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table - MR20 Invert Register Pin Mapping

Pin	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	No-invert	OP4	OP5	OP6	OP7

3.3.22. MR21 Register Information (MA[7:0] = 15H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Mode Registor							

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

3.3.23. MR22 Register Information (MA[7:0] = 16H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTD-CA	ODTE-CS	ODTE-CK	CODT		

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration	Write	OP[2:0]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3,8
ODTE-CK (CK ODT enabled for non-terminating rank)		OP[3]	0B: ODT-CK Over-ride Disabled (Default) 1B: ODT-CK Over-ride Enabled	2,3,4,6
ODTE-CS (CS ODT enable for non-terminating rank)		OP[4]	0B: ODT-CS Over-ride Disabled (Default) 1B: ODT-CS Over-ride Enabled	2,3,5,6
ODTD-CA (CA ODT termination disable)		OP[5]	0B: ODT-CA Obeys ODT_CA bond pad (default) 1B: ODT-CA Disabled	2,3,6,7

Notes:
1. All values are "typical".
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. When OP[3]=1, then the CK signals will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CK is not, allowing CK to terminate on all DRAMs.
5. When OP[4]=1, then the CS signal will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CS is not, allowing CS to terminate on all DRAMs.
6. For system configurations where the CK, CS, and CA signals are shared between packages, the package design should provide for the ODT_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared Command Bus signals.
7. When OP[5]=0, CA[5:0] will terminate when the ODT_CA bond pad is HIGH and MR11-OP[6:4] is VALID, and disables termination when ODT_CA is LOW or MR11-OP[6:4] is disabled. When OP[5]=1, termination for CA[5:0] is disabled, regardless of the state of the ODT_CA bond pad or MR11-OP[6:4].
8. To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including Active Self-refresh, Self-refresh Power-down, Active Power-down and Precharge Power-down.

3.3.24. MR23 Register Information (MA[7:0] = 17H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS oscillator run time setting							

Function	Register Type	Operand	Data	Notes
DQS oscillator run time	Write	OP[7:0]	00000000B: DQS timer stops via MPC Command (Default) 00000001B: DQS timer stops automatically at 16th clocks after timer start 00000010B: DQS timer stops automatically at 32nd clocks after timer start 00000011B: DQS timer stops automatically at 48th clocks after timer start 00000100B: DQS timer stops automatically at 64th clocks after timer start -------------- Thru ---------------------- 00111111B: DQS timer stops automatically at (63X16)th clocks after timer start 01XXXXXXB: DQS timer stops automatically at 2048th clocks after timer start 10XXXXXXB: DQS timer stops automatically at 4096th clocks after timer start 11XXXXXXB: DQS timer stops automatically at 8192nd clocks after timer start	1, 2

Note:
1. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000B.
2. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

3.3.25. MR24 Register Information (MA[7:0] = 18H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TRR Mode	TRR Mode Bank Address			Unlimited MAC	MAC Value		

Function	Register Type	Operand	Data	Notes
MAC Value	Read	OP[2:0]	000B: Unknown when bit OP3 =0 (note 1) Unlimited when bit OP3=1 (note 2) 001B: 700K 010B: 600K 011B: 500K 100B: 400K 101B: 300K 110B: 200K 111B: Reserved	
Unlimited MAC		OP[3]	0B: OP[2:0] define MAC value 1B: Unlimited MAC value (note 2, note 3)	

Function	Register Type	Operand	Data	Notes
TRR Mode BAn	Write	OP[6:4]	000B: Bank 0 001B: Bank 1 010B: Bank 2 011B: Bank 3 100B: Bank 4 101B: Bank 5 110B: Bank 6 111B: Bank 7	
TRR Mode		OP[7]	0B: Disabled (default) 1B: Enabled	

Note:
1. Unknown means that the device is not tested for tMAC and pass/fail value in unknown.
2. There is no restriction to number of activates.
3. MR24 OP [2:0] is set to zero.

3.3.26. MR25 Register Information (MA[7:0] = 19H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

Function	Register Type	Operand	Data	Notes
PPR Resource	Read	OP[7:0]	0B: PPR Resource is not available 1B: PPR Resource is available	

3.3.27. MR26:31 Register Information (MA[7:0] = 1AH:1FH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved							

3.3.28. MR32 Register Information (MA[7:0] = 20H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern “A” (default = 5AH)							

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	XB: An MPC command with OP[6:0]=0000011B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "5AH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)	1,2,3,4

1. The pattern contained in MR40 is contatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111B.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

3.3.29. MR33:39 Register Information (MA[7:0] = 21H:27H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Do Not Use							

3.3.30. MR40 Register Information (MA[7:0] = 28H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "B" (default = 3CH)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	XB: A default pattern "3CH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1,2,3,4

Notes:
1. The pattern contained in MR40 is contatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111B.
2. MR15 and MR22 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR22 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

3.3.31. MR41:47 Register Information (MA[7:0] = 29H:2FH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Do Not Use							

3.3.32. MR48:63 Register Information (MA[7:0] = 30H:3FH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Future Use							

4. LPDDR4 Command Definitions and Timing Diagrams

4.1. Activate Command

The ACTIVATE command is composed of two consecutive commands, Activate-1 command and Activate-2. Activate-1 command is issued by holding CS HIGH, CA0 HIGH and CA1 LOW at the first rising edge of the clock and Activate-2 command issued by holding CS HIGH, CA0 HIGH and CA1 HIGH at the first rising edge of the clock. The bank addresses BA0, BA1 and BA2 are used to select desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at t_{RCD} after the ACTIVATE command is issed. After a bank has been activated it must be precharged before another ACTIVATE commnand can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP} respectively. The minimum time interval between ACTIVATE commands to the same bank is determined by the RAS cycle time of the device(t_{RC}). The minimum time interval between ACTIVATE commands to different banks is t_{RRD}.

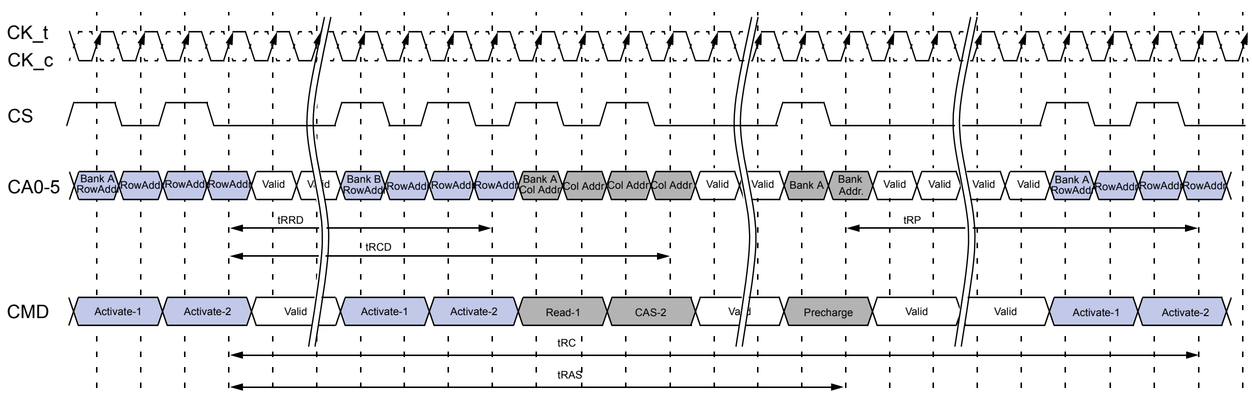


Figure - Activate Command Timing Example

Note : A PRECHARGE command uses t_{RPab} timing for all-bank PRECHARGE and t_{RPpb} timing for single-bank PRE-CHARGE. In this figure, t_{RP} is used to denote either all-bank PRECHARGE or a single-bank PRECHARGE.

4.1.1. 8-Bank Device Operation

Certain restrictions on operation of the 8-bank LPDDR4 devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is de-pendent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

an example of the rolling window, if RU(tFAW/tCK) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceeds the tFAW time.

The 8-Bank Device Precharge-All Allowance: tRP for a PRECHRGE ALL command must equal tRPab, which is greater than tRPpb.

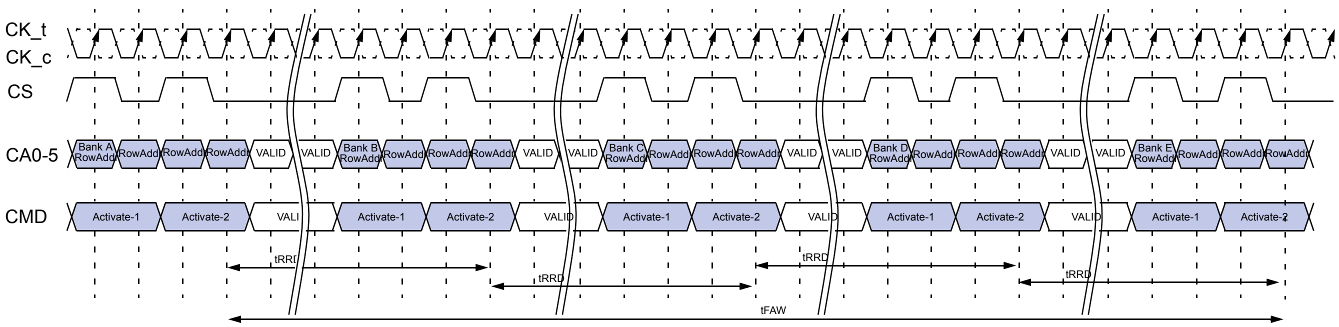


Figure - tFAW Timing Example

4.2. Read and Write access modes

After a bank has been activated, a read or write command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see Command Truth Table) at a rising edge of CK.

The LPDDR4-SDRAM provides a fast column access operation. A single Read or Write command will initiate a burst read or write operation, where data is transferred to/from the DRAM on successive clock cycles. Burst interrupts are not allowed, but the optimal burst length may be set on the fly (see command truth table).

4.3. Burst Read Operation

A burst Read command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be “0”, so that the starting burst address is always a multiple of four (ex. 0x0, 0x4, 0x8, 0xC). The read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL * tCK + tDQSCK + tDQSQ after the rising edge of Clock that completes a read command. The data strobe output is driven tRPRE before the first valid rising strobe edge.

The first data-bit of the burst is synchronized with the first valid (i.e. post-preamble) rising edge of the data strobe. Each subsequent dataout appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle postamble if the programmable post-amble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS_t and DQS_c.

Figure - Read Output Timing. 2tCK Preamble (toggling)

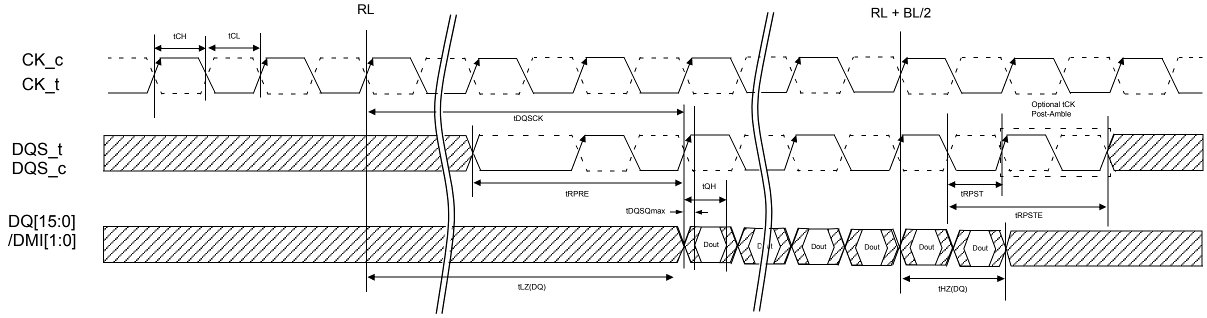


Figure - Read Output Timing. 2tCK Preamble (Non-toggling)

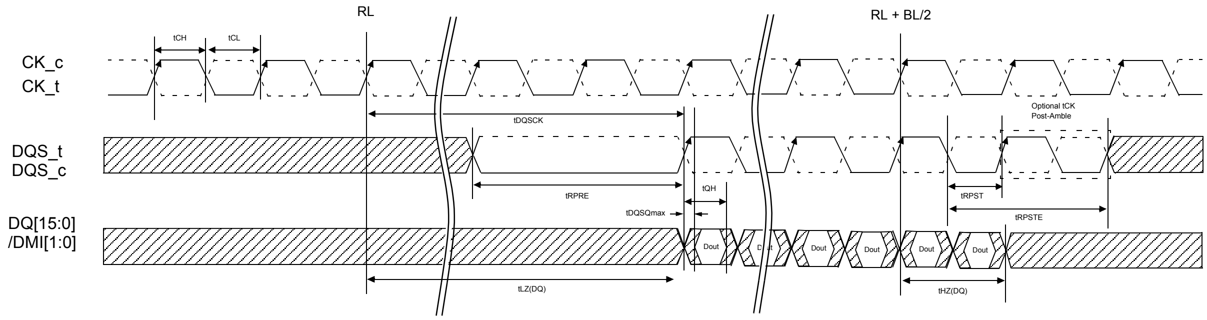
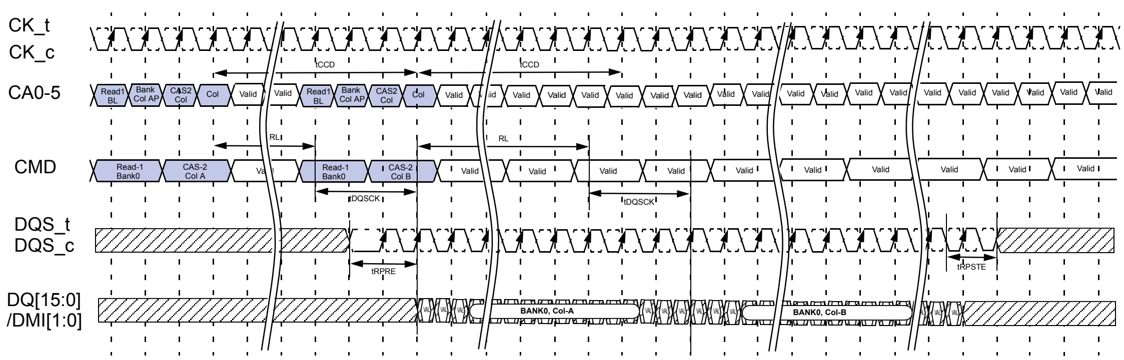
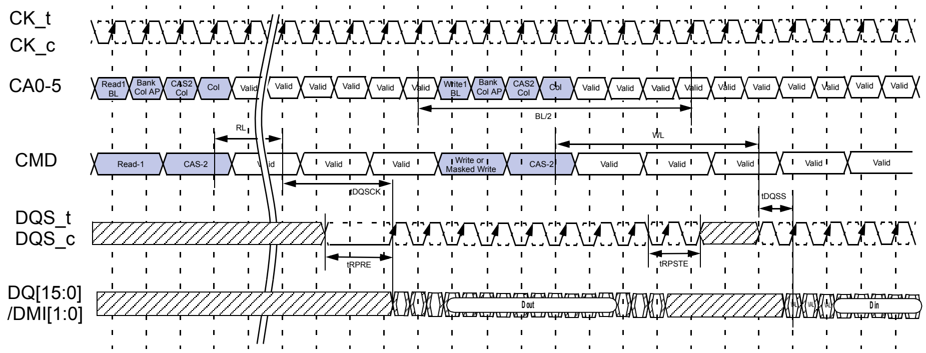


Figure - Burst Read Timing. BL=16, Toggling tRPRE, Extended tRPST



1. tDQSCK may span multiple clock periods.

Figure - Burst Read followed by Burst Write. BL=16, Non-toggling tRPRE, Extended tRPST



The minimum time from a Burst Read command to a Write or MASK WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE or MASK WRITE latency is defined with tRTW paramter and it is as following equation:

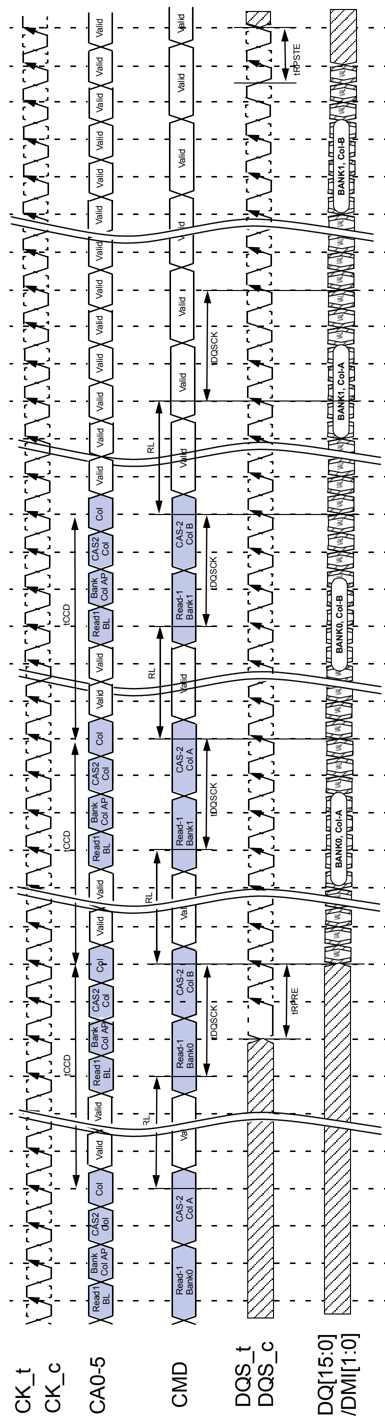
DQ ODT Disabled case; MR11 OP[2:0]=000b

tRTW = RL + RU(tDQSCK(max)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)

DQ ODT Enabled case; MR11 OP[2:0]≠000b

tRTW = RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon,min/tCK) + 1

Figure - Seamless Burst Read. BL=16, Toggling tRPRE, Extended tRPST



The seamless Burst READ operation is supported by placing a READ command at every tCCD interval for BL16 (or every 2 x tCCD for BL32). The seamless Burst READ can access any open bank.

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

4.4. Burst Write Operation

A burst WRITE command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. Column addresses C[3:2] should be driven LOW for Burst WRITE commands, and column addresses C[1:0] are not transmitted on the CA bus (and are assumed to be zero), so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the last rising edge of the clock that completes a write command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which tDQSS is measured. The first valid "latching" edge of DQS must be driven WL * tCK + tDQSS after the rising edge of Clock that completes a write command.

The LPDDR4-SDRAM uses an un-matched DQS-DQ path for lower power, so the DQS-strobe must arrive at the SDRAM ball prior to the DQ signal by the amount of tDQS2DQ. The DQS-strobe output is driven tWPRE before the first valid rising strobe edge. The tWPRE, write pre-amble, is required to be 2 x tCK at all frequency ranges. The DQS-strobe must be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data must be held for tDIVW (data input valid window) and the DQS must be periodically trained to stay centered in the tDIVW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of DQS
until the 16 or 32 bit data burst is complete. The DQS-strobe must remain active (toggling) for tWPST (WRITE post-amble) after the completion of the burst WRITE. After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS_t and DQS_c.

Figure - Data Input (Write) Timing. 2tCK Write Preamble

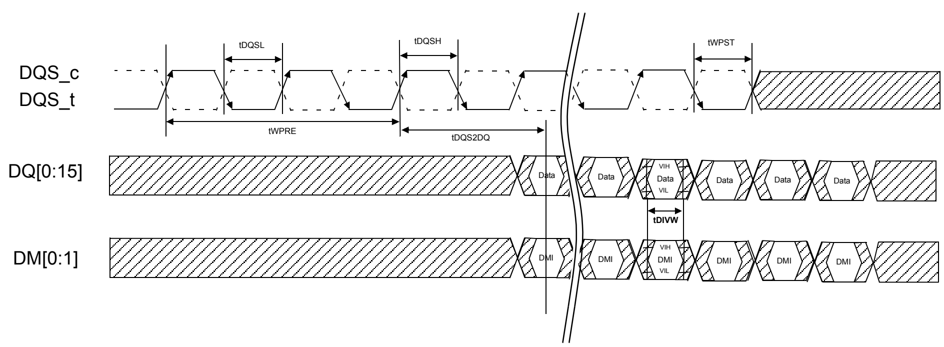
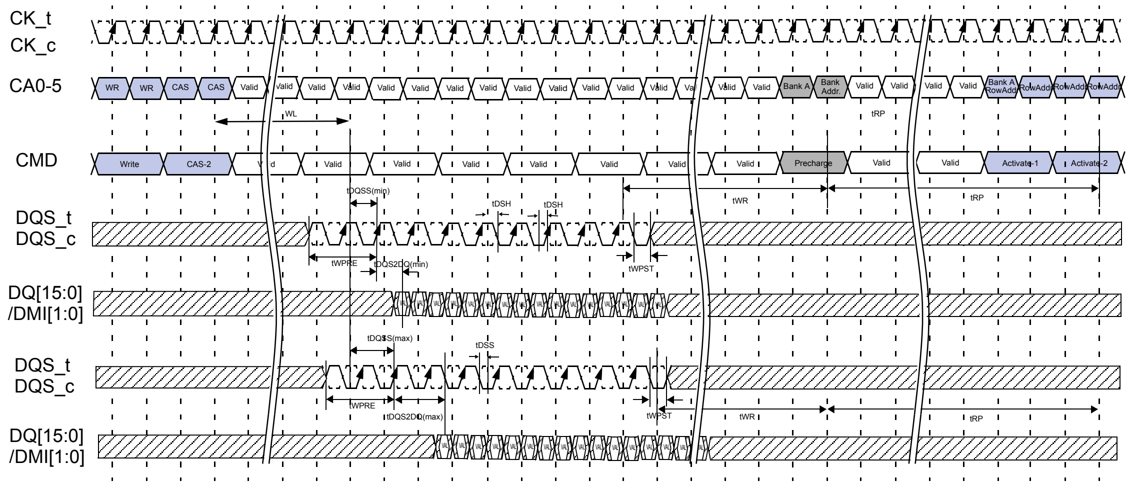
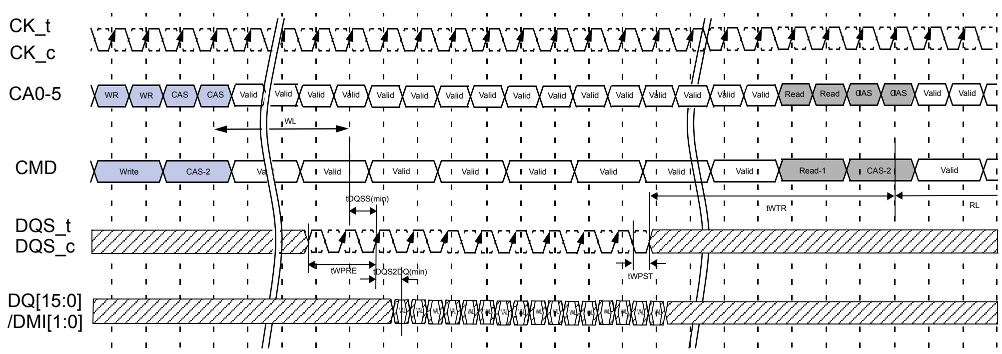


Figure - Burst Write Operation. BL=16, 2tCK tWPRE



1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWR/tCK)].
2. tWR starts at the rising edge of CK after the last latching edge of DQS.

Figure - Burst Write Followed by Burst Read. BL=16, 2tCK tWPRE



1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2. tWTR starts at the rising edge of CK after the last latching edge of DQS.

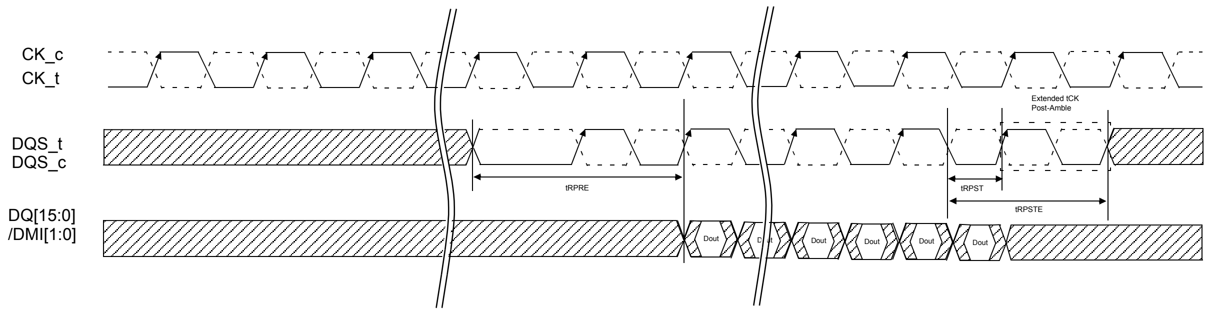
4.5. LPDDR4 Pre-amble and Post-amble

The DQS strobe for the LPDDR4-SDRAM requires a pre-amble prior to the first latching edge (the rising edge of DQS_t with DATA “valid”), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

For WRITE operations, a 2*tCK pre-amble for all frequencies.
For READ operations the pre-amble is 2*tCK, but the pre-amble is static (no-toggle) or toggling, selectable via mode register.

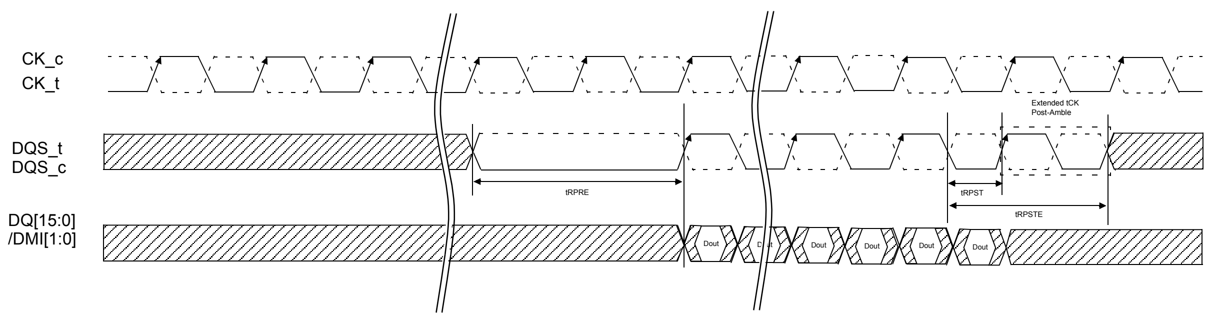
LPDDR4 will have a DQS Write post-amble of 0.5*tCK, and a DQS Read post-amble of 0.5*tCK (or extended to 1.5*tCK). Standard DQS post-amble will be 0.5*tCK driven by the memory controller for Writes and by the DRAM for Reads. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Read post-amble. The drawings below show examples of DQS Read post-amble for both standard (tRPST) and extended (tRPSTE) post-amble operation.

Figure - DQS Read Pre/Post-amble
(Shown with toggling pre-amble and extended post-amble)



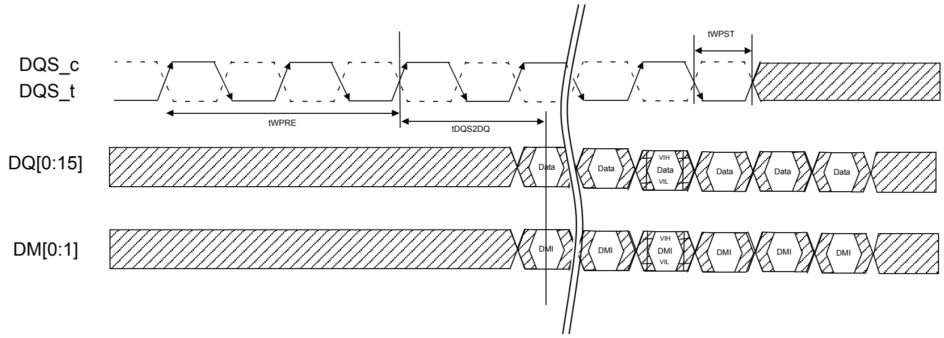
Note: DQS_t/DQS_c is “don’t care” prior to the start of tRPRE. No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tRPRE.

Figure - DQS Read Pre/Post-amble
(Shown with static pre-amble and extended post-amble)



Note: DQS_t/DQS_c is “don’t care” prior to the start of tRPRE. No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tRPRE.

Figure - DQS Write Pre/Post-amble
(Shown with 2*tCK pre-amble and 0.5*tCK post-amble)

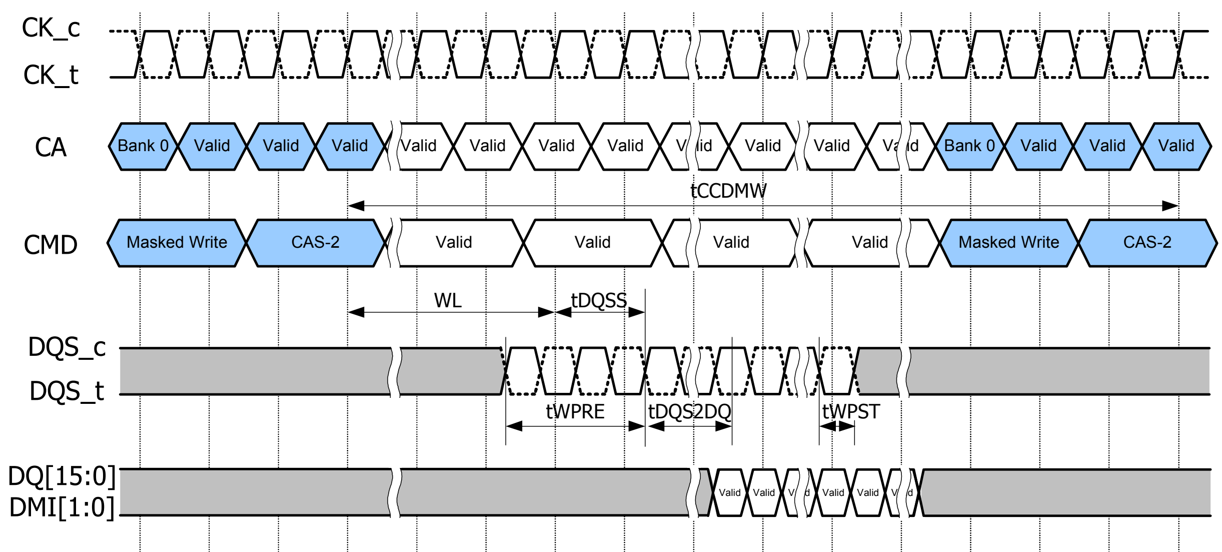


Note: DQS_t/DQS_c is "don't care" prior to the start of tWPRE. No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tWPRE.

4.6. Masked Write Operation

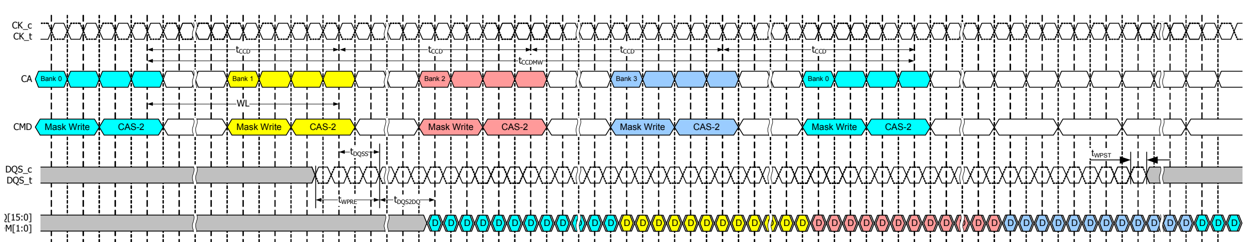
The LPDDR4-SDRAM requires that Write operations which include a byte mask anywhere in the burst sequence must use the Masked Write command. This allows the DRAM to implement efficient data protection schemes based on larger data blocks. The Masked Write-1 command is used to begin the operation, followed by a CAS-2 command. A Masked Write command to the same bank cannot be issued until tCCDMW is met, to allow the LPDDR4-SDRAM to finish the internal Read-Modify-Write. One Data Mask-Invert (DMI) pin is provided per byte lane, and the Data Mask-Invert timings match data bit (DQ) timing. See the section on "Data Mask Invert" for more information on the use of the DMI signal.

Figure - Masked Write Command - Same Bank (Shown with BL16, 2tCK Preamble)



Notes:
1. Masked Write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.

Figure - Masked Write Command - Different Bank (shown with BL16, 2tCK Preamble)



Notes:
1. Masked Write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.

4.6.1. Masked Write Timing constraints

Table - Masked Write Timing constraints - Same bank

Next CMD / Current CMD	Activate	Read (BL16 or 32)	Write (BL16 or 32)	Masked Write	Precharge
Activate	Illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
Read (BL16)	Illegal	8[1)]	RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+tRPST	RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+tRPST	BL/2+max{(8,RU(tRTP/ tCK)}-8
Read (BL32)	Illegal	16[2)]	RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+tRPST	RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+tRPST	BL/2+max{(8,RU(tRTP/ tCK)}-8
Write (BL16)	Illegal	WL+1+BL/2 +RU(tWTR/tCK)	8[1)]	tCCDMW[3)]	WL+ 1 + BL/2 +RU(tWR/tCK)
Write (BL32)	Illegal	WL+1+BL/2 +RU(tWTR/tCK)	16[2)]	tCCDMW + 8[4)]	WL+ 1 + BL/2 +RU(tWR/tCK)
Masked Write	Illegal	WL+1+BL/2 +RU(tWTR/tCK)	tCCD	tCCDMW[3)]	WL+ 1 + BL/2 +RU(tWR/tCK)
Precharge	RU(tRP/tCK), RU(tRPab/tCK)	Illegal	Illegal	Illegal	4

Notes:
1) In the case of BL = 16, tCCD is 8*tCK.
2) In the case of BL = 32, tCCD is 16*tCK.
3) tCCDMW = 32*tCK (4*tCCD at BL=16)
4) Write with BL=32 operation has 8*tCK longer than BL =16.
5) Units : tCK

Table - Masked Write Timing constraints - Different bank

Next CMD / Current CMD	Activate	Read (BL16 or 32)	Write (BL16 or 32)	Masked Write (BL16)	Precharge
Activate	RU(tRRD/tCK)	4	4	4	2
Read (BL16)	4	8[1)]	RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+tRPST	RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+tRPST	2
Read (BL32)	4	16[1)]	RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+tRPST	RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+tRPST	2
Write (BL16)	4	WL+1+BL/2 +RU(tWTR/tCK)	8[1)]	8[1)]	2
Write (BL32)	4	WL+1+BL/2 +RU(tWTR/tCK)	16[1)]	16[1)]	2
Masked Write	4	WL+1+BL/2 +RU(tWTR/tCK)	8[1)]	8[1)]	2
Precharge	4	4	4	4	4

Notes:
1) In the case of BL = 16, tCCD is 8*tCK.
2) In the case of BL = 32, tCCD is 16*tCK.
3) Units : tCK

4.7. DMI

4.7.1. LPDDR4 Data Mask (DM) and Data Bus Inversion (DBIdc) Function

LPDDR4 SDRAM supports the function of Data Mask and Data Bus inversion. Its details are shown below.

- LPDDR4 device supports Data Mask (DM) function for Write operation.
- LPDDR4 device supports Data Bus Inversion (DBIdc) function for Write and Read operation.
- LPDDR4 supports DM and DBIdc function with a byte granularity.
- DBIdc function during Write or Masked Write can be enabled or disabled through MR3 OP[7].
- DBIdc function during Read can be enabled or disabled through MR3 OP[6].
- DM function during Masked Write can be enabled or disabled through MR13 OP[5].
- LPDDR4 device has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals per channel.
- DMI signal is a bi-directional DDR signal and is sampled along with the DQ signals for Read and Write or Masked Write operation.

There are eight possible combinations for LPDDR4 device with DM and DBIdc function. Table below describes the functional behavior for all combinations.

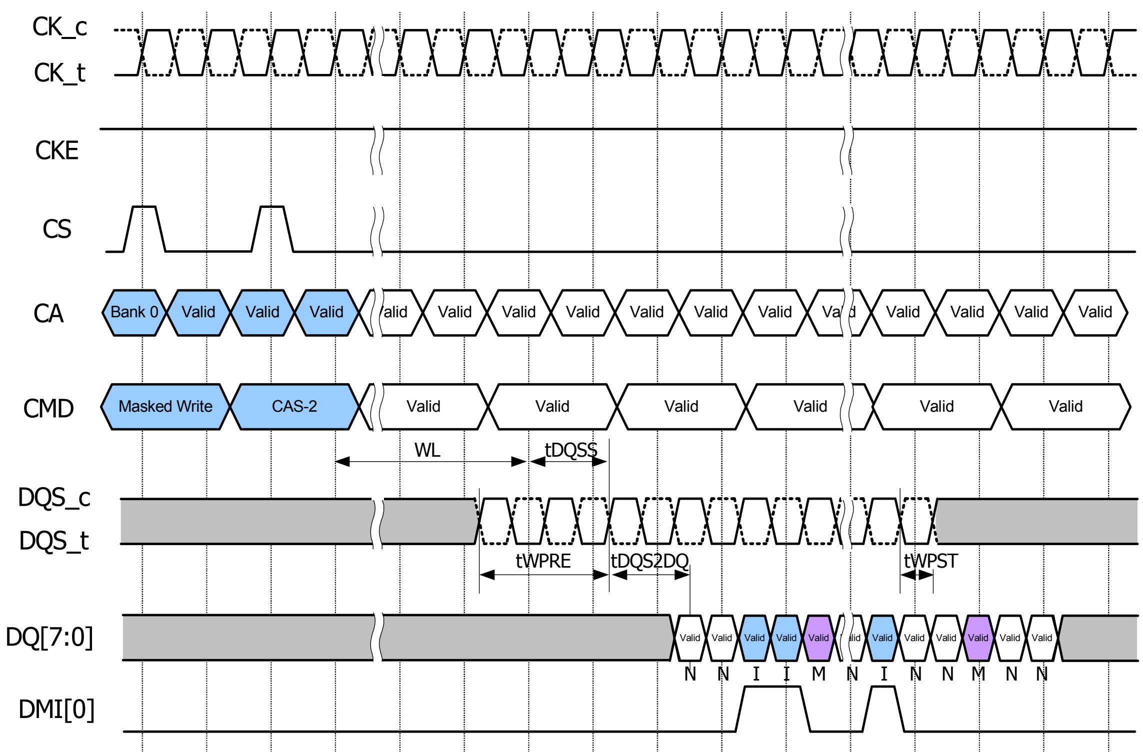
Table - Function Behaviour of DMI Signal During Write, Masked Write and Read Operation

DM Fuction	Write DBIdc Fuction	Read DBIdc Fuction	DMI Signal during Write Command	DMI Signal during Masked Write Command	DMI Signal during Read	DMI Signal during MPC [WR FIFO]	DMI Signal during MPC [RD FIFO]	DMI Signal during MPC [DQ Read calibration]	DMI Signal during MRR Command
Disable	Disable	Disable	Note: 1	Note: 1, 3	Note: 2	Note: 1	Note: 2	Note: 2	Note: 2
Disable	Enable	Disable	Note: 4	Note: 3	Note: 2	Note: 9	Note: 10	Note: 11	Note: 2
Disable	Disable	Enable	Note: 1	Note: 3	Note: 5	Note: 9	Note: 10	Note: 11	Note: 12
Disable	Enable	Enable	Note: 4	Note: 3	Note: 5	Note: 9	Note: 10	Note: 11	Note: 12
Enable	Disable	Disable	Note: 6	Note: 7	Note: 2	Note: 9	Note: 10	Note: 11	Note: 2
Enable	Enable	Disable	Note: 4	Note: 8	Note: 2	Note: 9	Note: 10	Note: 11	Note: 2
Enable	Disable	Enable	Note: 6	Note: 7	Note: 5	Note: 9	Note: 10	Note: 11	Note: 12
Enable	Enable	Enable	Note: 4	Note: 8	Note: 5	Note: 9	Note: 10	Note: 11	Note: 12

1. DMI input signal is a don't care. DMI input receivers are turned OFF.
2. DMI output drivers are turned OFF.
3. Masked Write Command is not allowed and is considered an illegal command as DM function is disabled.
4. DMI signal is treated as DBI signal and it indicates whether DRAM needs to invert the Write data received on DQs within a byte. The LPDDR4 device inverts Write data received on the DQ inputs in case DMI was sampled HIGH, or leaves the Write data non-inverted in case DMI was sampled LOW.
5. The LPDDR4 DRAM inverts Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.
6. The LPDDR4 DRAM does not perform any mask operation when it receives Write command. During the Write burst associated with Write command, DMI signal must be driven LOW.
7. The LPDDR4 DRAM requires an explicit Masked Write command for all masked write operations. DMI signal is treated as DM signal and it indicates which bit time within the burst is to be masked. When DMI signal is HIGH, DRAM masks that bit time across all DQs associated within a byte. All DQ input signals within a byte are don't care (either HIGH or LOW) when DMI signal is HIGH. When DMI signal is LOW, the LPDDR4 DRAM does not perform mask operation and data received on DQ input is written to the array.
8. The LPDDR4 DRAM requires an explicit Masked Write command for all masked write operations. The LPDDR4 device masks the Write data received on the DQ inputs if the total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively) is equal to or greater than five and DMI signal is LOW. Otherwise the LPDDR4 DRAM does not perform mask operation and treats it as a legal DBI pattern; DMI signal is treated as DBI signal and data received on DQ input is written to the array.

9. DMI signal is treated as a training pattern. The LPDDR4 SDRAM does not perform any mask operation and does not invert Write data received on the DQ inputs.
10. DMI signal is treated as a training pattern. The LPDDR4 SDRAM returns DMI pattern written in WR-FIFO.
11. DMI signal is treated as a training pattern. For more details, see MPC RD DQ Calibration session.
12. DBI may apply or may not apply during normal MRR. It's vendor specific. If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DBI pin status should be low.
    If read DBI is enable with MRS and vendor can support the DBI during MRR, the LPDDR4 DRAM inverts Mode Register Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.

Figure - Masked Write Operation w/ Write DBI Enabled; DM Enabled



Valid — Input data is written to DRAM cell.

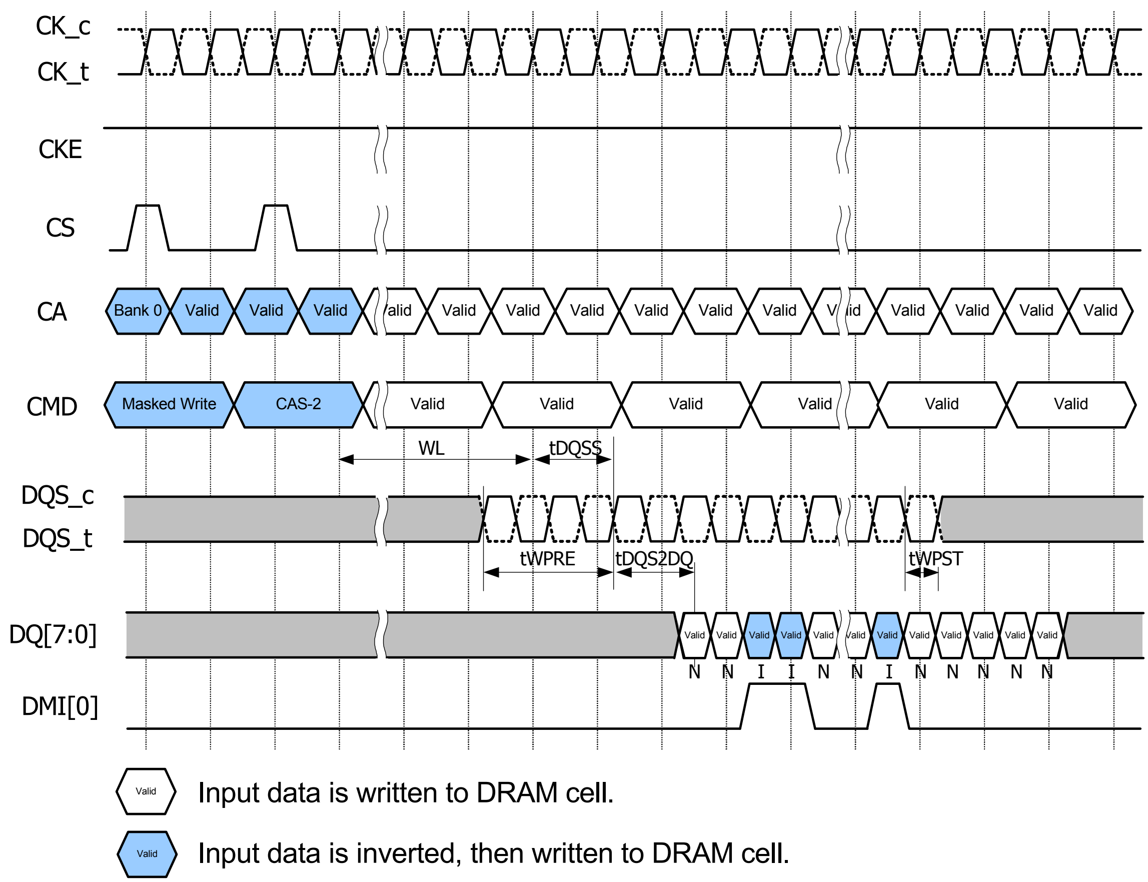
Valid — Input data is inverted, then written to DRAM cell.

Valid — Input data is masked. The total count on DQ[7:2] is equal or greater than five.

Notes:
1. Data Mask (DM) is Enabled; MR13 OP[5]=1, Data Bus Inversion (DBI) Write is Enabled; MR3 OP[7]=1.

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

Figure - Write Command w/ Write DBI Enabled; DM Disabled



Notes:
1. Data Mask (DM) is Disabled; MR13 OP[5]=0, Data Bus Inversion (DBI) Write is Enabled; MR3 OP[7]=1.

4.8. Precharge Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS, and CA[5:0] in the proper state as defined by the Command Truth Table. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access tRPab after an all-bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR4 devices can meet the instantaneous current demands, the row-precharge time for an all-bank PRECHARGE (tRPab) is longer than the perbank precharge time (tRPpb).

Table - Precharge Bank Selection

AB (CA[5], R1)	BA2 (CA[2], R2)	BA1 (CA[1], R2)	BA0 (CA[0], R2)	Precharged Bank(s)
0	0	0	0	Bank 0 Only
0	0	0	1	Bank 1 Only
0	0	1	0	Bank 2 Only
0	0	1	1	Bank 3 Only
0	1	0	0	Bank 4 Only
0	1	0	1	Bank 5 Only
0	1	1	0	Bank 6 Only
0	1	1	1	Bank 7 Only
1	Valid	Valid	Valid	All banks

4.8.1. Burst Read Operation followed by Precharge

The PRECHARGE command can be issued as early as BL/2 clock cycles after a READ command, but PRECHARGE cannot be issued until after tRAS is satisfied. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (tRP) has elapsed. The minimum READ-to-PRECHARGE time must also satisfy a minimum analog time from the 2nd rising clock edge of the CAS-2 command. tRTP begins BL/2 . 8 clock cycles after the READ command. For LPDDR4 READ-to-PRECHARGE timings see Table "Timing Between Commands (Precharge and Auto-Precharge)".

Figure - Burst Read followed by Precharge (BL16, toggling pre-amble)

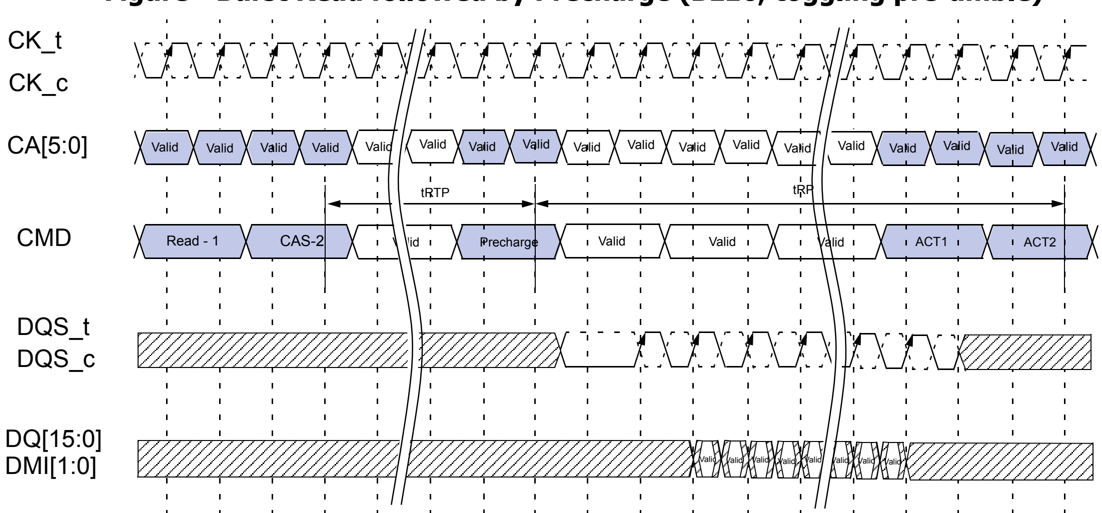
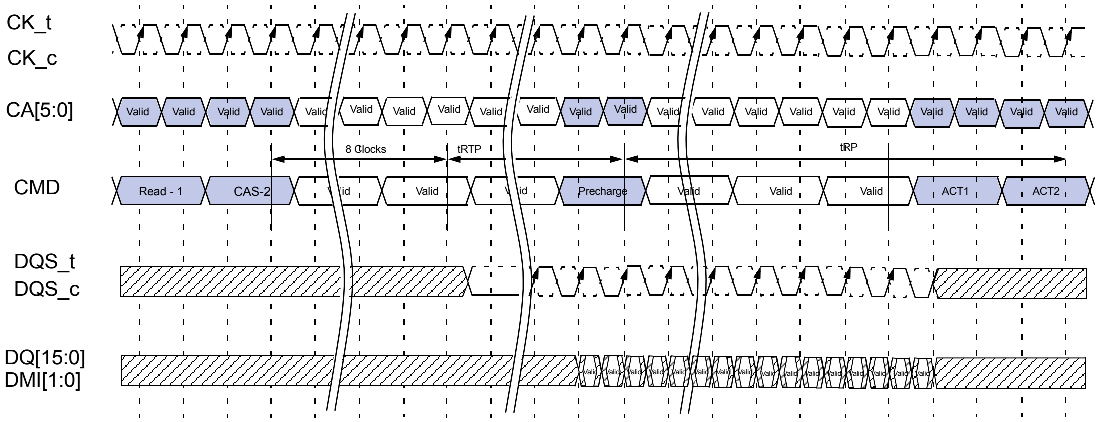


Figure - Burst Read followed by Precharge (BL32, Toggling Preamble)

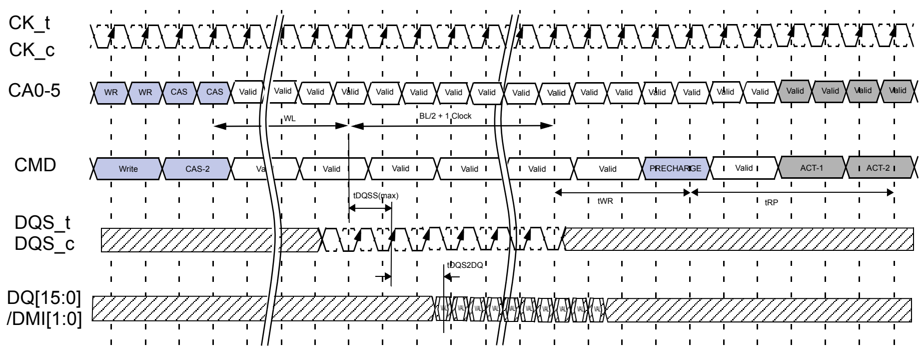


4.8.2. Burst Write followed by Precharge

A Write Recovery time (tWR) must be provided before a PRECHARGE command may be issued. This delay is referenced from the next rising edge of CK_t after the last latching DQS clock of the burst.

LPDDR4-SDRAM devices write data to the memory array in prefetch multiples (prefetch=16). An internal WRITE operation can only begin after a prefetch group has been clocked, so tWR starts at the prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles.

Figure - Burst Write followed by Precharge (BL16, 2tCK preamble)



4.8.3. Auto Precharge operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the Auto-PRECHARGE function. When a READ, WRITE or Masked Write command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ, WRITE or Masked Write cycle.

If AP is LOW when the READ, WRITE or Masked Write command is issued, then the normal READ, WRITE or Masked Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ, WRITE or Masked Write command is issued, the Auto-PRECHARGE function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

4.8.3.1. Burst Read with Auto-Precharge

If AP is HIGH when a READ command is issued, the READ with Auto-PRECHARGE function is engaged. An internal precharge procedure starts a following delay time after the READ command. And this delay time depends on BL setting.

BL = 16: tRTP

BL = 32: 8tCK + tRTP

For LPDDR4 Auto-PRECHARGE calculations, see Table 2. Following an Auto-PRECHARGE operation, an ACTIVATE command can be issued to the same bank if the following two conditions are both satisfied:

a. The RAS precharge time (tRP) has been satisfied from the clock at which the Auto-PRECHARGE began, or

b. The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Figure - Burst Read with Auto-Precharge (BL16, Toggling preamble)

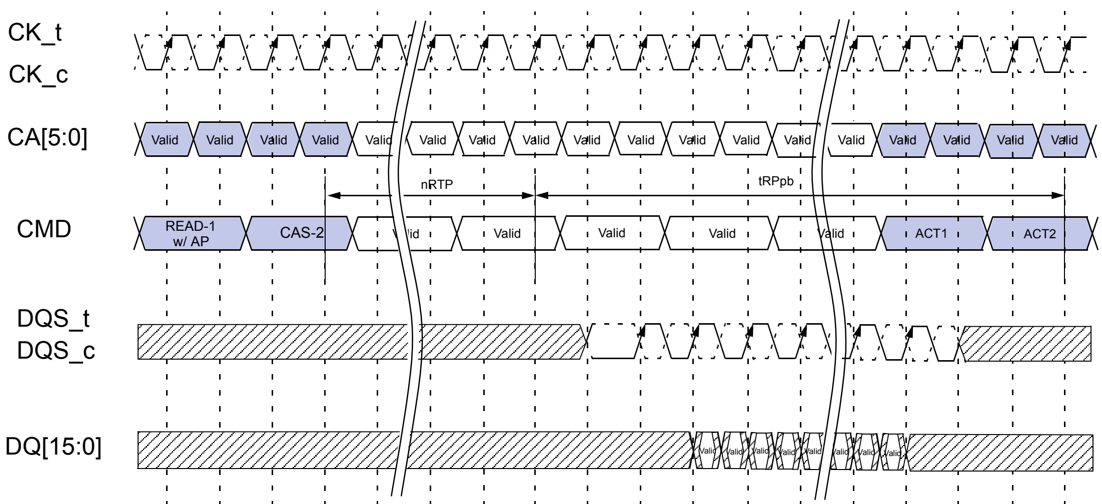
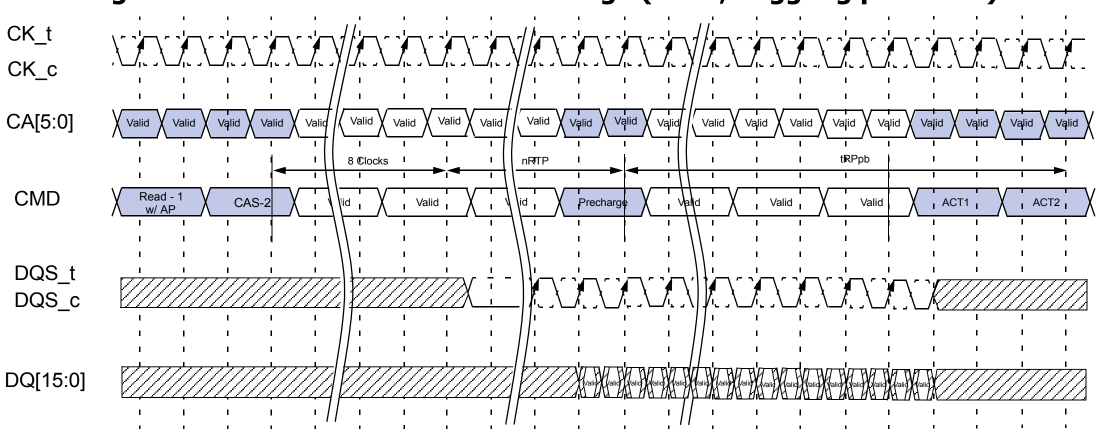


Figure - Burst Read with Auto-Precharge (BL32, Toggling preamble)



4.8.3.2. Burst Write with Auto-Precharge

If AP is HIGH when a WRITE command is issued, the WRITE with Auto-PRECHARGE function is engaged. The device starts an Auto-PRECHARGE on the rising edge tWR cycles after the completion of the Burst WRITE.

Following a WRITE with Auto-PRECHARGE, an ACTIVATE command can be issued to the same bank if the following conditions are met:

a. The RAS precharge time (tRP) has been satisfied from the clock at which the Auto-PRECHARGE began, and

b. The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Table - Burst Write with Auto-Precharge (BL16, 2tCK preamble)

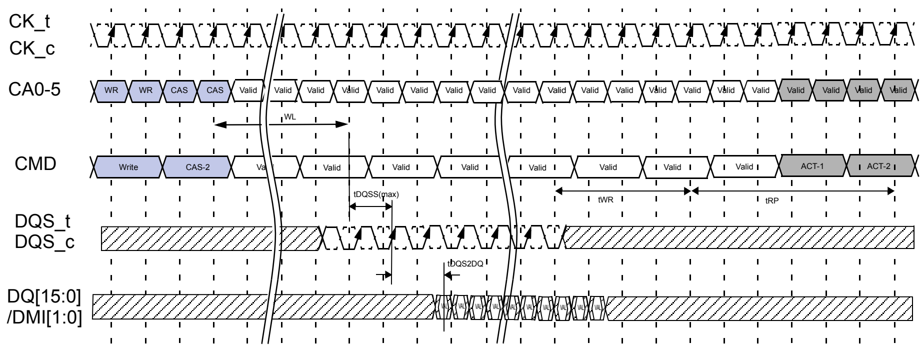


Table - Timing Between Commands (Precharge and Auto-Precharge) - DQ ODT is Disabled

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
Read (BL16)	Precharge (to same bank as Read)	tRTP	tCK	1,6
	Precharge All	tRTP	tCK	1,6
Read (BL32)	Precharge (to same bank as Read)	8*tCK + tRTP	tCK	1,6
	Precharge All	8*tCK + tRTP	tCK	1,6
Read w/ AP (BL16)	Precharge (to same bank as Read w/ AP)	nRTP	tCK	1,10
	Precharge All	nRTP	tCK	1,10
	Activate (to same bank as Read w/ AP)	nRTP + tRPpb	tCK	1,8,10
	Write or Write w/ AP (same bank)	Illegal	-	3
	Masked Write or Masked Write w/ AP (same bank)	Illegal	-	
	Write or Write w/ AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE	tCK	3,4,5
	Masked Write or Masked Write w/ AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE	tCK	3,4,5

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
Read w/ AP (BL16)	Read or Read w/ AP (same bank)	Illegal	-	
	Read or Read w/ AP (different bank)	BL/2	tCK	3
Read w/ AP (BL32)	Precharge (to same bank as Read w/ AP)	8*tCK + nRTP	tCK	1,10
	Precharge All	8*tCK + nRTP	tCK	1,10
	Activate (to same bank as Read w/ AP)	8*tCK + nRTP + tRPpb	tCK	1,8,10
	Write or Write w/ AP (same bank)	Illegal	-	
	Masked Write or Masked Write w/ AP (same bank)	Illegal	-	
	Write or Write w/ AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE	tCK	3,4,5
	Masked Write or Masked Write w/ AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE	tCK	3,4,5
	Read or Read w/ AP (same bank)	Illegal	-	
	Read or Read w/ AP (different bank)	BL/2	tCK	3
Write (BL16 & BL32)	Precharge (to same bank as Masked Write)	WL + BL/2 + tWR + 1	tCK	1,7
	Precharge All	WL + BL/2 + tWR + 1	tCK	1,7
Masked Write	Precharge (to same bank as Masked Write)	WL + BL/2 + tWR + 1	tCK	1,7
	Precharge All	WL + BL/2 + tWR + 1	tCK	1,7
Write w/ AP	Precharge (to same bank as Write w/ AP)	WL + BL/2 + nWR + 1	tCK	1,11
	Precharge All	WL + BL/2 + nWR + 1	tCK	1,11
	Activate (to same bank as Write w/ AP)	WL + BL/2 + nWR + 1 + tRPpb	tCK	1,8,11
	Write or Write w/ AP (same bank)	Illegal	-	
	Write or Write w/ AP (different bank)	BL/2	tCK	3
	Read or Read w/ AP (same bank)	Illegal	-	
	Read or Read w/ AP (different bank)	WL + BL/2 + tWTR + 1	tCK	3,9

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
Masked Write w/ AP	Precharge (to same bank as Masked Write w/ AP)	WL + BL/2 + nWR + 1	tCK	1,11
	Precharge all	WL + BL/2 + nWR + 1	tCK	1,11
	Activate (to same bank as Masked Write w/ AP)	WL + BL/2 + nWR + 1 + tRPpb	tCK	1,8,11
	Write or Write w/ AP (same bank)	Illegal	-	
	Masked Write or Masked Write w/ AP (same bank)	Illegal	-	
	Write or Write w/ AP (different bank)	BL/2	tCK	3
	Masked Write or Masked Write w/ AP (differenet bank)	BL/2	tCK	3
	Read or Read w/ AP (same bank)	Illegal	-	
	Read or Read w/ AP (different bank)	WL + BL/2 + tWTR + 1	tCK	3,9
Precharge	Precharge (to same bank as Precharge)	4	tCK	1
	Precharge All	4	tCK	1
Precharge All	Precharge	4	tCK	1
	Precharge All	4	tCK	1

Notes
1. For a given bank, the precharge period should be counted from the latest precharge command, whether per-bank or all-bank, issued to that bank. The precharge period is satisfied tRP after that latest precharge command.
2. Any command issued during the minimum delay time as specified in the table above is illegal.
3. After READ w/AP, seamless read operations to different banks are supported. After WRITE w/AP or Masked Write w/AP, seamless write operations to different banks are supported. READ, WRITE, and Masked Write operations may not be truncated or interrupted.
4. tRPST values depend on MR1 OP[7] repectively
5. tWPRE values depend on MR1 OP[2] respectively
6. Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRTP(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRTP[ns] / tCK[ns])
7. Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWR[ns] / tCK[ns])
8. Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRPpb(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRPpb[ns] / tCK[ns])
9. Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWTR(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWTR[ns] / tCK[ns])
10. For Read w/AP the value is nRTP which is defined in Mode Register 2.
11. For Write w/AP the value is nWR which is defined in Mode Register 1.

Table - Timing Between Commands (Precharge and Auto-Precharge) - DQ ODT is Enabled

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
Read w/ AP (BL16)	Write or Write w/ AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)	tCK	2,3
	Masked Write or Masked Write w/ AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)	tCK	2,3
Read w/ AP (BL32)	Write or Write w/ AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE	tCK	2,3
	Masked Write or Masked Write w/ AP (different bank)	RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE	tCK	2,3

Notes
1. The rest of Precharge and Auto-Precharge timings are as same as DQ ODT disabled case.
2. After READ w/AP, seamless read operations to different banks are supported. READ, WRITE, and Masked Write operations may

not be truncated or interrupted.
3. tRPST values depend on MR1 OP[7] respectively.

4.9. Refresh command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of the clock. Per-bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. All-bank REFRESH is initiated with CA5 HIGH at the first rising edge of the clock.

A per-bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1 and CA2 at the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1 and bank address BA2 is transferred on CA2. A per-bank REFRESH command (REFpb) to the eight banks can be issued in any order. e.g. REFpb commands are issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per-bank REFRESH command the controller can send another set of per-bank REFRESH commands in the same order or a different order. e.g. REFpb commands are issued in the following order that is different from the previous order: 7-1-3-5-0-4-2-6. One of the possible order can also be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all eight banks have been refreshed using the per-bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. REFab command also synchronizes the counter between the controller and SDRAM to zero. The SDRAM device can be placed in self-refresh or a REFab command can be issued at any time without cycling through all eight banks using per-bank REFRESH command. After the bank count is synchronized to zero the controller can issue per-bank REFRESH commands in any order as described above.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met:
- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after the prior PRECHARGE command to that bank
- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.
After issuing REFpb, these conditions must be met:
- tRFCpb must be satisfied before issuing a REFab command
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank
- tRFCpb must be satisfied before issuing another REFpb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:
- tRFCab has been satisfied following the prior REFab command
- tRFCpb has been satisfied following the prior REFpb command
- tRP has been satisfied following the prior PRECHARGE commands.

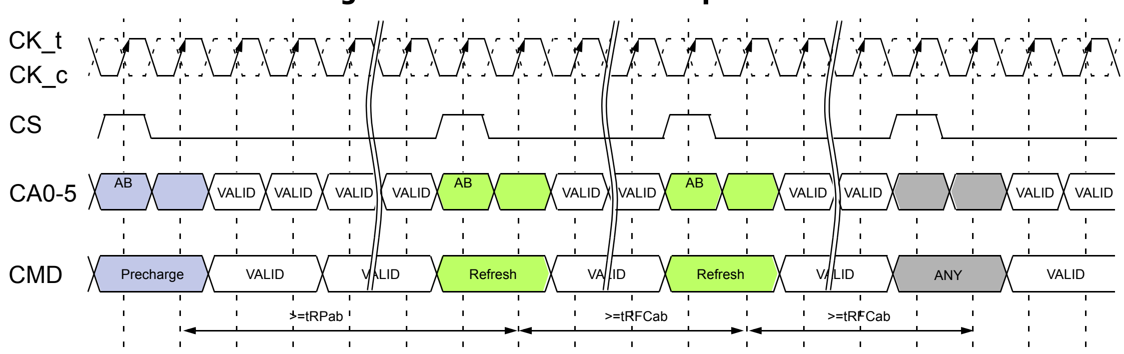
When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:
- tRFCab latency must be satisfied before issuing an ACTIVATE command
- tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Table - REFRESH Command Scheduling Seperation requirements

Symbol	minimum delay from	to	Notes
tRFCab	REFab	REFab	
		Activate command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate command to same bank as REFpb	
		REFpb	
tRRD	REFpb	Activate command to different bank than REFpb	
	Activate	REFpb	1
		Activate command to different bank than prior Activate command	

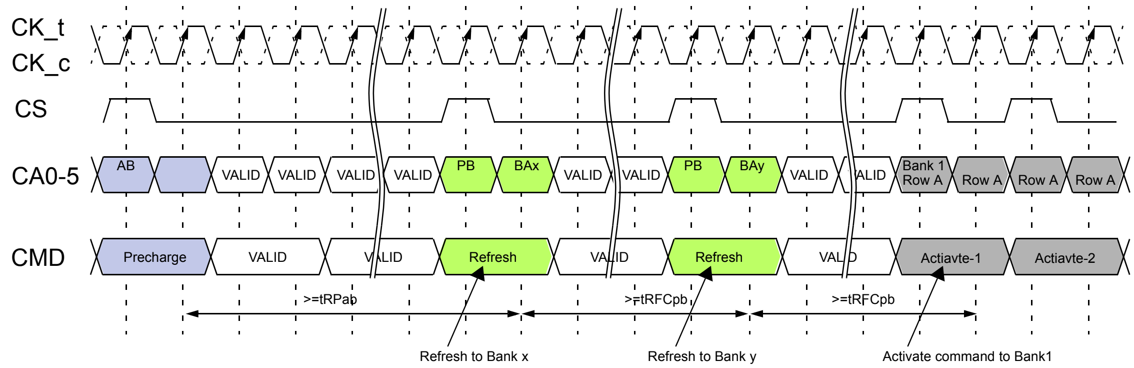
Note:
1. A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

Figure - All-Bank REFRESH Operation



PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

Figure - Per-Bank REFRESH Operation



1. Operations to banks other than the bank being refreshed are supported during the tRFCpb period.

In general, a Refresh command needs to be issued to the LPDDR4 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR4 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed and maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in the table below. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI. At any given time, a maximum of 16 REF commands can be issued within 2 x tREFI.
Self-Refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight. During Self-Refresh Mode, the number of postponed or pulled-in REFcommands does not change.

Table - Legacy Refresh Command Timing Constraints

MR4 OP[2:0]	Refresh rate	Max. No. of pulled in or postponed REFab	Max. interval between two REFab	Max. No. of REFab within max(2*tREFI*Refresh rate multiplier, 16*tRFC)	Per-bank Refresh
000B	Low Temp. Limit	N/A	N/A	N/A	N/A
001B	4 x tREFI	8	9 x 4 x tREFI	16	1/8 of REFab
010B	2 x tREFI	8	9 x 2 x tREFI	16	1/8 of REFab
011B	1 x tREFI	8	9 x tREFI	16	1/8 of REFab
100B	0.5 x tREFI	8	9 x 0.5 x tREFI	16	1/8 of REFab
101B	0.25 x tREFI	8	9 x 0.25 x tREFI	16	1/8 of REFab
110B	0.25 x tREFI	8	9 x 0.25 x tREFI	16	1/8 of REFab
111B	High Temp. Limit	N/A	N/A	N/A	N/A

Table - Modified Refresh Command Timing Constraints

MR4 OP[2:0]	Refresh rate	Max. No. of pulled in or postponed REFab	Max. interval between two REFab	Max. No. of REFab within max(2*tREFI*Refresh rate multiplier, 16*tRFC)	Per-bank Refresh
000B	Low Temp. Limit	N/A	N/A	N/A	N/A
001B	4 x tREFI	2	9 x 4 x tREFI	16	1/8 of REFab
010B	2 x tREFI	4	9 x 2 x tREFI	16	1/8 of REFab
011B	1 x tREFI	8	9 x tREFI	16	1/8 of REFab
100B	0.5 x tREFI	8	9 x 0.5 x tREFI	16	1/8 of REFab
101B	0.25 x tREFI	8	9 x 0.25 x tREFI	16	1/8 of REFab
110B	0.25 x tREFI	8	9 x 0.25 x tREFI	16	1/8 of REFab
111B	High Temp. Limit	N/A	N/A	N/A	N/A

Notes:
1. For any thermal transition phase where Refresh mode is transitioned to either 2x tREFI or 4x tREFI, DRAM will support 8 postponed refresh for maximum of 15.6us after MR4 OP[2:0] is read-out by host. After this time, DRAM supports # of postponed refresh as noted in the table.

Figure - Postponing Refresh Commands (Example)

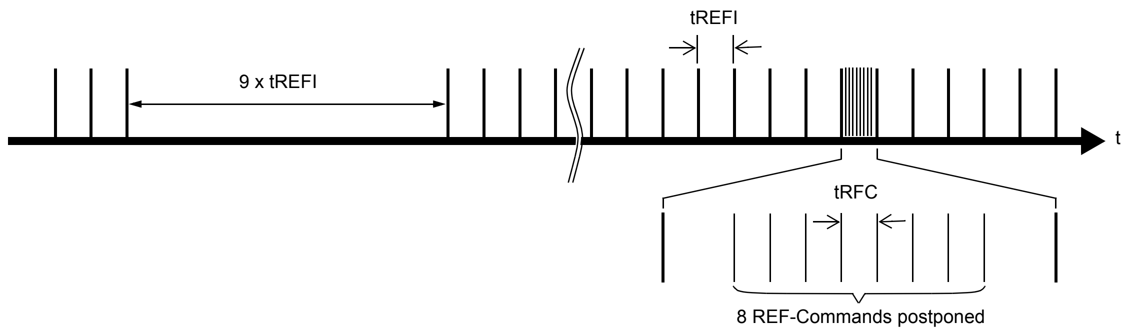
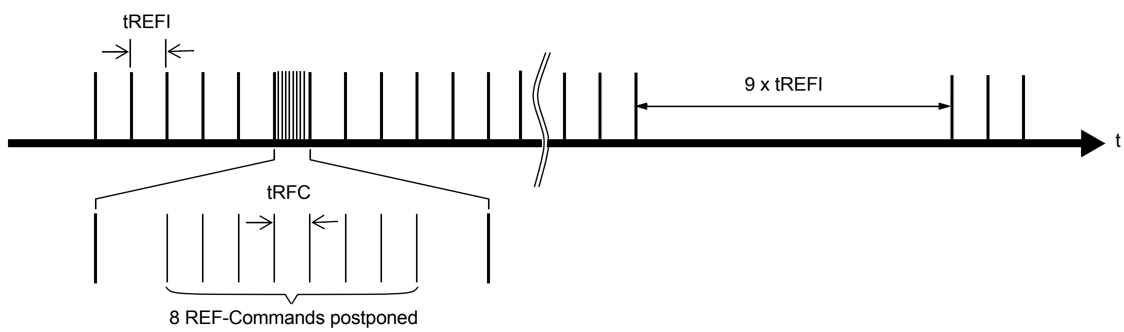


Figure - Pulling-in Refresh Commands (Example)



PDF-XChange Viewer Click to buy NOW! www.docu-track.com

4.10. LPDDR4 Refresh Requirements by Device Density

Density		Symbol	4Gb	6Gb	8Gb	12Gb	16Gb	Unit
Density per channel			2Gb	3Gb	4Gb	6Gb	8Gb	-
Number of Banks			8					-
Refresh Window 1 x tREFI		tREFW	32					ms
Refresh Window 0.5 x tREFI		tREFW	16					ms
Refresh Window 0.25 x tREFI		tREFW	8					ms
Required number of REFRESH commands		R	8,192					-
Average Refresh Interval 1 x tREFI	REFab	tREFI	3.906					us
	REFpb	tREFIpb	488					ns
Average Refresh Interval 0.5 x tREFI	REFab	tREFI	1.953					us
	REFpb	tREFIpb	244					ns
Average Refresh Interval 0.25 x tREFI	REFab	tREFI	0.977					us
	REFpb	tREFIpb	122					ns
Refresh Cycle Time (All Banks)		tRFCab	130	180	180	TBD	TBD	ns
Refresh Cycle Time (per Bank)		tRFCpb	60	90	90	TBD	TBD	ns

Notes:
1. Refresh is defined with a 32ms window, which refreshes . of the channel (or die). The entire channel (or die) is refreshed every 64ms.
2. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the LPDDR4 DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

4.11. Self Refresh Operation

4.11.1. Self Refresh Entry and Exit

The Self Refresh command can be used to retain data in the LPDDR4 SDRAM, the SDRAM retains data without external Refresh command. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh is entered by Self Refresh Entry Command defined by having CKE High, CS High, CA0 Low, CA1 Low, CA2 Low; CA3 High; CA4 High, CA5 Valid (Valid that means it is Logic Level, High or Low) for the first rising edge and CKE High, CS Low, CA0 Valid, CA1 Valid, CA2 Valid, CA3 Valid, CA4 Valid, CA5 Valid at the second rising edge of the clock. Self Refresh command is only allowed when SDRAM is idle state.

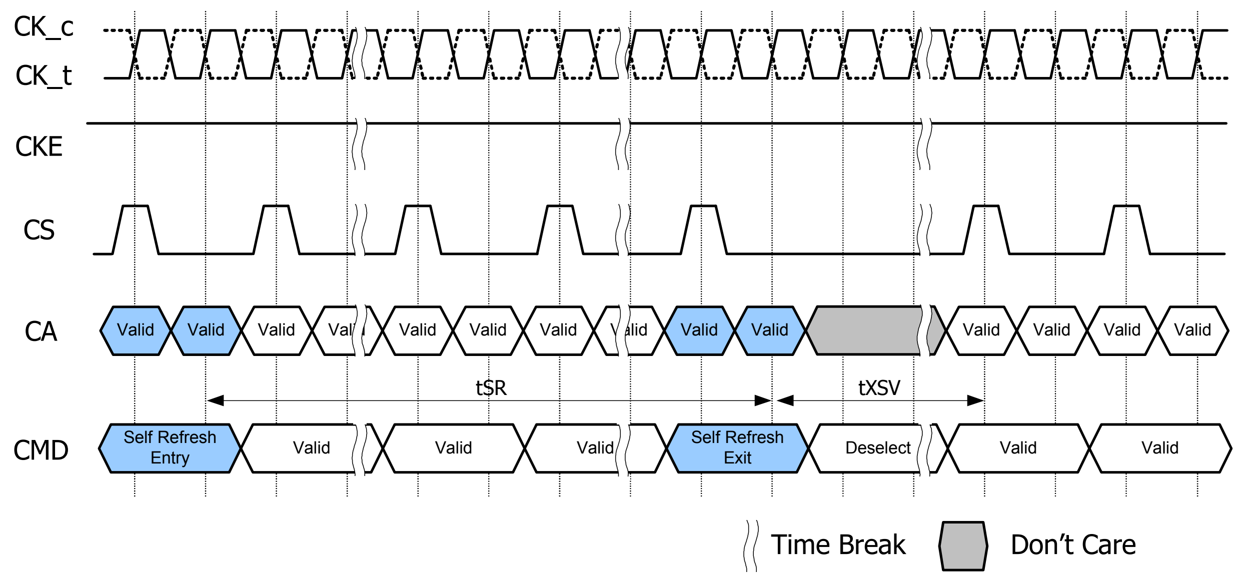
During Self Refresh mode, external clock input is needed and all input pin of SDRAM are activated.
SDRAM can accept the following commands, MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 except PASR Bank/Segment setting.

LPDDR4 SDRAM can operate in Self Refresh in both the standard or elevated temperature ranges. SDRAM will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperatures.

For proper Self Refresh operation, power supply pins (VDD1 and VDD2) must be at valid levels. VDDQ may be turned off during Self-Refresh after tESCKE is satisfied (Refer to Figure-Self Refresh Entry/Exit Timing with Power Down Entry/Exit for tESCKE).

Prior to exiting Self-Refresh VDDQ must be within specified limits. The minimum time that the SDRAM must remain in Self Refresh model is tSR,min.

Figure - Self Refresh Entry/Exit Timing

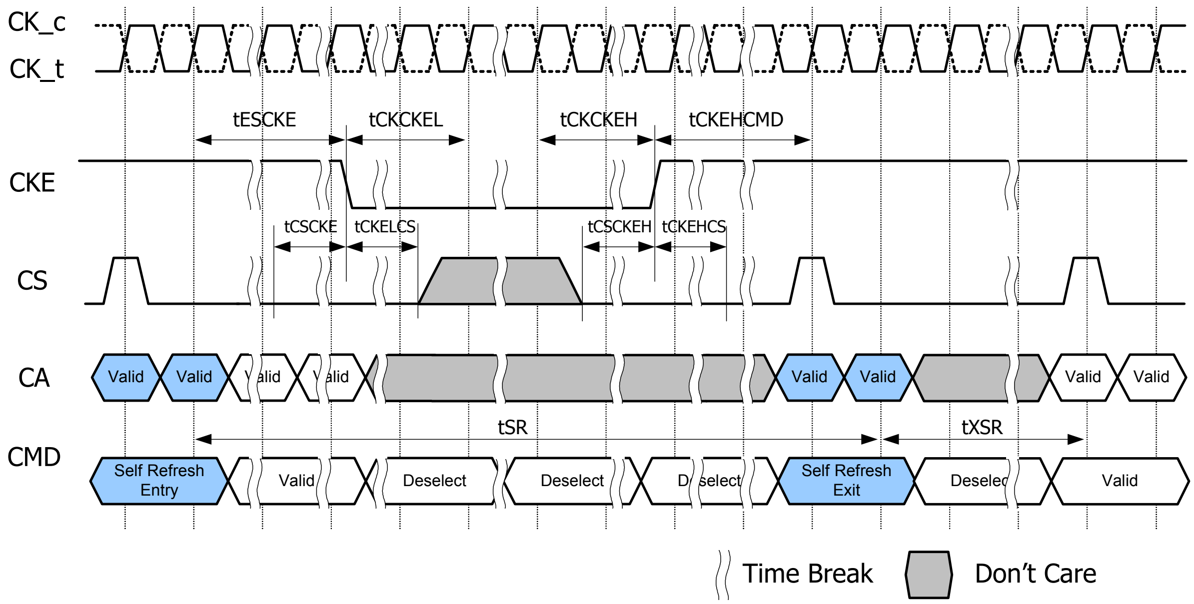


1. MRR-1, CAS-2, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. Address input may be don't care when input command is Deselect.

4.11.2. Power Down Entry and Exit during Self Refresh

Entering/Exiting Power Down Mode is allowed during Self Refresh mode in LPDDR4 SDRAM. The related timing parameters between Self Refresh Entry/Exit and Power Down Entry/Exit are shown in Figure-Self Refresh Entry/Exit Timing with Power Down Entry/Exit.

Figure - Self Refresh Entry/Exit Timing with Power Down Entry/Exit

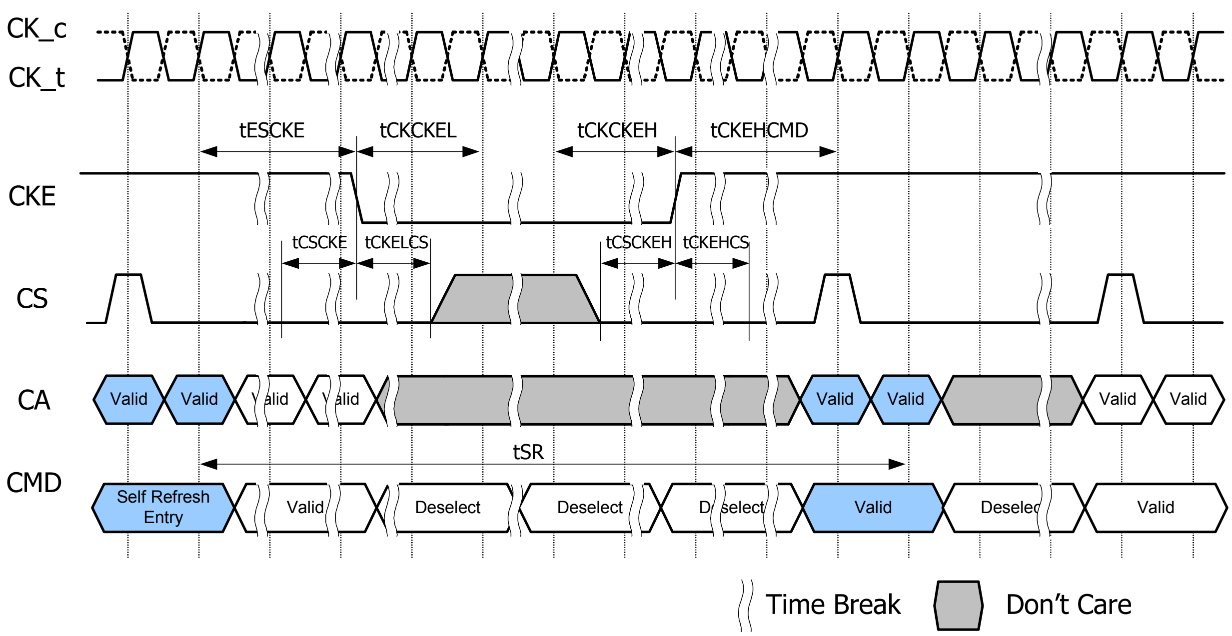


1. MRR-1, CAS-2, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is also allowed during Self Refresh.
2. Address input may be don't care when input command is Deselect.
3. CS input must be low when input command is Deselct.
4. Deselect is only allowed during tCMDCKE(min) and tCKELCMD(min)
5. Deselect is only allowed during tCSCKEH(min) and tCKEHCMD(min)
6. The input clock frequency can be changed after tCKCKEL(min) satisfied.

4.11.3. Command Input Timing after Power Down Exit

Command input timings after Power Down Exit during Self Refresh mode are shown in Figure-Command input timings after Power Dwon Exit during Self Refresh.

Figure - Command input timings after Power Down Exit during Self Refresh



1. MRR-1, CAS-2, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is also allowed during Self Refresh.
2. Address input may be don't care when input command is Deselect.
3. CS input must be low when input command is Deselct.
4. Deselect is only allowed during tCMDCKE(min) and tCKELCMD(min)
5. Deselect is only allowed during tCSCKEH(min) and tCKEHCMD(min)
6. The input clock frequency can be changed after tCKCKEL(min) satisfied.

4.11.4. Partial Array Self-Refresh (PASR)

4.11.4.1. PASR Bank Masking

The LPDDR4 SDRAM has eight banks (additional banks may be required for higher densities). Each bank of an LPDDR4 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16 session.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, "unmasked". When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is decribed in the following chapter.

4.11.4.2. PASR Segment Masking

A segment masking scheme may be used in lieu of or in combination with the bank masking scheme in LPDDR4 SDRAM. LPDDR4 devices utilize eight segments per bank. For segment masking bit assignments, see Mode Register 17 session.

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, "masked". Programming of segment mask bits is similar to the one of bank mask bits. Eight segments are used as listed in Mode Register 17 session. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. Programming of bits in the reserved registers has no effect on the device operation.

Table - Example of Bank and Segment Masking use in LPDDR4 devices

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

1. This table illustrates an example of an 8-bank LPDDR4 SDRAM device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

4.11.5. Self Refresh Abort

If MR4 OP[3] is enabled then DRAM aborts any ongoing refresh during Self Refresh exit and does not increment the internal refresh counter. Controller can issue a valid command after a delay of tXSR_abort instead of tXSR.

The value of tXSR_abort(min) is defined as tRFCpb + TBD ns.
Upon exit from Self Refresh mode, the LPDDR4 SDRAM requires a minimum of one extra refresh (8 per bank or 1 all bank) before entry into a subsequent Self Refresh mode. This requirement remains the same irrespective of the setting of the MR bit for self refresh abort.

Self refresh abort feature is available for higher density devices starting with12 Gb device.

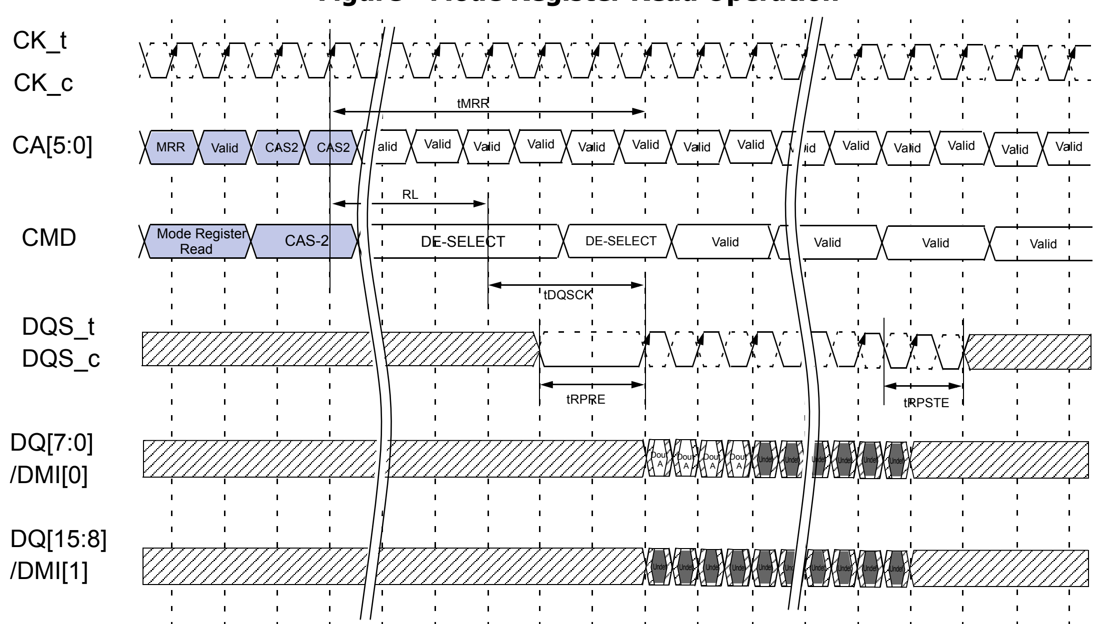
4.12. Mode Register Read (MRR) command

The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR4-SDRAM registers.The MRR command is initiated with CKE, CS and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) allow the user to select one of 64 registers. The mode register contents are available on the first 4UI's data bits of DQ[7:0] after RL x tCK + tDQSCK + tDQSQ following the MRR command. Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length 16. MRR operation must not be interrupted.

BL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DQ0	OP0				V											
DQ1	OP1				V											
DQ2	OP2				V											
DQ3	OP3				V											
DQ4	OP4				V											
DQ5	OP5				V											
DQ6	OP6				V											
DQ7	OP7				V											
DMI	V															

Notes:
1. MRR data are extended to first 4 UI's for DRAM controller to sample data easily.
2. DBI may apply or may not apply during normal MRR. It's vendor specific. If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DBI pin status should be low.
3. The read pre-amble and post-amble of MRR are same as normal read.

Figure - Mode Register Read Operation



1. Only BL=16 is supported.
2. Only De-Select is allowed during tMRR period.

4.12.1. MRR Following Idle Power-Down State

Following the idle power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from standby, idle power-down mode.

4.12.2. Mode Register Read - Temperature Sensor

LPDDR4 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

LPDDR4 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4[2:0] equals ‘b011. LPDDR4 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

TempGradient x (ReadInterval + tTSI + SysRespDelay) <= 2C

Table - Temperature Sensor

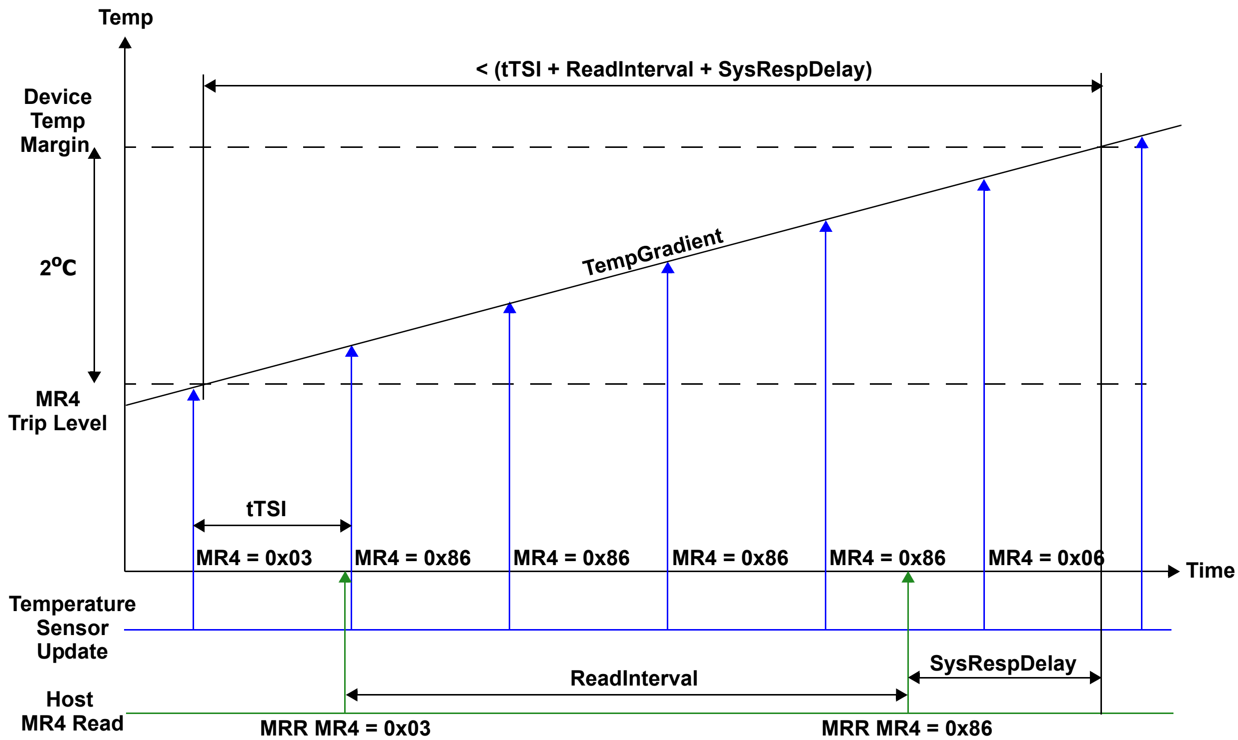
Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

(10’C/s) x (ReadInterval + 32ms + 1ms) <= 2’C

In this case, ReadInterval shall be no greater than 167ms.

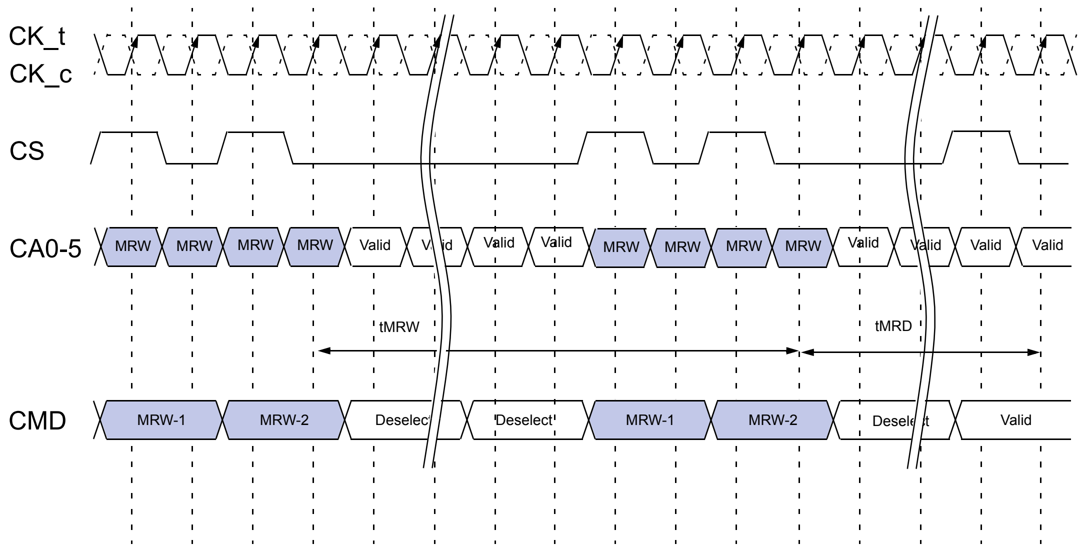
Figure - Temp sensor Timing



4.13. Mode Register Write (MRW) command

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CKE, CS, and CA[5:0] to valid levels at a rising edge of the clock (see Command Truth Table). The mode register address and the data written to the mode registers is contained in CA[5:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode register Writes to read-only registers have no impact on the functionality of the device.

Figure - Mode Register Write Timing



1. Only De-select command is allowed during tMRW and tMRD periods

4.13.1. Mode Register Write

MRW can be issued from either a Bank-Idle or Bank-Active state. Certain restrictions may apply for MRW from an Active state.

Table - Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

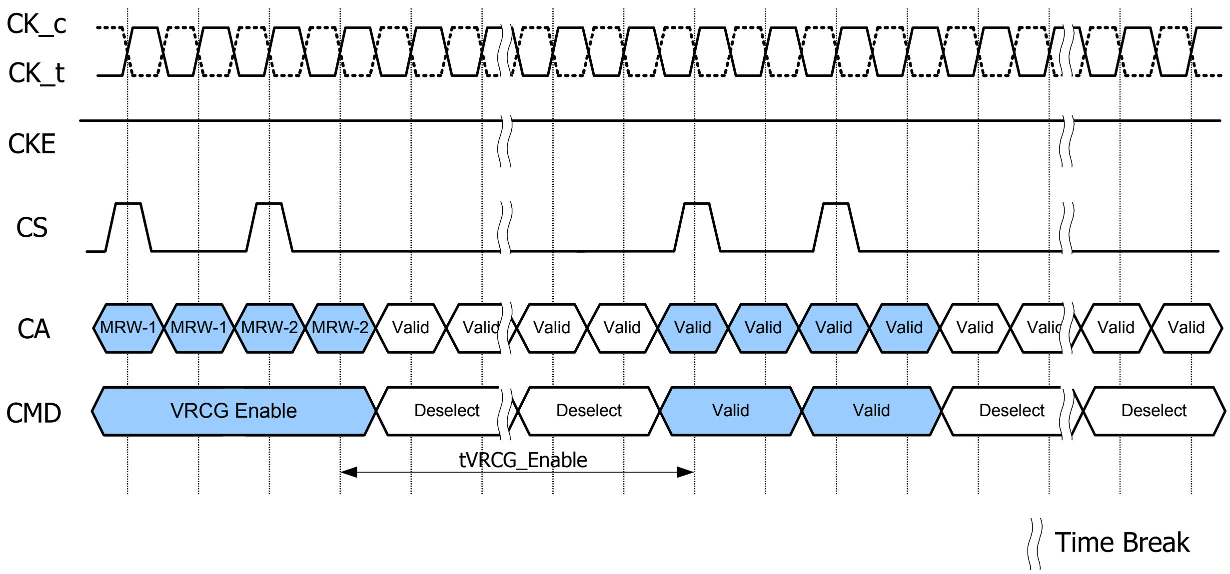
Current State	Command	Intermediate State	Next State
SDRAM		SDRAM	SDRAM
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading	Bank(s) Active
	MRW	Mode Register Writing	Bank(s) Active

4.13.2. Vref Current Generator (VRCG)

LPDDR4 SDRAM Vref current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal Vref(DQ) and Vref(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13[OP3] = 1. Only Deselect commands may be issued until tVRCG_ENABLE is satisfied. tVRCG_ENABLE timing is shown in figure below.

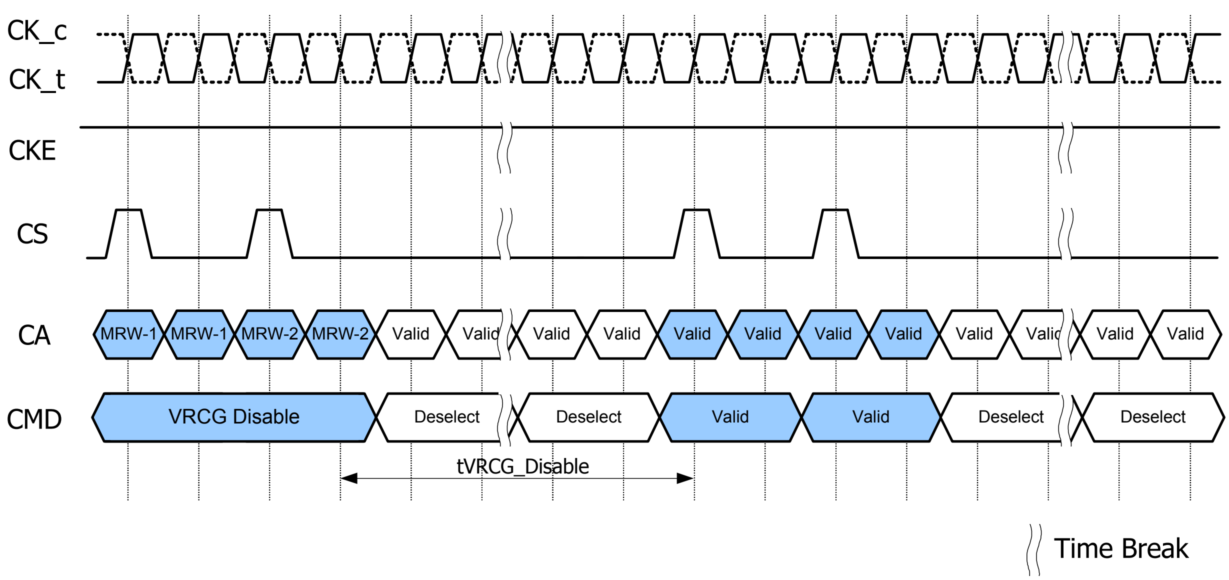
PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

Figure - VRCG Enable timing



VRCG high current mode is disabled by setting MR13[OP3] = 0. Only Deselect commands may be issued until tVRCG_DISABLE is satisfied. tVRCG_DISABLE timing is shown in figure below.

Figure - VRCG Disable timing



Note that LPDDR4 SDRAM devices support Vref(CA) and Vref(DQ) range and value changes without enabling VRCG high current mode.

Click to buy NOW! PDF-XChange Viewer www.docu-track.com

4.13.3. Mode Reister Write - WR Leveling Mode

To improve signal-integrity performance, the LPDDR4 SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair.

All data bits (DQ[7:0] for DQS_t/DQS_c[0], and DQ[15:8] for DQS_t/DQS_c[1]) carry the training feedback to the controller. Both DQS signals in each channel must be leveled independently. Write-leveling entry/exit is independent between channels.

The LPDDR4 SDRAM enters into write-leveling mode when mode register MR2-OP[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only DESELECT commands are allowed, or a MRW command to exit the write-leveling operation. Depending on the absolute values of tQSL and tQSH in the application, the value of tDQSS may have to be better than the limits provided in the chapter "AC Timing Parameters" in order to satisfy the tDSS and tDSH specification. Upon completion of the write-leveling operation, the DRAM exits from write-leveling mode when MR2-OP[7] is reset LOW.

Write Leveling should be performed before Write Training (DQS2DQ Training).

Write Leveling Procedure:

1. Enter into Write-leveling mode by setting MR2-OP[7]=1,
2. Once entered into Write-leveling mode, DQS_t must be driven LOW and DQS_c HIGH after a delay of tWLDQSEN.
3. Wait for a time tWLMRD before providing the first DQS signal input. The delay time tWLMRD(MAX) is controller-dependent.
4. DRAM may or may not capture first rising edge of DQS_t due to an unstable first risign edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal during Write Training Mode.
   The captured clock level by each DQS edges are overwritten at any time and the DRAM provides asynchronous feedback on all the DQ bits after time tWLO.
5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings.
6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established.
7. Exit from Write-leveling mode by setting MR2-OP[7]=0.

A Write Leveling timing example is shown in figure below.

Figure - Write Leveling Timing, tDQSL(max)

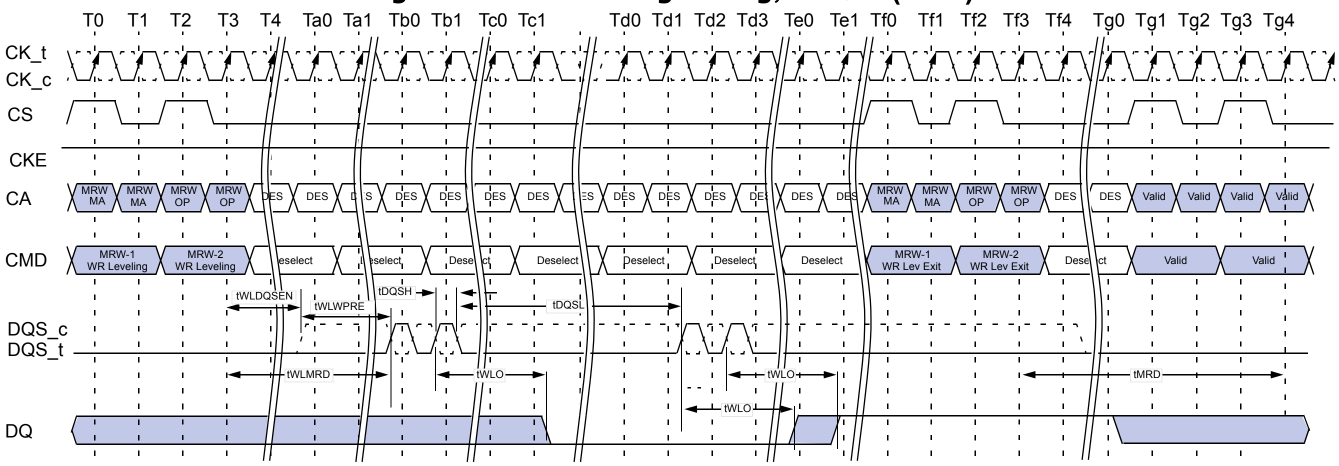
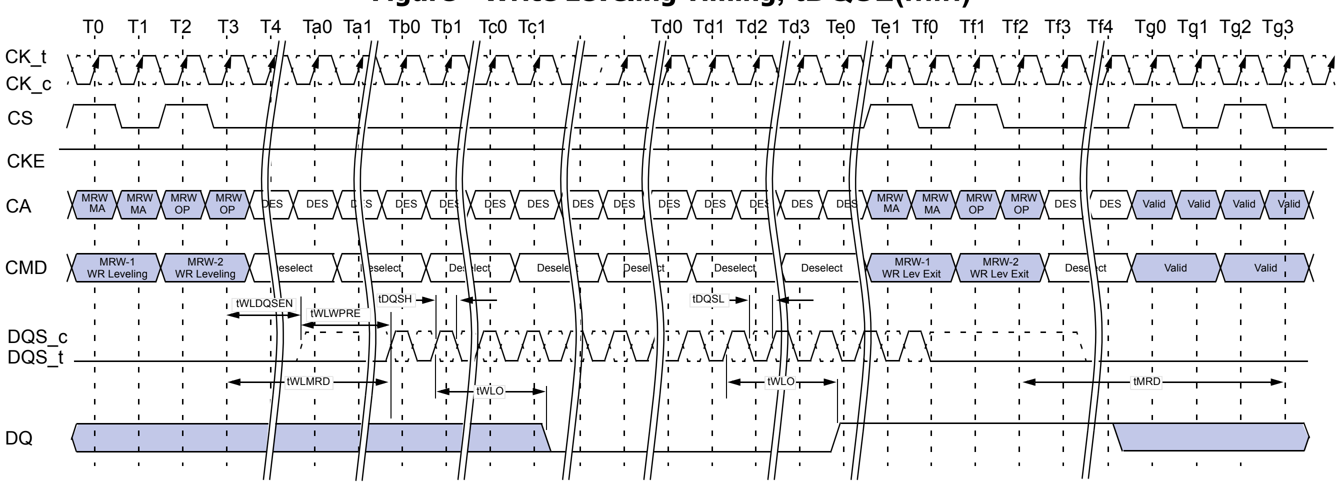


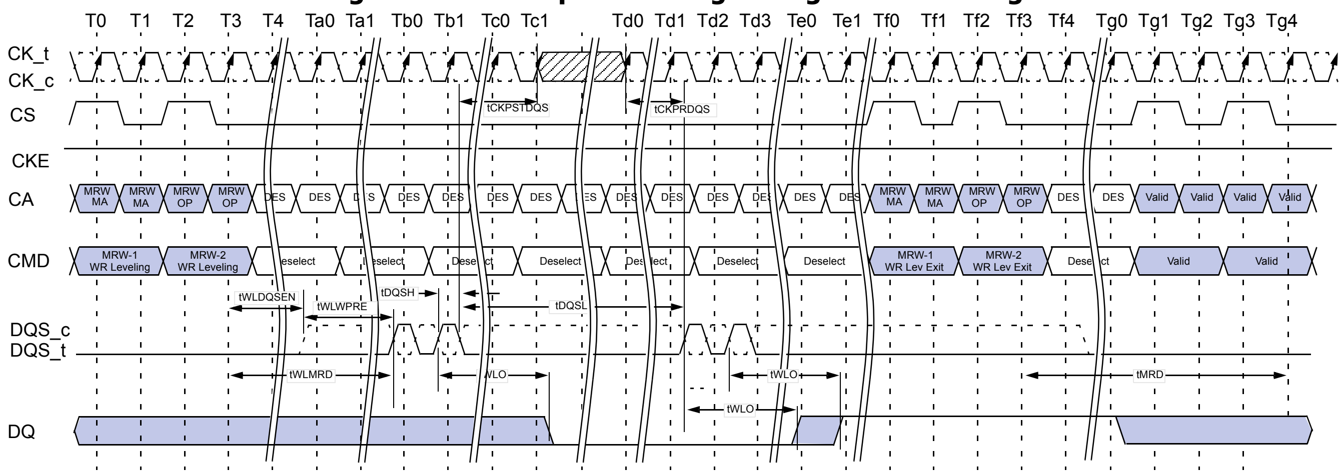
Figure - Write Leveling Timing, tDQSL(min)



4.13.3.1. Clock stop during Write Leveling

During Write Leveling, the clock can be temporarily stopped when CS and DQS_t is de-asserted. The clock signal must be resumed 2*tCK prior to the DQS pulses and maintained at least 1*tCK after the last DQS pulse.

Figure - Clock stop and timing during Write Leveling



4.13.4. Command Bus Training

The LPDDR4-SDRAM command bus must be trained before enabling termination for high-frequency operation. LPDDR4 provides an internal VREF(ca) that defaults to a level suitable for un-terminated, low-frequency operation, but the VREF(ca) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation. The training mode described here centers the internal VREF(ca) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training mode.

Note: it is up to the system designer to determine what constitutes "low-frequency" and "high-frequency" based on the capabilities of the system. Low-frequency should then be defined as an operating frequency in which the system can reliably communicate with the SDRAM before Command Bus Training is executed.

The LPDDR4-SDRAM die has a bond-pad (ODT-CA) for multi-rank operation. In a multi-rank system, the terminating rank should be trained first, followed by the non-terminating rank(s). See the ODT section for more information.

The LPDDR4-SDRAM uses Frequency Set-Points to enable multiple operating settings for the die. The LPDDR4-SDRAM defaults to FSP-OP[0] at power-up, which has the default settings to operate in un-terminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR13 OP[6]=1B (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Prior to entering Command Bus Training, the SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when CKE is driven LOW, the LPDDR4-SDRAM will automatically switch to the alternate FSP register set (FSP-OP[y]) and use the alternate register settings during training (See note 6 in Figure "Entering Command Bus Training Mode and CA Training Pattern Input and Output with VrefCA Value Update" for more information on FSP-OP register sets). Upon training exit when CKE is driven HIGH, the LPDDR4-SDRAM will automatically switch back to the original FSP register set (FSP-OP[x]), returning to the "known-good" state that was operating prior to training. The training values for VREF(ca) are not retained by the DRAM in FSP-OP[y] registers, and must be written to the registers after training exit.

1. To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0]=1B (Command Bus Training Mode Enabled).

2. After time tMRD, CKE may be set LOW, causing the LPDDR4-SDRAM to switch from FSP-OP[x] to FSP-OP[y], and completing the entry into Command Bus Training mode.
A status of DQS_t, DQS_c, DQ and DMI are as follows, and DQ ODT state will be followed Frequency Set Point function except output pins.
- DQS_t[0], DQS_c[0] become input pins for capturing DQ[6:0] levels by its toggling.
- DQ[5:0] become input pins for setting VREF(ca) Level.
- DQ[6] becomes a input pin for setting VREF(ca) Range.
- DQ[7] and DMI[0] become input pins and their input level is Valid level or floating, either way is fine.
- DQ[13:8] become output pins to feedback its capturing value via command bus by CS signal.
- DQS_t[1], DQS_c[1],DMI[1] and DQ[15:14] become output pins or disable, it means that SDRAM may drive to a valid level or left floating.

3. At time tCAENT later, LPDDR4 SDRAM can accept to chage its VREF(ca) Range and Value using input signals of DQS_t[0], DQS_c[0] and DQ[6:0] from existing value that's setting via MR12 OP[6:0]. The mapping between MR12 OP code and DQ signals is shown in the table below. At least one Vref CA setting is required before proceed to next training steps.

Table - Mapping of MR12 OP Code and DQ Numbers

	Mapping						
MR12 OP code	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Number	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

4. The new VREF(ca) value must "settle" for time tVREF_LONG before attempting to latch CA information.

5. To verify that the receiver has the correct VREF(ca) setting and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.

6. To exit Command Bus Training mode, drive CKE HIGH, and after time tVREF_LONG issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0]=0B. After time tMRW the LPDDR4-SDRAM is ready for normal operation. After training exit the LPDDR4-SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

Command Bus Training may executed from IDLE, or Self Refresh states. When executing CBT within the Self Refresh state, the SDRAM must not be a power down state (i.e. CKE must be HIGH prior to training entry). Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

4.13.4.1. Training Sequence for single-rank systems:

Note that an example shown here is assuming an initial low-frequency, no-terminating operating point, training a high-frequency, terminating operating point. The green text is low-frequency, magenta text is high-frequency. Any operating point may be trained from any known good operating point)

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-OP[x], See note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels to set up high-frequency operating parameters.

3. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
4. Drive CKE LOW, and change CK frequency to the high-frequency operating point.
5. Perform Command Bus Training (VREFca, CS, and CA).
6. Exit training by driving CKE HIGH, a change CK frequency to the low-frequency operating point prior to driving CKE HIGH, then issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
7. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
8. Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the highfrequency operating point. At this point the Command Bus is trained and you may proceed to other training or normal operation.

4.13.4.2. Training Sequence for multi-rank systems:

(Example shown here is assuming an initial low-frequency operating point, training a high-frequency operating point. The green text is low-frequency, magenda text is high-frequency. Any operating point may be trained from any known good operating point)

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-WR[x], See Note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels and ranks to set up highfrequency operating parameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7]=1B.
4. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), and change CK frequency to the high-frequency operating point.
6. Perform Command Bus Training on the terminating rank (VREFca, CS, and CA).
7. Exit training by driving CKE HIGH, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[y] (or FSP-WR[x]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
8. Issue MRW-1 and MRW-2 command to enter training mode on the non-terminating rank (but keep CKE HIGH)
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the highfrequency operating point.
10. Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y] (or FSP-OP[x]).
11. Perform Command Bus Training on the non-terminating rank (VREFca, CS, and CA).
12. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] (or FSP-OP[y]) to turn off termination.
13. Exit training by driving CKE HIGH on the non-terminating rank, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
14. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the highfrequency operating point. At this point the Command Bus is trained for both ranks and you may proceed to other training or normal operation.

4.13.4.3. Relation between CA input pin and DQ output pin

The relation between CA input pin and DQ out pin is shown in the following table.

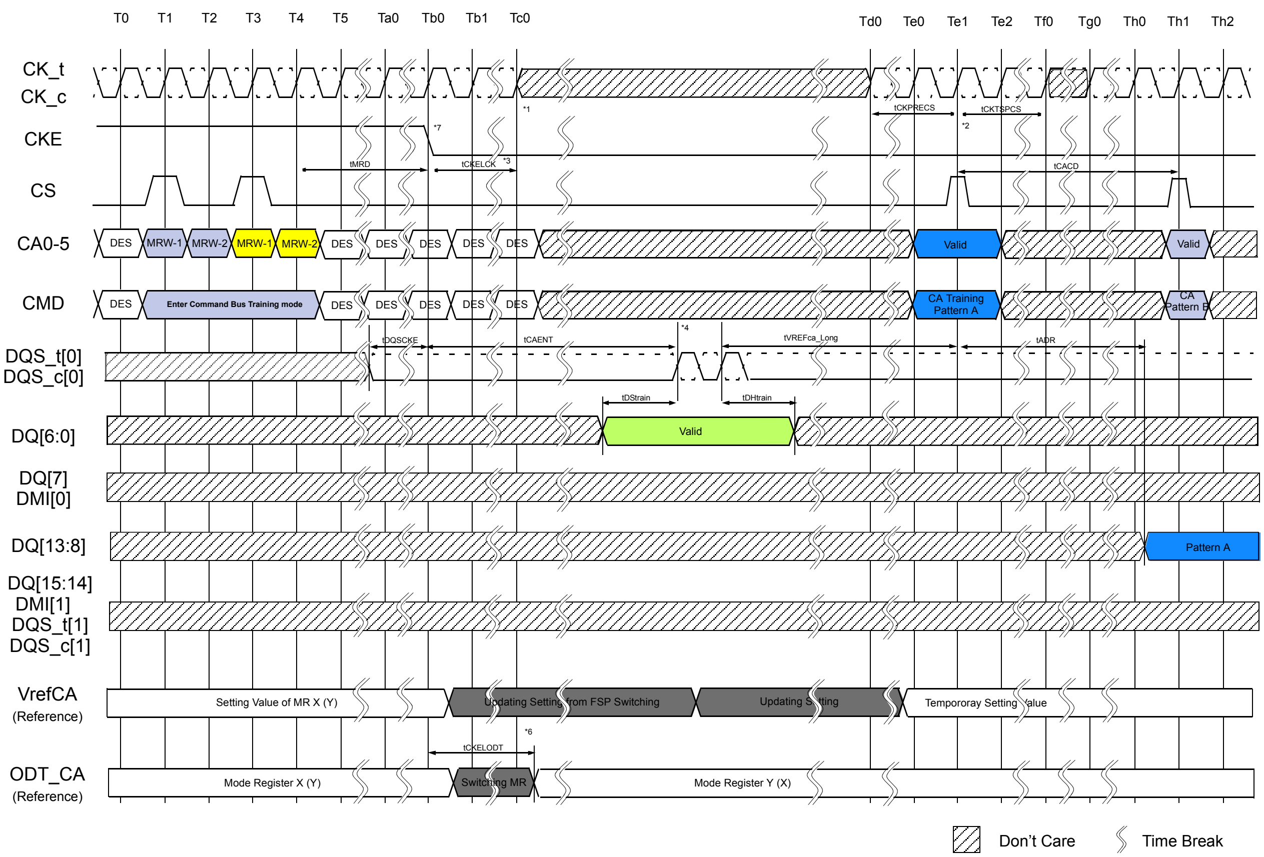
Table - Mapping of CA input pin to DQ ouput pin

	Mapping					
CA Number	CA5	CA4	CA3	CA2	CA1	CA0
DQ Number	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8

4.13.4.4. Timing Diagram

The basic timing diagrams of Command Bus Training are shown in following figures.

Figure - Entering Command Bus Training Mode and CA Training Pattern Input and Output with VrefCA Value Update



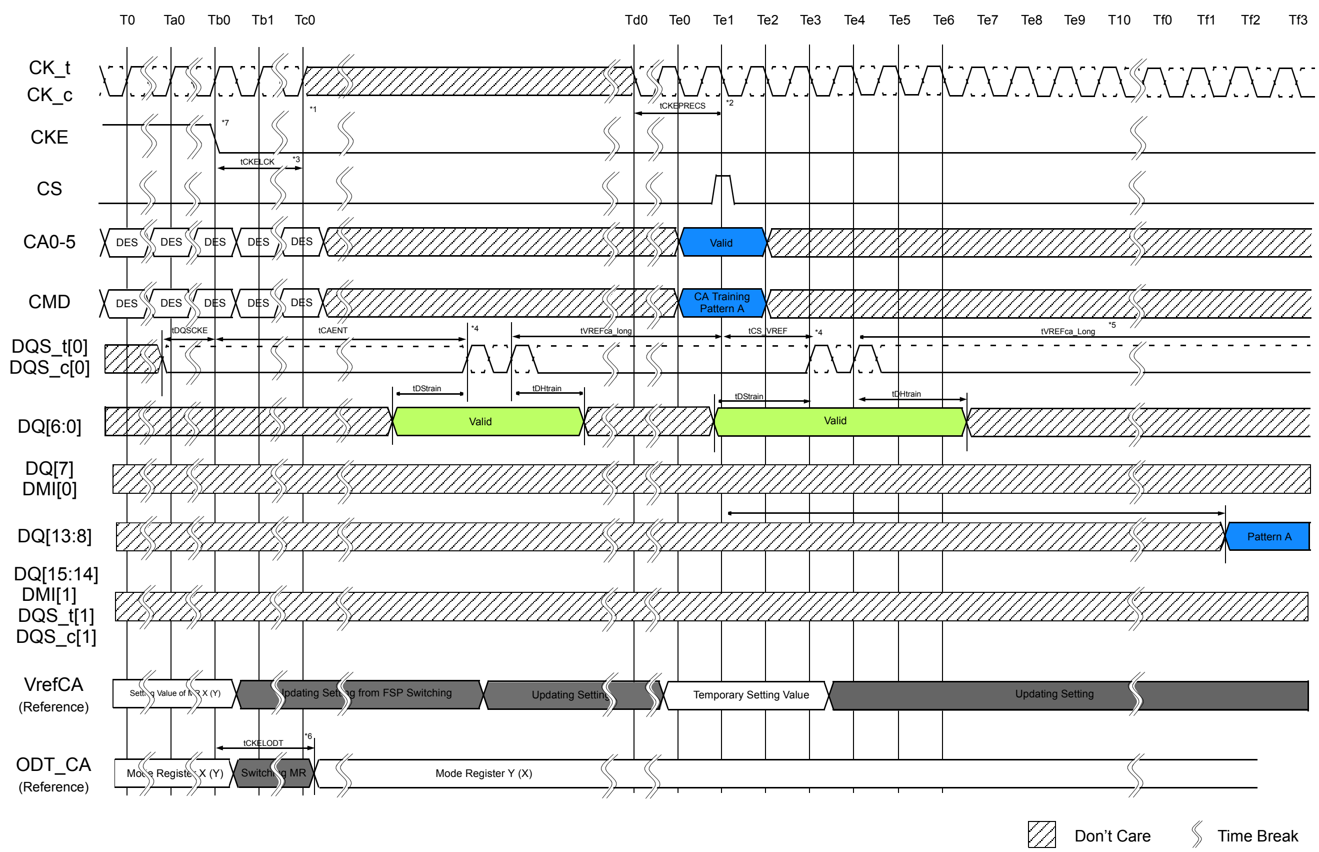
Notes:

1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS and tCKPSTCS.
3. Continue to Drive CK and Hold CA & CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. DRAM may or may not capture first rising/falling edge of DQS_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ[6:0] signals.
   The captured value of DQ[6:0] signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFca setting of MR12 temporary after time tVREFca_Long.
5. tVREF_LONG may be reduced to tVREF_SHORT if the following conditions are met: 1) The new Vref setting is a single step above or below the old Vref setting, and 2) The DQS pulses a single time, or the new Vref setting value on DQ[6:0] is static and meets

tDSTRAIN/tDHTRAIN for every DQS pulse applied.

6. When CKE is driven LOW, the SDRAM will switch its FSP-OP registers to use the alternate (i.e. non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT_CA disabled then termination will not enable in CA Bus Training mode. If the ODT_CA pad is bonded to Vss or floating, ODT_CA termination will never enable for that die.
7. When CKE is driven low in Command Bus Training mode, the LPDDR4-SDRAM will change operation to the alternate FSP, i.e. the inverse of the FSP programmed in the FSP-OP mode register.

Figure - Consecutive VrefCA Value Update

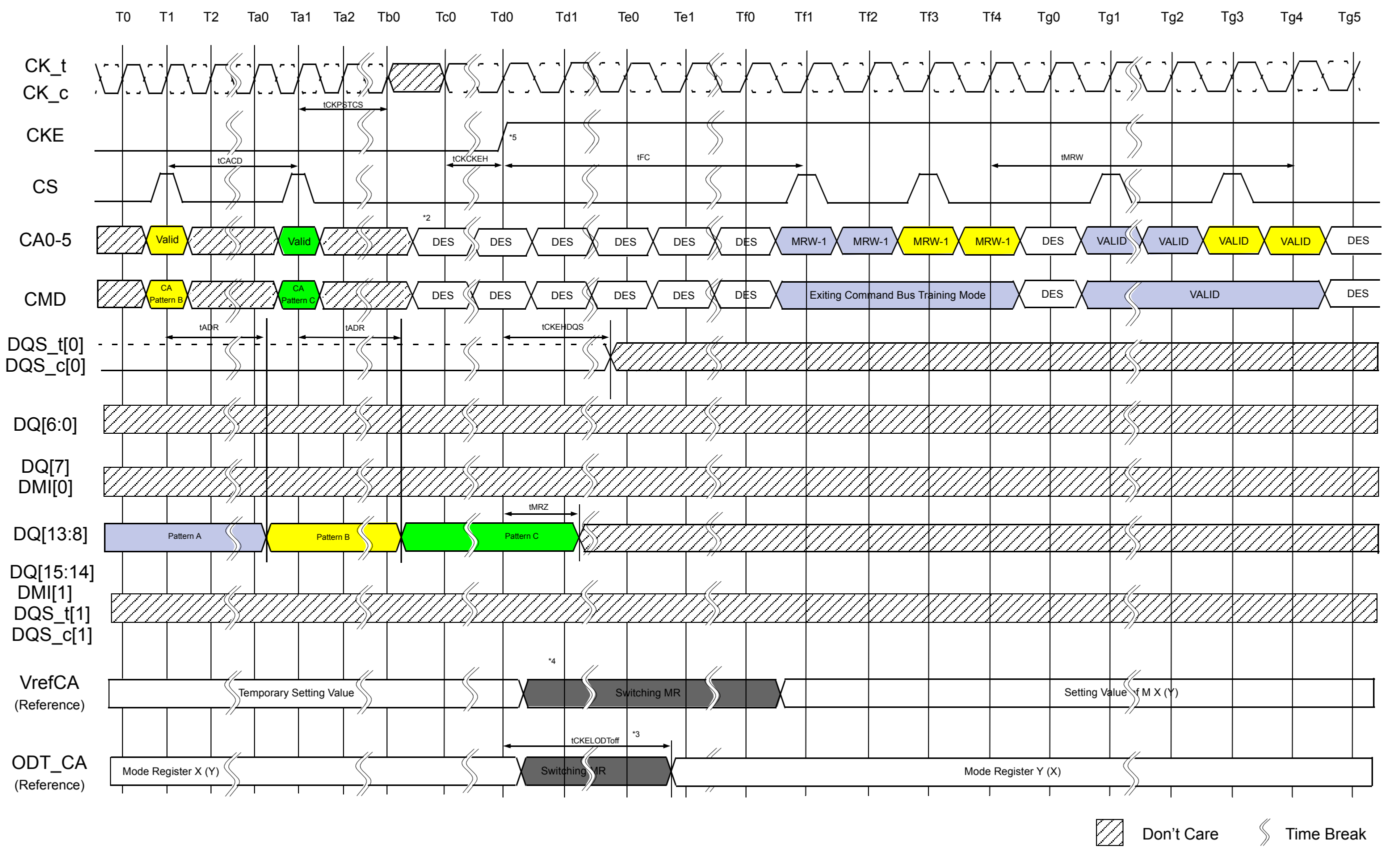


Notes:
1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS.
3. Continue to Drive CK and Hold CA & CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. DRAM may or may not capture first rising/falling edge of DQS_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ6:0 signals.
   The captured value of DQ[6:0] signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFca setting of MR12 temporary after time tVREFca_Long.
5. tVREF_LONG may be reduced to tVREF_SHORT if the following conditions are met: 1) The new Vref setting is a single step above or below the old Vref setting, and 2) The DQS pulses a single time, or the new Vref setting value on DQ[6:0] is static and meets tDSTRAIN/tDHTRAIN for every DQS pulse applied.
6. When CKE is driven LOW, the SDRAM will switch its FSP-OP registers to use the alternate (i.e. non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT_CA disabled then termination will not enable in CA Bus Training mode. If the ODT_CA pad is bonded to Vss or floating, ODT_CA termination will never enable for that die.

PDF-XChange Viewer Click to buy NOW! www.docu-track.com

7. When CKE is driven low in Command Bus Training mode, the LPDDR4-SDRAM will change operation to the alternate FSP, i.e. the inverse of the FSP programmed in the FSP-OP mode register.

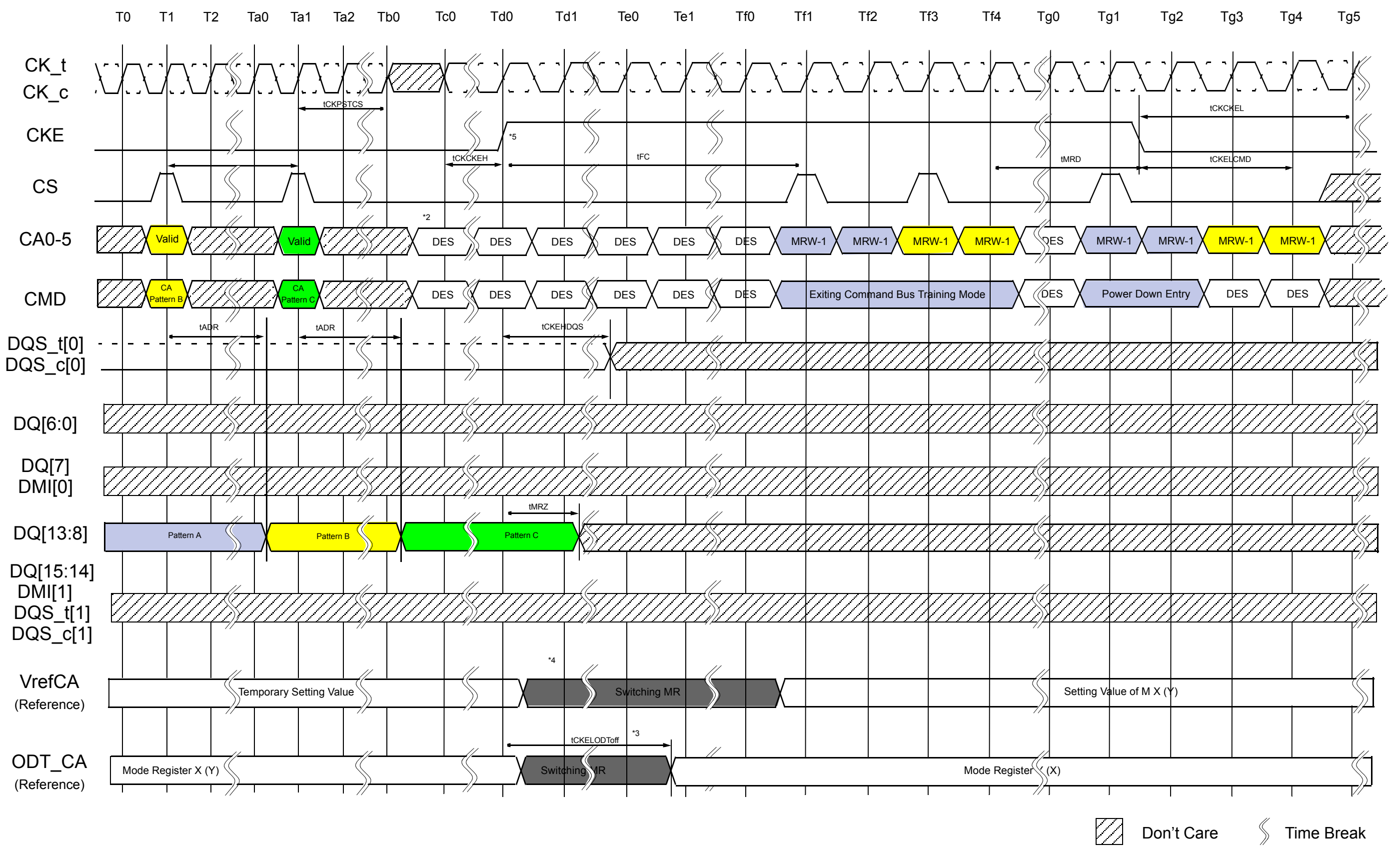
Figure - Exiting Command Bus Training Mode with Valid Command



Notes:

1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high. When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS and CA[5:0] must be Deselect (all low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the SDRAM's ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).
   Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency.
   Example: VREF(ca) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4-SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

Figure - Exiting Command Bus Training Mode with Power Down Entry



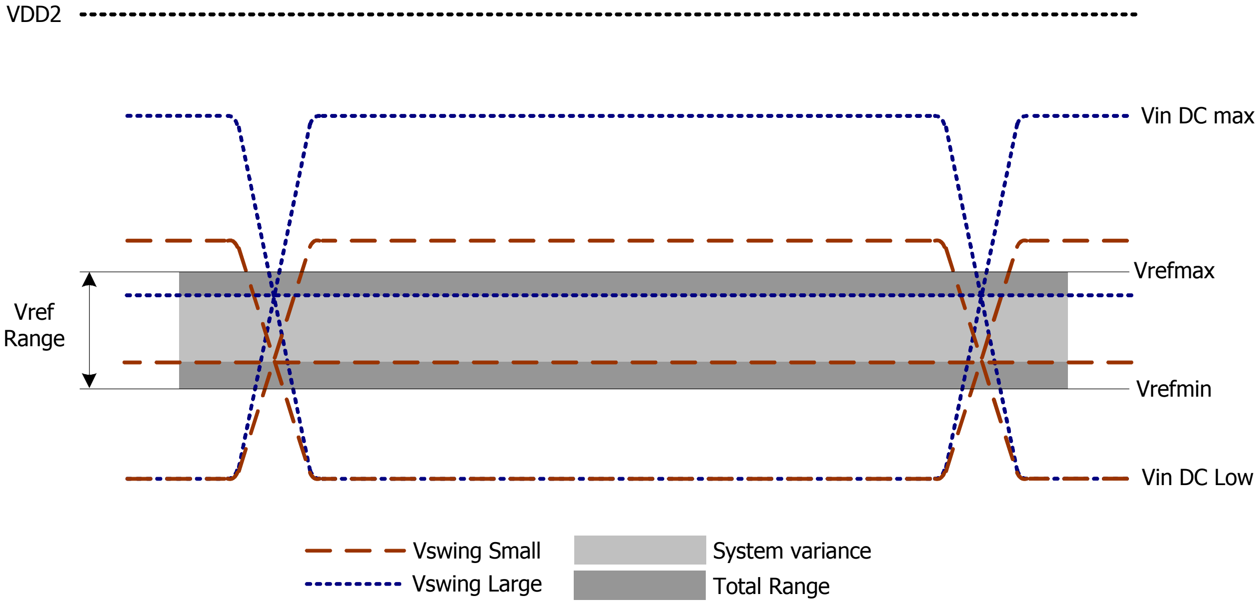
Notes:
1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high. When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS and CA[5:0] must be Deselect (all low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the SDRAM's ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).
   Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency.
   Example: VREF(ca) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4-SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

4.13.5. CA Vref Training

The DRAM internal CA Vref specification parameters are voltage operating range, stepsize, Vref set tolerance, Vref step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for LPDDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure "Vref operating range (Vref.min, Vref.max)".

Figure - Vref operating range (Vref.min, Vref.max)

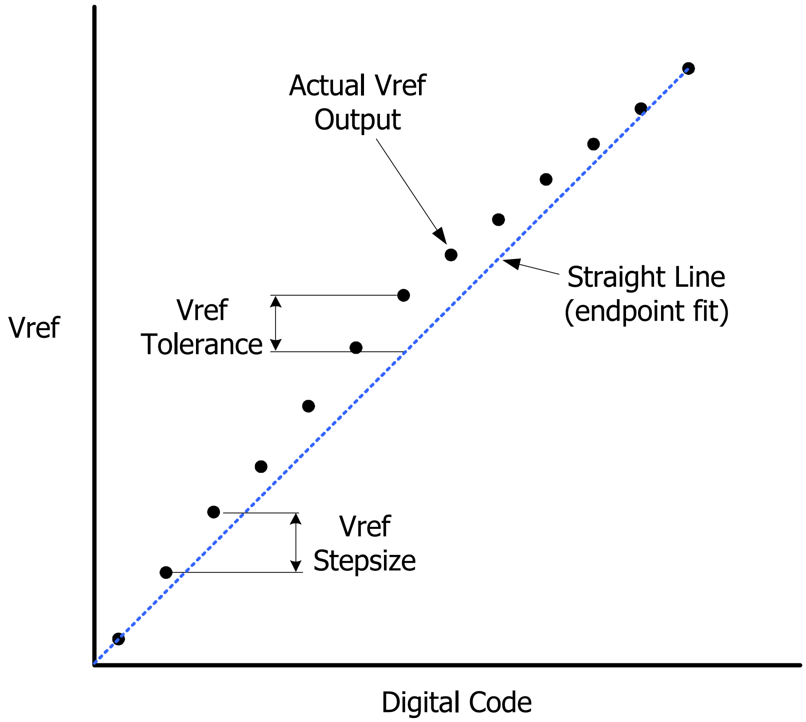


The Vref stepsize is defined as the stepsize between adjacent steps. Vref stepsize ranges from 0.5% VDDQ to 0.8%VD-DQ. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainity. The range of Vref set tolerance uncertainity is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the end-points are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

Figure - Example of Vref set tolerance (max case only shown) and stepsize



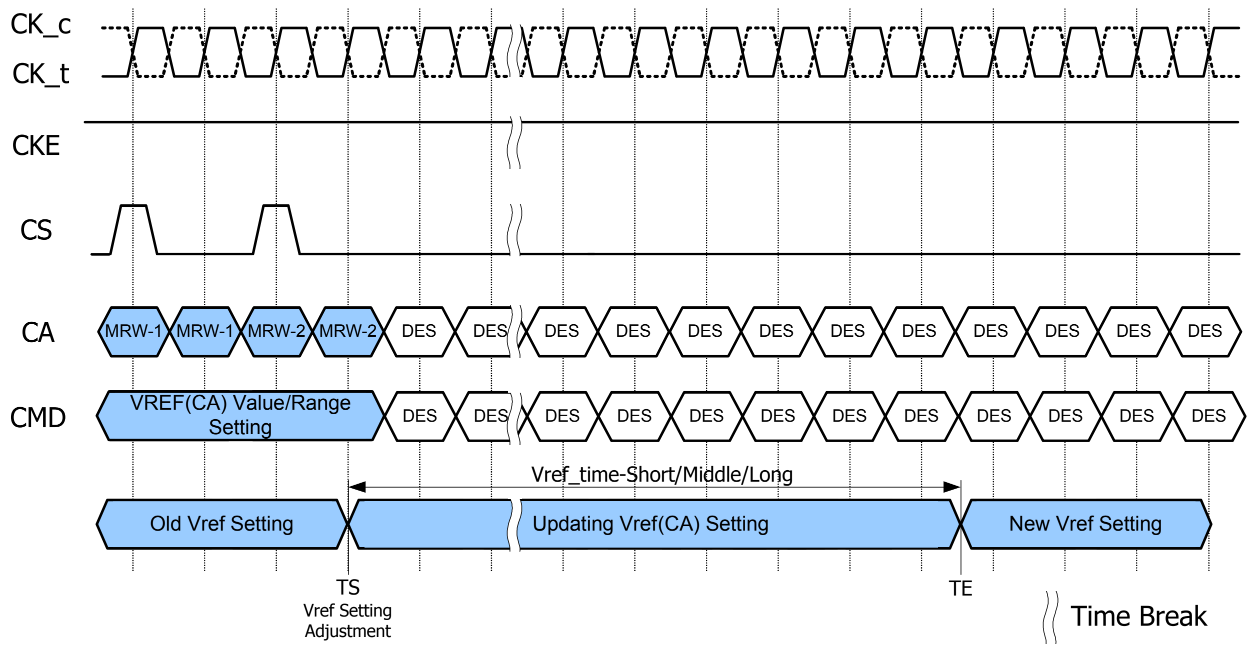
The Vref increment/decrement step times are define by Vref_time-short, middle and long. The Vref_time-short, Vref_time-middle and Vref_time-long is defined from TS to TE as shown in the Figure "Vref_time for short, middlg and long timing diagram" below where TE is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time TE as shown in Figure "Vref step single stepsize increment case". This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characerization.

Vref_time-Short is for a single stepsize increment/decrement change in Vref voltage.
Vref_time-Middle is at least 2 stepsizes increment/decrement change within the same VrefCA range in Vref voltage.
Vref_time-Long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefCA Range in Vref voltage.

TS - is referenced to MRS command clock
TE - is referenced to the Vref_val_tol

Figure - Vref_time for short, middlg and long timing diagram



The MRW command to the mode register bits are as follows.

MR12 OP[5:0] : VREF(CA) Setting
MR12 OP[6] : VREF(CA) Range

The minimum time required between two Vref MRS commands is Vref_time-short for single step and Vref_time-Middle for a full voltage range step.

Figure - Vref step single stepsize increment case

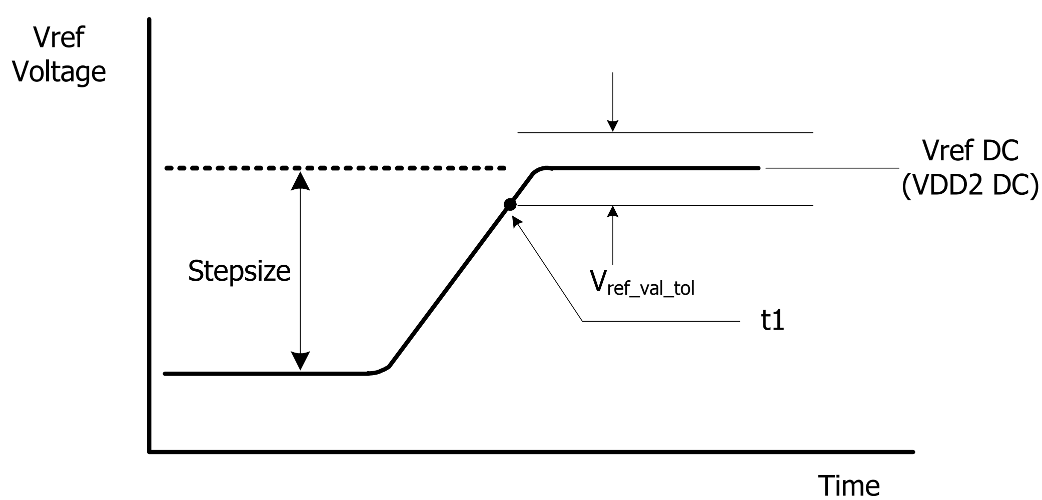


Figure - Vref step single stepsize decrement case

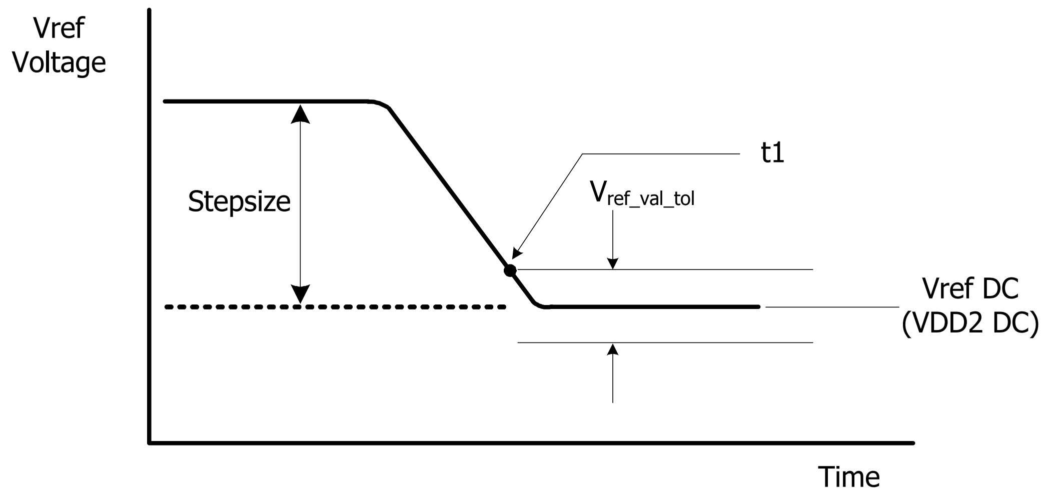
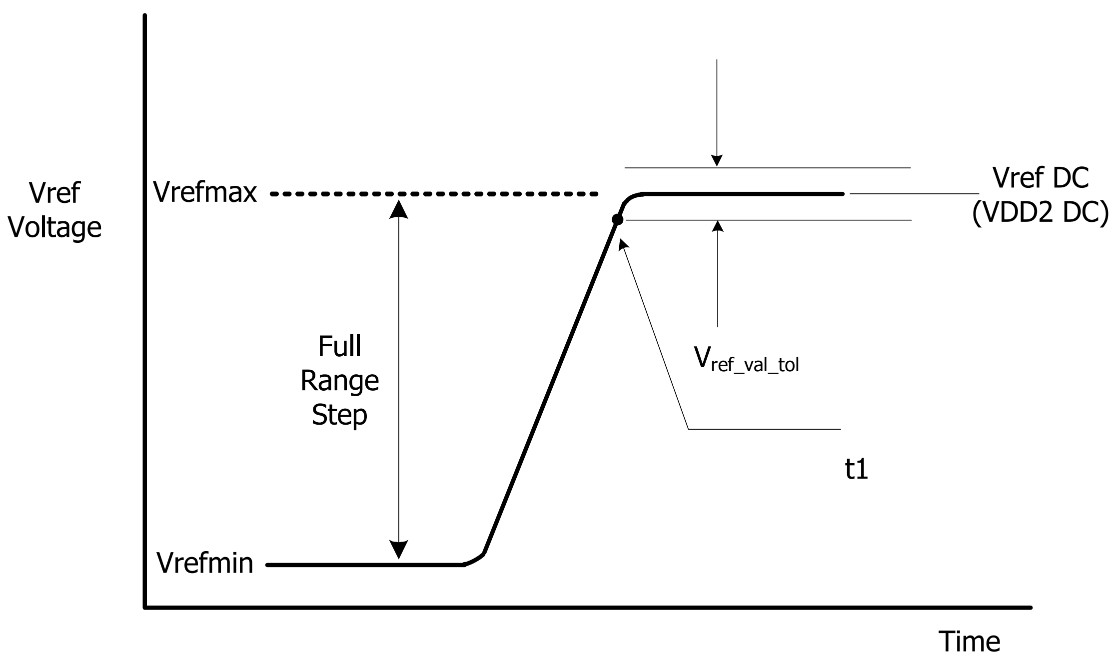
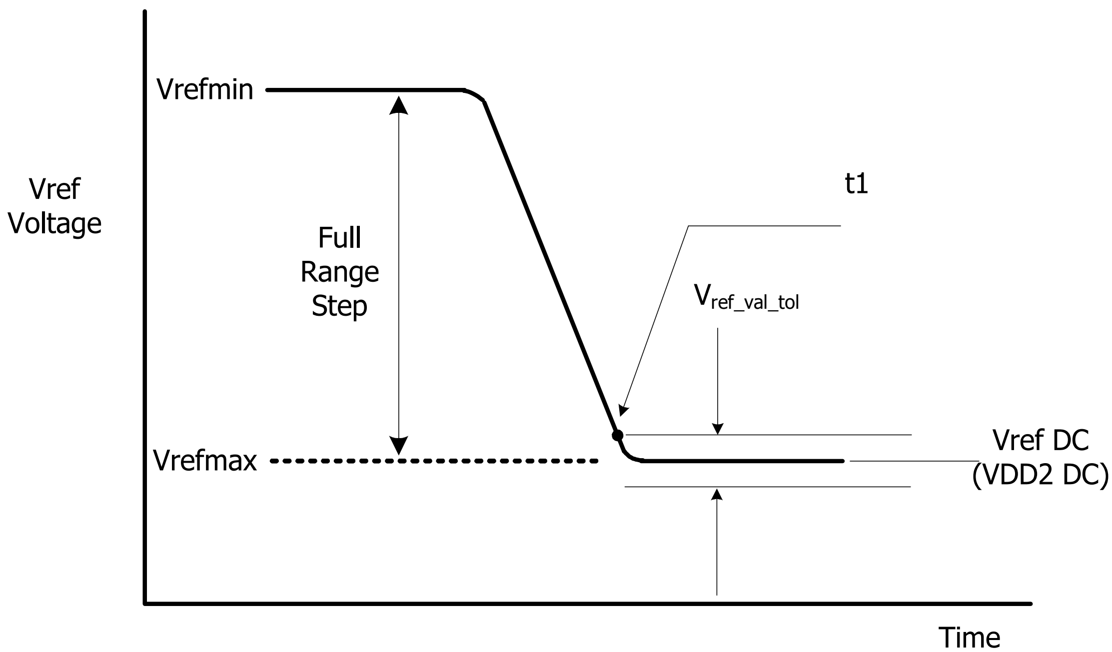


Figure - Vref full step from Vrefmin to Vrefmax case



PDF-XChange Viewer Click to buy NOW! www.docu-track.com

Figure - Vref full step from Vrefmax to Vrefmin case



The table below contains the CA internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

Table - CA Internal Vref Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Vref Max operating point Range[0]	Vref_max_R0	30%	-	-	VDDQ	1,11
Vref Min operating point Range[0]	Vref_min_R0	-	-	10%	VDDQ	1,11
Vref Max operating point Range[1]	Vref_max_R1	42%	-	-	VDDQ	1,11
Vref Min operating point Range[1]	Vref_min_R1	-	-	22%	VDDQ	1,11
Vref Stepsize	Vref_step	0.30%	0.40%	0.50%	VDDQ	2
Vref Set Tolerance	Vref_set_tol	-1.000%	0.000%	1.000%	VDDQ	3,4,6
		-0.10	0.00%	0.10%	VDDQ	3,5,7
Vref Step Time	Vref_time-short	-	-	100	ns	8
	Vref_time-middle			200	ns	12
	Vref_time-Long	-	-	250	ns	9
	Vref_time-weak	-	-	2	ms	13,14
Vref Valid tolerance	Vref_val_tol	-0.10%	0.00%	0.10%	VDDQ	10

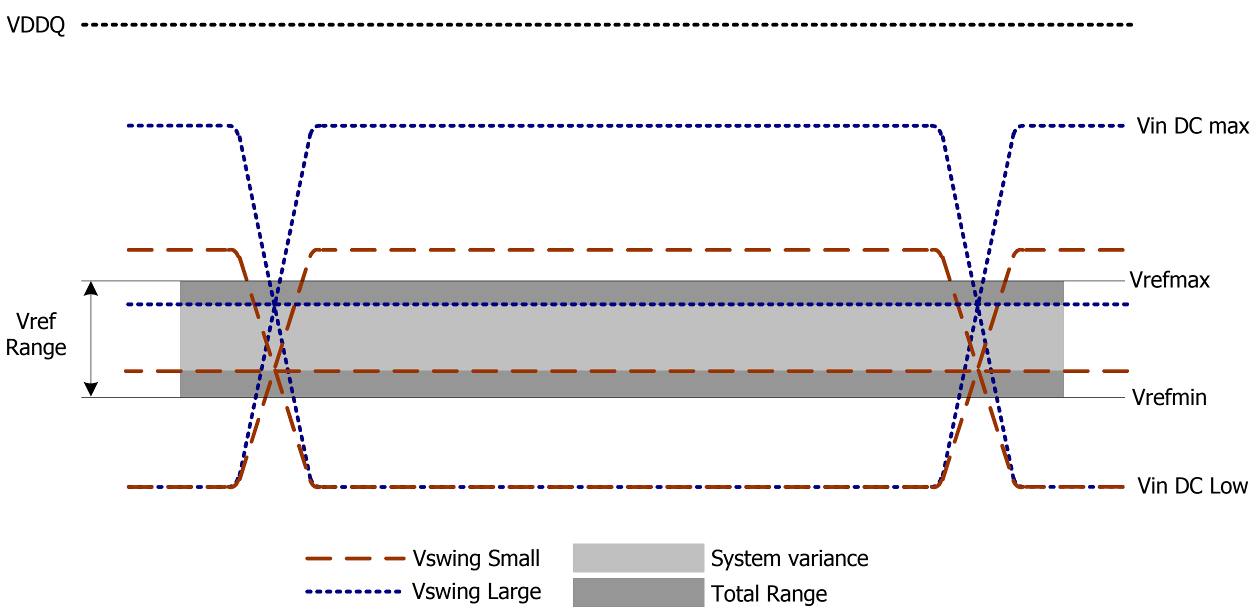
Notes:
1. Vref DC voltage referenced to VDDQ_DC.
2. Vref stepsize increment/decrement range. Vref at DC level.
3. Vref_new = Vref_old + n*Vref_step; n= number of steps; if increment use "+"; If decrement use "-".
4. The minimum value of Vref setting tolerance = Vref_new - 1.0%*VDDQ. The maximum value of Vref setting tolerance = Vref_new + 1.0%*VDDQ. For n>4
5. The minimum value of Vref setting tolerance = Vref_new - 0.10%*VDDQ. The maximum value of Vref setting tolerance = Vref_new + 0.10%*VDDQ. For n≤4.
6. Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.
7. Measured by recording the min and max values of the Vref output across 4 consectuive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.
8. Time from MRS command to increment or decrement one step size for Vref.
9. Time from MRS command to increment or decrement Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefCA Range in Vref voltage.
10. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
11. DRAM range 0 or 1 set by MR12 OP[6].
12. Time from MRS command to increment or decrement more than one step size up a full range of Vref voltage within the same VrefCA range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 OP[3] = 0.
14. Vref_time_weak covers all Vref(CA) Range and Value change conditions are applied to Vref_time_Short/Middle/Long.

4.13.6. DQ Vref Training

The DRAM internal DQ Vref specification parameters are voltage operating range, stepsize, Vref set tolerance, Vref step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for LPDDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure "Vref operating range (Vref.min, Vref.max)".

Figure - Vref operating range (Vref.min, Vref.max)

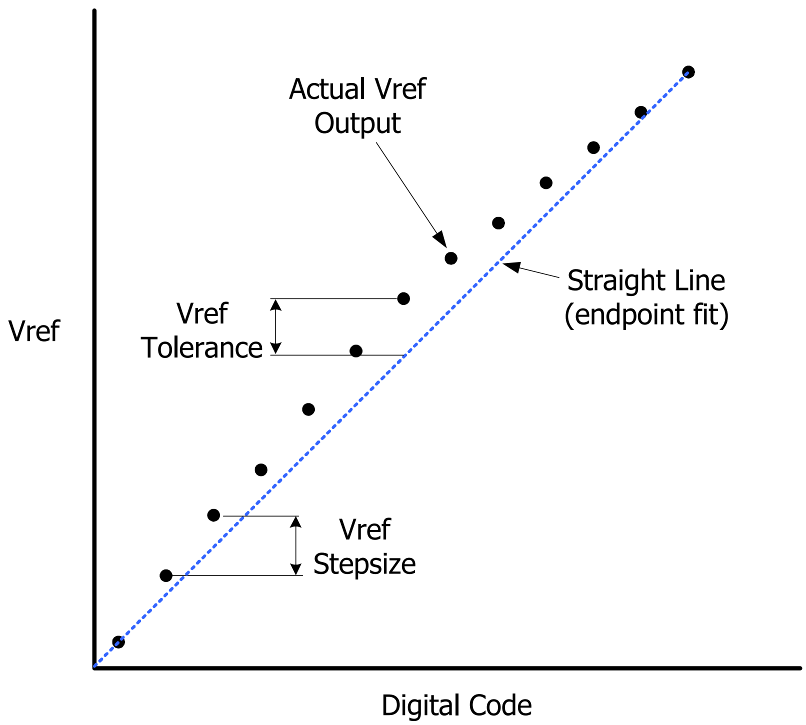


The Vref stepsize is defined as the stepsize between adjacent steps. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainity. The range of Vref set tolerance uncertainity is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the end-points are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

Figure - Example of Vref set tolerance (max case only shown) and stepsize



The Vref increment/decrement step times are define by Vref_time-short and long. The Vref_time-short and Vref_time-long is defined from TS to TE as shown in the Figure "Vref_time for short and long timing diagram" below where TE is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance(Vref_val_tol).

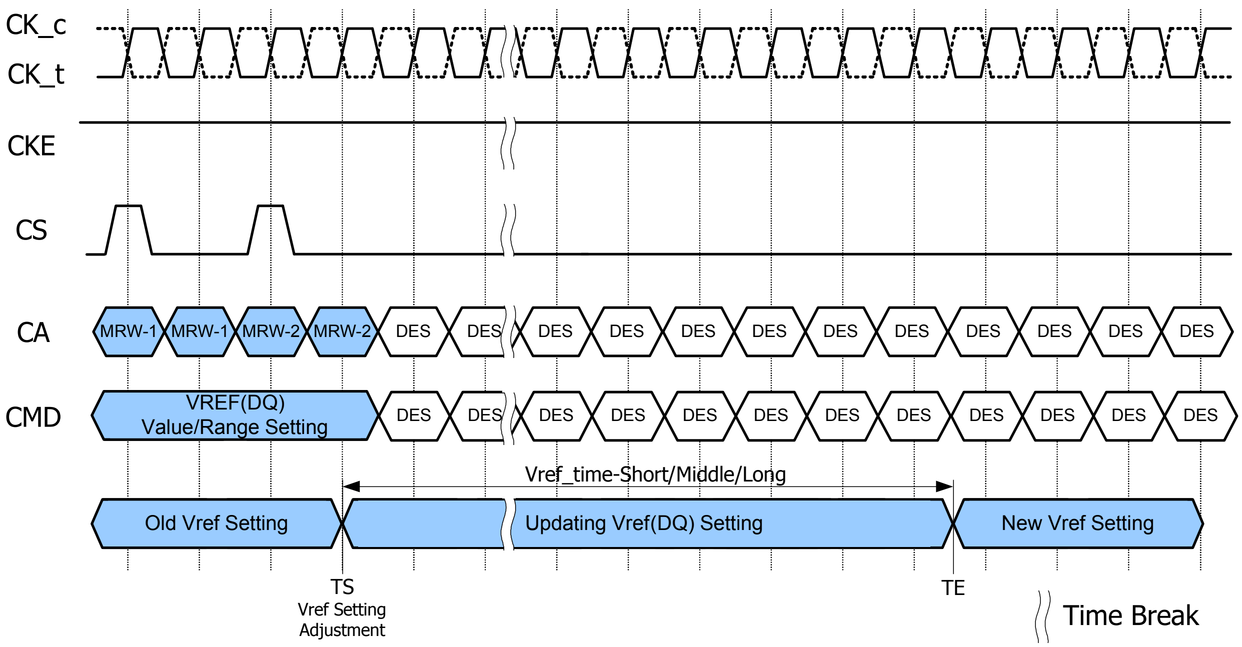
The Vref valid level is defined by Vref_val tolerance to qualify the step time TE as shown in Figure "Vref step single stepsize increment case". This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characerization.

Vref_time-Short is for a single stepsize increment/decrement change in Vref voltage.
Vref_time-Middle is at least 2 stepsizes increment/decrement change within the same VrefDQ range in Vref voltage.
Vref_time-Long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefDQ Range

in Vref voltage.

TS - is referenced to MRS command clock
TE - is referenced to the Vref_val_tol

Figure - Vref_time for short and long timing diagram



The MRW command to the mode register bits are as follows.
MR14 OP[5:0] : VREF(DQ) Setting
MR14 OP[6] : VREF(DQ) Range

The minimum time required between two Vref MRS commands is Vref_time-short for single step and Vref_time-Middle for a full voltage range step

Figure - Vref step single stepsize increment case

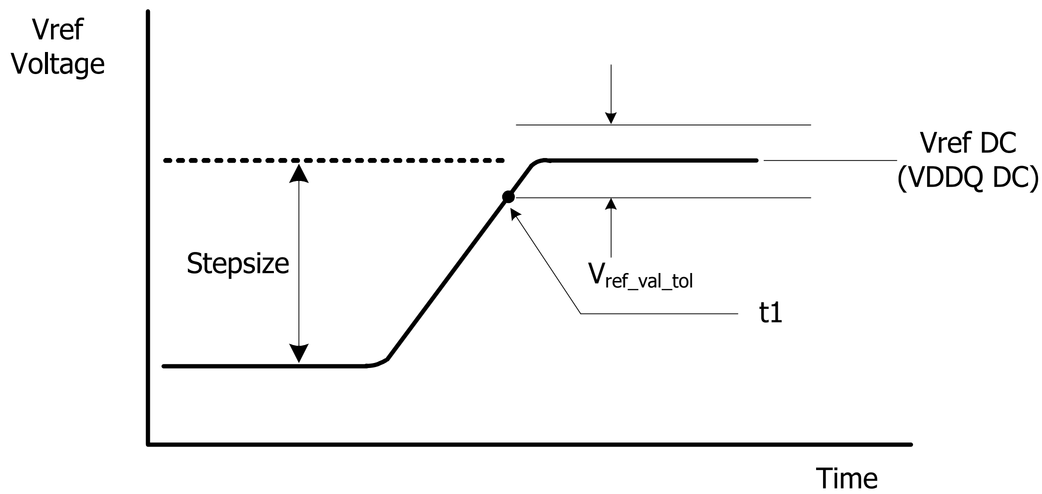


Figure - Vref step single stepsize decrement case

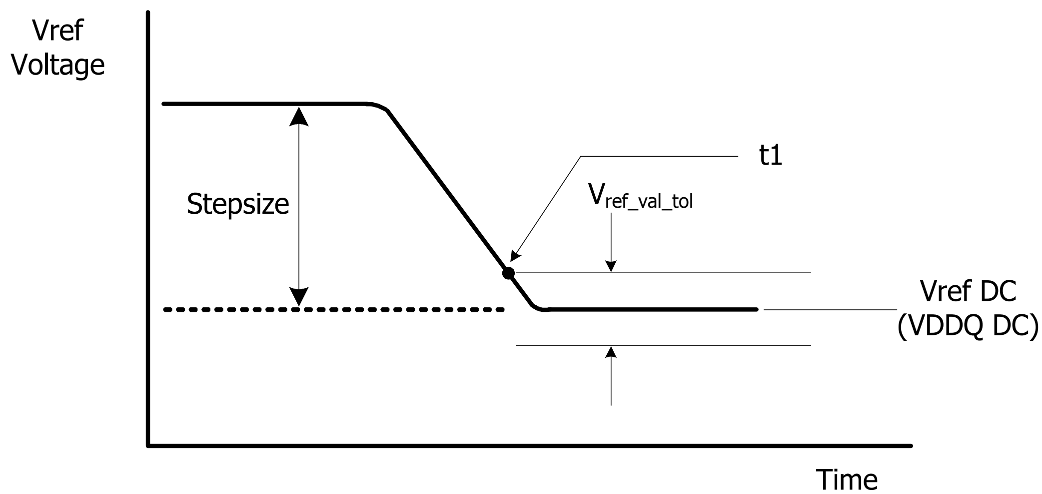


Figure - Vref full step from Vrefmin to Vrefmax case

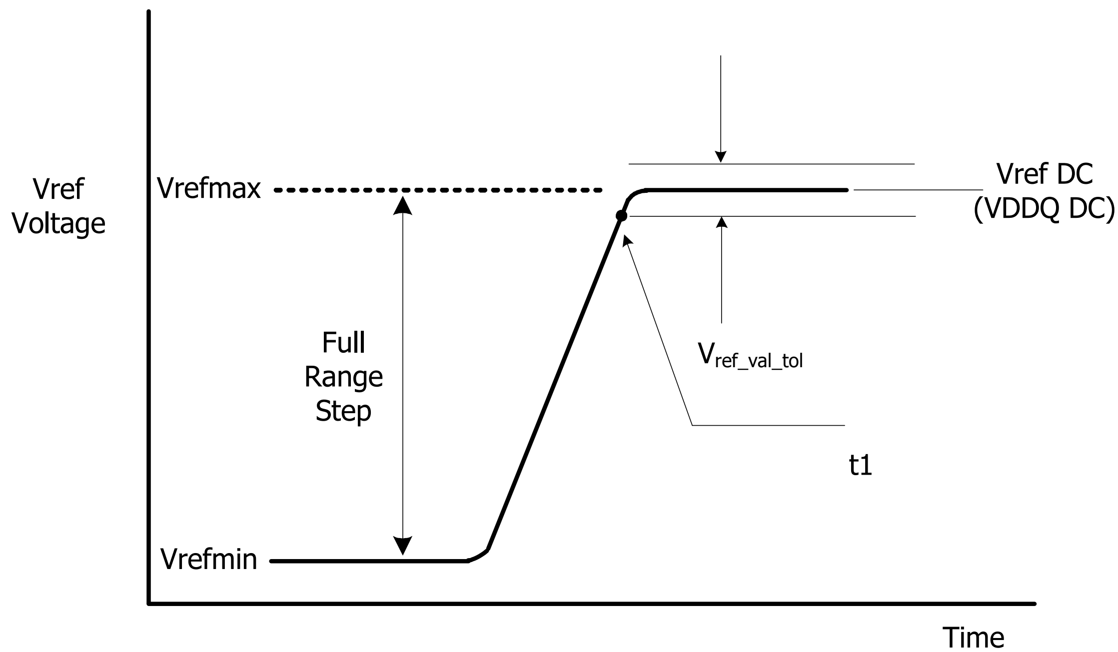
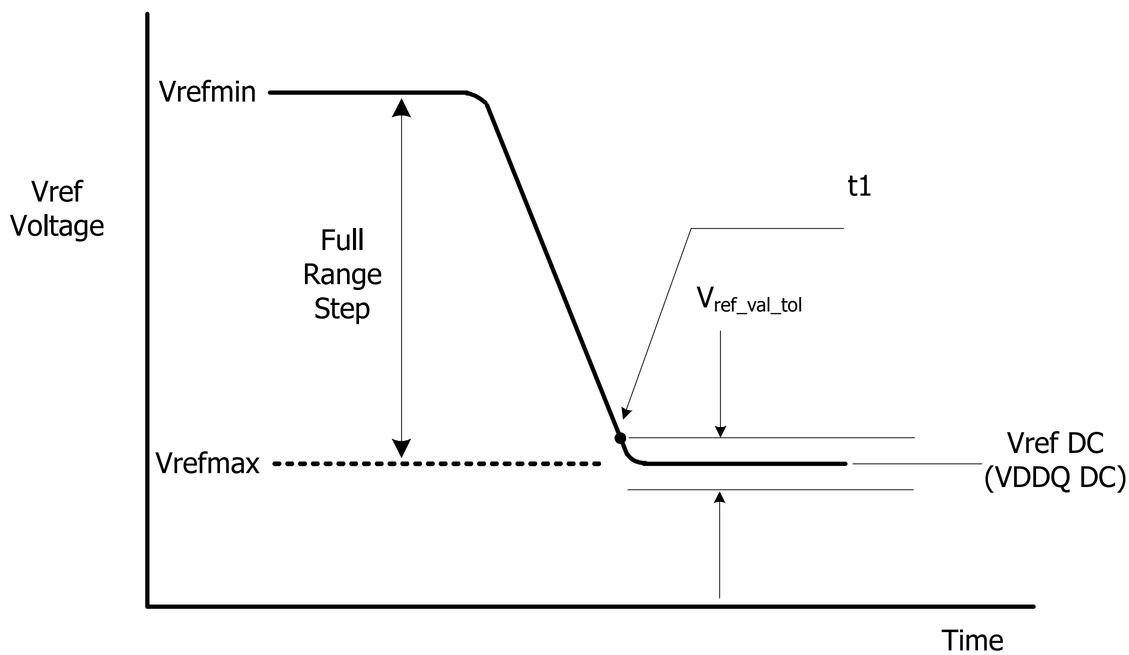


Figure - Vref full step from Vrefmax to Vrefmin case



The table below contains the DQ internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

Table - DQ Internal Vref Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Vref Max operating point Range[0]	Vref_max_R0	30%	-	-	VDDQ	1,11
Vref Min operating point Range[0]	Vref_min_R0	-	-	10%	VDDQ	1,11
Vref Max operating point Range[1]	Vref_max_R1	42%	-	-	VDDQ	1,11
Vref Min operating point Range[1]	Vref_min_R1	-	-	22%	VDDQ	1,11
Vref Stepsize	Vref_step	0.30%	0.40%	0.50%	VDDQ	2
Vref Set Tolerance	Vref_set_tol	-1.000%	0.000%	1.000%	VDDQ	3,4,6
		-0.10	0.00%	0.10%	VDDQ	3,5,7
Vref Step Time	Vref_time-short	-	-	100	ns	8
	Vref_time-Middle	-	-	200	ns	12
	Vref_time-Long	-	-	250	ns	9
	Vref_time-weak	-	-	2	ms	13,14
Vref Valid tolerance	Vref_val_tol	-0.10%	0.00%	0.10%	VDDQ	10

Notes:
1. Vref DC voltage referenced to VDDQ_DC.
2. Vref stepsize increment/decrement range. Vref at DC level.
3. Vref_new = Vref_old + n*Vref_step; n= number of steps; if increment use "+"; If decrement use "-".
4. The minimum value of Vref setting tolerance = Vref_new - 1.0%*VDDQ. The maximum value of Vref setting tolerance = Vref_new + 1.0%*VDDQ. For n>4.
5. The minimum value of Vref setting tolerance = Vref_new - 0.10%*VDDQ. The maximum value of Vref setting tolerance = Vref_new + 0.10%*VDDQ. For n< 4.
6. Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.
7. Measured by recording the min and max values of the Vref output across 4 consectuive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.
8. Time from MRS command to increment or decrement one step size for Vref.
9. Time from MRS command to increment or decrement Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefDQ Range in Vref voltage.
10. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
11. DRAM range 0 or 1 set by MR14 OP[6].
12. Time from MRS command to increment or decrement more than one step size up to a full range of Vref voltage withiin the same VrefDQ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.
14. Vref_time_weak covers all Vref(DQ) Range and Value change conditions are applied to Vref_time_Short/Middle/Long.

4.13.7. Target Row Refresh - TRR

Following TRR specification is based on current JEDEC ballot. It allows controller to other banks to have activities after 2nd Activate command. SK hynix 8Gb LPDDR4 does not allow other banks activities untile TRR mode is ended. Unlike to DDR4, LPDDR doesn’t have bank groups, that difference makes LPDDR4 difficult to support to other banks to have activities.

A LPDDR4 SDRAM's row has a limited number of times a given row can be accessed within a refresh period (tREFW * 2) prior to requiring adjacent rows to be refreshed. The Maximum Activate Count (MAC) is the maximum number of activates that a single row can sustain within a refresh period before the adjacent rows need to be refreshed. The row receiving the excessive actives is the Target Row (TRn), the adjacent rows to be refreshed are the victim rows. When

PDF-XChange Viewer
Click to buy NOW!
www.docu-track.com

the MAC limit is reached on TRn, either the LPDRR4 SDRAM receive all (R * 2) Refresh Commands before another row activate is issued, or the LPDRR4 SDRAM should be placed into Targeted Row Refresh (TRR) mode. The TRR Mode will re-fresh the rows adjacent to the TRn that encountered tMAC limit.

There could be a maximum of two target rows to a victim row in a bank. The cumulative value of the activates from the two target rows on a victim row in a bank should not exceed MAC value as well.

Fields required to support the TRR settings are shown in the MR24 table. Setting MR24 [OP7=1] enables TRR Mode and setting MR24 [OP7=0] disables TRR Mode. MR24 [OP6:OP4] defines which bank (BAn) the target row is located in.

The TRR mode must be disabled during initialization as well as any other LPDRR4 SDRAM calibration modes. The TRR mode is entered from a DRAM Idle State, once TRR mode has been entered, no other Mode Register commands are allowed until TRR mode is completed, except setting MR24 [OP7=0] to interrupt and reissue the TRR mode is allowed . When enabled; TRR Mode is self-clearing; the mode will be disabled automatically after the completion of defined TRR flow; after the 3rd BAn precharge has completed plus tMRD. Optionally the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR4 [OP7=0]; if the TRR is exited via another MRS command, the value written to MR24 [OP6:OP4] are don't cares.

TRR Mode Operation

1. The timing diagram in Figure "TRR Mode Timing Example" depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2 and ACT3) and three cor-responding PRE commands (PRE1, PRE2 and PRE3) to complete TRR mode. A Precharge All (PREA) commands issued while LPDRR4 SDRAM is in TRR mode will also perform precharge to BAn and counts towards a PREn command.

2. Prior to issuing the MRW command to enter TRR mode, the SDRAM should be in the idle state. A MRW command must be issued with MR24 [OP7=1] and MR24 [OP6:OP3] defining the bank in which the targeted row is located. All other MR24 bits should remain unchanged.

3. No activity is to occur in the DRAM until tMRD has been satisfied. Once tMRD has been satis-fied, the only commands to BAn allowed are ACT and PRE until the TRR mode has been com-pleted.

4. The first ACT to the BAn with the TRn address can now be applied, no other command is al-lowed at this point. All other banks must remain inactive from when the first BAn ACT command is issued until [(1.5 * tRAS) + tRP] is satisfied.

5. After the first ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued (1.5 * tRAS) later; and then followed tRP later by the second ACT to the BAn with the TRn address. ~~Once the 2nd activate to the BAn is issued, nonBAn banks are allowed to have activity.~~

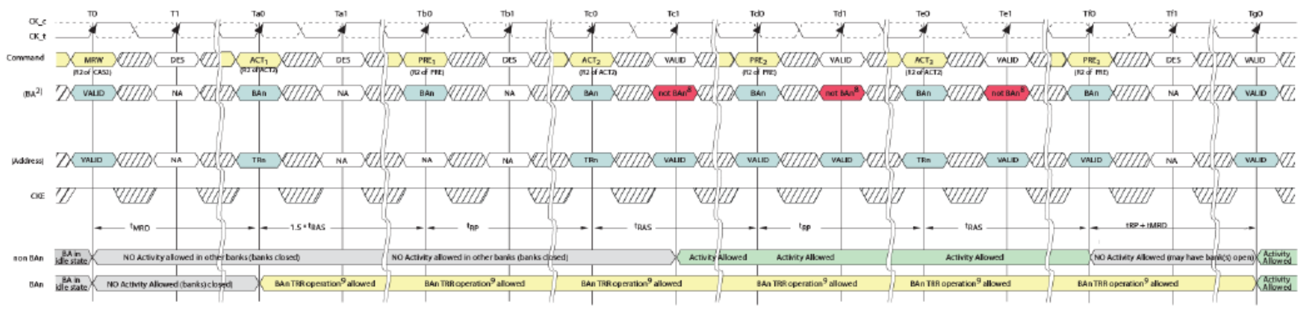
6. After the second ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued tRAS later and then followed tRP later by the third ACT to the BAn with the TRn address.

7. After the third ACT to the BAn with the TRn address is issued, a PRE to BAn would be issued tRAS later; and once the third PRE has been issued, nonBAn bank groups are not allowed to have activity until TRR mode is exited. The TRR mode is completed once tRP plus tMRD is satisfied.

8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Any-time the TRR mode is interrupted and not completed, the interrupted TRR Mode must be cleared and then subsequently performed again. To clear an interrupted TRR mode, an MR24 change is required with setting MR24 [OP7=0], MR24 [OP6:OP3] are don't care, followed by three PRE to BAn, tRP time in between each PRE command. The complete TRR sequence (Steps 2-7) must be then re-issued and completed to guarantee that the adjacent rows are refreshed.

9. Refresh command to the LPDRR4 SDRAM or entering Self-Refresh mode is not allowed while the DRAM is in TRR mode.

Figure - TRR Mode Timing Example



Notes
1. TRn is targeted row.
2. Bank group BAn represents the bank in which the targeted row is located.
3. TRR mode self-clears after tMRD + tRP measured from 3rd BAn precharge PRE_3 at clock edge Tg0.
4. TRR mode or any other activity can be re-engaged after tRP + tMRD from 3rd BAn precharge PRE_3. PRE_ALL also counts if issued instead of PREn. TRR mode is cleared by DRAM after PRE_3 to the BAn bank.
5. Activate commands to BAn during TRR Mode do not provide refreshing support, i.e. the Refresh counter is unaffected.
6. The DRAM must restore the degraded row(s) caused by excessive activation of the targeted row (TRn) neccessary to meet refresh requirements.
7. A new TRR mode must wait tMRD + tRP time after the third precharge.
8. BAn may not be used with any other command.
9. ACT and PRE are the only allowed commands to BAn during TRR Mode.
10. Refresh commands are not allowed during TRR mode.
11. All DRAM timings are to be met by DRAM during TRR mode such as tFAW. Issuing of ACT1, ACT2 and ACT3 counts towards tFAW budget.

4.13.8. Post Package Repair - PPR

LPDDR4 supports Fail Row address repair as an optional feature and it is readable through MR25 OP[7:0].

PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With PPR, LPDDR4 can correct 1Row per Bank.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the PPR mode entry and repair.

4.13.8.1. Fail Row Address Repair

The following is procedure of PPR.

1. Before entering 'PPR' mode, All banks must be Precharged
2. Enable PPR using MR4 bit "OP4=1" and wait tMOD
3. Issue ACT command with Fail Row address
4. Wait tPGM to allow DRAM repair target Row Address internally and issue PRE
5. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address

6. Exit PPR with setting MR4 bit “OP4=0”
7. LPDDR4 will accept any valid command after tPGMPST
8. In More than one fail address repair case, Repeat Step 2 to 7

Once PPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after PPR exit with MR4 [OP4=0] and tPGMPST.

The following table and Timing diagram show PPR related MR bits and its operation.

4.13.8.2. Programming PPR support in MR25

PPR is optional feature of LPDDR4 so Host can recognize if DRAM is supporting PPR or not by reading out MR25

Post Package Repair (MR25)	Read only	OP[7:0]	0B: PPR not supported 1B: PPR supported

4.13.8.3. PPR Timing Parameters

Repair requires additional time period to repair Fail Row Address into spare Row address and the followings are requirement timing parameters for PPR.

Table - PPR Timing Parameters

Parameter	Symbol	LPDDR4		Unit	Notes
		Min	Max		
PPR Programming Time	tPGM	1000	-	ms	
PPR Exit Time	tPGM_Exit	15	-	ns	
New Address Setting Time	tPGMPST	50	-	us	

4.13.9. Mode Register Write - Frequency Set Point (FSP)

Frequency Set-Points allow the LPDDR4-SDRAM CA Bus to be switched between two differing operating frequencies, with changes in voltage swings and termination values, without ever being in an un-trained state which could result in a loss of communication to the DRAM. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the DRAM operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSP-WR bit allows MR parameters to be changed for an alternate Frequency Set-Point without affecting the LPDDR4-SDRAM's current operation. Once all necessary parameters have been written to the alternate Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have two physical registers controlled by FSP-WR and FSP-OP include:

Table - Mode Register Function with two physical registers

MR#	Operand	Function	Note
MR1	OP[2]	WR-PRE (WR Pre-amble Length)	
	OP[3]	RD-PRE (RD Pre-amble Type)	
	OP[6:4]	nWR (Write-Recovery for Auto-Pre-charge commands)	
	OP[7]	RPST (RD Post-Amble Length)	
MR2	OP[2:0]	RL (Read Latency)	
	OP[5:3]	WL (Write Latency)	
	OP[6]	WLS (Write Latency Set)	
MR3	OP[0]	PU-Cal (Pull-up Calibration Point)	1
	OP[1]	WR PST (WR Post-Amble Length)	
	OP[5:3]	PDDS (Pull-down Drive Strength)	
	OP[6]	DBI-RD (DBI Read Enable)	
	OP[7]	DBI-WR (DBI Write Enable)	
MR11	OP[2:0]	DQ ODT (DQ Bus Receiver On-Die-Termination)	
	OP[6:4]	CA ODT (CA Bus Receiver On-Die-Termination)	
MR12	OP[5:0]	VREF(ca) (Vref(ca) Setting)	
	OP[6]	VR-CA (Vref(ca) Range)	
MR14	OP[5:0]	Vref(dq) (Vref(dq) Setting)	
	OP[6]	VR-DQ (Vref(dq) Range)	
MR22	OP[2:0]	SoC ODT (Controller ODT Value for VOH calibration)	
	OP[3]	ODTE-CK (CK ODT Enabled for nonterminating rank)	
	OP[4]	ODTE-CS (CS ODT enable for non terminating rank)	
	OP[5]	ODTD-CA (CA ODT termination disable)	

Note:
1. The synchronization MR3 OP[0] setting between Ch.0 and Ch.1 then the ZQ calibration is required in order to achieve a Driver strength and ODT tolerance to change MR3 OP[0] PU-CAL is changed through FSP.

See Mode Register Definition for more details.

Following table shows how the two mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

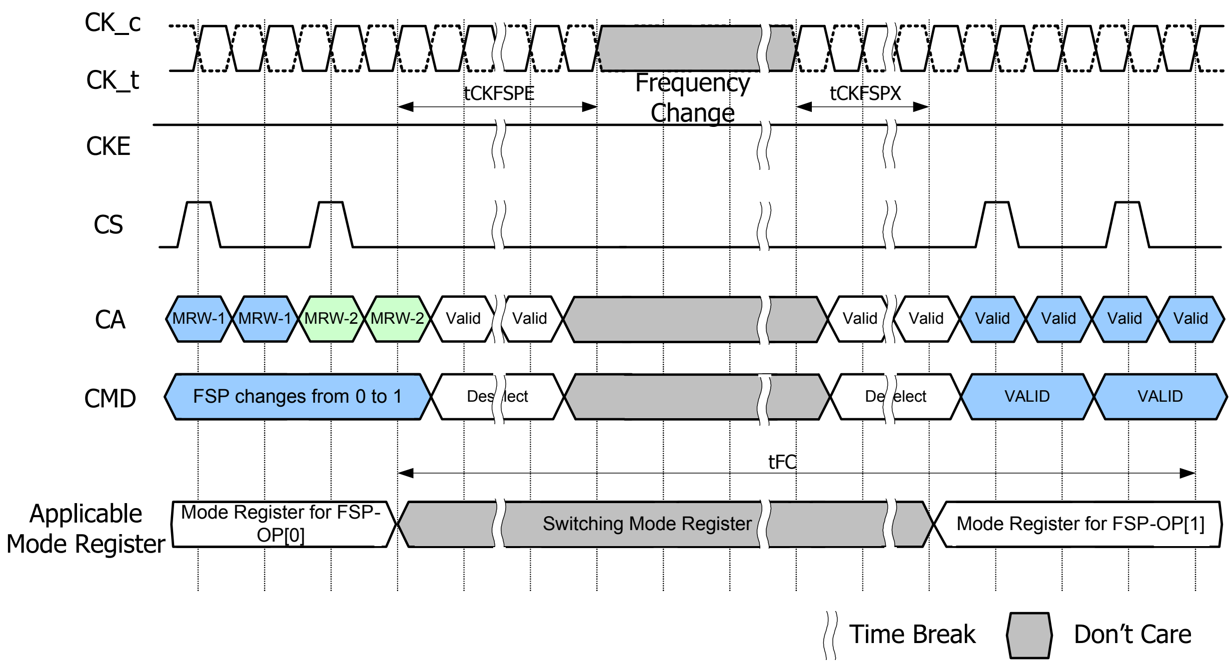
Function	MR# & Operand	Data	Operation	Note
FSP-WR	MR13 OP[6]	0 (Default)	Data write to Mode Register N for FSP-OP[0] by MRW command.	1
		1	Data write to Mode Register N for FSP-OP[1] by MRW command.	
FSP-OP	MR13 OP[7]	0 (Default)	DRAM operates with Mode Register N for FSP-OP[0] setting.	2
		1	DRAM operates with Mode Register N for FSP-OP[1] setting.	

Notes:
1. FSP-WR stands for Frequency Set Point Write/Read.
2. FSP-OP stands for Frequency Set Point Operating Point.

4.13.9.1. Frequency Set Point update timing

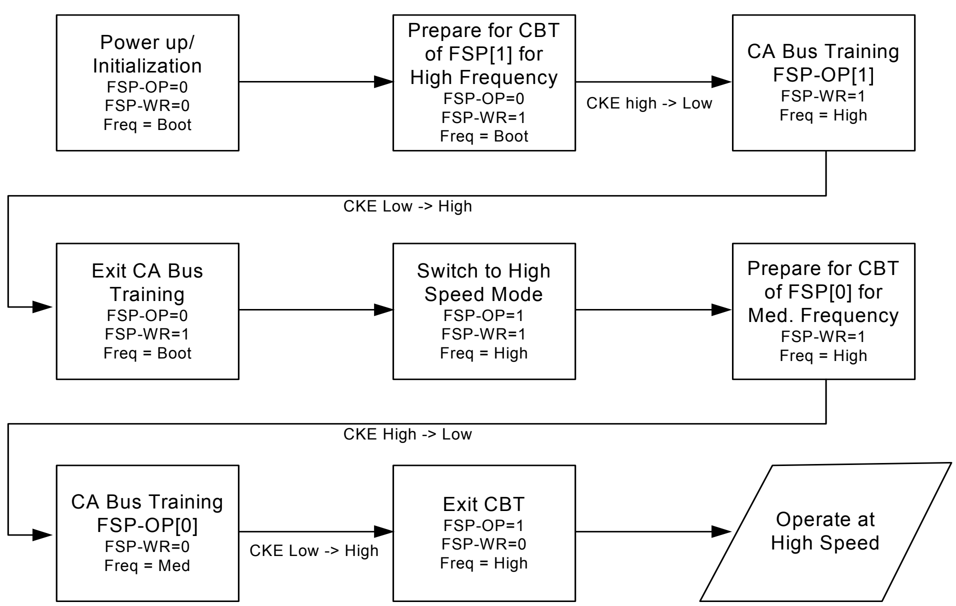
The Frequency set point update timing is shown in the timing diagram below.

Figure - Frequency Set Point Switching Timing



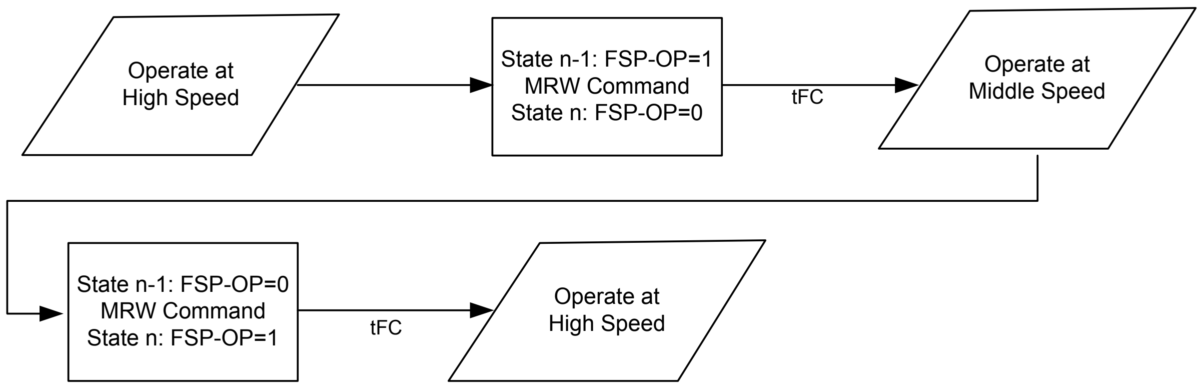
The LPDDR4-SDRAM defaults to FSP-OP[0] at power-up. Both Set-Points default to settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR4-SDRAM to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point (Figure "Training Two Frequency Set Points"). See the section Command Bus Training for more details on this training mode.

Figure - Training Two Frequency Set Points



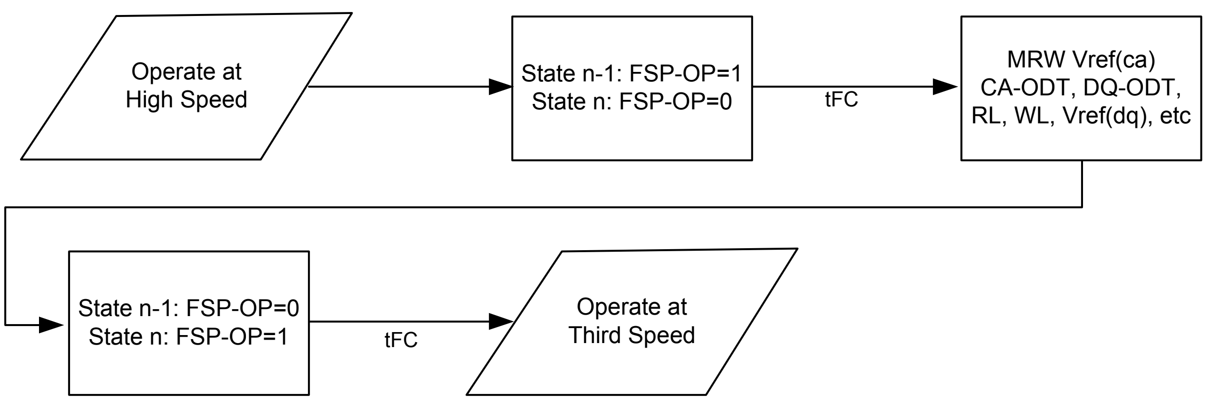
Once both Frequency Set Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (figure below)

Figure - Switching between two trained Frequency Set Points



Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously-trained values (in particular the Vref-CA calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure below).

Figure - Switching to a third trained Frequency Set Point



4.13.10. Read Preamble Training

LPDDR4 READ Preamble Training is supported through the MPC function.

This mode can be used to train or read level the DQS receivers. Once READ Preamble Training is enabled by MR13[OP1] = 1, the LPDDR4 DRAM will drive DQS_t LOW, DQS_c HIGH within tSDO and remain at these levels until an MPC DQ READ Training command is issued.

During READ Preamble Training the DQS preamble provided during normal operation will not be driven by the DRAM. Once the MPC DQ READ Training command is issued, the DRAM will drive DQS_t/DQD_c like a normal READ burst after RL. DRAM may or may not drive DQ[15:0] in this mode.

While in READ Preamble Training Mode, only READ DQ Training commands may be issued.
READ Preamble Training is exited within tSDO after setting MR13[OP1] = 0.

Figure - Read Preamble Training