

# eMCP Specification

32GB eMMC (x8)  
+ 24Gb LPDDR4X (x16, 2CH/2CS)

## Document Title

eMCP

32GB eMMC(x8) Flash / 24Gb (x16, 2CH/2CS) LPDDR4X

## Revision History

| Revision No. | History         | Draft Date | Remark      |
|--------------|-----------------|------------|-------------|
| 0.1          | - Initial Draft | Jan. 2019  | Preliminary |
| 1.0          | - Final Version | Mar. 2019  |             |

## FEATURES

### [ eMCP ]

- Operation Temperature
  - (-25)°C ~ 85°C
- Package
  - 254-ball FBGA
  - 11.5x13.0mm<sup>2</sup>, 1.0t, 0.5mm pitch
  - Lead & Halogen Free

### [ eMMC ]

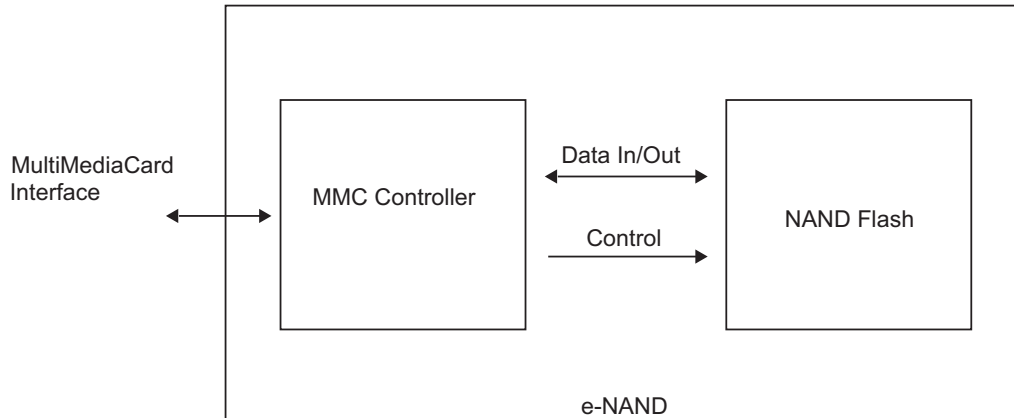
- **eMMC5.1 compatible**  
(Backward compatible to eMMC4.5&eMMC5.0)
- **Bus mode**
  - Data bus width : 1bit(default), 4bits, 8bits
  - Data transfer rate: up to 400MB/s (HS400)
  - MMC I/F Clock frequency : 0~200MHz
  - MMC I/F Boot frequency : 0~52MHz
- **Operating voltage range**
  - V<sub>cc</sub> (NAND) : 2.7V - 3.6V
  - V<sub>ccq</sub> (Controller) : 1.7V - 1.95V
- **Temperature**
  - Operation (-25°C ~ +85°C)
  - Storage without operation (-40°C ~ +85°C)
- **Others**
  - This product is compliance with the RoHS directive
- **Supported features**
  - HS400, HS200
  - HPI, BKOPS, **BKOP operation control**
  - Packed CMD, **CMD queuing**
  - Cache, **Cache barrier, Cache flushing report**
  - Partitioning, RPMB, RPMB throughput improve
  - Discard, Trim, Erase, Sanitize
  - Write protect, Secure write protection
  - Lock/Unlock
  - PON, Sleep/Awake
  - Reliable Write
  - Boot feature, Boot partition
  - HW/SW Reset
  - Field Firmware Update
  - Configurable driver strength
  - Health(Smart) report
  - Production state awareness
  - Secure removal type
  - Data Strobe pin, **Enhanced data strobe**  
(**Bold features are added in eMMC5.1**)

### [ LPDDR4X ]

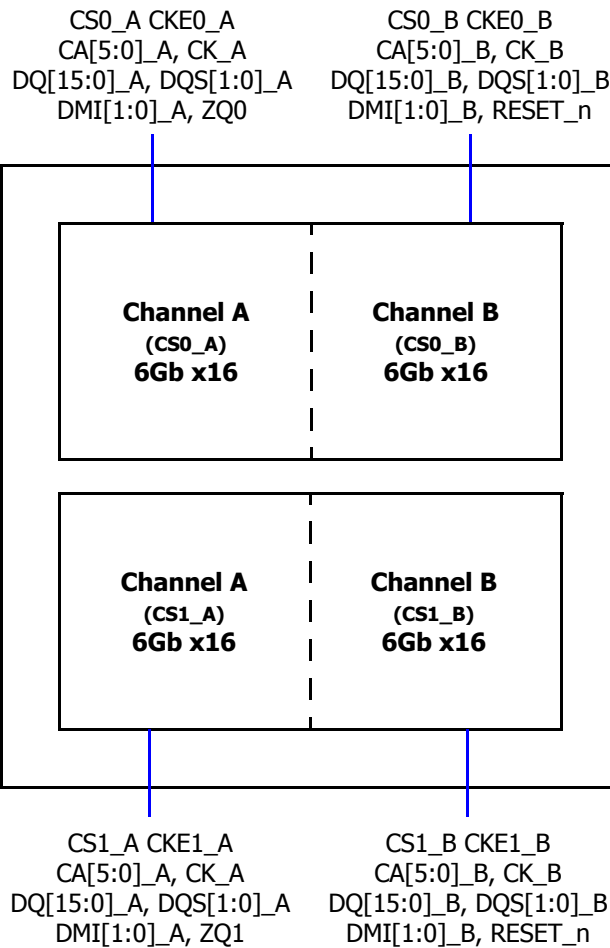
- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2 = 1.1V (1.06V to 1.17V)
- VDDQ = 0.6V (0.57V to 0.65V)
- Programmable CA ODT and DQ ODT with VSSQ termination
- VOH compensated output driver
- Single data rate command and address entry
- Double data rate architecture for data Bus;
  - two data accesses per clock cycle
- Differential clock inputs (CK<sub>t</sub>, CK<sub>c</sub>)
- Bi-directional differential data strobe (DQS<sub>t</sub>, DQS<sub>c</sub>)
- DMI pin support for write data masking and DBIdc functionality
- Programmable RL (Read Latency) and WL (Write Latency)
- Burst length: 16 (default), 32 and On-the-fly
  - On the fly mode is enabled by MRS
- Auto refresh and self refresh supported
- All bank auto refresh and directed per bank auto refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- Background ZQ Calibration

## Functional Block Diagram

**eMMC Block Diagram**



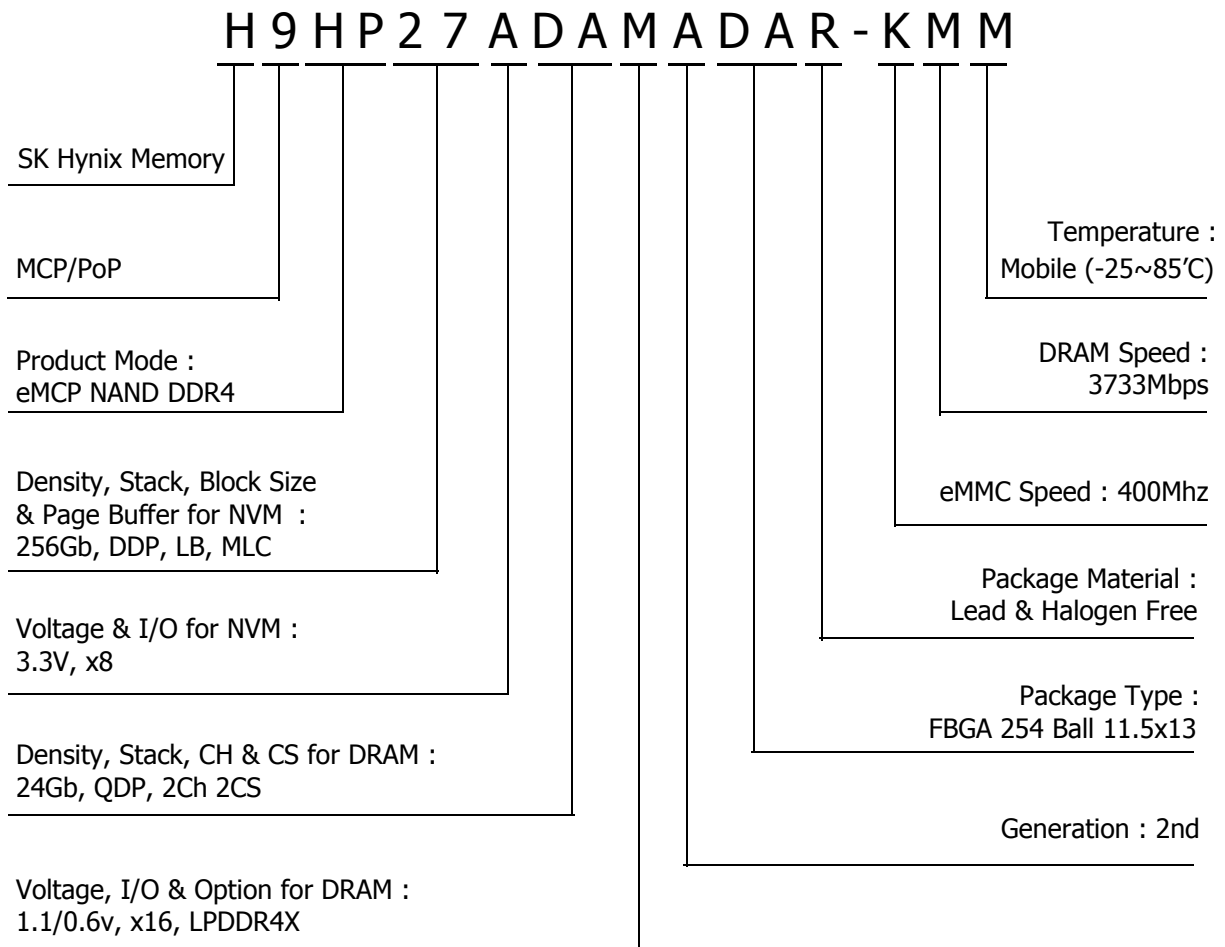
**DRAM Block Diagram**



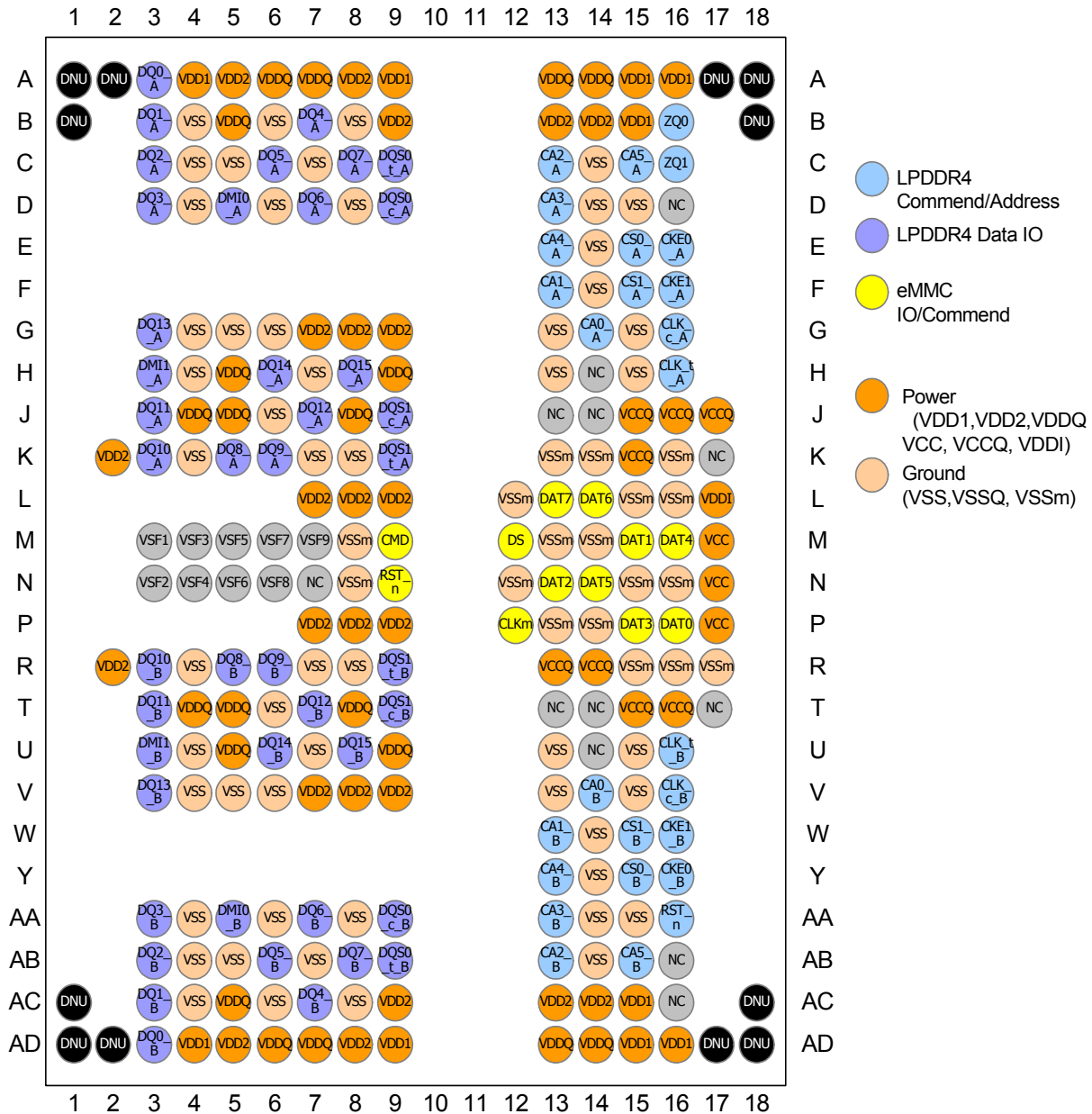


## ORDERING INFORMATION

| Part Number        | Memory Combination | Operation Voltage      | Density                 | Speed               | Package                               |
|--------------------|--------------------|------------------------|-------------------------|---------------------|---------------------------------------|
| H9HP27ADAMADAR-KMM | eMMC<br>LPDDR4X    | 3.3V<br>1.8V/1.1V/0.6V | 32GB (x8)<br>24Gb (x16) | 400Mhz<br>DDR4 3733 | 254Ball FBGA<br>(Lead & Halogen Free) |



## Ball ASSIGNMENT



*Top View*

*254ball MCP  
eMMC + x32 LPDDR4 (2CH)*

Note: 1. Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

**eMMC Pin Description****< 32GB (x8, MMC) eMMC >**

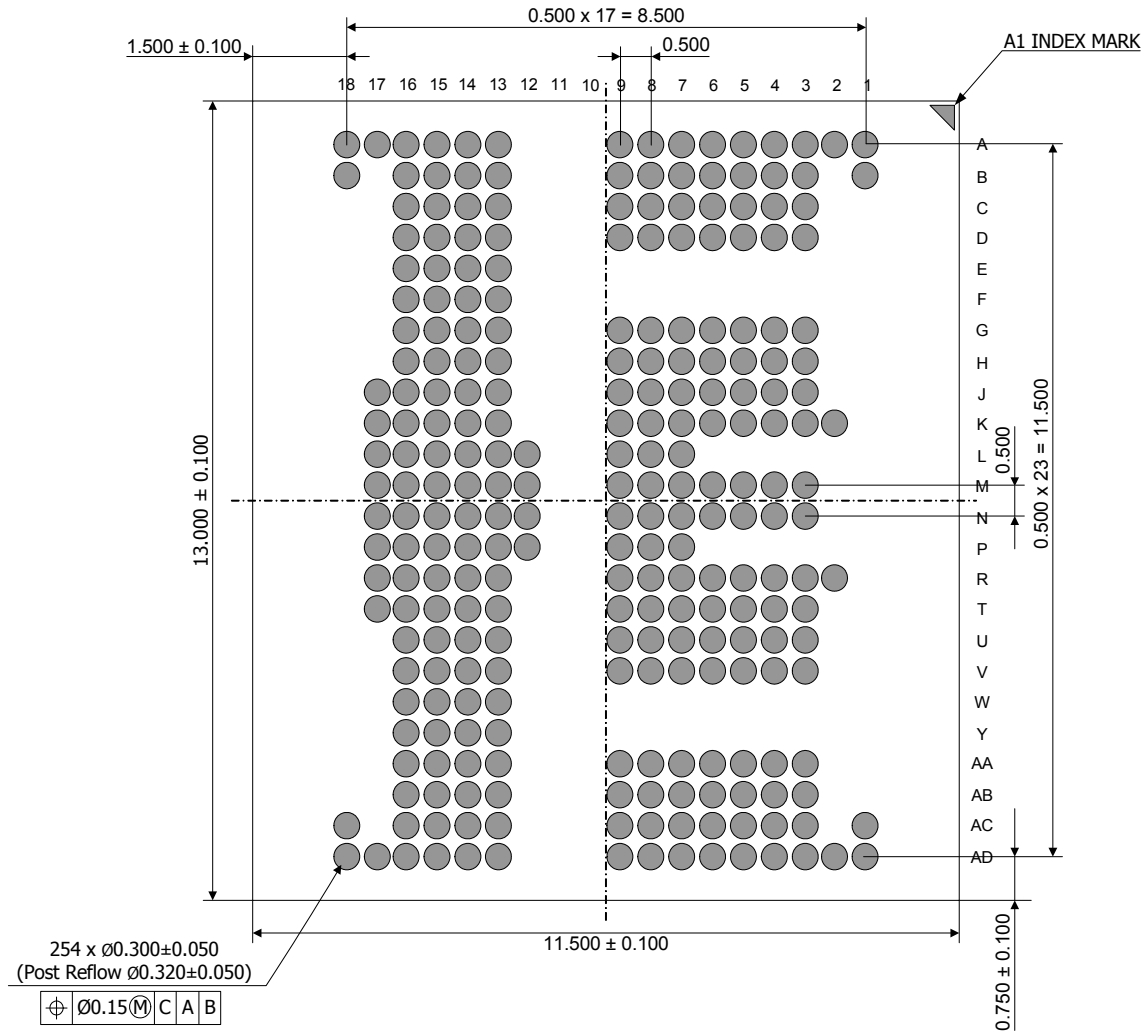
| <b>SYMBOL</b> | <b>DESCRIPTION</b>                                             | <b>Type</b>  |
|---------------|----------------------------------------------------------------|--------------|
| CLK           | Clock                                                          | Input        |
| CMD           | Command                                                        | Input/Output |
| DAT0~DAT7     | Data Input/Output                                              | Input/Output |
| DS            | Data Strobe                                                    | Output       |
| VCC           | Core Power Supply                                              | Power        |
| VCCQ          | I/O Power Supply                                               | Power        |
| VSS           | Ground                                                         | Ground       |
| VDDI          | By pass                                                        | Power        |
| VSF           | Vendor Specific Function<br>SK hynix use M7, N6 Pin as VSF Pin | Supply       |
| RST           | Reset signal                                                   | Input        |

## DRAM Pin Description

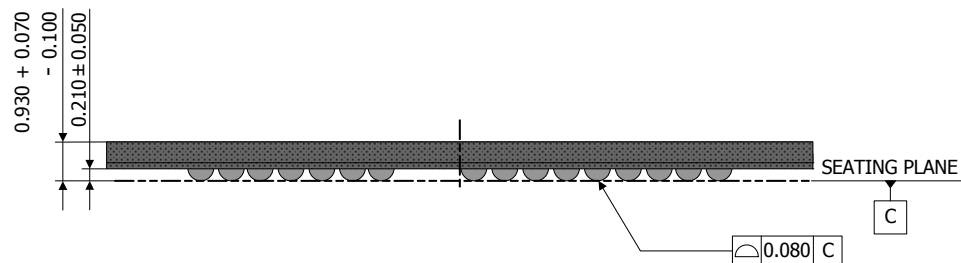
| Symbol                                                          | Type      | Description                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------------------------------------------------------------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK_t_A, CK_c_A<br>CK_t_B, CK_c_B                                | Input     | <b>Clock:</b> CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.                                                                                                                           |
| CKE_A<br>CKE_B                                                  | Input     | <b>Clock Enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions.<br>CKE is part of the command code. Each channel (A & B) has its own CKE signal.                                                                                                                                              |
| CS_A<br>CS_B                                                    | Input     | <b>Chip Select:</b> CS is part of the command code. Each channel (A & B) has its own CS signal.                                                                                                                                                                                                                                                                                                                              |
| CA[5:0]_A,<br>CA[5:0]_B                                         | Input     | <b>Command/Address Inputs:</b> Provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.                                                                                                                                                                                                                                                                       |
| ODT_CA_A<br>ODT_CA_B                                            | Input     | <b>CA ODT Control:</b> The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.                                                                                                                                                                                                                                                                                       |
| DQ[15:0]_A,<br>DQ[15:0]_B                                       | I/O       | <b>Data Input/Output :</b> Bi-direction data bus.                                                                                                                                                                                                                                                                                                                                                                            |
| DQS[1:0]_t_A,<br>DQS[1:0]_c_A,<br>DQS[1:0]_t_B,<br>DQS[1:0]_c_B | I/O       | <b>Read Strobe:</b> DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and is center aligned with Data. Each byte of data has a Data Strobe signal pair.<br>Each channel (A & B) has its own DQS strobes. |
| DMI[1:0]_A,<br>DMI[1:0]_B                                       | I/O       | <b>Data Mask Inversion:</b> DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals.                                                                                                 |
| ZQ                                                              | Reference | <b>Calibration Reference:</b> Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240-Ω ± 1% resistor.                                                                                                                                                                                                                  |
| VDD1, VDD2, VDDQ                                                | Supply    | <b>Power Supplies:</b> Isolated on the die for improved noise immunity.                                                                                                                                                                                                                                                                                                                                                      |
| VSS                                                             | GND       | <b>Ground Reference:</b> Power supply ground reference.                                                                                                                                                                                                                                                                                                                                                                      |
| RESET_n                                                         | Input     | <b>RESET:</b> When asserted LOW, the RESET pin resets both channels of the die.                                                                                                                                                                                                                                                                                                                                              |

## PACKAGE INFORMATION

254 Ball 0.5mm pitch 11.5mm x 13.0mm FBGA [t = 1.0mm max]



Bottom View



Front View

## 32GB(x8) eMMC Flash

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## 1. Introduction

### 1.1 General Description

SK hynix eMMC consists of NAND flash and MMC controller.

eMMC has the built-in intelligent controller which manages interface protocols, wear leveling, bad block management, garbage collection, and ECC. eMMC protects the data contents from the host sudden power off failure.

eMMC is compatible with JEDEC standard eMMC5.1 specification.

## 2. eMMC Characteristics

### 2.1 Performance

| Density       | Sequential Write<br>(MB/s) | Sequential Read<br>(MB/s) |
|---------------|----------------------------|---------------------------|
| 32GB<br>(DDP) | 90                         | 280                       |

- Tool : Device level
- eMMC I/F speed : HS400
- Seq. chunk size : 512KB
- Adapted feature : Cache on
- Not 100% tested



## 2.2 Power

### 2.2.1 Active Power Consumption During Operation

| Density    |           | $I_{cc}$ | $I_{ccq}$ |
|------------|-----------|----------|-----------|
| 32GB (DDP) | Avg (mA)  | 80       | 200       |
|            | Peak (mA) | 150      | 250       |

- Temperature : 25°C
- Average current consumption : over a period of 100ms
- Peak current consumption : averaged over a period of 20us
- Vcc : 3.3V
- Vccq : 1.8V
- Not 100% tested

### 2.2.2 Low Power Mode (Idle)

| Density    | Room Temperature (25℃) |                  | Hot Temperature (85℃) |                  |
|------------|------------------------|------------------|-----------------------|------------------|
|            | I <sub>cc</sub>        | I <sub>ccq</sub> | I <sub>cc</sub>       | I <sub>ccq</sub> |
| 32GB (DDP) | Typ. 60uA              | Typ. 120uA       | Max. 100uA            | Max. 500uA       |

- In Standby Power mode, CTRL V<sub>ccq</sub> & NAND V<sub>cc</sub> power supply is switched on
- No data transaction period before entering sleep status
- Not 100% tested.

### 2.2.3 Low Power Mode (CMD5 Sleep)

| Density    | Room Temperature (25℃) |                  | Hot Temperature (85℃) |                  |
|------------|------------------------|------------------|-----------------------|------------------|
|            | I <sub>cc</sub>        | I <sub>ccq</sub> | I <sub>cc</sub>       | I <sub>ccq</sub> |
| 32GB (DDP) | 0                      | Typ. 120uA       | 0                     | Max. 500uA       |

- In Sleep state, triggered by CMD5, NAND V<sub>cc</sub> power supply is switched off (CTRL V<sub>ccq</sub> on)
- Temperature : 25℃
- Not 100% tested.

### 3. eMMC New features (eMMC5.0 and eMMC5.1)

#### 3.1 eMMC5.0 New features

##### 3.1.1 HS400 mode

eMMC supports HS400 signaling to achieve a bus speed of 400MB/s via a 200MHz DDR clock frequency. HS400 mode supports only 8-bit bus width and the 1.8V  $V_{CCQ}$ . Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data (Read Data and CRC Response) with DS pin. eMMC supports up to 5 Driver Strength.

| Driver type values | Support   | Nominal Impedance | Approximated driving capability compared to Type_0 | Remark                                                                                    |
|--------------------|-----------|-------------------|----------------------------------------------------|-------------------------------------------------------------------------------------------|
| 0                  | Mandatory | 50 $\Omega$       | x 1                                                | Default Driver Type. Supports up to 200MHz operation.                                     |
| 1                  | Optional  | 33 $\Omega$       | x 1.5                                              | Supports up to 200MHz operation.                                                          |
| 2                  |           | 66 $\Omega$       | x 0.75                                             | The weakest driver that supports up to 200MHz operation.                                  |
| 3                  |           | 100 $\Omega$      | x 0.5                                              | For low noise and low EMI systems. Maximal operating frequency is decided by host design. |
| 4                  |           | 40 $\Omega$       | x 1.2                                              |                                                                                           |

[Table 1] I/O Driver strength types

Selecting **HS\_Timing** depends on Host I/F speed, default is 0, but all of value can be selected by host.

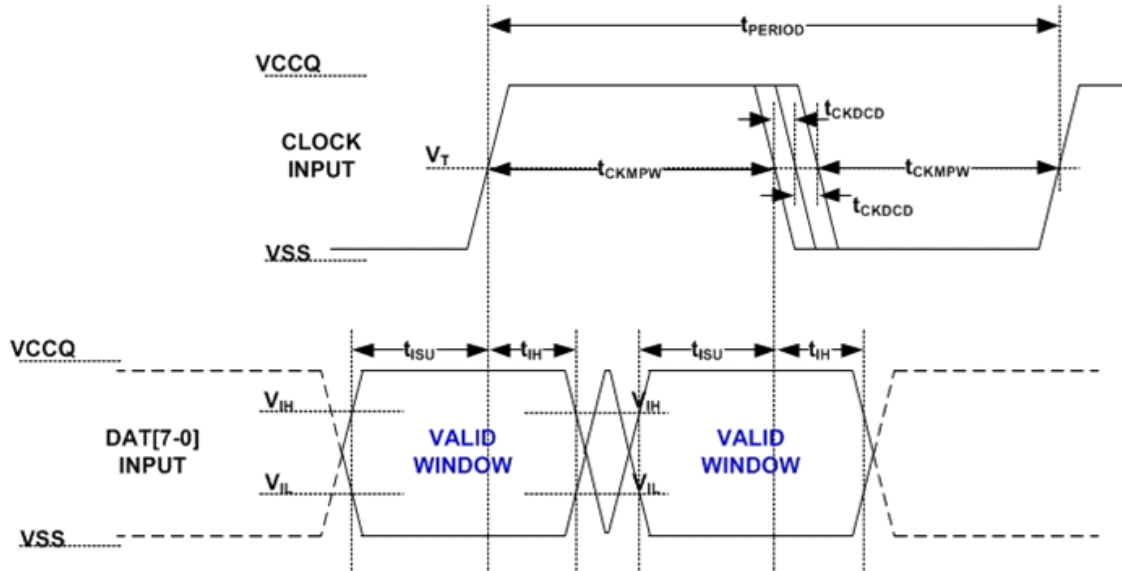
| Value | Timing                                            | Supportability for eMMC |
|-------|---------------------------------------------------|-------------------------|
| 0x00  | Selecting backward compatibility interface timing | Support                 |
| 0x01  | High speed                                        | Support                 |
| 0x02  | HS200                                             | Support                 |
| 0x03  | HS400                                             | Support                 |

[Table 2] HS\_Timing values

### 3.1.1.1 Bus timing specification in HS400 mode

#### ■ HS400 Device input timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.



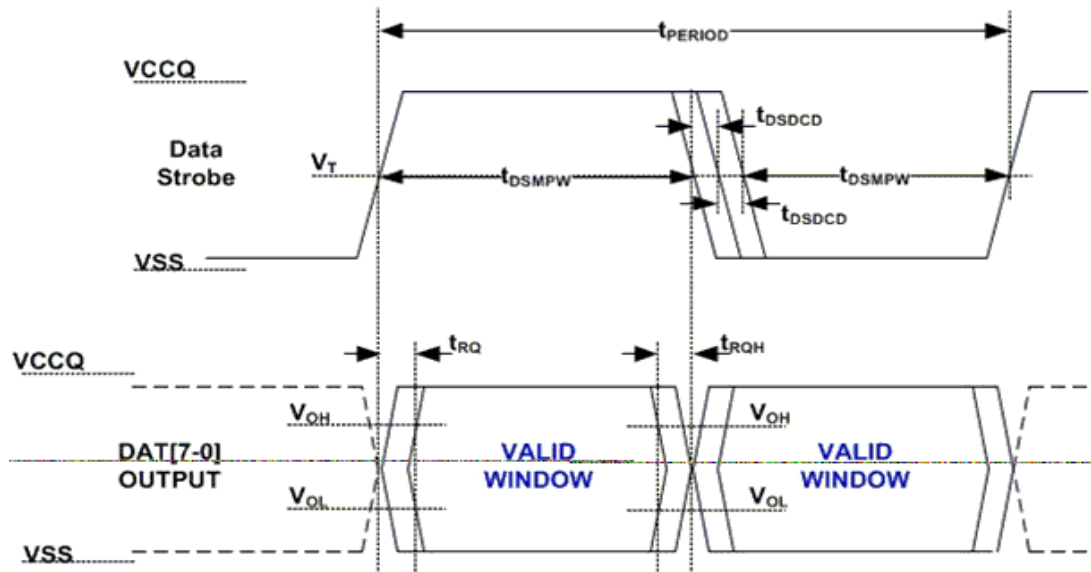
[Figure 1] HS400 Device input timing

| Parameter                     | Symbol       | Min   | Max | Unit | Remark                                                                                                 |
|-------------------------------|--------------|-------|-----|------|--------------------------------------------------------------------------------------------------------|
| Input CLK                     |              |       |     |      |                                                                                                        |
| Cycle time data transfer mode | $t_{PERIOD}$ | 5     |     |      | 200MHz(Max), between rising edges with respect to $V_T$                                                |
| Slew rate                     | SR           | 1.125 |     | V/ns | With respect to $V_{IH}/V_{IL}$                                                                        |
| Duty cycle distortion         | $t_{CKDCD}$  | 0.0   | 0.3 | ns   | Allowable deviation from an ideal 50% duty cycle. With respect to $V_T$ . Includes jitter, phase noise |
| Minimum pulse width           | $t_{CKMPW}$  | 2.2   |     | ns   | With respect to $V_T$                                                                                  |
| Input DAT (referenced to CLK) |              |       |     |      |                                                                                                        |
| Input set-up time             | $t_{ISUddr}$ | 0.4   |     | ns   | $C_{DEVICE} \leq 6pF$<br>With respect to $V_{IH}/V_{IL}$                                               |
| Input hold time               | $t_{IHddr}$  | 0.4   |     | ns   | $C_{DEVICE} \leq 6pF$<br>With respect to $V_{IH}/V_{IL}$                                               |
| Slew rate                     | SR           | 1.125 |     | V/ns | With respect to $V_{IH}/V_{IL}$                                                                        |

[Table 3] HS400 Device input timing

### ■ HS400 Device output timing

Data strobe is for reading data in HS400 mode. Data strobe is toggled only during data read or CRC status response.



[Figure 2] HS400 Device output timing

| Parameter                              | Symbol       | Min   | Max                    | Unit         | Remark                                                                                                                            |
|----------------------------------------|--------------|-------|------------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Data Strobe                            |              |       |                        |              |                                                                                                                                   |
| Cycle time data transfer mode          | $t_{PERIOD}$ | 5     |                        |              | 200MHz(Max), between rising edges with respect to $V_T$                                                                           |
| Slew rate                              | SR           | 1.125 |                        | V/ns         | With respect to $V_{OH}/V_{OL}$ and HS400 reference load                                                                          |
| Duty cycle distortion                  | $t_{DSDCD}$  | 0.0   | 0.2                    | ns           | Allowable deviation from the input CLK duty cycle distortion( $t_{CKDCD}$ )<br>With respect to $V_T$ Includes jitter, phase noise |
| Minimum pulse width                    | $t_{DSMPW}$  | 2.0   |                        | ns           | With respect to $V_T$                                                                                                             |
| Read pre-amble                         | $t_{RPRE}$   | 0.4   | 5 (One Clock Cycle)    | $t_{PERIOD}$ | Max value is specified by manufacturer. value up to infinite is valid.                                                            |
| Read post-amble                        | $t_{RPST}$   | 0.4   | 2.5 (Half Clock Cycle) | $t_{PERIOD}$ | Max value is specified by manufacturer. value up to infinite is valid.                                                            |
| Output DAT (referenced to Data strobe) |              |       |                        |              |                                                                                                                                   |
| Output skew                            | $t_{RQ}$     |       | 0.4                    | ns           | With respect to $V_{OH}/V_{OL}$ and HS400 reference load                                                                          |
| Output hold skew                       | $t_{RQH}$    |       | 0.4                    | ns           | With respect to $V_{OH}/V_{OL}$ and HS400 reference load                                                                          |
| Slew rate                              | SR           | 1.125 |                        | V/ns         | With respect to $V_{OH}/V_{OL}$ and HS400 reference load                                                                          |

[Table 4] HS400 Device output timing

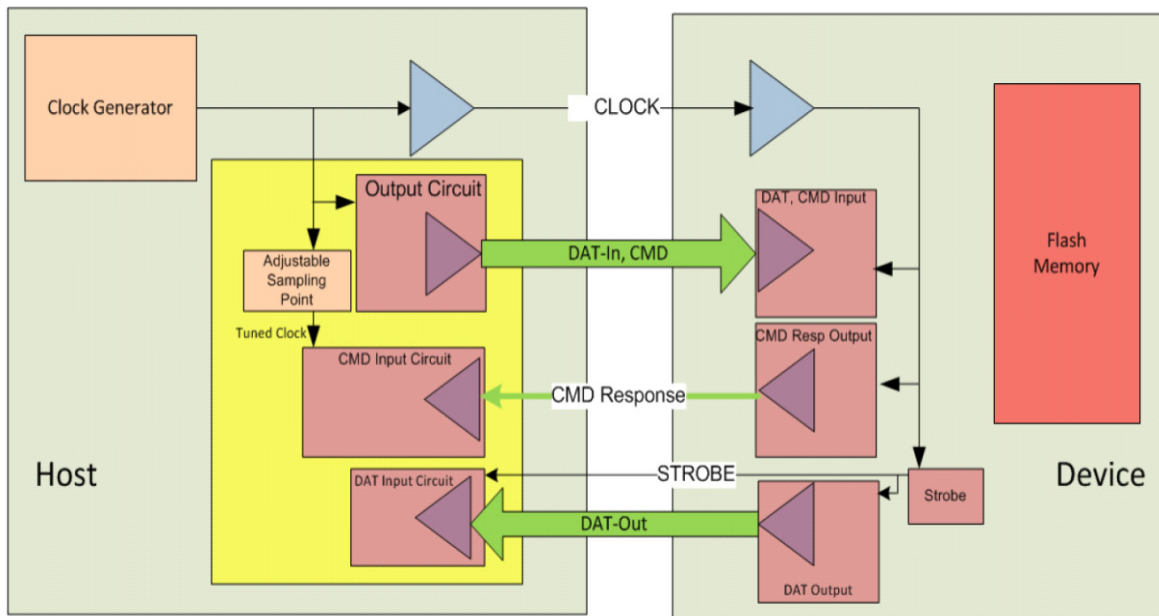
| Parameter                             | Symbol       | Min | Type | Max | Unit | Remark |
|---------------------------------------|--------------|-----|------|-----|------|--------|
| Pull-up resistance for CMD            | $R_{CMD}$    | 4.7 |      | 100 | Kohm |        |
| Pull-up resistance for DAT0-7         | $R_{DAT}$    | 10  |      | 100 | Kohm |        |
| Pull-down resistance for Data strobe  | $R_{DS}$     | 10  |      | 100 | Kohm |        |
| Internal pull up resistance DAT1-DAT7 | $R_{int}$    | 10  |      | 150 | Kohm |        |
| Bus signal line capacitance           | $C_L$        |     |      | 13  | pF   |        |
| Single Device capacitance             | $C_{Device}$ |     |      | 6   | pF   |        |

**[Table 5] HS400 Device input timing\***

\* For connection guide, see Table 14.

## ■ Data Strobe for HS400

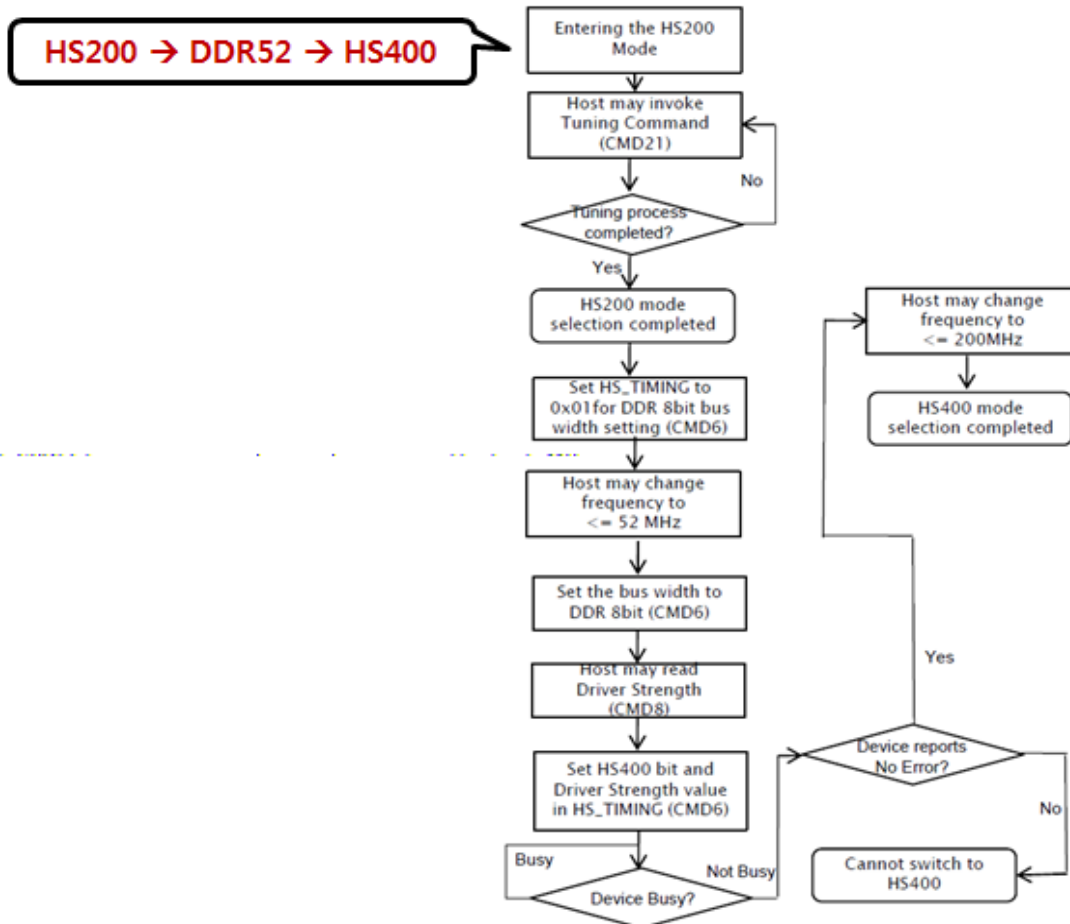
Data strobe is Return Clock signal used in HS400 mode. This signal is generated by the device and used for data output and CRC status response output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output, the CRC status is latched on the positive edge only, and don't care on the negative edge. Data strobe signal is toggled only for Data out and CRC response (Align CMD response as well as CRC response to the DS in eMMC5.1)



[Figure 3] HS400 Host and Device block diagram

### 3.1.1.2 HS400 Mode selection

Following JEDEC standard for eMMC5.0, changing bus mode directly from HS200 to HS400 is not allowed. It has a rule for changing bus width from SDR mode to DDR mode that HS\_TIMING must be set to "0x01"(HS mode : 52MHz) before setting BUS\_WIDTH for DDR operation. We recommend the HS400 bus mode selection sequence as following. (eMMC5.1 has basically same flow, but 'enhanced strobe feature' is added. Please refer to 4.2.6 Enhanced strobe)



[Figure 4] HS400 Bus mode selection sequence



**■ EXT\_CSD register for Data strobe****• Enhanced Strobe field in BUS\_WIDTH [183]**

| Bit 7           | Bit 6    | Bit 5 | Bit 4 | Bit 3              | Bit 2 | Bit 1 | Bit 0 |
|-----------------|----------|-------|-------|--------------------|-------|-------|-------|
| Enhanced Strobe | Reserved |       |       | Bus Mode Selection |       |       |       |

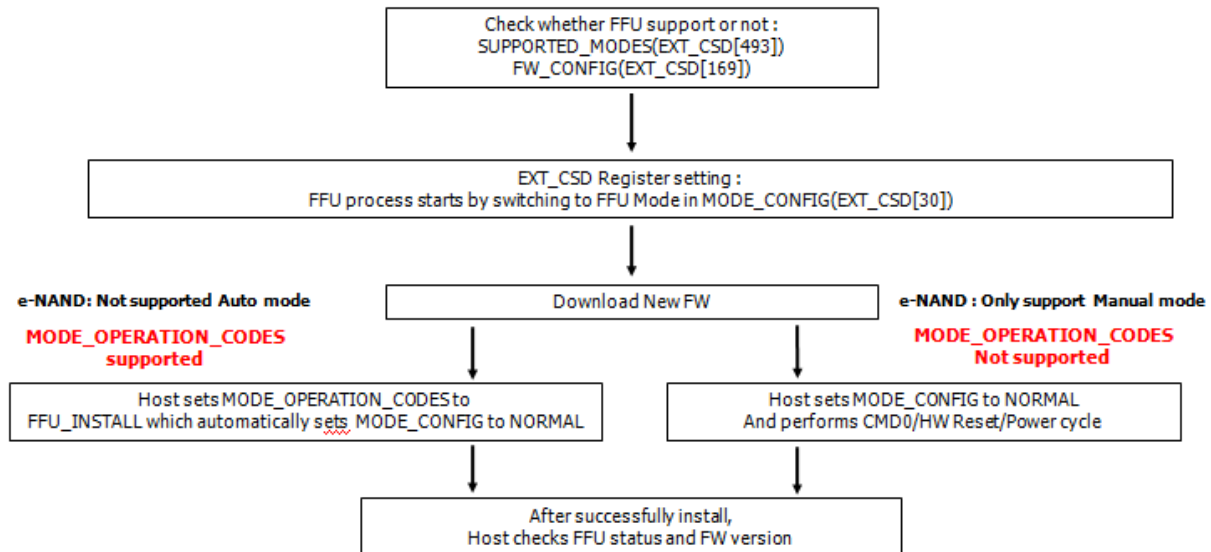
BIT[7] : 0: Strobe is provided only during data out and CTC response [Default]

1: Strobe is provided during data out, CRC response and CMD response

The support of STROBE\_ENHANCED mode is optional for devices. STROBE\_SUPPORT[184] register of EXT\_CSD indicates whether a device supports that mode.

### 3.1.2 Field firmware update (FFU)

To download a new firmware, the eMMC requires instruction sequence following JEDEC standard. SK hynix eMMC only supports Manual mode (MODE\_OPERATION\_CODES is not supported). For more details, see as the following chart and register table given below.



[Figure 5] FFU flow chart

#### 3.1.2.1 Field F/W update flow - CMD sequence

| Operation                    | CMD                     | Remark                                                                                                |
|------------------------------|-------------------------|-------------------------------------------------------------------------------------------------------|
| Set bus width (1bit or 4bit) |                         | Bus width should be 1bit or 4bit                                                                      |
| Set block length 512B        | CMD16, arg : 0x00000200 |                                                                                                       |
| Enter FFU mode               | CMD6, arg : 0x031E0100  |                                                                                                       |
| Send FW to device(Download)  | CMD25, arg : 0xFFFFAFF0 | Sending CMD25 is followed by sending FW data                                                          |
| CMD12 : Stop                 | CMD12, arg : 0x00000000 |                                                                                                       |
| CMD6 : Exit FFU mode         | CMD6, arg : 0x031E0000  |                                                                                                       |
| CMD0/HW Reset/Power cycle    |                         |                                                                                                       |
| Re-Init to trans state       | CMD0, CMD1 ...          |                                                                                                       |
| Check if FFU is succeeded    | CMD8, arg : 0x00000000  | Check EXT_CSD[26] : FFU_SUCCESS<br>If FFU_SUCCESS is 0, FFU is succeeded,<br>otherwise FFU is failed. |

### 3.1.2.2 EXT\_CSD Register for FFU

#### ■ SUPPORTED\_MODE[493] (Read Only)

BIT[0] : '0' FFU is not supported by the device. '1' FFU is supported by the device.

BIT[1] : '0' Vendor specific mode (VSM) is not supported by the device. '1' Vendor specific mode is supported by the device.

| Bit      | Field    | Supportability |
|----------|----------|----------------|
| Bit[7:2] | Reserved |                |
| Bit[1]   | VSM      | Not support    |
| Bit[0]   | FFU      | Supported      |

#### ■ FFU\_FEATURE[492] (Read Only)

BIT[0] : '0' Device does not support MODE\_OPERATION\_CODES field (Manual mode)

'1' Device supports MODE\_OPERATION\_CODES field (Auto mode)

| Bit      | Field                          | Supportability |
|----------|--------------------------------|----------------|
| Bit[7:1] | Reserved                       |                |
| Bit[0]   | SUPPORTED_MODE_OPERATION_CODES | Not support    |

#### ■ FF\_ARG[490-487] (Read Only)

Using this field the device reports to the host which value the host should set as an argument for read and write commands is FFU mode.

#### ■ FF\_CONFIG[169] (R/W)

BIT[0] : Update disable

0x0 : FW updates enabled. / 0x01 : FW update disabled permanently

| Bit      | Field          | Supportability           |
|----------|----------------|--------------------------|
| Bit[7:1] | Reserved       |                          |
| Bit[0]   | Update disable | FW updates enabled (0x0) |

### ■ FFU\_STATUS[26] (R/W/E\_P)

Using this field the device reports to the host the state of FFU process.

| Value       | Description                   |
|-------------|-------------------------------|
| 0x13 ~ 0xFF | Reserved                      |
| 0x12        | Error in downloading Firmware |
| 0x11        | Firmware install error        |
| 0x10        | General error                 |
| 0x01 ~ 0x0F | Reserved                      |
| 0x00        | Success                       |

### ■ OPERATION\_CODES\_TIMEOUT[491](Read Only)

Maximum timeout for the SWITCH command when setting a value to the MODE\_OPERATION\_CODES field

The register is set to '0', because the eMMC doesn't support MODE\_OPERATION\_CODES.

| Value       | Description                                                                 | Timeout value   |
|-------------|-----------------------------------------------------------------------------|-----------------|
| 0x01 ~ 0x17 | MODE_OPERATION_CODES_TIMEOUT = 100us x 2 <sub>OPERATION_CODES_TIMEOUT</sub> | 0 (Not defined) |
| 0x18 ~ 0xFF | Reserved                                                                    | -               |

### ■ MODE\_OPERATION\_CODES[29] (W/E\_P)

The host sets the operation to be performed at the selected modes, in case MODE\_CONFIGS is set to FFU\_MODE, MODE\_OPERATION\_CODES could have the following values :

| Bit          | Description |
|--------------|-------------|
| 0x01         | FFU_INSTALL |
| 0x02         | FFU_ABOUT   |
| 0x00, others | Reserved    |

### 3.1.3 Health(Smart) report

Using this feature is for monitoring device status and preventing the error and failure in advance.  
Host can check device information with EXT\_CSD as the register table given below.

| Field                            | CSD slice | Description                                                                                                   |
|----------------------------------|-----------|---------------------------------------------------------------------------------------------------------------|
| VENDOR_PROPRIETARY_HEALTH_REPORT | [301:270] | Reserved for vendor proprietary health report. (NONE)                                                         |
| DEVICE_LIFE_TIME_EST_TYPE_ A/B   | [268:269] | Current average P/E cycle of memory of Type A(SLC) / Type B(MLC) relative to its maximum estimated capability |
| PRE_EOL_INFO                     | [267]     | Consumed reserved blocks to notify before reaching the EOL (End of life) status                               |
| OPTIMAL_TRIM/WRITE_READ_SIZE     | [264:266] | Minimum optimal (for the device) Erase / Write / Read unit size for the different partitions                  |
| DEVICE_VERSION                   | [263:262] | Device version                                                                                                |
| FIRMWARE_VERSION                 | [261:254] | Device FW version                                                                                             |

**[Table 6] Using EXT\_CSD for health report (Read only)**

### 3.1.4 Sleep notification

Host may use to a power off notification when it intends to turn-off  $V_{CC}$  After moving the device to sleep state. Some features are added to clarify the spec for entering sleep mode when power off notification is enabled.

#### ■ Add the SLEEP\_NOTIFICATION on the interruptible Command List

| CMD  | Description                                                                        | Is interruptible? |
|------|------------------------------------------------------------------------------------|-------------------|
| CMD6 | SWITCH, Byte POWER_OFF_NOTIFICATION,<br>Value POWER_OFF_LONG or SLEEP_NOTIFICATION | Yes               |

#### ■ SLEEP\_NOTIFICATION\_TIME[216](Read Only)

Maximum timeout for the SWITCH command when notifying the device that it is about to move to sleep state by writing

SLEEP\_NOTIFICATION to POWER\_OFF\_NOTIFICATION[34]byte. (unit : 10us)

| Value       | Description                                                                 | Timeout value  |
|-------------|-----------------------------------------------------------------------------|----------------|
| 0x01 ~ 0x17 | Sleep Notification Timeout = $10\mu s \times 2_{SLEEP\_NOTIFICATION\_TIME}$ | 0x0E(163.84ms) |
| 0x18 ~ 0xFF | Reserved                                                                    |                |

#### ■ POWER\_OFF\_NOTIFICATION[34]

Add 0x04h for the SLEEP\_NOTIFICATION as a valid value

| Value | Field              | Description                                                                                           |
|-------|--------------------|-------------------------------------------------------------------------------------------------------|
| :     | :                  | :                                                                                                     |
| 0x03  | POWER_OFF_LONG     | Host is going to power off the device.<br>The device shall respond within POWER_OFF_LONG_TIME         |
| 0x04  | SLEEP_NOTIFICATION | Host is going to put device in sleep mode.<br>The device shall respond within SLEEP_NOTIFICATION_TIME |

### 3.1.5 Secure removal type

This feature is used for how information is removed from the physical memory during a purge operation.

#### ■ Secure Removal Type[16]

Among four options for secure removal type, eMMC supports 0x3, 0x1 and 0x0 (0x2 option is not supported) eMMC recommends using a vendor defined removal type(type 3). If host want to erase the device physically using removal type0.

Secure erase & Secure trim time is longer than using removal type0

| BIT      | Description of Secure Removal Type  | Description |                                                                                                                         | Supportability                            |
|----------|-------------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| BIT[5:4] | Configure Secure Removal Type (R/W) | 0x3         | Information removed using a vendor defined                                                                              | -                                         |
|          |                                     | 0x2         | Information removed by an overwriting the addressed locations with a character, its complement, then a random character | -                                         |
|          |                                     | 0x1         | Information removed by an overwriting the addressed locations with a character followed by an erase                     | -                                         |
|          |                                     | 0x0         | Information removed by an erase of the physical memory                                                                  | -                                         |
| BIT[3:0] | Supported Secure Removal Type (R)   | BIT[3]      | Information removed using a vendor defined                                                                              | Supported                                 |
|          |                                     | BIT[2]      | Information removed by an overwriting the addressed locations with a character, its complement, then a random character | Not supported                             |
|          |                                     | BIT[1]      | Information removed by an overwriting the addressed locations with a character followed by an erase                     | Supported (but, same operating to type 0) |
|          |                                     | BIT[0]      | Information removed by an erase of the physical memory                                                                  | Supported                                 |

## 3.2 eMMC5.1 New features

### 3.2.1 Command queuing

eMMC manages an internal task queue to which the host can queue data transfer tasks to efficient operate.

#### 3.2.1.1 CMD list for Command queuing

| Index        | Abbreviation          | Argument                                                                                                                                                                                                                    | Remark                                                                                                                                                                                    |
|--------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>CMD44</b> | Queued Task parameter | [31] Reliable Write Request<br>[30] Data Direction (Read=1, Write=0)<br>[29] Tag Request<br>[28:25] context ID<br>[24] Forced Programming<br>[23] Priority ( simple =0, high=1)<br>[20:16] Task ID(31~0)<br>[15:0] # of BLK | Encodes parameter which are necessary for queuing the task and executing the transfer                                                                                                     |
| <b>CMD45</b> | Queued Task Address   | [31:0] Block address for the transaction                                                                                                                                                                                    | The host instructs the device to queue a data transfer task                                                                                                                               |
| <b>CMD46</b> | Execute Read Task     | [20:16] Task ID of the requested task which is must marked as "ready for execution" in the Queue Status Register                                                                                                            | In order to execute a data read task (CMD46) or write task(CMD47) which is already queued                                                                                                 |
| <b>CMD47</b> | Execute Write Task    |                                                                                                                                                                                                                             |                                                                                                                                                                                           |
| <b>CMD48</b> | CMDQ_TASK_MGMT        | [31:21] reserved<br>[20:16]: TaskID<br>[15:4]: reserved<br>[3:0] TM op-code                                                                                                                                                 | Device shall discard a specific task or entire queue (all tasks in the queue)<br>[20:16] when TM op-code = 2h these bits represent TaskID.<br>When TM op-code=1h these bits are reserved. |

| Index        | Abbreviation | Argument                                                     | Remark                                                                                                                                            |
|--------------|--------------|--------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>CMD13</b> | SEND_STATUS  | [31:16] RCA<br>[15] <b>SQS</b><br>[14] Stuff bits<br>[0] HPI | In case SQS bit = 1: indicate that this is CMD13 of CMD Queue.<br>In response device shall send the QSR. In this case HPI bit muse be set to '0'. |



### 3.2.1.2 EXT\_CSD Register for Command queuing

#### ■ CMDQ\_SUPPORT[308](Read only)

This field indicates whether command queuing is supported by the device.

BIT[0]: 0: Command queuing is not supported

1: Command queuing is supported

| Bit      | Field        | Supportability  |
|----------|--------------|-----------------|
| Bit[7:1] | Reserved     | -               |
| Bit[0]   | CMDQ Support | Supported (0x1) |

#### ■ CMDQ\_DEPTH[307](Read only)

This field is used to calculate the depth of the queue supported by the device. The maximum depth allowed by the standard is 32.

The range of allowed Task IDs is 0 through N.

BIT[4:0]: N, a parameter used to calculate the Queue Depth of task queue in the device.

Queue Depth = N+1.

| Bit      | Field    | CMD queue depth value |
|----------|----------|-----------------------|
| Bit[7:5] | Reserved | -                     |
| Bit[4:0] | N        | N=31 (0x1F)           |

#### ■ CMDQ\_MODE\_EN[15](R/W)

This field is used by the host enable command queuing mechanism if supported by the device.

BIT[0]: 0: Command queuing is disabled. Host should clear the queue empty using CMD48 prior disabling the queue.

1: Command queuing is enabled

| Bit      | Field       | Supportability |
|----------|-------------|----------------|
| Bit[7:1] | Reserved    | -              |
| Bit[0]   | CMDQ enable | -              |

To maintain backward compatibility with hosts, which do not support command queuing, when the command queuing is disabled other functionality of the device is as if the device does not support command queuing.

---

### 3.2.1.3 New register for Command queuing

#### ■ QSR (Queue Status Register)

The 32bit QSR carries the state of tasks in the queue at a specific point in time.

The host has read access to this register through device response to SEND\_STATUS command(CMD13 with bit[15]="1"), R1's argument will be the QSR.

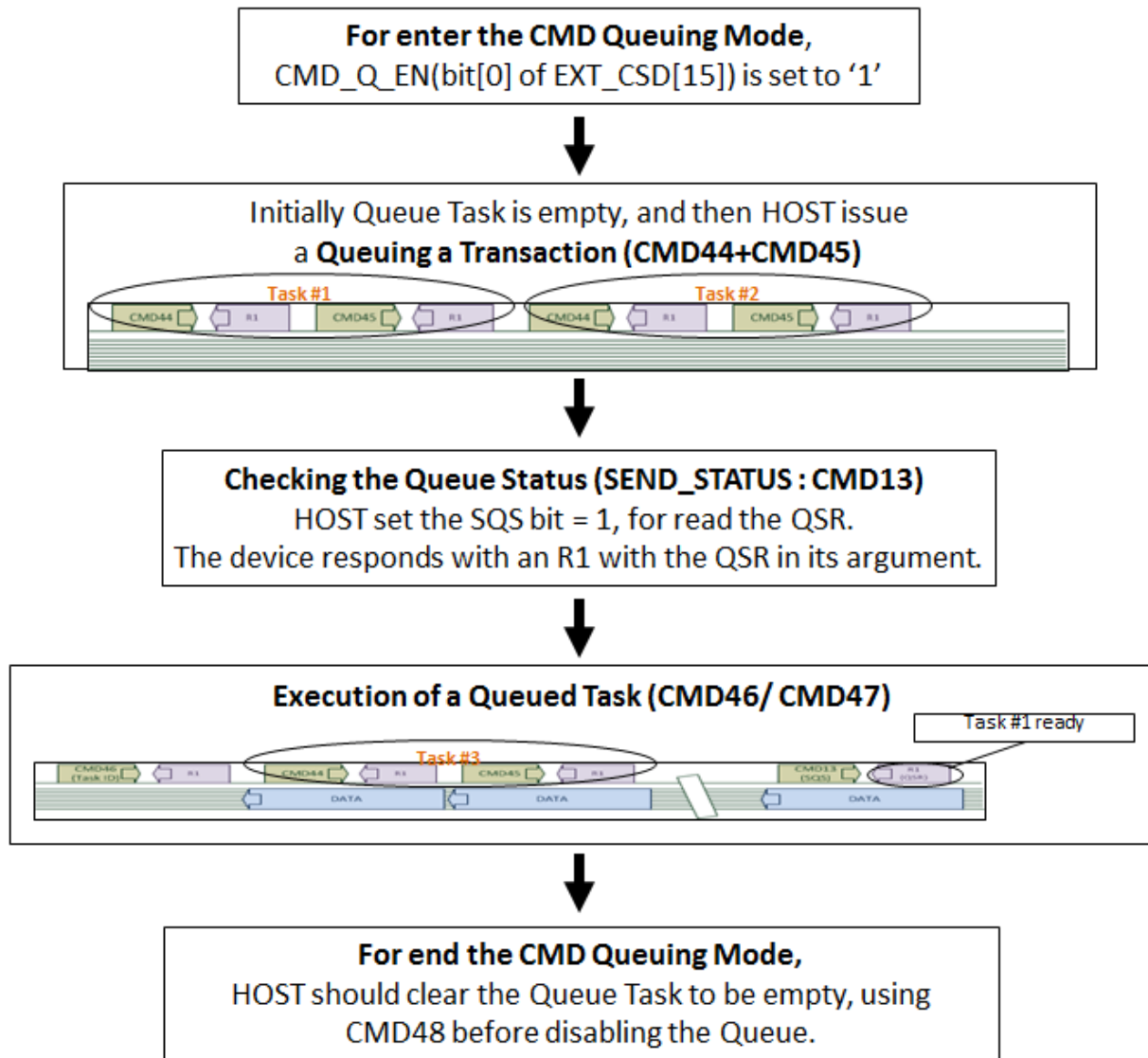
Every bit in the QSR represents the task who's ID corresponds to the bit index.

If bit QSR[i]='0', the queued task with a Task ID i is not ready for execution.

The task may be queued and pending, or the Task ID is unused.

If bit QSR[i]='1', the queued task with Task ID i is ready for execution.

### 3.2.1.4 Command queuing Flows



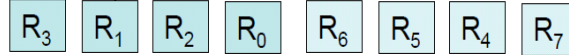
### 3.2.2 Cache Barrier

There are cases where the host is not interested in flushing the data right away, however it would like to keep an order between different cached data. The flushing can be delayed by the device to some later idle time. Barrier commands avoid the long delay by flush commands.

- Arrival sequence



- Flush sequence



#### 3.2.2.1 EXT\_CSD Register for Cache Barrier

##### ■ BARRIER\_SUPPORT[488](Read only)

This field indicates whether the device supports the barrier command.

BIT[7:0]: 0: Barrier command is not supported

1: Barrier command is supported

| Bit      | Field           | Supportability  |
|----------|-----------------|-----------------|
| Bit[7:0] | BARRIER_SUPPORT | Supported (0x1) |

##### ■ FLUSH\_CACHE[32](W/E\_P)

A barrier command is issued by setting BARRIER bit. All data cached before the barrier shall be flushed to the non-volatile memory before any request after the barrier command.

Data in the cache shall be flushed to the non-volatile storage by setting the FLUSH bit.

BIT[1]: 0: Reset value

1: Set barrier

BIT[0]: 0: Reset value

1: Triggers the flush

| Bit      | Field    | Supportability |
|----------|----------|----------------|
| Bit[7:2] | Reserved | -              |
| Bit[1]   | BARRIER  | -              |
| Bit[0]   | FLUSH    | -              |

#### ■ BARRIER\_CTRL[31](R/W)

This field is used by the host enable barrier command mechanism if supported by the device.

BIT[0]: 0: Barrier feature is OFF

1: Barrier feature is ON

| Bit      | Field      | Supportability |
|----------|------------|----------------|
| Bit[7:1] | Reserved   | -              |
| Bit[0]   | BARRIER_EN | -              |

#### 4.2.2.2 Cache barrier Flows

##### 1. Support Barrier command

- The device exposes its barrier support capability via the BARRIER\_SUPPORT (EXT\_CSD byte [486])

##### 2. Enable Barrier command

- The host shall set bit 0 of BARRIER\_EN (EXT\_CSD byte [31])

##### 3. Cache on

##### 4. Send data

##### 5. Set Barrier

- The host shall set both BARRIER bit and FLUSH bit of the FLUSH\_CACHE (EXT\_CSD byte [32])

### 3.2.3 Cache Flushing Report

For devices which flush cached data in an in-order manner, cache barrier commands are redundant and impose a needless overhead to the device and host.

#### 3.2.3.1 EXT\_CSD Register for Cache Flushing Report

##### ■ CACHE\_FLUSH\_POLICY[240](Read only)

BIT[0]: 0: Device flushing policy is not provided by the device.

1: Device is using a FIFO policy for cache flushing

| Bit      | Field    | Supportability   |
|----------|----------|------------------|
| Bit[7:1] | Reserved | -                |
| Bit[0]   | FIFO     | Supported (0x01) |

### 3.2.4 BKOP Control

This feature allows the host to indicate to the device if it is expected to periodically manually start background operations by writing to the BKOPS\_START field.

#### 3.2.4.1 EXT\_CSD Register for BKOP Control

##### ■ BKOP\_EN[163](R/W/E, R/W)

BIT[1](R/W/E): 0: Device shall not perform background operations while not servicing the host.

1: Device may perform background operations while not servicing the host.

BIT[0] (R/W): 0: Host does not support background operations handling and is not expected to write to BKOPS\_START field.

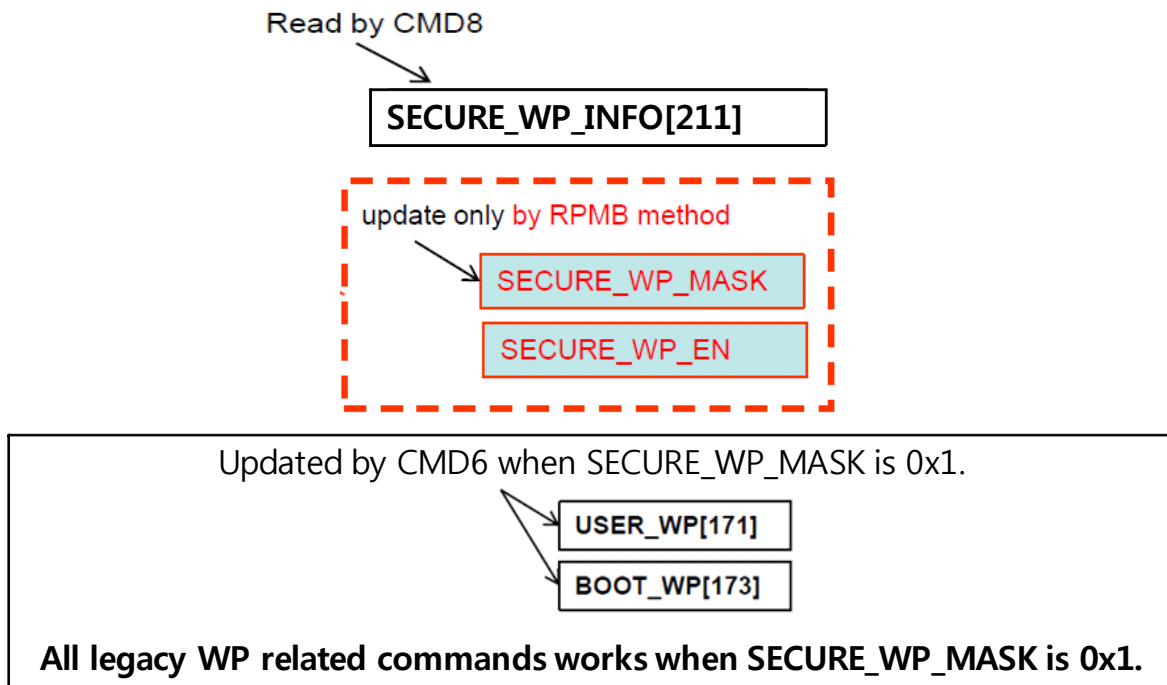
1: Host is indicating that it shall periodically write to BKOPS\_START field to manually start background operations.

| Bit      | Field     | Supportability |
|----------|-----------|----------------|
| Bit[7:2] | Reserved  | -              |
| Bit[1]   | AUTO_EN   | -              |
| Bit[0]   | MANUAL_EN | -              |

### 3.2.5 Secure Write Protection

Any application running on the host may issue write protection by updating fields of write protection related EXT\_CSD, like USER\_WP[171], BOOT\_WP[173], by issuing CMD6, CMD8, CMD28 and CMD29 (Legacy mode). However there are weak points in the legacy mode. To prevent un-authorized changes, host should enter the secure write protect mode

- In Secure WP Mode, WP related EXT\_CSDs (EXT\_CSD[171],[173]) can be updated only if SECURE\_WP\_MASK fields is 0x1.
- Secureness is provided by allowing only RPMB method to update the register for SECURE\_WP\_MASK.
- Automatic Write protection mode is added to prevent security hole by power-control security attack.



### 3.2.5.1 EXT\_CSD Register for Secure Write Protection

#### ■ SECURE\_WP\_INFO[211](Read Only)

The SECURE\_WP\_SUPPORT field indicates whether the device is supporting secure write protection mode. The SECURE\_WP\_EN\_STATUS is showing the value of SECURE\_WP\_EN defined in Authenticated Device Configuration Area.

BIT[1] 0: Legacy Write Protection mode  
 1: Secure Write Protection mode

BIT[0] 0: Secure Write Protection is NOT supported by this device  
 1: Secure Write Protection is supported by this device

| Bit      | Field               | Supportability   |
|----------|---------------------|------------------|
| Bit[7:2] | Reserved            | -                |
| Bit[1]   | SECURE_WP_EN_STATUS | -                |
| Bit[0]   | SECURE_WP_SUPPROT   | Supported (0x01) |

### 3.2.5.2 New register for Secure Write Protection

#### ■ Authenticated Device Configuration Area

- Hidden register instead of EXT\_CSD register for SECURE\_WP\_MODE\_CONFIG, ENABLE.
- Those two SECURE\_WP\_MODE\_CONFIG and SECURE\_WP\_MODE\_ENABLE registers are defined in Device Configuration area, and those register should be updated only by Authenticated Device Configuration write request. (RPMB)

| Name                               | Field                 | Size (Bytes) | Cell Type | Address |
|------------------------------------|-----------------------|--------------|-----------|---------|
| Reserved                           |                       | 253          | -         | [255:3] |
| Secure Write Protect Configuration | SECURE_WP_MODE_CONFIG | 1            | R/W/E_P   | [2]     |
| Secure Write Protect Enable        | SECURE_WP_MODE_ENABLE | 1            | R/W/E     | [1]     |
| Reserved                           |                       | 1            |           | [0]     |



### ■ Authenticated Device Configuration Area (1) : SECURE\_WP\_MODE\_ENABLE (R/W/E)

The byte is to enter/exit the secure write protection mode.

If host want a device to enter the secure Write Protection mode, host set the SECURE\_WP\_EN bit as '0x1' in this register using Authenticated Device Configuration Write request. This register can be read using Authenticated Device Configuration Read request. If there are already write protected groups or write protected boot partitions, those will be preserved when entering or exiting secure Write protected mode.

Bit [0] 0: Legacy Write Protection mode.

(TMP\_WRITE\_PROTECT[12] , PERM\_WRITE\_PROTECT[13] is updated by CMD27. USER\_WP[171], BOOT\_WP[173] and BOOT\_WP\_STATUS[174] are updated by CMD6.)

1: Secure Write Protection mode.

(The access to the write protection related EXT\_CSD and CSD fields depends on the value of SECURE\_WP\_MASK bit in SECURE\_WP\_MODE\_CONFIG field.)

The default value of this field is 0x0.

| Bit      | Field                 | Supportability |
|----------|-----------------------|----------------|
| Bit[7:1] | Reserved              | -              |
| Bit[0]   | SECURE_WP_MODE_ENABLE | -              |

## ■ Authenticated Device Configuration Area (2) : SECURE\_WP\_MODE\_CONFIG (R/W/E\_P)

In secure write protected mode, the updatability of USER\_WP[171], BOOT\_WP[173], TMP\_WRITE\_PROTECT[12] and PERM\_WRITE\_PROTECT[13] are controlled by this mask value.

Bit [0] 0: Disabling updating WP related EXT\_CSD and CSD fields. CMD27 (Program CSD) will generate generic error for setting TMP\_WRITE\_PROTECT[12], PERM\_WRITE\_PROTECT[13]. CMD6 for updating USER\_WP[171], BOOT\_WP[173] and BOOT\_WP\_STATUS[174] generates SWITCH\_ERROR. If a force erase command is issued, the command will fail (Device stays locked) and the LOCK\_UNLOCK\_FAILED error bit will be set in the status register. If CMD28 or CMD29 is issued, then generic error will be occurred. Power-on Write Protected boot partitions will keep protected mode after power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT\_WP in the EXT\_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.

1: Enabling updating WP related EXT\_CSD and CSD fields.  
(TMP\_WRITE\_PROTECT[12], PERM\_WRITE\_PROTECT[13], USER\_WP[171], BOOT\_WP[173] and BOOT\_WP\_STATUS[174] are accessed using CMD6, CMD8 and CMD27. If a force erase command is issued and accepted, then ALL THE DEVICE CONTENT WILL BE ERASED including the PWD and PWD\_LEN register content and the locked Device will get unlocked. If a force erase command is issued and power-on protected or a permanently-write-protected write protect groups exist on the device, the command will fail (Device stays locked) and the LOCK\_UNLOCK\_FAILED error bit will be set in the status register. An attempt to force erase on an unlocked Device will fail and LOCK\_UNLOCK\_FAILED error bit will be set in the status register. Write Protection is applied to the WPG indicated by CMD28 with the WP type indicated by the bit[2] and bit[0] of USER\_WP[171]. All temporary WP Groups and power-on Write Protected boot partitions become writable/erasable temporarily which means write protect type is not changed. All power-on and permanent WP Groups in user area will not become writable/erasable temporarily. Those temporarily writable/erasable area will become write protected when this bit is cleared to 0x0 by the host or when there is power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT\_WP CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.)

The default value of this field is 0x0.

| Bit      | Field                 | Supportability |
|----------|-----------------------|----------------|
| Bit[7:1] | Reserved              | -              |
| Bit[0]   | SECURE_WP_MODE_CONFIG | -              |

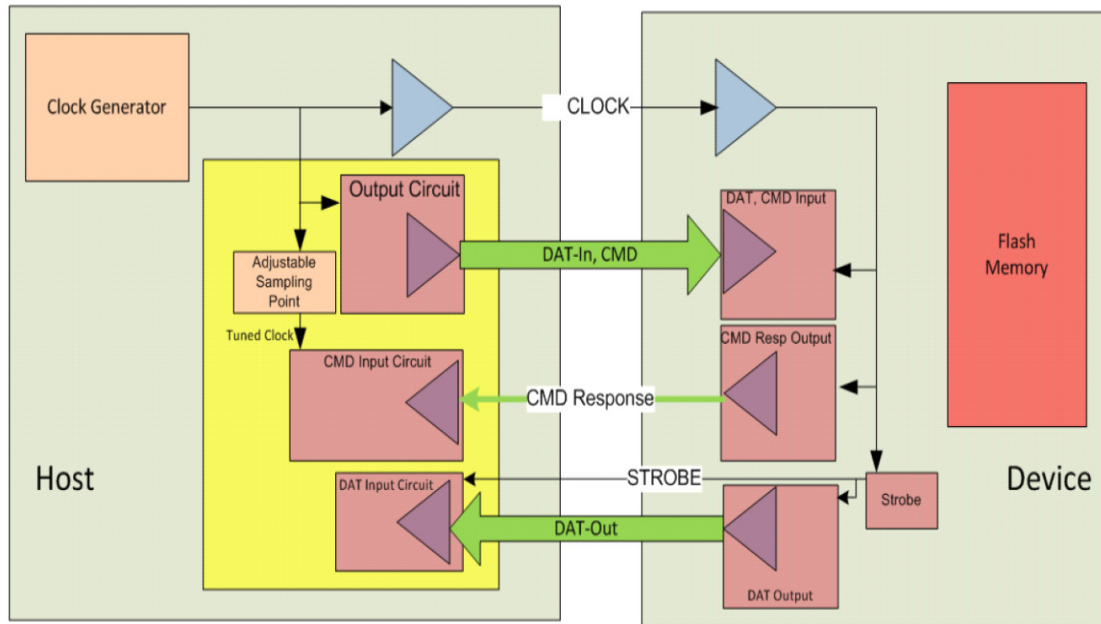
### 3.2.5.3 RPMB Types for accessing Authenticated Device Configuration Area

Secure WP Enable & Configuration registers are defined in Authenticated Device Configuration Area which only can be accessible by new RPMB operations.

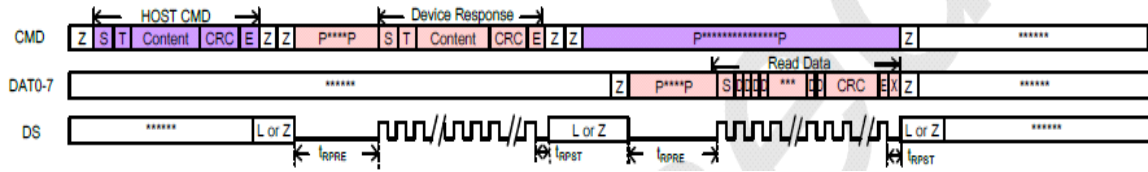
| Request Message Types  |                                                   |
|------------------------|---------------------------------------------------|
| 0x0001                 | Authentication key programming request            |
| 0x0002                 | Reading of the Write Counter value –request       |
| 0x0003                 | Authenticated data write request                  |
| 0x0004                 | Authenticated data read request                   |
| 0x0005                 | Result read request                               |
| 0x0006                 | Authenticated Device Configuration Write request  |
| 0x0007                 | Authenticated Device Configuration Read request   |
| Response Message Types |                                                   |
| 0x0100                 | Authentication key programming response           |
| 0x0200                 | Reading of the Write Counter value –response      |
| 0x0300                 | Authenticated data write response                 |
| 0x0400                 | Authenticated data read response                  |
| 0x0600                 | Authenticated Device Configuration Write response |
| 0x0700                 | Authenticated Device Configuration Read response  |

## 4.2.6 Enhanced strobe

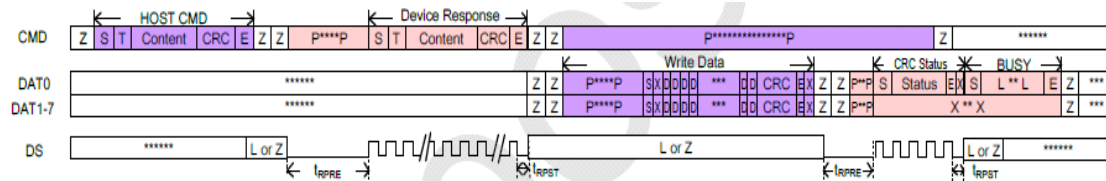
In Enhanced Strobe mode DATA OUT, CRC Response and CMD Response are all synched to STROBE clocks. The timing relation between CMD Response output signals and STROBE clocks is the same as defined for DATA Out to STROBE clocks.



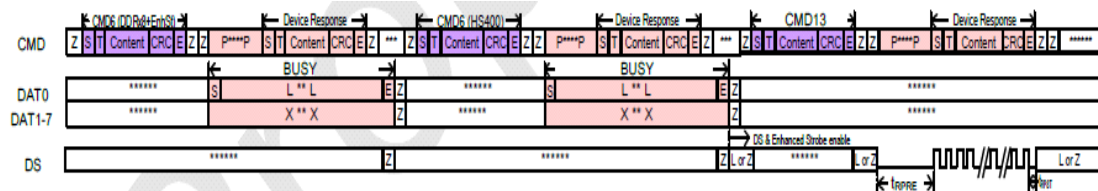
[Figure 7] HS400 Host and Device block diagram (when Enhanced Strobe is enabled)



[Figure 8] Enhanced Strobe signals for CMD Response and Data Out (Read operation)



[Figure 9] Enhanced Strobe signals for CMD Response and Data Out (Write operation)



[Figure 10] HS400 mode change with Enhanced Strobe

### 3.2.6.1 EXT\_CSD Register for Enhanced Strobe

#### ■ STROBE\_SUPPORT[184](Read only)

This register indicates whether a device supports Enhanced Strobe mode for operation modes that STROBE is used for HS400.

BIT[7:0]: 0: Indicates No support of Enhanced Strobe mode

1: Indicates the device supports Enhanced Strobe mode

| Bit      | Field          | Supportability   |
|----------|----------------|------------------|
| Bit[7:0] | STROBE_SUPPORT | Supported (0x01) |

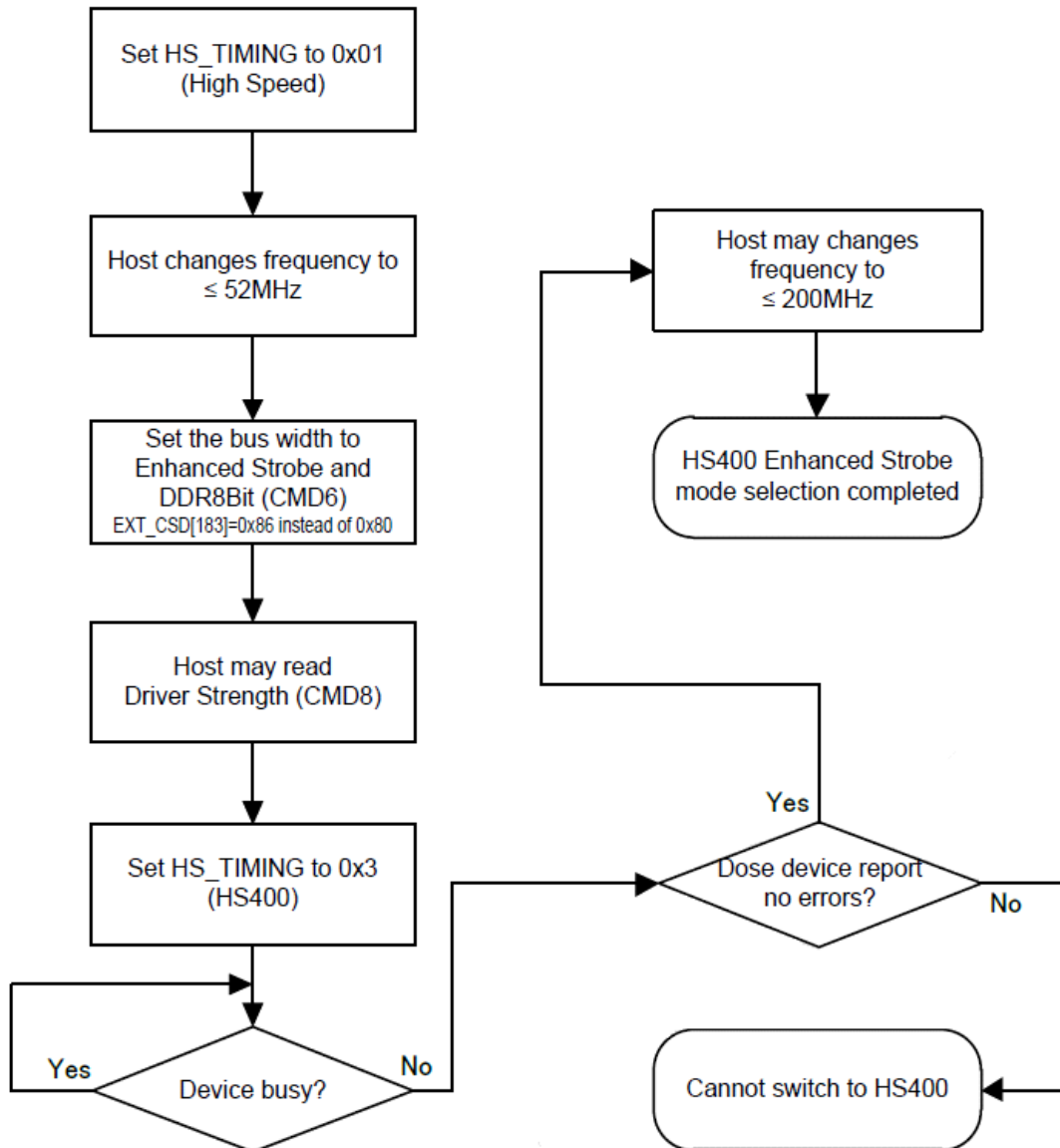
### 3.2.6.2 HS400 mode (Enhanced Strobe) selection

This selection flow describes how to initialize the eMMC device in HS400 mode while enabling Enhanced Strobe without the need for tuning procedure.

After the host initializes the device, host check whether the device supports the HS400 mode and Enhanced Strobe by reading the DEVICE\_TYPE and STROBE\_SUPPORT fields in the Extended CSD register.

After power-on or software reset (CMD0), the interface timing of the device is set as the default 'Backward Compatible Timing'.

In order to switch to HS400 mode with Enhanced Strobe, host should perform the following steps.



[Figure 11] HS400 Bus mode (Enhanced Strobe) selection flow diagram

### 3.2.7 RPMB throughput improvement

This feature is proposed for RPMB write data size to improve the RPMB throughput in eMMC5.1 spec. In the eMMC5.0 spec, REL\_WR\_SEC\_C[222] register shall be set to 1 (hence the granularity is always 512B.)

- For reliable write to RPMB partition, there is limitation that block count can not exceed the size of REL\_WR\_SEC\_C x 512B. In eMMC5.1, the supported RPMB write access size is 256B, 512B, and 8KB.

#### ■ WRITE\_REL\_PARAM (EXT\_CSD[166]): Read only

##### When EXT\_CSD[166][4] (R) = 0

- Device does not support large RPMB write transfer
- The behavior is same as eMMC v5.0 or earlier

##### When EXT\_CSD[166][4] (R) = 1

- Device supports large RPMB write transfer
- Host transfers small RPMB write with block count = 1 or 2 (256/512B)
- Host transfers large RPMB write with block count = 32 (8KB)
  - \* the start address should be 8KB aligned, and the transferred data (8KB) is all-new or all-old

| Bit    | Field          | Supportability   |
|--------|----------------|------------------|
| Bit[4] | EN_RPMB_REL_WR | Supported (0x01) |



### 3.3 Enhanced features from eMMC4.5 to eMMC5.1

Several eMMC features are changed from eMMC4.5 to eMMC5.1 enhance the eMMC performance.

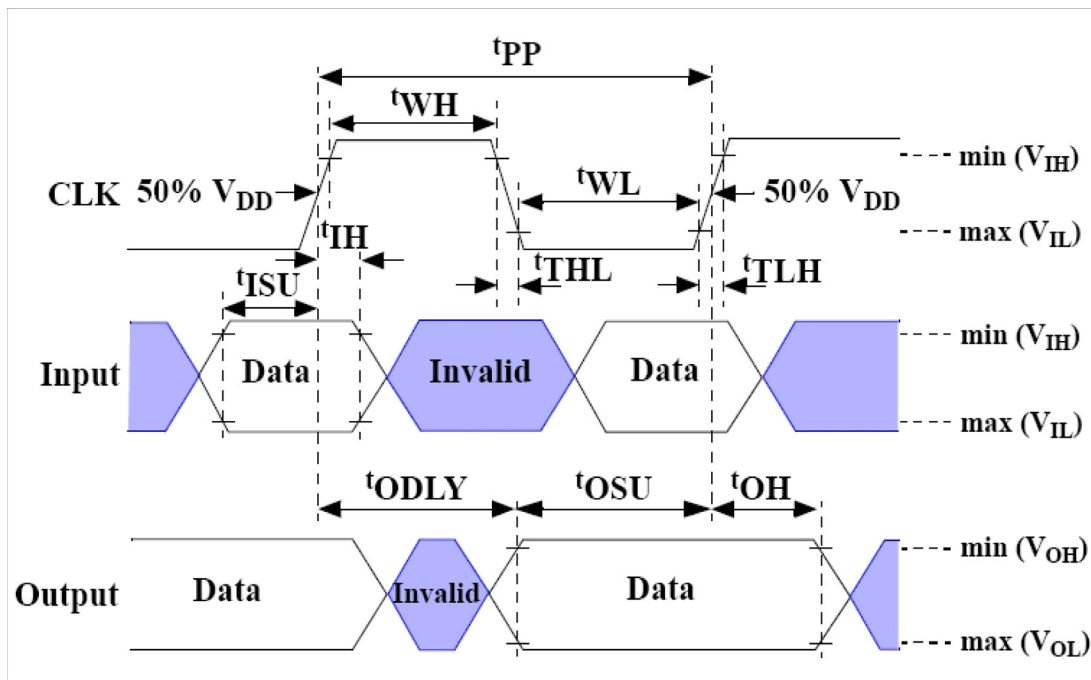
| Parameter             | eMMC4.5       | eMMC5.0          | eMMC5.1          | Description                                                                                     |
|-----------------------|---------------|------------------|------------------|-------------------------------------------------------------------------------------------------|
| HPI Features          | CMD12         | CMD13            | CMD13            | Following industry wise common configuration.                                                   |
| Max. Packed CMD count | 8ea           | 63ea             | 63ea             | Expended the packed CMD size for optimized device performance.                                  |
| Max. CMD Queue depth  | Not Support   | Not Support      | 32ea             | CMD queue is added in eMMC5.1                                                                   |
| Cache size            | <             | <                | <                | Cache size is increasing for optimized device performance with 4-way interleave implementation. |
| I/O Driver Strength   | Support Type0 | Support all type | Support all type | eMMC supports all of driver strength types for eMMC5.0                                          |

**[Table 7] Enhanced features from eMMC4.5 to eMMC5.1**

## 4. eMMC general parameters

### 4.1 Timing

#### 4.1.1 Bus timing



**Data must always be sampled on the rising edge of the clock.**

[Figure 12] Timing diagram: data input/output

| Parameter                                | Symbol     | Min | Max  | Unit | Remark                                 |
|------------------------------------------|------------|-----|------|------|----------------------------------------|
| Clock CLK                                |            |     |      |      |                                        |
| Clock frequency data transfer mode (PP)  | $f_{PP}$   | 0   | 52   | MHz  | $C_L \leq 30$ pF<br>Tolerance: +100KHz |
| Clock frequency identification mode (OD) | $f_{OD}$   | 0   | 400  | KHz  | Tolerance: +20KHz                      |
| Clock high time                          | $t_{WH}$   | 6.5 |      | ns   | $C_L \leq 30$ pF                       |
| Clock low time                           | $t_{WL}$   | 6.5 |      | ns   | $C_L \leq 30$ pF                       |
| Clock rise time                          | $t_{TLH}$  |     | 3    | ns   | $C_L \leq 30$ pF                       |
| Clock fall time                          | $t_{THL}$  |     | 3    | ns   | $C_L \leq 30$ pF                       |
| Inputs CMD, DAT (referenced to CLK)      |            |     |      |      |                                        |
| Input set-up time                        | $t_{ISU}$  | 3   |      | ns   | $C_L \leq 30$ pF                       |
| Input hold time                          | $t_{IH}$   | 3   |      | ns   | $C_L \leq 30$ pF                       |
| Outputs CMD, DAT (referenced to CLK)     |            |     |      |      |                                        |
| Output delay time during data transfer   | $t_{ODLY}$ |     | 13.7 | ns   | $C_L \leq 30$ pF                       |
| Output hold time                         | $t_{OH}$   | 2.5 |      | ns   | $C_L \leq 30$ pF                       |
| Signal rise time                         | $t_{RISE}$ |     | 3    | ns   | $C_L \leq 30$ pF                       |
| Signal fall time                         | $t_{FALL}$ |     | 3    | ns   | $C_L \leq 30$ pF                       |

**[Table 8] High-speed eMMC interface timing**

- CLK timing is measured at 50% of VDD.
- eMMC shall support the full frequency range from 0-26Mhz, or 0-52MHz
- CLK rising and falling times are measured by min ( $V_{IH}$ ) and max ( $V_{IL}$ ).
- Input CMD, DAT rising and falling times are measured by min ( $V_{IH}$ ) and max ( $V_{IL}$ ), and output CMD, DAT rising and falling times are measured by min ( $V_{OH}$ ) and max ( $V_{OL}$ ).

| Parameter                                   | Symbol    | Min  | Max | Unit | Remark                   |
|---------------------------------------------|-----------|------|-----|------|--------------------------|
| <b>Clock CLK</b>                            |           |      |     |      |                          |
| Clock frequency data transfer mode (PP)     | $f_{PP}$  | 0    | 26  | MHz  | $C_L \leq 30 \text{ pF}$ |
| Clock frequency identification mode (OD)    | $f_{OD}$  | 0    | 400 | KHz  |                          |
| Clock high time                             | $t_{WH}$  | 10   |     | ns   | $C_L \leq 30 \text{ pF}$ |
| Clock low time                              | $t_{WL}$  | 10   |     | ns   | $C_L \leq 30 \text{ pF}$ |
| Clock rise time                             | $t_{TLH}$ |      | 10  | ns   | $C_L \leq 30 \text{ pF}$ |
| Clock fall time                             | $t_{THL}$ |      | 10  | ns   | $C_L \leq 30 \text{ pF}$ |
| <b>Inputs CMD, DAT (referenced to CLK)</b>  |           |      |     |      |                          |
| Input set-up time                           | $t_{ISU}$ | 3    |     | ns   | $C_L \leq 30 \text{ pF}$ |
| Input hold time                             | $t_{IH}$  | 3    |     | ns   | $C_L \leq 30 \text{ pF}$ |
| <b>Outputs CMD, DAT (referenced to CLK)</b> |           |      |     |      |                          |
| Output set-up time                          | $t_{OSU}$ | 11.7 |     | ns   | $C_L \leq 30 \text{ pF}$ |
| Output hold time                            | $t_{OH}$  | 8.3  |     | ns   | $C_L \leq 30 \text{ pF}$ |

**[Table 9] Backward-compatible eMMC interface timing**

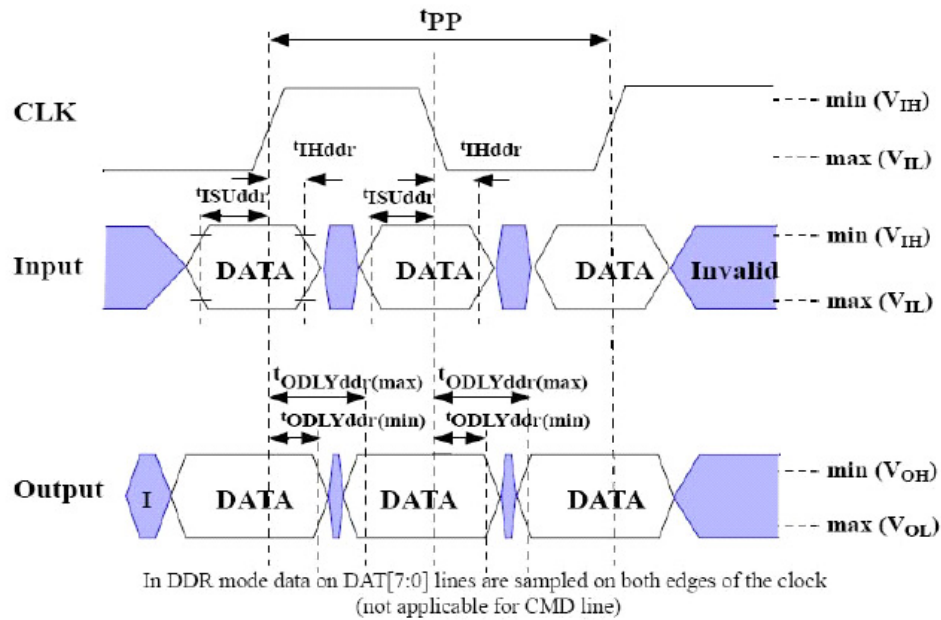
- eMMC must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed timing by the host sending the switch command (CMD6) with the argument for high speed interface select.
- CLK timing is measured at 50% of VDD.
- CLK rising and falling times are measured by min ( $V_{IH}$ ) and max ( $V_{IL}$ ).
- $t_{OSU}$  and  $t_{OH}$  are defined as values from clock rising edge. However, there may be cards or devices which utilize clock falling edge to output data in backward compatibility mode.

Therefore, it is recommended for hosts either to set  $t_{WL}$  value as long as possible within the range which should not go over  $t_{CK} \cdot t_{OH}(\text{min})$  in the system or to use slow clock frequency, so that host could have data set up margin for those devices.

In this case, each device which utilizes clock falling edge might show the correlation either between  $t_{WL}$  and  $t_{OSU}$  or between  $t_{CK}$  and  $t_{OH}$  for the device.

#### 4.1.2 Bus timing for DAT Signals During 2x Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK.



[Figure 13] Timing diagram: data input/output in dual data rate mode

| Parameter                                       | Symbol        | Min. | Max. | Unit | Remark                       |
|-------------------------------------------------|---------------|------|------|------|------------------------------|
| <b>Input CLK<sup>(1)</sup></b>                  |               |      |      |      |                              |
| Clock duty cycle                                |               | 45   | 55   | %    | Includes jitter, phase noise |
| Clock rise time                                 | $t_{TLH}$     |      | 3    | ns   | $CL \leq 30$ pF              |
| Clock fall time                                 | $t_{THL}$     |      | 3    | ns   | $CL \leq 30$ pF              |
| <b>Input CMD (referenced to CLK-SDR mode)</b>   |               |      |      |      |                              |
| Input set-up time                               | $t_{ISUddr}$  | 3    |      | ns   | $CL \leq 20$ pF              |
| Input hold time                                 | $t_{IHDDR}$   | 3    |      | ns   | $CL \leq 20$ pF              |
| <b>Output CMD (referenced to CLK-SDR mode)</b>  |               |      |      |      |                              |
| Output delay time during data transfer          | $t_{ODLY}$    |      | 13.7 | ns   | $CL \leq 20$ pF              |
| Output hold time                                | $t_{OH}$      | 2.5  |      | ns   | $CL \leq 20$ pF              |
| Signal rise time                                | $t_{RISE}$    |      | 3    | ns   | $CL \leq 20$ pF              |
| Signal fall time                                | $t_{FALL}$    |      | 3    | ns   | $CL \leq 20$ pF              |
| <b>Input DAT (referenced to CLK-DDR mode)</b>   |               |      |      |      |                              |
| Input set-up time                               | $t_{ISUddr}$  | 2.5  |      | ns   | $CL \leq 20$ pF              |
| Input hold time                                 | $t_{IHddr}$   | 2.5  |      | ns   | $CL \leq 20$ pF              |
| <b>Outputs DAT (referenced to CLK-DDR mode)</b> |               |      |      |      |                              |
| Output delay time during data transfer          | $t_{ODLYddr}$ | 1.5  | 7    | ns   | $CL \leq 20$ pF              |
| Signal rise time(DAT0-7) <sup>(2)</sup>         | $t_{RISE}$    |      | 2    | ns   | $CL \leq 20$ pF              |
| Signal fall time (DAT0-7)                       | $t_{FALL}$    |      | 2    | ns   | $CL \leq 20$ pF              |

**[Table 10] Dual data rate interface timings**

- **NOTE 1.** CLK timing is measured at 50% of VDD.
- **NOTE 2.** Inputs DAT rising and falling times are measured by min ( $V_{IH}$ ) and max ( $V_{IL}$ ), and outputs CMD, DAT rising and falling times are measured by min ( $V_{OH}$ ) and max ( $V_{OL}$ )

## 4.2 Power mode

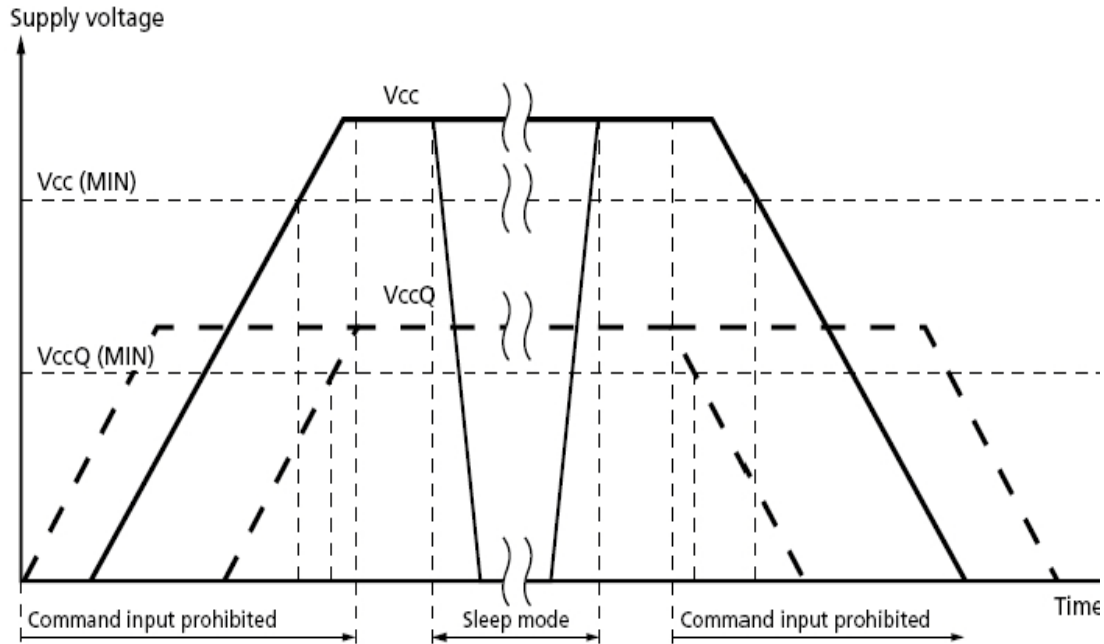
### 4.2.1 eMMC power-up guidelines

eMMC power-up must adhere to the following guidelines:

- When power-up is initiated, either  $V_{cc}$  or  $V_{ccq}$  can be ramped up first, or both can be ramped up simultaneously.
- After power up, eMMC enters the pre-idle state. The power up time of each supply voltage should be less than the specified tPRU (tPRUH, tPRUL or tPRUV) for the appropriate voltage range.
- If eMMC does not support boot mode or its BOOT\_PARTITION\_ENABLE bit is cleared, eMMC moves immediately to the idle state. While in the idle state, eMMC ignores all bus transactions until receiving CMD1. eMMC begins boot operation with the argument of 0xFFFFFFFF. If boot acknowledge is finished, eMMC shall send acknowledge pattern "010" to the host within the specified time. After boot operation is terminated, eMMC enters the idle state and shall be ready for CMD1 operation. If eMMC receives CMD1 in the pre-boot state, it begins to respond to the command and moves to the card identification mode.
- When eMMC is initiated by alternative boot command(CMD0 with arg=0xFFFFFFFF), all the data will be read from the boot partition and then eMMC automatically goes to idle state, but hosts are still required to issue CMD0 with arg=0x0000000000 in order to complete a boot mode properly and move to the idle state. While in the idle state, eMMC ignores all bus transactions until it receives CMD1.
- CMD1 is a special synchronization command which is used to negotiate the operating voltage range and poll the device until it is out of its power-up sequence. In addition to the operating voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready, and the host must wait until this bit is cleared. The device must complete its initialization within 1 second of the first CMD1 issued with a valid OCR range.
- If the eMMC device was successfully partitioned during the previous power up session (bit 0 of EXT\_CSD byte [155] PARTITION\_SETTING\_COMPLETE successfully set) then the initialization delay is (instead of 1s) calculated from INI\_TIMEOUT\_PA (EXT\_CSD byte [241]). This timeout applies only for the very first initialization after successful partitioning. For all the consecutive initialization 1sec time out will be applied.
- The bus master moves the device out of the idle state. Because the power-up time and the supply ramp-up time depend on the application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.
- After power-up, the host starts the clock and sends the initializing sequence on the CMD line. The sequence length is the longest of: 1ms, 74 clocks, the supply ramp-up time, or the boot operation period. An additional 10 clocks (beyond the 64 clocks of the power-up sequence) are provided to eliminate power-up synchronization problems.
- Every bus master must implement CMD1.

#### 4.2.2 eMMC Power Cycling

The master can execute any sequence of  $V_{CC}$  and  $V_{CCQ}$  power-up/power-down. However, the master must not issue any commands until  $V_{CC}$  and  $V_{CCQ}$  are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down  $V_{CC}$  to reduce power consumption. It is necessary for the slave to be ramped up to  $V_{CC}$  before the host issues CMD5 (SLEEP\_AWAKE) to wake the slave unit.



[Figure 14] eMMC power cycle

If  $V_{CC}$  or  $V_{CCQ}$  is below 0.5 V for longer than 1 ms, the slave shall always return to the pre-idle state, and perform the appropriate boot behavior. The slave will behave as in a standard power up condition once the voltages have returned to their functional ranges.

An exception to this behavior is if the device is in sleep state, in which the voltage on  $V_{CC}$  is not monitored.



#### 4.2.3 Leakage

| Parameter                                                                                                 | Symbol | Min  | Max.          | Unit    | Remark |
|-----------------------------------------------------------------------------------------------------------|--------|------|---------------|---------|--------|
|                                                                                                           | BGA    | -0.5 | $V_{CCQ}+0.5$ | V       |        |
| <b>All inputs</b>                                                                                         |        |      |               |         |        |
| Input leakage current<br>(before initialization sequence and/or the internal pull up resistors connected) |        | -100 | 100           | $\mu A$ |        |
| <b>All outputs</b>                                                                                        |        |      |               |         |        |
| Output leakage current (before initialization sequence)                                                   |        | -100 | 100           | $\mu A$ |        |
| Output leakage current (after initialization sequence)                                                    |        | -2   | 2             | $\mu A$ |        |

[Table 11] General operation conditions

#### 4.2.4 Power Supply

eMMC supports one or more combinations of  $V_{CC}$  and  $V_{CCQ}$  as shown in Table 12.

The available voltage configuration is shown in Table 13.

| Parameter                | Symbol     | Min | Max. | Unit | Remark |
|--------------------------|------------|-----|------|------|--------|
| Supply voltage (NAND)    | $V_{CC}$   | 2.7 | 3.6  | V    |        |
| Supply voltage (I/O)     | $V_{CCQ}$  | 1.7 | 1.95 | V    |        |
| Supply power-up for 3.3V | $t_{PRUH}$ |     | 35   | ms   |        |
| Supply power-up for 1.8V | $t_{PRUL}$ |     | 25   | ms   |        |

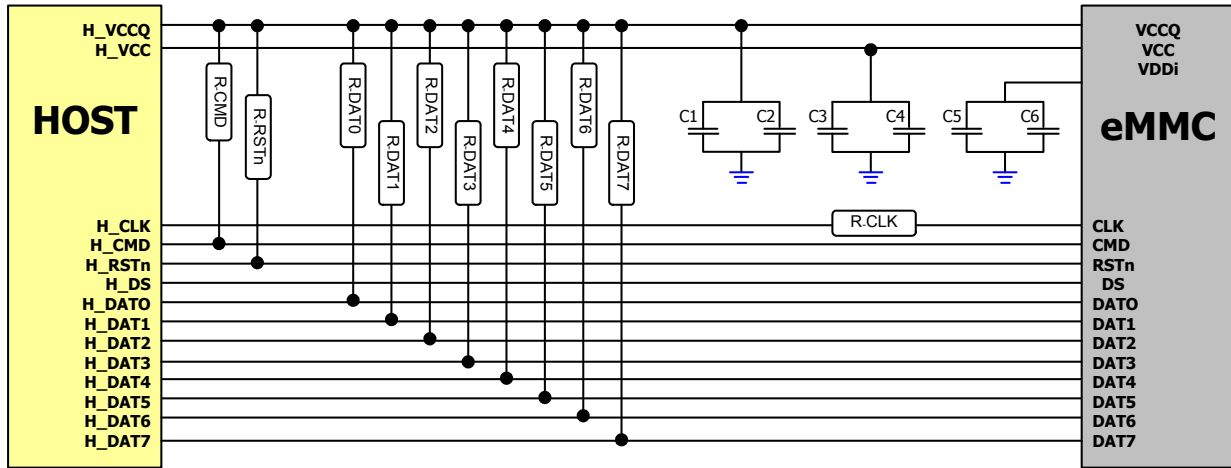
[Table 12] eMMC power supply voltage

|          |            | $V_{CCQ}$    |
|----------|------------|--------------|
|          |            | 1.7V ~ 1.95V |
| $V_{CC}$ | 2.7V–3.6V  | Valid        |
|          | 1.7V–1.95V | Not Valid    |

[Table 13] eMMC voltage combinations

- **NOTE 1.**  $V_{CCQ}$ (I/O) 3.3 volt range is not supported in either HS200 or HS400 devices.

### 4.3 Connection Guide



[Figure 16] Connection guide drawing

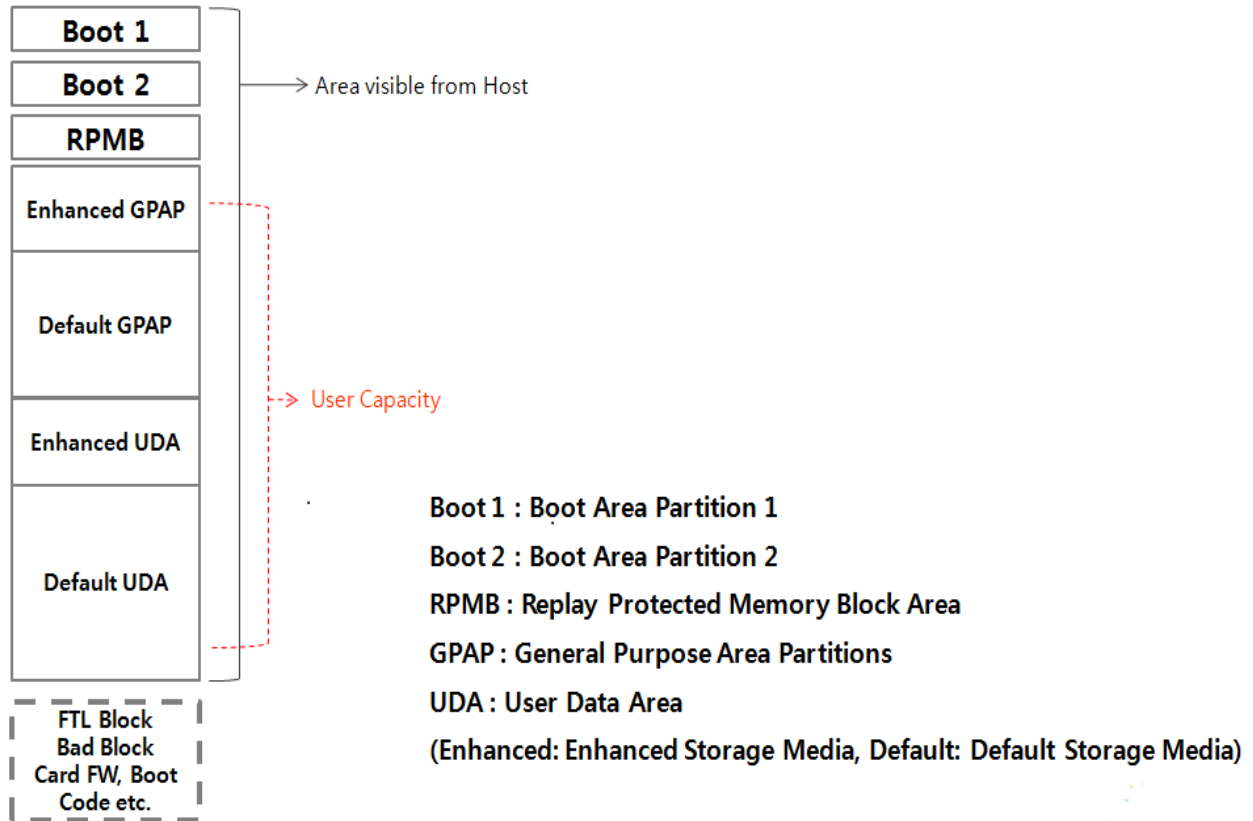
| Parameter                             | Symbol  | Min      | Max | Recommend | Unit | Remark                                                                                                                                                                                     |
|---------------------------------------|---------|----------|-----|-----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pull-up resistance for CMD            | R_CMD   | 4.7      | 100 | 10        | kohm | Pull-up resistance should be put on CMD line to prevent bus floating.                                                                                                                      |
| Pull-up resistance for DAT0~7         | R_DAT   | 10       | 100 | 50        | kohm | Pull-up resistance should be put on DAT line to prevent bus floating.                                                                                                                      |
| Data strobe(DS)                       | R_DS    | NC       | NC  | NC        | -    | It is not necessary to put pull-up/pull-down resistance on DS line since DS is internally pulled down. Direct connection to host is required and please float this pin if it is not used   |
| Pull-up resistance for RSTn           | R_RSTn  | 10       | 100 | 50        | kohm | It is not necessary to put pull-up resistance on RSTn line if host does not use H/W reset. (Extended CSD register [162] = 0b)                                                              |
| Serial resistance on CLK              | R_CLK   | 0        | 30  | 27        | ohm  | To reduce overshooting/undershooting<br>Note: If the host uses HS200, we recommend to remove this resistor for better CLK signal                                                           |
| V <sub>ccq</sub> capacitor value      | C1 & C2 | 2±0.22   | 4.7 | 2±0.22    | uF   | Coupling cap should be connected with V <sub>ccq</sub> closely.                                                                                                                            |
| V <sub>cc</sub> capacitor value(≤8GB) | C3 & C4 | 4.72±10% | 10  | 4.72±10%  | uF   | Coupling cap should be connected with V <sub>cc</sub> closely.<br>V <sub>cc</sub> /V <sub>ccq</sub> cap. value would be up to Host requirement and the application system characteristics. |
| V <sub>cc</sub> capacitor value(>8GB) |         |          |     |           |      |                                                                                                                                                                                            |
| VDDi capacitor value                  | C5 & C6 | 0        | 2.2 | 0.1       | uF   | Coupling cap should be connected with VDDi and Vssq as closely possible. (Internal Cap : 1uF)                                                                                              |

[Table 14] Connection guide specification

## 5. eMMC basic operations

### 5.1 Partitioning

#### 5.1.1 User density



[Figure 17] Partition diagram

#### ■ Boot and RPMB partition size

| Density | Boot 1,2 partition size | RPMB partition size |
|---------|-------------------------|---------------------|
| 32GB    | 4096KB (4MB)            | 16384KB (16MB)      |

#### ■ User density size

| Capacity    | SEC_COUNT                 | Capacity                          | Percentile |
|-------------|---------------------------|-----------------------------------|------------|
| <b>32GB</b> | 61,071,360<br>(0x3A3E000) | 31,268,536,320 Bytes<br>(29.12GB) | 91.00%     |

- 1sector=512 bytes.
- The total usable capacity of the eMMC may be less than total physical capacity because a small portion of the capacity is used for NAND flash management and maintenance purpose.

#### ■ Maximum enhanced partition size

Enhanced user data area can be configured to store read-centric data such as sensitive data or for other host usage models.

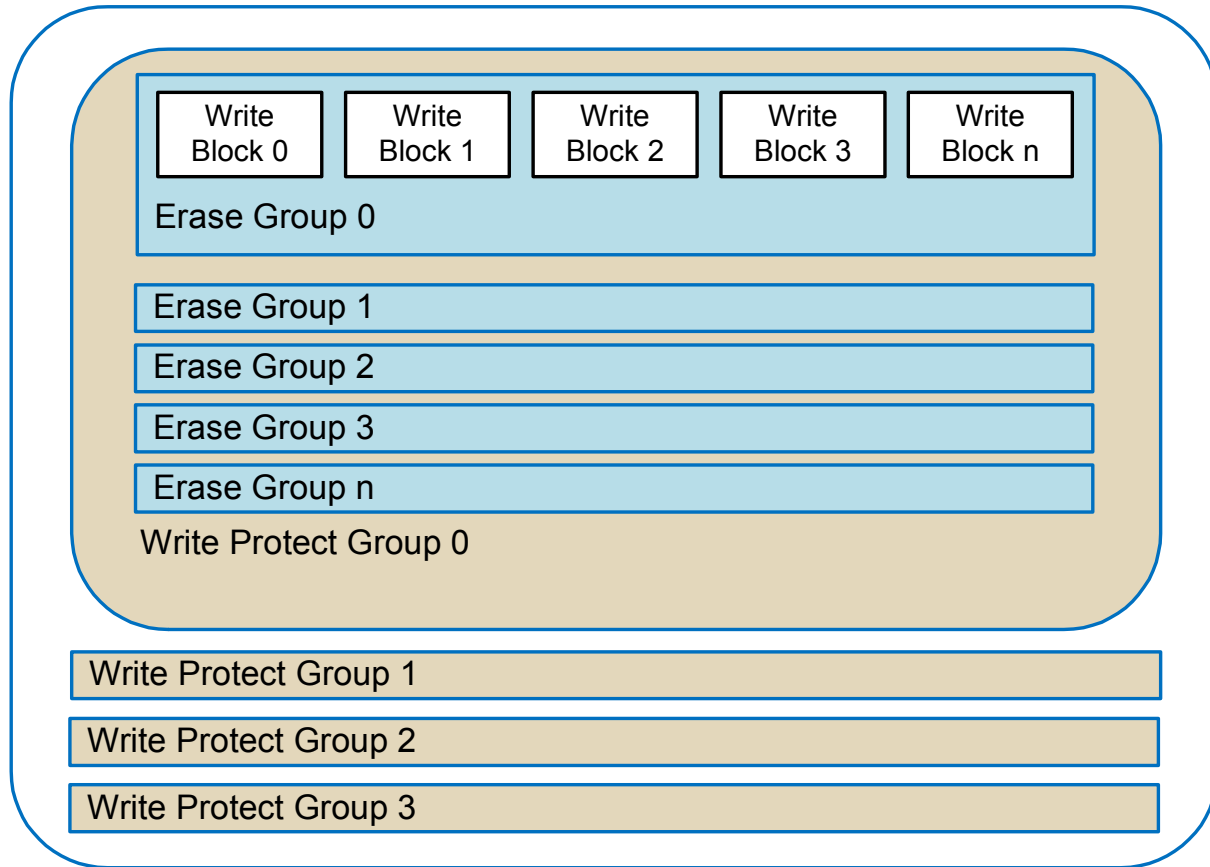
SK hynix eMMC supports Enhanced User Data Area as SLC Mode. When customer adopts some portion as enhanced user data area in User Data Area, that area occupies double the size of the original set-up size.

| Capacity    | Max ENH_SIZE_MULTI | HC_ERASE_GRP_SIZE | HC_WP_GRP_SIZE |
|-------------|--------------------|-------------------|----------------|
| <b>32GB</b> | 0x000747           | 1h                | 08h            |

- Max Enhanced Partition Size is defined as **MAX\_ENH\_SIZE\_MULT x HC\_WP\_GRP\_SIZE x HC\_ERASE\_GRP\_SIZE x 512KByte**.

| Capacity    | Capacity (KB) |
|-------------|---------------|
| <b>32GB</b> | 15,261,696    |

### 5.1.2 Erase / Write protect group size

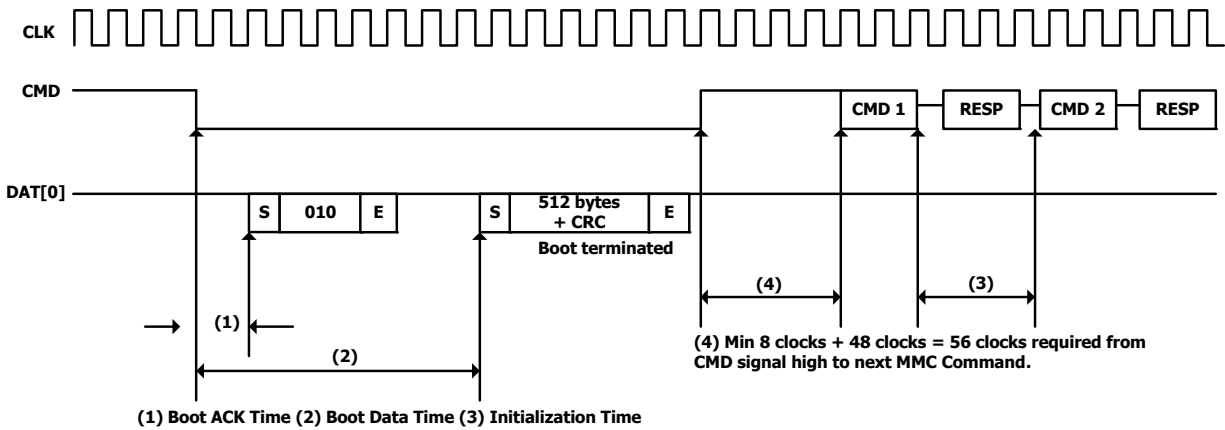


| Density | Erase group size  |                   | Write protect group size |
|---------|-------------------|-------------------|--------------------------|
|         | ERASE_GROUP_DEF=0 | ERASE_GROUP_DEF=1 |                          |
| 32GB    | 512KB             | 512KB             | 4MB                      |

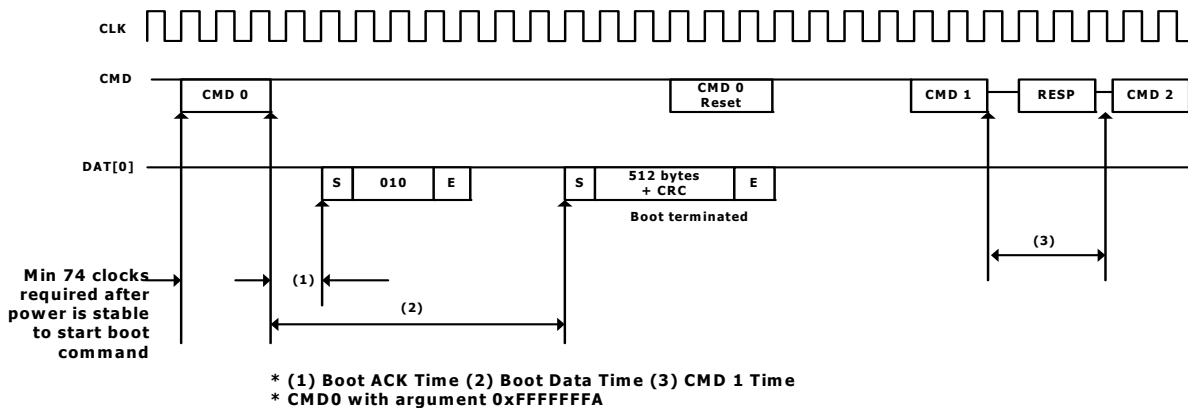
[Table 15] Erase/Write protect Group size

## 5.2 Boot operation

eMMC supports boot mode and alternative boot mode. eMMC also, supports high speed timing and dual data rate during boot.



[Figure 18] eMMC state diagram (Boot mode)



[Figure 19] eMMC state diagram (Alternative boot mode)

| Timing Factor           | Value   |
|-------------------------|---------|
| (1) Boot ACK Time       | < 50 ms |
| (2) Boot Data Time      | < 1 sec |
| (3) Initialization Time | < 1 sec |

- Initialization time includes partition setting, Please refer to INI\_TIMEOUT\_AP in 7.4 Extended CSD Register. Initialization time is completed within 1sec from issuing CMD1 until receiving response.
- The device has to send the acknowledge pattern "010" to the master within 50ms after the CMD0 with the argument of 0xFFFFFFFF is received.

## 6. Time out

| Latency Item                                         | Value                                | Remark |
|------------------------------------------------------|--------------------------------------|--------|
| <b>Write Time out<br/>(CMD To 512KB Write Done)</b>  | Max 1.2s<br>Median 30ms<br>99th 50ms |        |
| <b>Write Time out<br/>(Data To Data)</b>             | Max 500ms                            |        |
| <b>Read Time Out<br/>(CMD To the first data out)</b> | Max 50ms                             |        |
| <b>Initialization Time</b>                           | Max 1s                               |        |
| <b>Initialization Time<br/>(After Partitioning)</b>  | Max 1s                               |        |
| <b>Initialization after PON<br/>(Short/long)</b>     | Max 180ms                            |        |
| <b>Pre-Boot to ACK</b>                               | Max 50ms                             |        |
| <b>Pre-Boot to Boot Data</b>                         | Max 60ms                             |        |
| <b>Partition Switch</b>                              | Max 10ms                             |        |
| <b>CMD6 Switch</b>                                   | Max 100ms                            |        |
| <b>CMD8 time out</b>                                 | Max 5ms                              |        |
| <b>Erase<br/>(Erase Group)</b>                       | Max 600ms                            |        |
| <b>Trim<br/>(512B~512KB)</b>                         | Max 600ms                            |        |
| <b>Discard<br/>(512B~512KB)</b>                      | Max 600ms                            |        |

[Table 16] Time out value

| Latency Item                                    | Value            |           | Remark                                                                                                                                                        |
|-------------------------------------------------|------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Secure Trim1<br>Type 0, 1<br>(512B~512KB)       | Max 600s         |           | Type 0 : information removed by an erase of the physical memory<br>Type 1 : Same operation to type 0<br>Type 2 : Not support<br>Type 3 : information unmapped |
| Secure Trim1<br>Type 3<br>(512B~512KB)          | Max 600ms        |           |                                                                                                                                                               |
| Secure Erase<br>Type 0,1<br>(Write Block 512KB) | Max 600s         |           |                                                                                                                                                               |
| Secure Erase<br>Type 3<br>(Write Block 512KB)   | Max 600ms        |           |                                                                                                                                                               |
| Sanitize<br>(UDA Area)                          | 32GB             | Max 80min |                                                                                                                                                               |
| Force Erase<br>(UDA Area)                       | Max 3min         |           |                                                                                                                                                               |
| HPI                                             | Max 50ms         |           |                                                                                                                                                               |
| PON Busy Time<br>(Short/Long)                   | Max 50ms / 600ms |           | PON long includes GC<br>PON short not include GC                                                                                                              |

**[Table 17] Time out value (Continue)**

- Be advised timeout values specified in table above are for testing purpose under SK hynix test pattern only and actual timeout situations may vary



## 7. Device registers

There are six different registers within the device interface:

- Operation conditions register (OCR)
- Card identification register (CID)
- Card specific data register (CSD)
- Relative card address register (RCA)
- DSR (Driver Stage Register)
- Extended card specific data register (EXT\_CSD).

These registers are used for the serial data communication and can be accessed only using the corresponding commands.

eMMC has a status register to provide information about the current device state and completion codes for the last host command.

### 7.1 Operation conditions register (OCR)

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of eMMC and the access mode indication. In addition, this register includes a status information bit. This status bit is set if eMMC power up procedure has been finished.

| OCR bit | Description                                      | SK hynix eMMC     |
|---------|--------------------------------------------------|-------------------|
| [6:0]   | Reserved                                         | 000 0000b         |
| [7]     | 1.70 - 1.95V                                     | 1b                |
| [14:8]  | 2.0 - 2.6                                        | 000 0000b         |
| [23:15] | 2.7 - 3.6 (High $V_{CCQ}$ range)                 | 1111 1111 1b      |
| [28:24] | Reserved                                         | 000 000b          |
| [30:29] | Access mode                                      | 10b (sector mode) |
| [31]    | (card power up status bit (busy)) <sup>(1)</sup> |                   |

**[Table 18] OCR register definition**

- **NOTE 1.** This bit is set to LOW if the card has not finished the power up routine

## 7.2 Card identification (CID) register

The card identification (CID) register is 128 bits wide. It contains eMMC identification information used during eMMC identification phase (eMMC protocol). Every individual eMMC has a unique identification number. The structure of the CID register is defined in the following sections.

| Name                  | Field | Width | CID slice | CID value            | Remark    |
|-----------------------|-------|-------|-----------|----------------------|-----------|
| Manufacturer ID       | MID   | 8     | [127:120] | 0X90                 |           |
| Reserved              |       | 6     | [119:114] |                      |           |
| Card/BGA              | CBX   | 2     | [113:112] | 0X1                  | BGA       |
| OEM/application ID    | OID   | 8     | [111:104] | 0X4A                 |           |
| Product name          | PNM   | 48    | [103:56]  | 32GB: 0X68423861503E |           |
| Product revision      | PRV   | 8     | [55:48]   | -                    | Not fixed |
| Product serial number | PSN   | 32    | [47:16]   | -                    | 1)        |
| Manufacturing date    | MDT   | 8     | [15:8]    | -                    |           |
| CRC7 checksum         | CRC   | 7     | [7:1]     | -                    |           |
| Not used, always '1'  |       | 1     | [0:0]     | 0X1                  |           |

- 1) If PSN is to be used as a Unique ID, a composition PSN and MDT should be used.  
Whole CID can also be used to generate a unique ID

**[Table 19] Card identification (CID) fields**

### 7.3 Card specific data register (CSD)

The card specific data (CSD) register provides information on how to access eMMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed and so on. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the CSD Registry entries in the Table 20 below is coded as follows:

- R: Read only.
- W: One time programmable and not readable.
- R/W: One time programmable and readable.
- W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- R/W/C\_P: Writable after value cleared by power failure and HW/reset assertion (the value not cleared by CMD0 reset) and readable.
- R/W/E\_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- W/E\_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

| Name                                             | Field              | Width | Cell type | CSD slice | CSD value | Remark |
|--------------------------------------------------|--------------------|-------|-----------|-----------|-----------|--------|
| CSD structure                                    | CSD_STRUCTURE      | 2     | R         | [127:126] | 0X03      |        |
| System specification version                     | SPEC_VERS          | 4     | R         | [125:122] | 0X04      |        |
| Reserved                                         |                    | 2     | R         | [121:120] | -         |        |
| Data read access-time 1                          | TAAC               | 8     | R         | [119:112] | 0X27      |        |
| Data read access-time 2 in CLK cycles (NSAC*100) | NSAC               | 8     | R         | [111:104] | 0X00      |        |
| Max. bus clock frequency                         | TRAN_SPEED         | 8     | R         | [103:96]  | 0X32      |        |
| Card command classes                             | CCC                | 12    | R         | [95:84]   | 0X8F5     |        |
| Max. read data block length                      | READ_BL_LEN        | 4     | R         | [83:80]   | 0X09      |        |
| Partial blocks for read allowed                  | READ_BL_PARTIAL    | 1     | R         | [79:79]   | 0X00      |        |
| Write block misalignment                         | WRITE_BLK_MISALIGN | 1     | R         | [78:78]   | 0X00      |        |
| Read block misalignment                          | READ_BLK_MISALIGN  | 1     | R         | [77:77]   | 0X00      |        |
| DSR implemented                                  | DSR_IMP            | 1     | R         | [76:76]   | 0X00      |        |
| Reserved                                         |                    | 2     | R         | [75:74]   |           |        |
| Device size                                      | C_SIZE             | 12    | R         | [73:62]   | 0XFFF     |        |
| Max. read current @ VDD min                      | VDD_R_CURR_MIN     | 3     | R         | [61:59]   | 0X07      |        |
| Max. read current @ VDD max                      | VDD_R_CURR_MAX     | 3     | R         | [58:56]   | 0X07      |        |
| Max. write current @ VDD min                     | VDD_W_CURR_MIN     | 3     | R         | [55:53]   | 0X07      |        |
| Max. write current @ VDD max                     | VDD_W_CURR_MAX     | 3     | R         | [52:50]   | 0X07      |        |
| Device size multiplier                           | C_SIZE_MULT        | 3     | R         | [49:47]   | 0X07      |        |
| Erase group size                                 | ERASE_GRP_SIZE     | 5     | R         | [46:42]   | 0X1F      |        |
| Erase group size multiplier                      | ERASE_GRP_MULT     | 5     | R         | [41:37]   | 0X1F      |        |
| Write protect group size                         | WP_GRP_SIZE        | 5     | R         | [36:32]   | 0x0F      |        |
| Write protect group enable                       | WP_GRP_ENABLE      | 1     | R         | [31:31]   | 0X01      |        |
| Manufacturer default ECC                         | DEFAULT_ECC        | 2     | R         | [30:29]   | 0X00      |        |
| Write speed factor                               | R2W_FACTOR         | 3     | R         | [28:26]   | 0X03      |        |
| Max. write data block length                     | WRITE_BL_LEN       | 4     | R         | [25:22]   | 0X09      |        |
| Partial blocks for write allowed                 | WRITE_BL_PARTIAL   | 1     | R         | [21:21]   | 0X00      |        |
| Reserved                                         |                    | 4     | R         | [20:17]   |           |        |
| Content protection application                   | CONTENT_PROT_APP   | 1     | R         | [16:16]   | 0X00      |        |
| File format group                                | FILE_FORMAT_GRP    | 1     | R/W       | [15:15]   | 0X00      |        |

[Table 20]CSD fields

| Name                       | Field              | Width | Cell type | CSD slice | CSD value | Remark    |
|----------------------------|--------------------|-------|-----------|-----------|-----------|-----------|
| Copy flag (OTP)            | COPY               | 1     | R/W       | [14:14]   | 0X00      |           |
| Permanent write protection | PERM_WRITE_PROTECT | 1     | R/W       | [13:13]   | 0X00      |           |
| Temporary write protection | TMP_WRITE_PROTECT  | 1     | R/W/E     | [12:12]   | 0X00      |           |
| File format                | FILE_FORMAT        | 2     | R/W       | [11:10]   | 0X00      |           |
| ECC code                   | ECC                | 2     | R/W/E     | [9:8]     | 0X00      |           |
| CRC                        | CRC                | 7     | R/W/E     | [7:1]     | -         | Not fixed |
| Not used, always '1'       |                    | 1     |           | [0:0]     | 0X01      |           |

**[Table 20] CSD fields (continued)**

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

## 7.4 Extended CSD register

The Extended CSD register defines eMMC properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines eMMC capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment, which defines the configuration eMMC is working in. These modes can be changed by the host by means of the switch command.

| Name                                      | Field                                     | CSD slice | Cell Type | CSD value  | Remark |
|-------------------------------------------|-------------------------------------------|-----------|-----------|------------|--------|
| Properties segment                        |                                           |           |           |            |        |
| Reserved                                  |                                           | [511:506] |           |            |        |
| Extended Security Commands Error          | EXT_SECURITY_ERR                          | [505]     | R         | 0x00       |        |
| Supported command sets                    | S_CMD_SET                                 | [504]     | R         | 0x01       |        |
| HPI features                              | HPI_FEATURES                              | [503]     | R         | 0x01       |        |
| Background operations support             | BKOPS_SUPPORT                             | [502]     | R         | 0x01       |        |
| Max packed read commands                  | MAX_PACKED_READS                          | [501]     | R         | 0x3F       |        |
| Max packed write commands                 | MAX_PACKED_WRITES                         | [500]     | R         | 0x3F       |        |
| Data Tag Support                          | DATA_TAG_SUPPORT                          | [499]     | R         | 0x01       |        |
| Tag Unit Size                             | TAG_UNIT_SIZE                             | [498]     | R         | 0x00       |        |
| Tag Resources Size                        | TAG_RES_SIZE                              | [497]     | R         | 0x00       |        |
| Context management capabilities           | CONTEXT_CAPABILITIES                      | [496]     | R         | 0x05       |        |
| Large Unit size                           | LARGE_UNIT_SIZE_M1                        | [495]     | R         | 0x01       |        |
| Extended partitions attribute support     | EXT_SUPPORT                               | [494]     | R         | 0x03       |        |
| Supported modes                           | SUPPORTED_MODES                           | [493]     | R         | 0x01       |        |
| FFU features                              | FFU_FEATURES                              | [492]     | R         | 0x00       |        |
| Operation codes timeout                   | OPERATION_CODE_TIME OUT                   | [491]     | R         | 0x00       |        |
| FFU Argument                              | FFU_ARG                                   | [490:487] | R         | 0xFFFFAFF0 |        |
| Barrier support                           | BARRIER_SUPPORT                           | [486]     | R         | 0x01       |        |
| Reserved                                  |                                           | [485:309] |           |            |        |
| CMD Queuing Support                       | CMDQ_SUPPORT                              | [308]     | R         | 0x1        |        |
| CMD Queuing Depth                         | CMDQ_DEPTH                                | [307]     | R         | 0x1F       |        |
| Reserved                                  |                                           | [306]     |           |            |        |
| Number of FW sectors correctly programmed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | [305:302] | R         | 0x00000000 |        |
| Vendor proprietary health report          | VENDOR_PROPRIETARY_HEALTH_REPORT          | [301:270] | R         |            |        |

[Table 21] Extended CSD

| Name                                                       | Field                      | CSD slice | Cell Type | CSD value        | Remark      |
|------------------------------------------------------------|----------------------------|-----------|-----------|------------------|-------------|
| Device life time estimation type B                         | DEVICE_LIFE_TIME_EST_TYP_B | [269]     | R         | Variable         |             |
| Device life time estimation type A                         | DEVICE_LIFE_TIME_EST_TYP_A | [268]     | R         | Variable         |             |
| Pre EOL information                                        | PRE_EOL_INFO               | [267]     | R         | 0x01             |             |
| Optimal read size                                          | OPTIMAL_READ_SIZE          | [266]     | R         | 0x20             |             |
| Optimal write size                                         | OPTIMAL_WRITE_SIZE         | [265]     | R         | 0x20             |             |
| Optimal trim unit size                                     | OPTIMAL_TRIM_UNIT_SIZE     | [264]     | R         | 0x01             |             |
| Device version                                             | DEVICE_VERSION             | [263:262] | R         | 32GB :<br>0x420E | Not fixed   |
| Firmware version                                           | FIRMWARE_VERSION           | [261:254] | R         | -                | Not fixed   |
| Power class for 200MHz, DDR<br>at Vcc=3.6V                 | PWR_CL_DDR_200_360         | [253]     | R         | 0x04             |             |
| Cache size                                                 | CACHE_SIZE                 | [252:249] | R         | 0x00000800       |             |
| Generic CMD6 timeout                                       | GENERIC_CMD6_TIME          | [248]     | R         | 0x0A             |             |
| Power off Notification (long)<br>timeout                   | POWER_OFF_LONG_TIME        | [247]     | R         | 0x3C             |             |
| Background operations status                               | BKOPS_STATUS               | [246]     | R         | 0x00             |             |
| Number of correctly<br>programmed sectors                  | CORRECTLY_PRG_SECTORS_NUM  | [245:242] | R         | -                | Not fixed   |
| 1st initialization time<br>after partitioning              | INI_TIMEOUT_AP             | [241]     | R         | 0x0A             |             |
| Cache Flushing Policy                                      | CACHE_FLUSH_POLICY         | [240]     | R         | 0x01             |             |
| Power class for 52MHz, DDR<br>at Vcc=3.6V                  | PWR_CL_DDR_52_360          | [239]     | R         | 0x00             |             |
| Power class for 52MHz, DDR<br>at Vcc=1.95V                 | PWR_CL_DDR_52_195          | [238]     | R         | 0x00             | Not support |
| Power class for 200MHz<br>at Vccq=1.95, Vcc=3.6V           | PWR_CL_200_195             | [237]     | R         | 0x00             |             |
| Power class for 200MHz<br>at Vccq=1.3, Vcc=3.6V            | PWR_CL_200_130             | [236]     | R         | 0x00             | Not support |
| Minimum write performance<br>for 8bit at 52MHz in DDR mode | MIN_PERF_DDR_W_8_52        | [235]     | R         | 0x00             |             |
| Minimum read performance<br>for 8bit at 52MHz in DDR mode  | MIN_PERF_DDR_R_8_52        | [234]     | R         | 0x00             |             |
| Reserved                                                   |                            | [233]     |           |                  |             |
| TRIM multiplier                                            | TRIM_MULT                  | [232]     | R         | 0x02             |             |
| Secure feature support                                     | SEC_FEATURE_SUPPORT        | [231]     | R         | 0x55             |             |
| Secure erase multiplier                                    | SEC_ERASE_MULT             | [230]     | R         | 0xFA             |             |
| Secure TRIM multiplier                                     | SEC_TRIM_MULT              | [229]     | R         | 0xFA             |             |

**[Table 21] Extended CSD(Continued)**

| Name                                                           | Field                               | CSD slice | Cell Type | CSD value            | Remark      |
|----------------------------------------------------------------|-------------------------------------|-----------|-----------|----------------------|-------------|
| Boot information                                               | BOOT_INFO                           | [228]     | R         | 0x07                 |             |
| Reserved                                                       |                                     | [227]     |           |                      |             |
| Boot partition size                                            | BOOT_SIZE_MULTI                     | [226]     | R         | 0x20                 |             |
| Access size                                                    | ACC_SIZE                            | [225]     | R         | 0x07                 |             |
| High-capacity erase unit size                                  | HC_ERASE_GRP_SIZE                   | [224]     | R         | 0x01                 |             |
| High-capacity erase timeout                                    | ERASE_TIMEOUT_MULT                  | [223]     | R         | 0x02                 |             |
| Reliable write sector count                                    | REL_WR_SEC_C                        | [222]     | R         | 0x01                 |             |
| High-capacity write protect group size                         | HC_WP_GRP_SIZE                      | [221]     | R         | 0x10                 |             |
| Sleep current(Vcc)                                             | S_C_Vcc                             | [220]     | R         | 0x08                 |             |
| Sleep current(Vccq)                                            | S_C_Vccq                            | [219]     | R         | 0x09                 |             |
| Production state awareness timeout                             | PRODUCTION_STATE_AWARENES S_TIMEOUT | [218]     | R         | 0x0A                 |             |
| Sleep/awake timeout                                            | S_A_TIMEOUT                         | [217]     | R         | 0x15                 |             |
| Sleep Notification Timeout                                     | SLEEP_NOTIFICATION_TIME             | [216]     | R         | 0x0E                 |             |
| Sector count                                                   | SEC_COUNT                           | [215:212] | R         | 32GB :<br>0X03A3E000 |             |
| Secure Write Protect information                               | SECURE_WP_INFO                      | [211]     | R         | 0x01                 |             |
| Minimum write performance for 8bit at 52MHz                    | MIN_PERF_W_8_52                     | [210]     | R         | 32GB : 0x78          |             |
| Minimum read performance for 8bit at 52MHz                     | MIN_PERF_R_8_52                     | [209]     | R         | 0x8C                 |             |
| Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_W_8_26_4_52                | [208]     | R         | 32GB : 0x46          |             |
| Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz  | MIN_PERF_R_8_26_4_52                | [207]     | R         | 0x46                 |             |
| Minimum write performance for 4bit at 26MHz                    | MIN_PERF_W_4_26                     | [206]     | R         | 0x1E                 |             |
| Minimum read performance for 4bit at 26MHz                     | MIN_PERF_R_4_26                     | [205]     | R         | 0x1E                 |             |
| Reserved                                                       |                                     | [204]     |           |                      |             |
| Power class for 26MHz at 3.6V                                  | PWR_CL_26_360                       | [203]     | R         | 0x00                 |             |
| Power class for 52MHz at 3.6V                                  | PWR_CL_52_360                       | [202]     | R         | 0x00                 |             |
| Power class for 26MHz at 1.95V                                 | PWR_CL_26_195                       | [201]     | R         | 0x00                 | Not support |
| Power class for 52MHz at 1.95V                                 | PWR_CL_52_195                       | [200]     | R         | 0x00                 | Not support |

**[Table 21] Extended CSD(Continued)**



| Name                                   | Field                 | CSD slice | Cell Type          | CSD value | Remark |
|----------------------------------------|-----------------------|-----------|--------------------|-----------|--------|
| Partition switching timing             | PARTITION_SWITCH_TIME | [199]     | R                  | 0x01      |        |
| Out-of-interrupt busy timing           | OUT_OF_INTERRUPT_TIME | [198]     | R                  | 0x0A      |        |
| I/O Driver Strength                    | DRIVER_STRENGTH       | [197]     | R                  | 0x1F      |        |
| Device type                            | DEVICE_TYPE           | [196]     | R                  | 0x57      |        |
| Reserved                               |                       | [195]     |                    |           |        |
| CSD structure                          | CSD_STRUCTURE         | [194]     | R                  | 0x02      |        |
| Reserved                               |                       | [193]     |                    |           |        |
| Extended CSD revision                  | EXT_CSD_REV           | [192]     | R                  | 0x08      |        |
| Modes Segment                          |                       |           |                    |           |        |
| Command set                            | CMD_SET               | [191]     | R/W/E_P            | 0x00      |        |
| Reserved                               |                       | [190]     |                    |           |        |
| Command set revision                   | CMD_SET_REV           | [189]     | R                  | 0x00      |        |
| Reserved                               |                       | [188]     |                    |           |        |
| Power class                            | POWER_CLASS           | [187]     | R/W/E_P            | 0x00      |        |
| Reserved                               |                       | [186]     |                    |           |        |
| High-speed interface timing            | HS_TIMING             | [185]     | R/W/E_P            | 0x00      |        |
| Strobe Support                         | STROBE_SUPPORT        | [184]     | R                  | 0x01      |        |
| Bus width mode                         | BUS_WIDTH             | [183]     | W/E_P              | 0x00      |        |
| Reserved                               |                       | [182]     |                    |           |        |
| Erased memory content                  | ERASED_MEM_CONT       | [181]     | R                  | 0x00      |        |
| Reserved                               |                       | [180]     |                    |           |        |
| Partition configuration                | PARTITION_CONFIG      | [179]     | R/W/E &<br>R/W/E_P | 0x00      |        |
| Boot config protection                 | BOOT_CONFIG_PROT      | [178]     | R/W/E &<br>R/W/C_P | 0x00      |        |
| Boot bus conditions                    | BOOT_BUS_CONDITIONS   | [177]     | R/W/E              | 0x00      |        |
| Reserved                               |                       | [176]     |                    |           |        |
| High-density erase group definition    | ERASE_GROUP_DEF       | [175]     | R/W/E_P            | 0x00      |        |
| Boot write protection status registers | BOOT_WP_STATUS        | [174]     | R                  | 0x00      |        |
| Boot area write protection register    | BOOT_WP               | [173]     | R/W/E &<br>R/W/C_P | 0x00      |        |
| Reserved                               |                       | [172]     |                    |           |        |

**[Table 21] Extended CSD(Continued)**

| Name                                   | Field                       | CSD slice | Cell Type                     | CSD value         | Remark |
|----------------------------------------|-----------------------------|-----------|-------------------------------|-------------------|--------|
| User area write protection register    | USER_WP                     | [171]     | R/W, R/W/<br>C_P & /W/<br>E_P | 0x00              |        |
| Reserved                               |                             | [170]     |                               |                   |        |
| FW configuration                       | FW_CONFIG                   | [169]     | R/W                           | 0x00              |        |
| RPMB Size                              | RPMB_SIZE_MULT              | [168]     | R                             | 0x80              |        |
| Write reliability setting register     | WR_REL_SET                  | [167]     | R/W                           | 0x1F              |        |
| Write reliability parameter register   | WR_REL_PARAM                | [166]     | R                             | 0x15              |        |
| Sanitize start                         | SANITIZE_START              | [165]     | W/E_P                         | 0x00              |        |
| Manually start background operations   | BKOPS_START                 | [164]     | W/E_P                         | 0x00              |        |
| Enable background operations Handshake | BKOPS_EN                    | [163]     | R/W                           | 0x00              |        |
| H/W reset function                     | RST_n_FUNCTION              | [162]     | R/W                           | 0x00              |        |
| HPI management                         | HPI_MGMT                    | [161]     | R/W/E_P                       | 0x00              |        |
| Partitioning support                   | PARTITIONING_SUPPORT        | [160]     | R                             | 0x07              |        |
| Max enhanced area size                 | MAX_ENH_SIZE_MULT           | [159:157] | R                             | 32GB:<br>0x000747 |        |
| Partitions attribute                   | PARTITIONS_ATTRIBUTE        | [156]     | R/W                           | 0x00              |        |
| Partitioning setting                   | PARTITION_SETTING_COMPLETE  | [155]     | R/W                           | 0x00              |        |
| General purpose partition size         | GP_SIZE_MULT                | [154:143] | R/W                           | 0x00...00         |        |
| Enhanced user data area size           | ENH_SIZE_MULT               | [142:140] | R/W                           | 0x000000          |        |
| Enhanced user data start address       | ENH_START_ADDR              | [139:136] | R/W                           | 0x00000000        |        |
| Reserved                               |                             | [135]     |                               |                   |        |
| Bad Block management mode              | SEC_BAD_BLK_MGMNT           | [134]     | R/W                           | 0x00              |        |
| Production state awareness             | PRODUCTION_STATE_AWARENESS  | [133]     | R/W/E                         | 0x00              |        |
| Package Case Temperature is Controlled | TCASE_SUPPORT               | [132]     | W/E_P                         | 0x00              |        |
| Periodic Wake-up                       | PERIODIC_WAKEUP             | [131]     | R/W/E                         | 0x00              |        |
| Program CID/CSD in DDR mode support    | PROGRAM_CID_CSD_DDR_SUPPORT | [130]     | R                             | 0x01              |        |
| Reserved                               |                             | [129:128] |                               |                   |        |
| Vendor Specific Fields                 | VENDOR_SPECIFIC_FIELD       | [127:64]  | Vendor specific               |                   |        |

[Table 21] Extended CSD(Continued)

| Name                                                     | Field                              | CSD slice | Cell Type | CSD value           | Remark |
|----------------------------------------------------------|------------------------------------|-----------|-----------|---------------------|--------|
| Native sector size                                       | NATIVE_SECTOR_SIZE                 | [63]      | R         | 0x01                |        |
| Sector size emulation                                    | USE_NATIVE_SECTOR                  | [62]      | R/W       | 0x00                |        |
| Sector size                                              | DATA_SECTOR_SIZE                   | [61]      | R         | 0x00                |        |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU                    | [60]      | R         | 0x0A                |        |
| Class 6 commands control                                 | Class6_CTRL                        | [59]      | R/W/E_P   | 0x00                |        |
| Number of addressed group to be Released                 | DYNCAP_NEEDED                      | [58]      | R         | 0x00                |        |
| Exception events control                                 | EXCEPTION_EVENTS_CTRL              | [57:56]   | R/W/E_P   | 0x00                |        |
| Exception events status                                  | EXCEPTION_EVENTS_STATUS            | [55:54]   | R         | 0x0000              |        |
| Extended Partitions Attribute                            | EXT_PARTITIONS_ATTRIBUTE           | [53:52]   | R/W       | 0x0000              |        |
| Context configuration                                    | CONTEXT_CONF                       | [51:37]   | R/W/E_P   | 0x00...00           |        |
| Packed command status                                    | PACKED_COMMAND_STATUS              | [36]      | R         | 0x00                |        |
| Packed command failure index                             | PACKED_FAILURE_INDEX               | [35]      | R         | 0x00                |        |
| Power Off Notification                                   | POWER_OFF_NOTIFICATION             | [34]      | R/W/E_P   | 0x00                |        |
| Control to turn the Cache ON/OFF                         | CACHE_CTRL                         | [33]      | R/W/E_P   | 0x00                |        |
| Flushing of the cache                                    | FLUSH_CACHE                        | [32]      | W/E_P     | 0x00                |        |
| Control to turn the barrier ON/OFF                       | BARRIER_CONTROL                    | [31]      | R/W       | 0x00                |        |
| Mode config                                              | MODE_CONFIG                        | [30]      | R/W/E_P   | 0x00                |        |
| Mode operation codes                                     | MODE_OPERATION_CODES               | [29]      | W/E_P     | 0x00                |        |
| Reserved                                                 |                                    | [28:27]   |           |                     |        |
| FFU Status                                               | FFU_STATUS                         | [26]      | R         | 0x00                |        |
| Pre loading data size                                    | PRE_LOADING_DATA_SIZE              | [25:22]   | R/W/E_P   | 0x00000000          |        |
| Max pre loading data size                                | MAX_PRE_LOADING_DATA_SIZE          | [21:18]   | R         | 32GB:<br>0x01D1F000 |        |
| Product state awareness enablement                       | PRODUCT_STATE_AWARENESS_ENABLEMENT | [17]      | R/W/E & R | 0x01                |        |
| Secure Removal Type                                      | SECURE_REMOVAL_TYPE                | [16]      | R/W & R   | 0x0B                |        |
| Command Queue Mode Enable                                | CMDQ_MODE_EN                       | [15]      | R/W/E_P   | 0x00                |        |
| Reserved                                                 |                                    | [14:0]    |           |                     |        |

[Table 21] Extended CSD(Continued)

- Reserved bits should read as "0"
- Obsolete values should be don't care

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## 7.5 RCA (Relative card address)

The writable 16-bit relative card address (RCA) register carries the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

## 7.6 DSR (Driver stage register)

It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

## LPDDR4X SDRAM

## 1. Functional Description

LPDDR4-SDRAM is a high-speed synchronous DRAM device internally configured as an 2-channel memory with 8-bank memory per each channel.

These devices contain the following number of bits per die:

4Gb has 4,294,967,296 bits

6Gb has 6,442,450,944 bits

8Gb has 8,589,934,592 bits

12Gb has 12,884,901,888 bits

16Gb has 17,179,869,184 bits

24Gb has 25,769,803,776 bits

32Gb has 34,359,738,368 bits

LPDDR4 devices use multi cycle of single data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address and bank information. Each command uses two clock cycles, during which command information is transferred on positive edge of the corresponding clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4 SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and sixteen corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR4 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation

### 1.1. LPDDR4 SDRAM Addressing

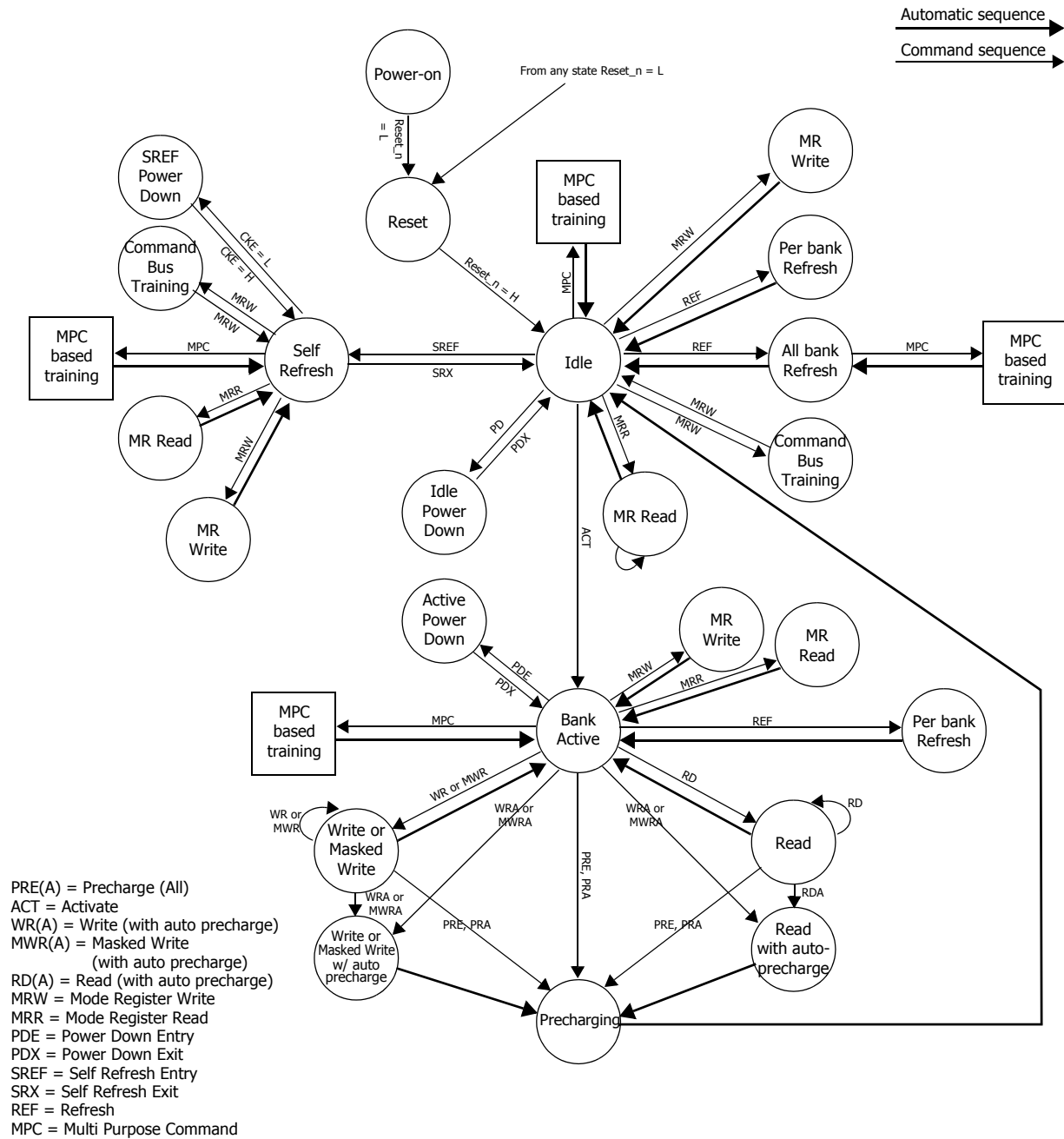
| Memory Density (per Die)             |                  | 4Gb                                        | 6Gb                                        | 8Gb                                        | 12Gb                                     | 16Gb                                       |
|--------------------------------------|------------------|--------------------------------------------|--------------------------------------------|--------------------------------------------|------------------------------------------|--------------------------------------------|
| Memory Density (per channel)         |                  | 2Gb                                        | 3Gb                                        | 4Gb                                        | 6Gb                                      | 8Gb                                        |
| Configuration                        |                  | 16 Mb x 16 DQ<br>x 8 banks<br>x 2 channels | 24 Mb x 16 DQ<br>x 8 banks<br>x 2 channels | 32 Mb x 16 DQ<br>x 8 banks<br>x 2 channels | 48Mb x 16DQ<br>x 8 banks<br>x 2 channels | 64 Mb x 16 DQ<br>x 8 banks<br>x 2 channels |
| Number of Channels per die           |                  | 2                                          | 2                                          | 2                                          | 2                                        | 2                                          |
| Number of Banks per Channel          |                  | 8                                          | 8                                          | 8                                          | 8                                        | 8                                          |
| Array Pre-fetch (bits, per channel)  |                  | 256                                        | 256                                        | 256                                        | 256                                      | 256                                        |
| Number of Rows per Channel           |                  | 16,384                                     | 24,576                                     | 32,768                                     | 49,152                                   | 65,536                                     |
| Number of Columns (fetch boundaries) |                  | 64                                         | 64                                         | 64                                         | 64                                       | 64                                         |
| Page Size (Bytes)                    |                  | 2048                                       | 2048                                       | 2048                                       | 2048                                     | 2048                                       |
| Channel Density (Bits per channel)   |                  | 2,147,483,648                              | 3,221,225,472                              | 4,294,967,296                              | 6,442,450,944                            | 8,589,934,592                              |
| Total Density (Bits per die)         |                  | 4,294,967,296                              | 6,442,450,944                              | 8,589,934,592                              | 12,884,901,888                           | 17,179,869,184                             |
| Bank Address                         |                  | BA0 - BA2                                  | BA0 - BA2                                  | BA0 - BA2                                  | BA0 - BA2                                | BA0 - BA2                                  |
| x16                                  | Row Addresses    | R0 - R13                                   | R0 - R14<br>(R13=0 when R14=1)             | R0 - R14                                   | R0 - R15<br>(R14=0 when R15=1)           | R0 - R15                                   |
|                                      | Column Addresses | C0 - C9                                    | C0 - C9                                    | C0 - C9                                    | C0 - C9                                  | C0 - C9                                    |
| Burst Starting Address Boundary      |                  | 64-bit                                     | 64-bit                                     | 64-bit                                     | 64-bit                                   | 64-bit                                     |

1. The lower two column addresses (C0-C1) are assumed to be "zero" and are not transmitted on the CA bus.
2. Row and Column address values on the CA bus that are not used for a particular density are "don't care."
3. For non-binary memory densities, only half of the row address space is valid. When the MSB address bit is "HIGH", then the MSB-1 address bit must be "LOW".

## 1.2. Simplified State Diagram

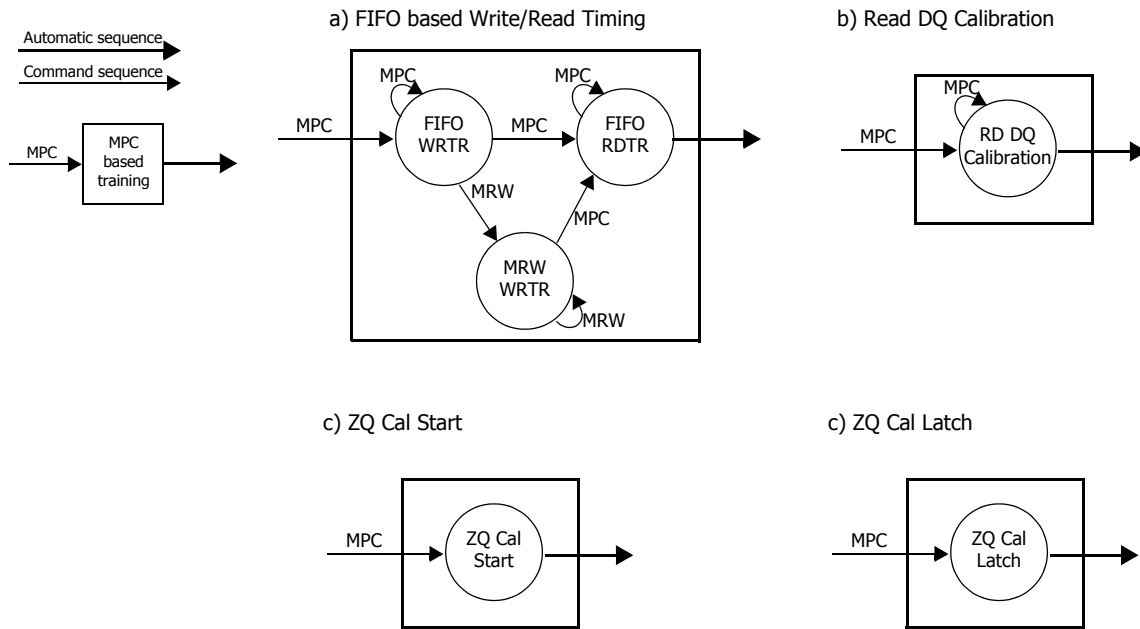
The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the Commands and Timing section.

**Figure - Simplified State Diagram**





**Figure - Simplified Bus Interface State Diagram**



**Notes:**

1. From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self-Refresh for more information.
2. In IDLE state, all banks are pre-charged.
3. In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
4. In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
5. This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7. The RESET\_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET\_n.

### 1.2.1. Power-up and Initialization

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as following table.

**Table - MRS defaults settings**

| Item             | MRS          | Default setting | Description                     |
|------------------|--------------|-----------------|---------------------------------|
| FSP-OP/WR        | MR13 OP[7:6] | 00B             | FS-OP/WR[0] are enabled         |
| WLS              | MR2 OP[6]    | 0B              | Write Latency Set 0 is selected |
| WL               | MR2 OP[5:3]  | 000B            | WL = 4                          |
| RL               | MR2 OP[2:0]  | 000B            | RL = 6, nRTP = 8                |
| nWR              | MR1 OP[6:4]  | 000B            | nWR = 6                         |
| DBI-WR/RD        | MR3 OP[7:6]  | 00B             | Write & Read DBI are disabled   |
| CA ODT           | MR11 OP[6:4] | 000B            | CA ODT is disabled              |
| DQ ODT           | MR11 OP[2:0] | 000B            | DQ ODT is disabled              |
| Vref(ca) Setting | MR12 OP[6]   | 1B              | Vref(ca) Range[1] enabled       |
| Vref(ca) value   | MR12 OP[5:0] | 011101B         | Range1: 50.4% of VDDQ           |
| Vref(DQ) Setting | MR14 OP[6]   | 1B              | Vref(DQ) Range[1] enabled       |
| Vref(DQ) Value   | MR14 OP[5:0] | 011101B         | Range1: 50.4% of VDDQ           |

#### 1.2.1.1. Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET\_n is recommended to be LOW ( $\leq 0.2 \times VDD2$ ) and all inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET\_n is held LOW. Power supply voltage ramp requirements are provided in Table "Voltage Ramp Conditions". VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

**Table - Voltage Ramp Conditions**

| After...      | Applicable Conditions                  |
|---------------|----------------------------------------|
| Ta is reached | VDD1 must be greater than VDD2         |
|               | VDD2 must be greater than VDDQ - 200mV |

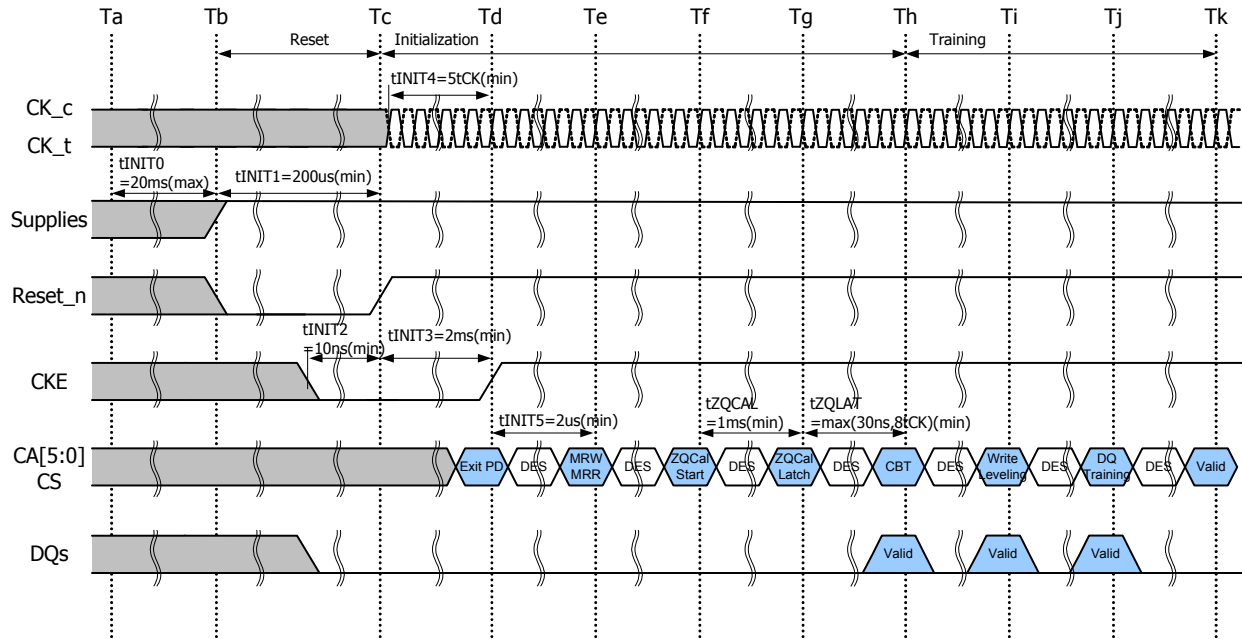
Note:

1. Ta is the point when any power supply first reaches 300mV.
2. Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined ranges.
4. Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
5. The voltage difference between any of VSS and VSSQ pins must not exceed 100mV.

2. Following the completion of the voltage ramp (Tb), RESET\_n must be maintained LOW. DQ, DMI, DQS\_t and DQS\_c voltage levels must be between Vssq and Vddq during voltage ramp to avoid latch-up. CKE, CK\_t, CK\_c, CS\_n and CA input levels must be between Vss and VDD2 during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET\_n must remain LOW for at least tINIT1(Tc), after which RESET\_n can be de-asserted to HIGH(Tc). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

**Figure - Power Ramp and Initialization Sequence**



**Note**

1. Training is optional and may be done at the system architects discretion. The training sequence after ZQ\_CAL Latch(Th, Sequence7~9) in the above figure, is simplified recommendation and actual training sequence may vary depending on systems.

4. After RESET\_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. Clock(CK\_t,CK\_c) is required to be started and stabilized for tINIT4 before CKE goes active(Td). CS is required to be maintained LOW when controller activates CKE.

5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands(Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory(Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th) the command bus (internal VREF(ca), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed operations, and VREF(ca) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high(Ti). See write leveling section for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS\_t/\_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal VREF(dq), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust VREF(dq)(Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and VREF(dq) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

10. At Tk the LPDDR4 device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

**Table - Initialization Timing Parameters**

| Parameter | Value          |           | Unit | Comment                                                   |
|-----------|----------------|-----------|------|-----------------------------------------------------------|
|           | Min            | Max       |      |                                                           |
| tINIT0    |                | 20        | ms   | Maximum Voltage Ramp Time                                 |
| tINIT1    | 200            |           | us   | Minimum RESET_n LOW time after completion of voltage ramp |
| tINIT2    | 10             |           | ns   | Minimum CKE LOW time before RESET_n goes HIGH             |
| tINIT3    | 2              |           | ms   | Minimum CKE LOW time after RESET_n goes HIGH              |
| tINIT4    | 5              |           | tCK  | Minimum stable clock before first CKE HIGH                |
| tINIT5    | 2              |           | us   | Minimum idle time before first MRW/MRR command            |
| tZQCAL    | 1              |           | us   | ZQ Calibration time                                       |
| tZQLAT    | Max(30ns,8tCK) |           | ns   | ZQCAL latch quite time                                    |
| tCKb      | Note 1, 2      | Note 1, 2 | ns   | Clock cycle time during boot                              |

Notes

1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent

### 1.2.1.2. Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET\_n below  $0.2 \times VDD2$  anytime when reset is needed. RESET\_n needs to be maintained for minimum tPW\_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET\_n.

2. Repeat steps 4 to 10 in "Voltage Ramp and Device Initialization" section.

**Table - Reset Timing Parameter**

| Parameter | Value |     | Unit | Comment                                                             |
|-----------|-------|-----|------|---------------------------------------------------------------------|
|           | Min   | Max |      |                                                                     |
| tPW_RESET | 100   | -   | ns   | Minimum RESET_n low time for Reset Initialization with stable power |

### 1.2.2. Power-off Sequence

#### 1.2.2.1. Controlled Power-off

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ( $\leq 0.2 \times VDD2$ ) and all other inputs must be between  $VIL_{min}$  and  $VIH_{max}$ . The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS<sub>t</sub> and DQS<sub>c</sub> voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. RESET<sub>n</sub>, CK<sub>t</sub>, CK<sub>c</sub>, CS and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After TZ, the device is powered off.

**Table - Power Supply Conditions for Power-off**

| Between... | Applicable Conditions                  |
|------------|----------------------------------------|
| TX and TZ  | VDD1 must be greater than VDD2         |
|            | VDD2 must be greater than VDDQ - 200mV |

Note: The voltage difference between any of VSS, VSSQ pins must not exceed 100mV

#### 1.2.2.2. Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5V/ $\mu$ s between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

**Table - Timing Parameters for Power-off**

| Symbol | Value |     | Unit | Comment                     |
|--------|-------|-----|------|-----------------------------|
|        | Min   | Max |      |                             |
| tPOFF  |       | 2   | s    | Maximum Power-off ramp time |

### 1.3. Mode Register Definition

Table below shows the mode registers for LPDDR4 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

**Table. Mode Register Assignment**

| MR# | MA<br><5:0> | Function                   | Access | OP7                                            | OP6              | OP5          | OP4     | OP3       | OP2          | OP1          | OP0          | Link     |      |
|-----|-------------|----------------------------|--------|------------------------------------------------|------------------|--------------|---------|-----------|--------------|--------------|--------------|----------|------|
| 0   | 00H         | Device Information         | R      | Reserved                                       | RFU              | Single Ended | RZQI    |           | RFU          | Latency Mode | Refresh Mode | MR0      |      |
| 1   | 01H         | Device Feature 1           | W      | RPST                                           | nWR (for AP)     |              |         | RD-PRE    | WR-PRE       | BL           |              | MR1      |      |
| 2   | 02H         | Device Feature 2           | W      | WR Lev                                         | WLS              | WL           |         |           | RL           |              |              | MR2      |      |
| 3   | 03H         | IO Configuration 1         | W      | DBI-WR                                         | DBI-RD           | PDDS         |         |           | PPRP         | WR-PST       | PU-CAL       | MR3      |      |
| 4   | 04H         | Refresh Rate               | R/W    | TUF                                            | Thermal Offset   |              | PPRE    | SR Abort  | Refresh Rate |              |              | MR4      |      |
| 5   | 05H         | Basic Configuration 1      | R      | LPDDR4 Manufacturer ID                         |                  |              |         |           |              |              |              | MR5      |      |
| 6   | 06H         | Basic Configuration 2      | R      | Revision ID-1                                  |                  |              |         |           |              |              |              | MR6      |      |
| 7   | 07H         | Basic Configuration 3      | R      | Revision ID-2                                  |                  |              |         |           |              |              |              | MR7      |      |
| 8   | 08H         | Basic Configuration 4      | R      | IO Width                                       |                  | Density      |         |           |              | Type         |              | MR8      |      |
| 9   | 09H         | Test Mode                  | W      | Vendor Specific Test Mode                      |                  |              |         |           |              |              |              | MR9      |      |
| 10  | 0AH         | ZQ Reset                   | W      | RFU                                            |                  |              |         |           |              |              |              | ZQ Reset | MR10 |
| 11  | 0BH         | ODT Feature                | W      | DQ ODT-nt                                      | CA ODT           |              |         | DQ ODT-nt | DQ ODT       |              |              | MR11     |      |
| 12  | 0CH         | VREF(ca) R0                | R/W    | CBT Mode                                       | VR-CA            | VREF(ca)     |         |           |              |              |              | MR12     |      |
| 13  | 0DH         | Functional options         | W      | FSP-OP                                         | FSP-WR           | DMD          | RRO     | VRCG      | VRO          | RPT          | CBT          | MR13     |      |
| 14  | 0EH         | VREF(dq)                   | R/W    | RFU                                            | VR(dq)           | VREF(dq)     |         |           |              |              |              | MR14     |      |
| 15  | 0FH         | Invert Register 0          | W      | Lower Byte Invert for DQ Calibration           |                  |              |         |           |              |              |              | MR15     |      |
| 16  | 10H         | PASR Bank                  | W      | PASR Bank Mask                                 |                  |              |         |           |              |              |              | MR16     |      |
| 17  | 11H         | PASR Segment               | W      | PASR Segment Mask                              |                  |              |         |           |              |              |              | MR17     |      |
| 18  | 12H         | DQS Oscillator 1           | R      | DQS Oscillator Count - LSB                     |                  |              |         |           |              |              |              | MR18     |      |
| 19  | 13H         | DQS Oscillator 2           | R      | DQS Oscillator Count - MSB                     |                  |              |         |           |              |              |              | MR19     |      |
| 20  | 14H         | Invert Register 1          | W      | Upper Byte Invert for DQ Calibration           |                  |              |         |           |              |              |              | MR20     |      |
| 21  | 15H         | Vendor Specific            | N/A    | RFU                                            |                  | LS CA buffer | RFU     |           |              |              |              | MR21     |      |
| 22  | 16H         | SOC ODT Feature            | W      | RFU                                            |                  | ODTD-CA      | ODTE-CS | ODTE-CK   | CODT         |              |              | MR22     |      |
| 23  | 17H         | DQS Oscillator Run Time    | W      | DQS Oscillator Interval Timer Run Time Setting |                  |              |         |           |              |              |              | MR23     |      |
| 24  | 18H         | TRR                        | R/W    | TRR                                            | TRR Bank Address |              |         | U-MAC     | MAC Value    |              |              | MR24     |      |
| 25  | 19H         | PPR Resource               | R      | Post Package Repair Resources                  |                  |              |         |           |              |              |              | MR25     |      |
| 26  | 1AH         | RFU                        | N/A    | Reserved for Future Use                        |                  |              |         |           |              |              |              | MR26     |      |
| 27  | 1BH         | RFU                        | N/A    | Reserved for Future Use                        |                  |              |         |           |              |              |              | MR27     |      |
| 28  | 1CH         | RFU                        | N/A    | Reserved for Future Use                        |                  |              |         |           |              |              |              | MR28     |      |
| 29  | 1DH         | RFU                        | N/A    | Reserved for Future Use                        |                  |              |         |           |              |              |              | MR29     |      |
| 30  | 1EH         | RFU                        | N/A    | Reserved for Future Use                        |                  |              |         |           |              |              |              | MR30     |      |
| 31  | 1FH         | RFU                        | N/A    | Reserved for Future Use                        |                  |              |         |           |              |              |              | MR31     |      |
| 32  | 20H         | DQ Calibration - Pattern A | W      | See "DQ Calibration" section                   |                  |              |         |           |              |              |              | MR32     |      |

| MR#   | MA<br><5:0> | Function                      | Access | OP7                          | OP6 | OP5 | OP4 | OP3          | OP2         | OP1         | OP0 | Link |
|-------|-------------|-------------------------------|--------|------------------------------|-----|-----|-----|--------------|-------------|-------------|-----|------|
| 33:39 | 21H:27H     | DNU                           | N/A    | Do Not Use                   |     |     |     |              |             |             |     |      |
| 40    | 28H         | DQ Calibration<br>- Pattern B | W      | See "DQ Calibration" section |     |     |     |              |             |             |     | MR40 |
| 41:47 | 29H:2FH     | DNU                           | N/A    | Do Not Use                   |     |     |     |              |             |             |     |      |
| 48:50 | 30H:32H     | RFU                           | N/A    | Reserved for Future Use      |     |     |     |              |             |             |     |      |
| 51    | 33H         | Single Ended Mode             | W      | RFU                          |     |     |     | S/E<br>Clock | S/E<br>WDQS | S/E<br>RDQS | RFU |      |
| 52:63 | 34H:3FH     | RFU                           | N/A    | Reserved for Future Use      |     |     |     |              |             |             |     |      |

1. RFU bits should be set to '0' during mode register writes
2. RFU bits should be read as '0' during mode register reads
3. All mode registers that are specified as RFU or Write-only shall return undefined data when read and DQS\_t/DQS\_c shall be toggled
4. All mode registers that are specified as RFU shall not be written
5. See vendor device datasheet for details on vendor-specific mode registers
6. Writes to Read-only registers shall have no effect on the functionality of the device

### 1.3.1. MR0 Register Information (MA[5:0] = 00H)

| OP[7]    | OP[6] | OP[5]                | OP[4] | OP[3] | OP[2] | OP[1]           | OP[0]           |
|----------|-------|----------------------|-------|-------|-------|-----------------|-----------------|
| Reserved | RFU   | Single Ended<br>Mode | RZQI  |       | RFU   | Latency<br>Mode | Refresh<br>Mode |

| Function                             | Register<br>Type | Operand | Data                                                                                                                                                                                                                                           | Notes   |
|--------------------------------------|------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| Refresh Mode                         | Read-only        | OP[0]   | 0B: Both legacy & modified refresh mode supported<br>1B: Only modified refresh mode supported                                                                                                                                                  |         |
| Latency Mode                         |                  | OP[1]   | 0B: Device supports normal latency<br>1B: Device supports byte mode latency                                                                                                                                                                    | 6,7     |
| RZQI<br>(Built-in Self-Test for RZQ) |                  | OP[4:3] | 00B: RZQ Self-Test Not Supported<br>01B: ZQ pin may connect to VSS or float<br>10B: ZQ-pin may short to VDDQ<br>11B: ZQ-pin Self-Test Completed, no error condition<br>detected (ZQ-pin may not connect to VDD2 or float,<br>nor short to VSS) | 1,2,3,4 |
| Single Ended Mode                    |                  | OP[5]   | 0B: No Support For Single Ended Mode<br>1B: Support For Single Ended Mode                                                                                                                                                                      | 8       |

#### Notes:

1. RZQI MR value, if supported, will be valid after the following sequence:
  - a. Completion of MPC ZQCAL Start command to either channel.
  - b. Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied. RZQI value will be lost after Reset.
2. If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01B or OP[4:3] = 10B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error, the LPDDR4-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.
4. If ZQ Self-Test returns OP[4:3] = 11B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).
5. CATR functionality may not provide right information whether CA termination is turned on or not. However, CA termination is required to be decided with the combination of MR22 OP[5] and MR11 OP[6:4] which shows CA ODT values. It is recommended

for user to have CATR information with the combination ODT\_PAD and MR11 OP[6:4]. MR0 OP[7] indicate 1'B only when MR22 OP[5] is high and MR11 OP[6:4] is not 000'b.

6. For the byte mode LPDDR4 SDRAM device, longer latency is required. The LPDDR4 SDRAM device will set MR0 OP[1]=1 to indicate which latencies are supported. See section for byte-mode latency for the details.
7. Devices not intended to be combined with byte mode devices are not required to support byte mode latency.
8. Support for Single Ended Mode is optional. If supported, single ended write DQS, read DQS, and CK can be enabled in MR51.

### 1.3.2. MR1 Register Information (MA[5:0] = 01H)

| OP[7] | OP[6]        | OP[5] | OP[4] | OP[3]  | OP[2]  | OP[1] | OP[0] |
|-------|--------------|-------|-------|--------|--------|-------|-------|
| RPST  | nWR (for AP) |       |       | RD-PRE | WR-PRE | BL    |       |

| Function                                            | Register Type | Operand | Data                                                                                                                                                  | Notes |
|-----------------------------------------------------|---------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| BL<br>(Burst Length)                                | Write-only    | OP[1:0] | 00B: BL=16 Sequential (default)<br>01B: BL=32 Sequential<br>10B: BL=16 or 32 Sequential (on-the-fly)<br>All Others: Reserved                          | 1,5,6 |
| WR-PRE<br>(WR Pre-ambble Length)                    |               | OP[2]   | 0B: Reserved<br>1B: WR Pre-ambble = 2nCK (default)                                                                                                    | 5,6   |
| RD-PRE<br>(RD Pre-ambble Type)                      |               | OP[3]   | 0B: RD Pre-ambble = Static (default)<br>1B: RD Pre-ambble = Toggle                                                                                    | 3,5,6 |
| nWR<br>(Write-Recovery for Auto Precharge commands) |               | OP[6:4] | 000B: nWR = 6 (default)<br>001B: nWR = 10<br>010B: nWR = 16<br>011B: nWR = 20<br>100B: nWR = 24<br>101B: nWR = 30<br>110B: nWR = 34<br>111B: nWR = 40 | 2,5,6 |
| RPST<br>(RD Post-ambble Length)                     |               | OP[7]   | 0B: RD Post-ambble = 0.5*tCK (default)<br>1B: RD Post-ambble = 1.5*tCK                                                                                | 4,5,6 |

1. Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the "BL" bit in the command operands. See the Command Truth Table.
2. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled. See Table, "Frequency Ranges for RL, WL, and nWR Settings" later in this section
3. For Read operations this bit must be set to select between a "toggling" pre-ambble and a "Non-toggling" pre-ambble. See the pre-ambble section for a drawing of each type of pre-ambble.
4. OP[7] provides an optional READ post-ambble with an additional rising and falling edge of DQS\_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.



### 1.3.2.1. Burst Sequence

**Table - Burst Sequence for Read**

| Burst Length | Burst Type | C4 | C3 | C2 | C1 | Co | Burst Cycle Number and Burst Address Sequence |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------------|------------|----|----|----|----|----|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|              |            |    |    |    |    |    | 1                                             | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 16           | SEQ        | V  | 0  | 0  | 0  | 0  | 0                                             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|              |            | V  | 0  | 1  | 0  | 0  | 4                                             | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|              |            | V  | 1  | 0  | 0  | 0  | 8                                             | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|              |            | V  | 1  | 1  | 0  | 0  | C                                             | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 32           | SEQ        | 0  | 0  | 0  | 0  | 0  | 0                                             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
|              |            | 0  | 0  | 1  | 0  | 0  | 4                                             | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 |
|              |            | 0  | 1  | 0  | 0  | 0  | 8                                             | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|              |            | 0  | 1  | 1  | 0  | 0  | C                                             | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B |
|              |            | 1  | 0  | 0  | 0  | 0  | 10                                            | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |
|              |            | 1  | 0  | 1  | 0  | 0  | 14                                            | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  |
|              |            | 1  | 1  | 0  | 0  | 0  | 18                                            | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
|              |            | 1  | 1  | 1  | 0  | 0  | 1C                                            | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  |

**Table - Burst Sequence for Write**

| Burst Length | Burst Type | C4 | C3 | C2 | C1 | Co | Burst Cycle Number and Burst Address Sequence |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------------|------------|----|----|----|----|----|-----------------------------------------------|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|              |            |    |    |    |    |    | 1                                             | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 16           | SEQ        | V  | 0  | 0  | 0  | 0  | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9  | A  | B  | C  | D  | E  | F  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 32           | SEQ        | 0  | 0  | 0  | 0  | 0  | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |

1. C1:Co input is not present on CA bus. It is implied zero.
2. The starting burst address is on 64-bit (4n) boundaries.
3. C2-C3 for BL16 and C2-C4 for BL32 shall be set to '0' for all Write operations.

### 1.3.3. MR2 Register Information (MA[5:0] = 02H)

| OP[7]  | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------|-------|-------|-------|-------|-------|-------|-------|
| WR Lev | WLS   | WL    |       |       | RL    |       |       |

Standard LPDDR4

| Function                   | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Notes |
|----------------------------|---------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| RL<br>(Read latency)       | Write only    | OP[2:0] | <b>DBI Disable (MR3 OP[6]=0B)</b><br>000B: RL= 6 & nRTP = 8 (Default)<br>001B: RL= 10 & nRTP = 8<br>010B: RL= 14 & nRTP = 8<br>011B: RL= 20 & nRTP = 8<br>100B: RL= 24 & nRTP = 10<br>101B: RL= 28 & nRTP = 12<br>110B: RL= 32 & nRTP = 14<br>111B: RL= 36 & nRTP = 16<br><b>DBI Enable (MR3 OP[6]=1B)</b><br>000B: RL= 6 & nRTP = 8<br>001B: RL= 12 & nRTP = 8<br>010B: RL= 16 & nRTP = 8<br>011B: RL= 22 & nRTP = 8<br>100B: RL= 28 & nRTP = 10<br>101B: RL= 32 & nRTP = 12<br>110B: RL= 36 & nRTP = 14<br>111B: RL= 40 & nRTP = 16 | 1,3,4 |
| WL<br>(Write latency)      |               | OP[5:3] | <b>Set "A" (MR2 OP[6]=0B)</b><br>000B: WL=4 (Default)<br>001B: WL=6<br>010B: WL=8<br>011B: WL=10<br>100B: WL=12<br>101B: WL=14<br>110B: WL=16<br>111B: WL=18<br><b>Set "B" (MR2 OP[6]=1B)</b><br>000B: WL=4<br>001B: WL=8<br>010B: WL=12<br>011B: WL=18<br>100B: WL=22<br>101B: WL=26<br>110B: WL=30<br>111B: WL=34                                                                                                                                                                                                                   | 1,3,4 |
| WLS<br>(Write latency set) |               | OP[6]   | 0B: WL Set "A" (default)<br>1B: WL Set "B"                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 1,3,4 |
| WR Lev<br>(Write Leveling) |               | OP[7]   | 0B: Disabled (default)<br>1B: Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 2     |

1. See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR/nRTP.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the LPDDR4-SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR operand, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4. There are two physical registers assigned to each bit of this MR operand, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

### 1.3.3.1. Read and Write Latencies (Frequency Ranges for RL, WL, and nWR Settings)

| Read Latency |        | Write Latency |         | nWR | nRTP | Freq. limit<br>(Greater than) | Freq. limit<br>(Same or less than) | Notes           |
|--------------|--------|---------------|---------|-----|------|-------------------------------|------------------------------------|-----------------|
| No DBI       | w/ DBI | Set "A"       | Set "B" |     |      |                               |                                    |                 |
| 6            | 6      | 4             | 4       | 6   | 8    | 10                            | 266                                | 1,2,3,4<br>,5,6 |
| 10           | 12     | 6             | 8       | 10  | 8    | 266                           | 533                                |                 |
| 14           | 16     | 8             | 12      | 16  | 8    | 533                           | 800                                |                 |
| 20           | 22     | 10            | 18      | 20  | 8    | 800                           | 1066                               |                 |
| 24           | 28     | 12            | 22      | 24  | 10   | 1066                          | 1333                               |                 |
| 28           | 32     | 14            | 26      | 30  | 12   | 1333                          | 1600                               |                 |
| 32           | 36     | 16            | 30      | 34  | 14   | 1600                          | 1866                               |                 |
| 36           | 40     | 18            | 34      | 40  | 16   | 1866                          | 2133                               |                 |
| nCK          | nCK    | nCK           | nCK     | nCK | nCK  | MHz                           | MHz                                |                 |

Notes:

1. The LPDDR4-SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3-OP[6]. When MR3-OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3-OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set "A" and Set "B" is determined by MR2-OP[6]. When MR2-OP[6]=0, then Write Latency Set "A" should be used. When MR2-OP[6]=1, then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled. It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Read burst with AP (auto-pre-charge) enabled. It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a pre-charge.

### 1.3.4. MR3 Register Information (MA[5:0] = 03H)

| OP[7]  | OP[6]  | OP[5] | OP[4] | OP[3] | OP[2] | OP[1]  | OP[0]  |
|--------|--------|-------|-------|-------|-------|--------|--------|
| DBI-WR | DBI-RD | PDDS  |       |       | PPRP  | WR-PST | PU-CAL |

| Function                              | Register Type | Operand | Data                                                                                                                            | Notes |
|---------------------------------------|---------------|---------|---------------------------------------------------------------------------------------------------------------------------------|-------|
| PU-CAL<br>(Pull-up Calibration Point) | Write only    | OP[0]   | 0B: VDDQ*0.6<br>1B: VDDQ*0.5 (default)                                                                                          | 1,4   |
| WR-PST<br>(Write Post-amble length)   |               | OP[1]   | 0B: WR Post-amble = 0.5*tCK (default)<br>1B: WR Post-amble = 1.5*tCK (Vendor Specific)                                          | 2,3,5 |
| Post Package Repair<br>Protection     |               | OP[2]   | 0B: PPR Protection Disabled (Default)<br>1B: PPR Protection Enabled                                                             | 6     |
| PDDS<br>(Pull-down Drive Strength)    |               | OP[5:3] | 000B: RFU<br>001B: RZQ/1<br>010B: RZQ/2<br>011B: RZQ/3<br>100B: RZQ/4<br>101B: RZQ/5<br>110B: RZQ/6 (default)<br>111B: Reserved | 1,2,3 |
| DBI-RD<br>(DBI-Read Enable)           |               | OP[6]   | 0B: Disabled (default)<br>1B: Enabled                                                                                           | 2,3   |
| DBI-WR<br>(DBI-WR Enable)             |               | OP[7]   | 0B: Disabled (default)<br>1B: Enabled                                                                                           | 2,3   |

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. PU-CAL setting is required as the same value for both Ch.A and Ch.B before ZQCAL start command.
5. SK hynix 8Gb LPDDR4 doesn't require 1.5\*tCK apply => 1.6GHz clock.
6. If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

### 1.3.5. MR4 Register Information (MA[5:0] = 04H)

| OP[7] | OP[6]          | OP[5] | OP[4] | OP[3]    | OP[2]        | OP[1] | OP[0] |
|-------|----------------|-------|-------|----------|--------------|-------|-------|
| TUF   | Thermal Offset |       | PPRE  | SR Abort | Refresh Rate |       |       |

| Function                                 | Register Type | Operand | Data                                                                                                                                                                                                                                                                               | Notes         |
|------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| Refresh Rate                             | Read          | OP[2:0] | 000B: SDRAM Low temperature operating limit exceeded<br>001B: 4x refresh<br>010B: 2x refresh<br>011B: 1x refresh (default)<br>100B: 0.5x refresh<br>101B: 0.25x refresh, no-rating<br>110B: 0.25x refresh, with de-rating<br>111B: SDRAM High temperature operating limit exceeded | 1,2,3,4,7,8,9 |
| Self Refresh Abort                       | Write         | OP[3]   | 0B: Disabled (default)<br>1B: Enabled                                                                                                                                                                                                                                              | 9             |
| PPRE<br>(Post-package repair entry/exit) | Write         | OP[4]   | 0B: Exit PPR mode (default)<br>1B: Enter PPR mode                                                                                                                                                                                                                                  | 5,9           |
| Thermal Offset                           | Write         | OP[6:5] | 00B: No offset, 0-5°C gradient (default)<br>01B: 5°C offset, 5-10°C gradient<br>10B: 10°C offset, 10-15°C gradient<br>11B: Reserved                                                                                                                                                |               |
| TUF<br>(Temperature Update Flag)         | Read          | OP[7]   | 0B: No change in OP[2:0] since last MR4 read (default)<br>1B: Change in OP[2:0] since last MR4 read                                                                                                                                                                                | 6,7,8         |

- The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. If OP[2]=0B, the device temperature is less or equal to 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1, the device temperature is greater than 85°C.
- At higher temperatures (>85°C), AC timing de-rating may be required. If de-rating is required the LPDDR4-SDRAM will set OP[2:0]=110B. See de-rating timing requirements in the AC Timing section.
- DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
- The device may not operate properly when OP[2:0]=000B or 111B.
- Post-package repair can be entered or exited by writing to OP[4].
- When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
- OP[7]=0 at power-up. OP[2:0] bits are undefined at power-up.
- See the section on "Temperature Sensor" for information on the recommended frequency of reading MR4.
- OP[6:3] bits are that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register

### 1.3.6. MR5 Register Information (MA[5:0] = 05H)

| OP[7]                  | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|------------------------|-------|-------|-------|-------|-------|-------|-------|
| LPDDR4 Manufacturer ID |       |       |       |       |       |       |       |

| Function               | Register Type | Operand | Data                 | Notes |
|------------------------|---------------|---------|----------------------|-------|
| LPDDR4 Manufacturer ID | Read-only     | OP[7:0] | 00000110B : SK hynix |       |

### 1.3.7. MR6 Register Information (MA[5:0] = 06H)

| OP[7]         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| Revision ID-1 |       |       |       |       |       |       |       |

| Function             | Register Type | Operand | Data                                         | Notes |
|----------------------|---------------|---------|----------------------------------------------|-------|
| LPDDR4 Revision ID-1 | Read-only     | OP[7:0] | 00000000B: A-version<br>00000001B: B-version | 1     |

1. Please contact SK hynix office for MR6 code for this device.

### 1.3.8. MR7 Register Information (MA[5:0] = 07H)

| OP[7]         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| Revision ID-2 |       |       |       |       |       |       |       |

| Function             | Register Type | Operand | Data                                         | Notes |
|----------------------|---------------|---------|----------------------------------------------|-------|
| LPDDR4 Revision ID-1 | Read-only     | OP[7:0] | 00000000B: A-version<br>00000001B: B-version | 1     |

1. Please contact SK hynix office for MR7 code for this device.

### 1.3.9. MR8 Register Information (MA[5:0] = 08H)

| OP[7]    | OP[6] | OP[5]   | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------|-------|---------|-------|-------|-------|-------|-------|
| IO Width |       | Density |       |       |       | Type  |       |

| Function | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                               | Notes |
|----------|---------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Type     | Read-only     | OP[1:0] | 00B: S16 SDRAM (16n pre-fetch)<br>01B: Low VDDQ(0.6V) Support<br>All Others: Reserved                                                                                                                                                                                                                              |       |
| Density  |               | OP[5:2] | 0000B: 4Gb per die (2Gb per channel)<br>0001B: 6Gb per die (3Gb per channel)<br>0010B: 8Gb per die (4Gb per channel)<br>0011B: 12Gb per die (6Gb per channel)<br>0100B: 16Gb per die (8Gb per channel)<br>0101B: 24Gb per die (12Gb per channel)<br>0110B: 32Gb per die (16Gb per channel)<br>All Others: Reserved |       |
| IO Width |               | OP[7:6] | 00B: x16 (per channel)<br>All Others: Reserved                                                                                                                                                                                                                                                                     |       |

### 1.3.10. MR9 Register Information (MA[5:0] = 09H)

| OP[7]                         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Vendor Specific Test Register |       |       |       |       |       |       |       |

- Only 00H should be written to this register.

### 1.3.11. MR10 Register Information (MA[5:0] = 0AH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0]    |
|-------|-------|-------|-------|-------|-------|-------|----------|
| RFU   |       |       |       |       |       |       | ZQ Reset |

| Function | Register Type | Operand | Data                                           | Notes |
|----------|---------------|---------|------------------------------------------------|-------|
| ZQ Reset | Write-only    | OP[0]   | 0B: Normal Operation (Default)<br>1B: ZQ Reset | 1,2   |

- See the AC Timing tables for calibration latency and timing
- If the ZQ-pin is connected to VDDQ through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to VSS, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

### 1.3.12. MR11 Register Information (MA[5:0] = 0BH)

| OP[7]     | OP[6]  | OP[5] | OP[4] | OP[3]     | OP[2]  | OP[1] | OP[0] |
|-----------|--------|-------|-------|-----------|--------|-------|-------|
| DQ ODT-nt | CA ODT |       |       | DQ ODT-nt | DQ ODT |       |       |

| Function                                       | Register Type | Operand | Data                                                                                                                                   | Notes   |
|------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------|---------|
| DQ ODT<br>(DQ Bus Receiver On-Die-Termination) | Write-only    | OP[2:0] | 000B: Disable (Default)<br>001B: RZQ/1<br>010B: RZQ/2<br>011B: RZQ/3<br>100B: RZQ/4<br>101B: RZQ/5<br>110B: RZQ/6<br>111B: RFU         | 1,2,3   |
| DQ ODTnt                                       |               | OP[7,3] | 00B: Disable (Default)<br>01B: RZQ/3<br>10B: RZQ/5<br>11B: RZQ/6                                                                       | 1,2,3,4 |
| CA ODT<br>(CA Bus Receiver On-Die-Termination) |               | OP[6:4] | 0000B: Disable (Default)<br>0001B: RZQ/1<br>0010B: RZQ/2<br>0011B: RZQ/3<br>0100B: RZQ/4<br>0101B: RZQ/5<br>0110B: RZQ/6<br>0111B: RFU | 1,2,3   |

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. ODT for non-target DRAM is optional.

### 1.3.13. MR12 Register Information (MA[5:0] = 0CH)

| OP[7]    | OP[6] | OP[5]    | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------|-------|----------|-------|-------|-------|-------|-------|
| CBT Mode | VR-CA | VREF(ca) |       |       |       |       |       |

| Function                       | Register Type | Operand | Data                                                                       | Notes         |
|--------------------------------|---------------|---------|----------------------------------------------------------------------------|---------------|
| VREF(ca)<br>(VREF(ca) Setting) | Read/Write    | OP[5:0] | 000000B:<br>-- Thru --<br>110010B: See table below<br>All Others: Reserved | 1,2,3,5<br>,6 |
| VREF(ca) Range                 |               | OP[6]   | 0B: VREF(ca) Range[0] enabled<br>1B: VREF(ca) Range[1] enabled (default)   | 1,2,4,5<br>,6 |
| CBT Mode                       |               | OP[7]   | 0B: Mode1 (Default)<br>1B: Mode2                                           | 7             |

1. This register controls the VREF(ca) levels for Frequency-Set-Point[1:0]. Values from either VR(ca)[0] or VR(ca)[1] may be selected by setting OP[6] appropriately.
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(ca) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(ca) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(ca) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal VREF(ca) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(ca) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
7. This field (MR12 OP[7]) is only available in Byte-mode Package and its mixed package (x8 2ch device)



**Table - VREF Settings for Range[0] and Range[1]**

| Function                     | Operand | Range[0] Values (% of VDDQ) |                      | Range[1] Values (% of VDDQ) |                      | Notes |
|------------------------------|---------|-----------------------------|----------------------|-----------------------------|----------------------|-------|
| VREF<br>Settings<br>for MR12 | OP[5:0] | 000000B: 15.0%              | 011010B: 30.5%       | 000000B: 32.9%              | 011010B: 48.5%       | 1,2,3 |
|                              |         | 000001B: 15.6%              | 011011B: 31.1%       | 000001B: 33.5%              | 011011B: 49.1%       |       |
|                              |         | 000010B: 16.2%              | 011100B: 31.7%       | 000010B: 34.1%              | 011100B: 49.7%       |       |
|                              |         | 000011B: 16.8%              | 011101B: 32.3%       | 000011B: 34.7%              | 011101B: 50.3%       |       |
|                              |         | 000100B: 17.4%              | 011110B: 32.9%       | 000100B: 35.3%              | 011110B: 50.9%       |       |
|                              |         | 000101B: 18.0%              | 011111B: 33.5%       | 000101B: 35.9%              | 011111B: 51.5%       |       |
|                              |         | 000110B: 18.6%              | 100000B: 34.1%       | 000110B: 36.5%              | 100000B: 52.1%       |       |
|                              |         | 000111B: 19.2%              | 100001B: 34.7%       | 000111B: 37.1%              | 100001B: 52.7%       |       |
|                              |         | 001000B: 19.8%              | 100010B: 35.3%       | 001000B: 37.7%              | 100010B: 53.3%       |       |
|                              |         | 001001B: 20.4%              | 100011B: 35.9%       | 001001B: 38.3%              | 100011B: 53.9%       |       |
|                              |         | 001010B: 21.0%              | 100100B: 36.5%       | 001010B: 38.9%              | 100100B: 54.5%       |       |
|                              |         | 001011B: 21.6%              | 100101B: 37.1%       | 001011B: 39.5%              | 100101B: 55.1%       |       |
|                              |         | 001100B: 22.2%              | 100110B: 37.7%       | 001100B: 40.1%              | 100110B: 55.7%       |       |
|                              |         | 001101B: 22.8%              | 100111B: 38.3%       | 001101B: 40.7%              | 100111B: 56.3%       |       |
|                              |         | 001110B: 23.4%              | 101000B: 38.9%       | 001110B: 41.3%              | 101000B: 56.9%       |       |
|                              |         | 001111B: 24.0%              | 101001B: 39.5%       | 001111B: 41.9%              | 101001B: 57.5%       |       |
|                              |         | 010000B: 24.6%              | 101010B: 40.1%       | 010000B: 42.5%              | 101010B: 58.1%       |       |
|                              |         | 010001B: 25.1%              | 101011B: 40.7%       | 010001B: 43.1%              | 101011B: 58.7%       |       |
|                              |         | 010010B: 25.7%              | 101100B: 41.3%       | 010010B: 43.7%              | 101100B: 59.3%       |       |
|                              |         | 010011B: 26.3%              | 101101B: 41.9%       | 010011B: 44.3%              | 101101B: 59.9%       |       |
|                              |         | 010100B: 26.9%              | 101110B: 42.5%       | 010100B: 44.9%              | 101110B: 60.5%       |       |
|                              |         | 010101B: 27.5%              | 101111B: 43.1%       | 010101B: 45.5%              | 101111B: 61.1%       |       |
|                              |         | 010110B: 28.1%              | 110000B: 43.7%       | 010110B: 46.1%              | 110000B: 61.7%       |       |
|                              |         | 010111B: 28.7%              | 110001B: 44.3%       | 010111B: 46.7%              | 110001B: 62.3%       |       |
|                              |         | 011000B: 29.3%              | 110010B: 44.9%       | 011000B: 47.3%              | 110010B: 62.9%       |       |
|                              |         | 011001B: 29.9%              | All Others: Reserved | 011001B: 47.9%              | All Others: Reserved |       |

1. These values may be used for MR12 OP[5:0] to set the VREF(ca) levels in the LPDDR4-SDRAM.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

### 1.3.14. MR13 Register Information (MA[5:0] = 0DH)

| OP[7]  | OP[6]  | OP[5] | OP[4] | OP[3] | OP[2] | OP[1]   | OP[0] |
|--------|--------|-------|-------|-------|-------|---------|-------|
| FSP-OP | FSP-WR | DMD   | RRO   | VRCG  | VRO   | RPRE-TR | CBT   |

| Function                                       | Register Type | Operand | Data                                                                                                     | Notes |
|------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------|-------|
| CBT<br>(Command Bus Training)                  | Write         | OP[0]   | 0B: Normal Operation (default)<br>1B: Command Bus Training mode enabled                                  | 1     |
| RPRE-TR<br>(Read Preamble Training)            |               | OP[1]   | 0B: Normal Operation (default)<br>1B: Read Preamble Training mode enabled                                |       |
| VRO<br>(Vref Output)                           |               | OP[2]   | 0B: Normal Operation (default)<br>1B: Output the Vref(ca) value on DQ[0] and the Vref(dq) value on DQ[1] | 2     |
| VRCG<br>(VREF Current Generator)               |               | OP[3]   | 0B: Normal Operation (default)<br>1B: VREF Fast Response (high current) mode                             | 3     |
| RRO<br>(Refresh Rate Option)                   |               | OP[4]   | 0B: Disable MR4 OP[2:0] (default)<br>1B: Enable MR4 OP[2:0]                                              | 4,5   |
| DMD<br>(Data Mask Disable)                     |               | OP[5]   | 0B: Data Mask Operation Enabled (default)<br>1B: Data Mask Operation Disabled                            | 6     |
| FSP-WR<br>(Frequency Set Point Write Enable)   |               | OP[6]   | 0B: Frequency-Set-Point[0] (default)<br>1B: Frequency-Set-Point[1]                                       | 7     |
| FSP-OP<br>(Frequency Set Point Operation Mode) |               | OP[7]   | 0B: Frequency-Set-Point[0] (default)<br>1B: Frequency-Set-Point[1]                                       | 8     |

1. A write to set OP[0]=1 causes the LPDDR4-SDRAM to enter the VREF(ca) training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the VREF(ca) training section for more information.
2. When set, the LPDDR4-SDRAM will output the VREF(ca) voltage on DQ[0] and the VREF(dq) voltage on DQ[1]. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels.
3. When OP[3]=1, the VREF circuit uses a high-current mode to improve VREF settling time.
4. MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4 devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), Masked Write Command is not allowed and it is illegal. See the Data Mask section for more information.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions: Vref(CA) Setting, Vref(CA) Range, Vref(DQ) Setting, Vref(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions: Vref(CA) Setting, Vref(CA) Range, Vref(DQ) Setting, Vref(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.

### 1.3.15. MR14 Register Information (MA[5:0] = 0EH)

| OP[7] | OP[6]  | OP[5]    | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|--------|----------|-------|-------|-------|-------|-------|
| RFU   | VR(dq) | VREF(dq) |       |       |       |       |       |

| Function                          | Register Type | Operand | Data                                                                       | Notes           |
|-----------------------------------|---------------|---------|----------------------------------------------------------------------------|-----------------|
| VREF(dq) Setting for Set Point[0] | Read / Write  | OP[5:0] | 000000B:<br>-- Thru --<br>110010B: See table below<br>All Others: Reserved | 1,2,3,4<br>,5,6 |
| VREF(dq) Range                    |               | OP[6]   | 0B: VREF(dq) Range[0] enabled<br>1B: VREF(dq) Range[1] enabled (default)   | 1,2,3,4<br>,5,6 |

1. This register controls the VREF(dq) levels for Frequency-Set-Point[1:0]. Values from either VR(dq)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(dq) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(dq) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(dq) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal VREF(dq) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(dq) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

**Table - VREF Settings for Range[0] and Range[1]**

| Function                     | Operand | Range[0] Values (% of VDDQ) |                      | Range[1] Values (% of VDDQ) |                      | Notes |
|------------------------------|---------|-----------------------------|----------------------|-----------------------------|----------------------|-------|
| VREF<br>Settings<br>for MR14 | OP[5:0] | 000000B: 15.0%              | 011010B: 30.5%       | 000000B: 32.9%              | 011010B: 48.5%       | 1,2,3 |
|                              |         | 000001B: 15.6%              | 011011B: 31.1%       | 000001B: 33.5%              | 011011B: 49.1%       |       |
|                              |         | 000010B: 16.2%              | 011100B: 31.7%       | 000010B: 34.1%              | 011100B: 49.7%       |       |
|                              |         | 000011B: 16.8%              | 011101B: 32.3%       | 000011B: 34.7%              | 011101B: 50.3%       |       |
|                              |         | 000100B: 17.4%              | 011110B: 32.9%       | 000100B: 35.3%              | 011110B: 50.9%       |       |
|                              |         | 000101B: 18.0%              | 011111B: 33.5%       | 000101B: 35.9%              | 011111B: 51.5%       |       |
|                              |         | 000110B: 18.6%              | 100000B: 34.1%       | 000110B: 36.5%              | 100000B: 52.1%       |       |
|                              |         | 000111B: 19.2%              | 100001B: 34.7%       | 000111B: 37.1%              | 100001B: 52.7%       |       |
|                              |         | 001000B: 19.8%              | 100010B: 35.3%       | 001000B: 37.7%              | 100010B: 53.3%       |       |
|                              |         | 001001B: 20.4%              | 100011B: 35.9%       | 001001B: 38.3%              | 100011B: 53.9%       |       |
|                              |         | 001010B: 21.0%              | 100100B: 36.5%       | 001010B: 38.9%              | 100100B: 54.5%       |       |
|                              |         | 001011B: 21.6%              | 100101B: 37.1%       | 001011B: 39.5%              | 100101B: 55.1%       |       |
|                              |         | 001100B: 22.2%              | 100110B: 37.7%       | 001100B: 40.1%              | 100110B: 55.7%       |       |
|                              |         | 001101B: 22.8%              | 100111B: 38.3%       | 001101B: 40.7%              | 100111B: 56.3%       |       |
|                              |         | 001110B: 23.4%              | 101000B: 38.9%       | 001110B: 41.3%              | 101000B: 56.9%       |       |
|                              |         | 001111B: 24.0%              | 101001B: 39.5%       | 001111B: 41.9%              | 101001B: 57.5%       |       |
|                              |         | 010000B: 24.6%              | 101010B: 40.1%       | 010000B: 42.5%              | 101010B: 58.1%       |       |
|                              |         | 010001B: 25.1%              | 101011B: 40.7%       | 010001B: 43.1%              | 101011B: 58.7%       |       |
|                              |         | 010010B: 25.7%              | 101100B: 41.3%       | 010010B: 43.7%              | 101100B: 59.3%       |       |
|                              |         | 010011B: 26.3%              | 101101B: 41.9%       | 010011B: 44.3%              | 101101B: 59.9%       |       |
|                              |         | 010100B: 26.9%              | 101110B: 42.5%       | 010100B: 44.9%              | 101110B: 60.5%       |       |
|                              |         | 010101B: 27.5%              | 101111B: 43.1%       | 010101B: 45.5%              | 101111B: 61.1%       |       |
|                              |         | 010110B: 28.1%              | 110000B: 43.7%       | 010110B: 46.1%              | 110000B: 61.7%       |       |
|                              |         | 010111B: 28.7%              | 110001B: 44.3%       | 010111B: 46.7%              | 110001B: 62.3%       |       |
|                              |         | 011000B: 29.3%              | 110010B: 44.9%       | 011000B: 47.3%              | 110010B: 62.9%       |       |
|                              |         | 011001B: 29.9%              | All Others: Reserved | 011001B: 47.9%              | All Others: Reserved |       |

1. These values may be used for MR14 OP[5:0] to set the VREF(dq) levels in the LPDDR4-SDRAM.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

### 1.3.16. MR15 Register Information (MA[5:0] = 0FH)

| OP[7]                                         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Lower Byte Invert Register for DQ Calibration |       |       |       |       |       |       |       |

| Function                             | Register Type | Operand | Data                                                                                                                                                                                                                                                                            | Notes |
|--------------------------------------|---------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Lower Byte Invert for DQ Calibration | Write         | OP[7:0] | <p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane:</p> <p>0B: Do not invert<br/>1B: Invert the DQ Calibration patterns in MR32 and MR40</p> <p>Default value for OP[7:0]=55H</p> | 1     |

Notes:

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

**Table - MR15 Invert Register Pin Mapping**

| Pin  | DQ0 | DQ1 | DQ2 | DQ3 | DMI0      | DQ4 | DQ5 | DQ6 | DQ7 |
|------|-----|-----|-----|-----|-----------|-----|-----|-----|-----|
| MR15 | OP0 | OP1 | OP2 | OP3 | No-invert | OP4 | OP5 | OP6 | OP7 |

### 1.3.17. MR16 Register Information (MA[5:0] = 10H)

| OP[7]          | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| PASR Bank Mask |       |       |       |       |       |       |       |

| Function       | Register Type | Operand | Data                                                                                        | Notes |
|----------------|---------------|---------|---------------------------------------------------------------------------------------------|-------|
| Bank[7:0] Mask | Write-only    | OP[7:0] | <p>0B: Bank Refresh enabled (default) : Unmasked<br/>1B: Bank Refresh disabled : Masked</p> | 1     |

| OP[n] | Bank Mask | 8-Bank SDRAM |
|-------|-----------|--------------|
| 0     | xxxxxx1   | Bank 0       |
| 1     | xxxxx1x   | Bank 1       |
| 2     | xxxx1xx   | Bank 2       |
| 3     | xxx1xxx   | Bank 3       |
| 4     | xx1xxxx   | Bank 4       |
| 5     | x1xxxxx   | Bank 5       |
| 6     | 1xxxxxx   | Bank 6       |
| 7     | 1xxxxxx   | Bank 7       |

1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank masking is on a per channel basis. The two channels on the die may have different bank masking.

### 1.3.18. MR17 Register Information (MA[5:0] = 11H)

| OP[7]             | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| PASR Segment Mask |       |       |       |       |       |       |       |

| Function          | Register Type | Operand | Data                                                                  | Notes |
|-------------------|---------------|---------|-----------------------------------------------------------------------|-------|
| PASR Segment Mask | Write-only    | OP[7:0] | 0B: Segment Refresh enabled (default)<br>1B: Segment Refresh disabled | 1     |

| Seg-<br>ment | OP[n] | Seg-<br>ment<br>Mask | 4Gb                   | 6Gb                   | 8Gb                   | 12Gb                  | 16Gb                  | 24Gb    | 32Gb |
|--------------|-------|----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|---------|------|
|              |       |                      | R13:R11               | R14:R12               | R14:R12               | R15:R13               | R15:R13               | TBD     | TBD  |
|              |       |                      | R14:R12<br>(Bytemode) | R15:R13<br>(Bytemode) | R15:R13<br>(Bytemode) | R16:R14<br>(Bytemode) | R16:R14<br>(Bytemode) | TBD     | TBD  |
| 0            | 0     | xxxxxxx1             | 000B                  |                       |                       |                       |                       |         |      |
| 1            | 1     | xxxxxxx1x            | 001B                  |                       |                       |                       |                       |         |      |
| 2            | 2     | xxxxx1xx             | 010B                  |                       |                       |                       |                       |         |      |
| 3            | 3     | xxx1xxx              | 011B                  |                       |                       |                       |                       |         |      |
| 4            | 4     | xxx1xxxx             | 100B                  |                       |                       |                       |                       |         |      |
| 5            | 5     | xx1xxxxx             | 101B                  |                       |                       |                       |                       |         |      |
| 6            | 6     | x1xxxxxx             | 110B                  | Not                   | 110B                  | Not                   | 110B                  | Not     | 110B |
| 7            | 7     | 1xxxxxxx             | 111B                  | Allowed               | 111B                  | Allowed               | 111B                  | Allowed | 111B |

1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking.
3. For 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00B).

### 1.3.19. MR18 Register Information (MA[5:0] = 12H)

| OP[7]                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQS Oscillator Count - LSB |       |       |       |       |       |       |       |

| Function                                       | Register Type | Operand | Data                                | Notes |
|------------------------------------------------|---------------|---------|-------------------------------------|-------|
| DQS Oscillator<br>(WR Training DQS Oscillator) | Read-only     | OP[7:0] | 0:255 LSB DRAM DQS Oscillator Count | 1,2,3 |

1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

### 1.3.20. MR19 Register Information (MA[5:0] = 13H)

| OP[7]                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQS Oscillator Count - MSB |       |       |       |       |       |       |       |

| Function                                       | Register Type | Operand | Data                                | Notes |
|------------------------------------------------|---------------|---------|-------------------------------------|-------|
| DQS Oscillator<br>(WR Training DQS Oscillator) | Read-only     | OP[7:0] | 0:255 MSB DRAM DQS Oscillator Count | 1,2   |

- MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
- Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
- A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

### 1.3.21. MR20 Register Information (MA[5:0] = 14H)

| OP[7]                                         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Upper Byte Invert Register for DQ Calibration |       |       |       |       |       |       |       |

| Function                             | Register Type | Operand | Data                                                                                                                                                                                                                                                                             | Notes |
|--------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Upper Byte Invert for DQ Calibration | Write         | OP[7:0] | <p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane:</p> <p>0B: Do not invert<br/>1B: Invert the DQ Calibration patterns in MR32 and MR40</p> <p>Default value for OP[7:0]=55H</p> | 1,2   |

- This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
- DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
- No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

**Table - MR20 Invert Register Pin Mapping**

| Pin  | DQ8 | DQ9 | DQ10 | DQ11 | DMI1      | DQ12 | DQ13 | DQ14 | DQ15 |
|------|-----|-----|------|------|-----------|------|------|------|------|
| MR20 | OP0 | OP1 | OP2  | OP3  | No-invert | OP4  | OP5  | OP6  | OP7  |

### 1.3.22. MR21 Register Information (MA[5:0] = 15H)

| OP[7]                        | OP[6] | OP[5]               | OP[4]                        | OP[3] | OP[2] | OP[1] | OP[0] |
|------------------------------|-------|---------------------|------------------------------|-------|-------|-------|-------|
| Vendor Internal Use for Test |       | Low Speed CA Buffer | Vendor Internal Use for Test |       |       |       |       |

| Function            | Register Type | Operand | Data                                                      | Notes               |
|---------------------|---------------|---------|-----------------------------------------------------------|---------------------|
| Low Speed CA Buffer | Write Only    | OP[5]   | 0B: Normal CA buffer (Default)<br>1B: Low Speed CA buffer | 1,2,3,4,5<br>,6,7,8 |

#### Notes :

- Support for the Low Speed CA Buffer feature enabled by MR21 OP[5] is optional..
- Low Speed CA Buffer feature can enable lower power for some manufacturers' designs. The maximum clock speed for this mode is 800 MHz.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
- Low Power CA Buffer cannot be enabled prior to full device initialization (completion of Step 9 in power up sequence)
- Low speed CA buffer is allowed to be enabled only when CA ODT is disabled.
- Devices not supporting Low Speed CA Buffer will ignore MR21 OP[5] setting.
- MR21 OP bits other than OP[5] is highly recommended to set "0" since the other OP can be used with DRAM internal purpose.



### 1.3.23. MR22 Register Information (MA[5:0] = 16H)

| OP[7]                          | OP[6] | OP[5]   | OP[4]   | OP[3]   | OP[2]   | OP[1] | OP[0] |
|--------------------------------|-------|---------|---------|---------|---------|-------|-------|
| ODTD for x8_2ch<br>(Byte) mode |       | ODTD-CA | ODTE-CS | ODTE-CK | SOC ODT |       |       |

| Function                                                                   | Register Type | Operand | Data                                                                                                                                                                                                                               | Notes     |
|----------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| SoC ODT<br>(Controller ODT Value for VOH calibration)                      | Write         | OP[2:0] | 000B: Disable (Default)<br>001B: RZQ/1(illegal if MR3 OP[0]=0B)<br>010B: RZQ/2<br>011B: RZQ/3(illegal if MR3 OP[0]=0B)<br>100B: RZQ/4<br>101B: RZQ/5(illegal if MR3 OP[0]=0B)<br>110B: RZQ/6(illegal if MR3 OP[0]=0B)<br>111B: RFU | 1,2,3     |
| ODTE-CK<br>(CK ODT enabled for non-terminating rank)                       |               | OP[3]   | ODT bond PAD is ignored<br>0B: ODT-CK Enable (Default)<br>1B: ODT-CK Disable                                                                                                                                                       | 2,3,4,6,8 |
| ODTE-CS<br>(CS ODT enable for non-terminating rank)                        |               | OP[4]   | ODT bond PAD is ignored<br>0B: ODT-CS Enable (Default)<br>1B: ODT-CS Disable                                                                                                                                                       | 2,3,5,6,8 |
| ODTD-CA<br>(CA ODT termination disable)                                    |               | OP[5]   | ODT bond PAD is ignored<br>0B: ODT-CA Enable (Default)<br>1B: ODT-CA Disable                                                                                                                                                       | 2,3,6,7,8 |
| x8 ODTD[7:0]<br>(CA/CLK ODT termination disable [7:0] Lower byte select)   |               | OP[6]   | 0B: Default<br>1B: Not Allowed                                                                                                                                                                                                     |           |
| x8 ODTD[15:8]<br>(CA/CLK ODT termination disable [15:8] upper byte select) |               | OP[7]   | 0B: Default<br>1B: Not Allowed                                                                                                                                                                                                     |           |

#### Notes:

1. All values are "typical".
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. When OP[3]=1, then the CK signals will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT\_CA bond pad. This overrides the ODT\_CA bond pad for configurations where CA is shared by two or more DRAMs but CK is not, allowing CK to terminate on all DRAMs.
5. When OP[4]=1, then the CS signal will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT\_CA bond pad. This overrides the ODT\_CA bond pad for configurations where CA is shared by two or more DRAMs but CS is not, allowing CS to terminate on all DRAMs.
6. For system configurations where the CK, CS, and CA signals are shared between packages, the package design should provide for the ODT\_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared Command Bus signals.
7. When OP[5]=0, CA[5:0] will terminate when the ODT\_CA bond pad is HIGH and MR11-OP[6:4] is VALID, and disables termination when ODT\_CA is LOW or MR11-OP[6:4] is disabled. When OP[5]=1, termination for CA[5:0] is disabled, regardless of the state of the ODT\_CA bond pad or MR11-OP[6:4].
8. To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabled via MR11 OP[6:4] and also via MR22

**LPDDR4X Byte Mode Device (MR11 OP[6:4]! = 000<sub>B</sub> Case)**
**Truth Table(T=Terminated)**

| MR22  | ODTD<br>byte mode |       | ODT<br>CA | ODT<br>CS | ODT<br>CK | ODT PAD Ignore |    |    |    |     |    |
|-------|-------------------|-------|-----------|-----------|-----------|----------------|----|----|----|-----|----|
|       |                   |       |           |           |           | CA             |    | CS |    | CK  |    |
|       | OP[7]             | OP[6] | OP[5]     | OP[4]     | OP[3]     | 0B             | 1B | 0B | 1B | 0Bz | 1B |
| LPD4X | 0                 | 0     | 0         | 0         | 0         | T              | T  | T  | T  | T   | T  |
|       | 0                 | 0     | 0         | 0         | 1         | T              | T  | T  | T  |     |    |
|       | 0                 | 0     | 0         | 1         | 0         | T              | T  |    |    | T   | T  |
|       | 0                 | 0     | 0         | 1         | 1         | T              | T  |    |    |     |    |
|       | 0                 | 0     | 1         | 0         | 0         |                |    | T  | T  | T   | T  |
|       | 0                 | 0     | 1         | 0         | 1         |                |    | T  | T  |     |    |
|       | 0                 | 0     | 1         | 1         | 0         |                |    |    |    | T   | T  |
|       | 0                 | 0     | 1         | 1         | 1         |                |    |    |    |     |    |
|       | 0                 | 1     | 0         | 0         | 0         |                | T  |    | T  |     | T  |
|       | 0                 | 1     | 0         | 0         | 1         |                | T  |    | T  |     |    |
|       | 0                 | 1     | 0         | 1         | 0         |                | T  |    |    |     | T  |
|       | 0                 | 1     | 0         | 1         | 1         |                | T  |    |    |     |    |
|       | 0                 | 1     | 1         | 0         | 0         |                |    |    | T  |     | T  |
|       | 0                 | 1     | 1         | 0         | 1         |                |    |    | T  |     |    |
|       | 0                 | 1     | 1         | 1         | 0         |                |    |    |    |     | T  |
|       | 0                 | 1     | 1         | 1         | 1         |                |    |    |    |     |    |
|       | 1                 | 0     | 0         | 0         | 0         | T              |    | T  |    | T   |    |
|       | 1                 | 0     | 0         | 0         | 1         | T              |    | T  |    |     |    |
|       | 1                 | 0     | 0         | 1         | 0         | T              |    |    |    | T   |    |
|       | 1                 | 0     | 0         | 1         | 1         | T              |    |    |    |     |    |
|       | 1                 | 0     | 1         | 0         | 0         |                |    | T  |    | T   |    |
|       | 1                 | 0     | 1         | 0         | 1         |                |    | T  |    |     |    |
|       | 1                 | 0     | 1         | 1         | 0         |                |    |    |    | T   |    |
|       | 1                 | 0     | 1         | 1         | 1         |                |    |    |    |     |    |

Notes:

1. T means "terminated" condition. Blank is "un-terminated"

### 1.3.24. MR23 Register Information (MA[5:0] = 17H)

| OP[7]                           | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---------------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQS oscillator run time setting |       |       |       |       |       |       |       |

| Function                | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Notes |
|-------------------------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| DQS oscillator run time | Write         | OP[7:0] | 00000000B: DQS timer stops via MPC Command (Default)<br>00000001B: DQS timer stops automatically at 16th clocks after timer start<br>00000010B: DQS timer stops automatically at 32nd clocks after timer start<br>00000011B: DQS timer stops automatically at 48th clocks after timer start<br>00000100B: DQS timer stops automatically at 64th clocks after timer start<br>----- Thru -----<br>00111111B: DQS timer stops automatically at (63X16)th clocks after timer start<br>01XXXXXXB: DQS timer stops automatically at 2048th clocks after timer start<br>10XXXXXXB: DQS timer stops automatically at 4096th clocks after timer start<br>11XXXXXXB: DQS timer stops automatically at 8192nd clocks after timer start | 1, 2  |

Note:

1. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000B.
2. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

### 1.3.25. MR24 Register Information (MA[5:0] = 18H)

| OP[7]    | OP[6]                 | OP[5] | OP[4] | OP[3]         | OP[2]     | OP[1] | OP[0] |
|----------|-----------------------|-------|-------|---------------|-----------|-------|-------|
| TRR Mode | TRR Mode Bank Address |       |       | Unlimited MAC | MAC Value |       |       |

| Function      | Register Type | Operand | Data                                                                                                                                                                              | Notes |
|---------------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| MAC Value     | Read          | OP[2:0] | 000B: Unknown when bit OP3 =0 (note 1)<br>Unlimited when bit OP3=1 (note 2)<br>001B: 700K<br>010B: 600K<br>011B: 500K<br>100B: 400K<br>101B: 300K<br>110B: 200K<br>111B: Reserved |       |
| Unlimited MAC |               | OP[3]   | 0B: OP[2:0] define MAC value<br>1B: Unlimited MAC value (note 2, note 3)                                                                                                          |       |
| TRR Mode BAN  | Write         | OP[6:4] | 000B: Bank 0<br>001B: Bank 1<br>010B: Bank 2<br>011B: Bank 3<br>100B: Bank 4<br>101B: Bank 5<br>110B: Bank 6<br>111B: Bank 7                                                      |       |
| TRR Mode      |               | OP[7]   | 0B: Disabled (default)<br>1B: Enabled                                                                                                                                             |       |

Note:

1. Unknown means that the device is not tested for tMAC and pass/fail value in unknown.
2. There is no restriction to number of activates.
3. MR24 OP [2:0] is set to zero.

### 1.3.26. MR25 Register Information (MA[5:0] = 19H)

| OP[7]  | OP[6]  | OP[5]  | OP[4]  | OP[3]  | OP[2]  | OP[1]  | OP[0]  |
|--------|--------|--------|--------|--------|--------|--------|--------|
| Bank 7 | Bank 6 | Bank 5 | Bank 4 | Bank 3 | Bank 2 | Bank 1 | Bank 0 |

| Function     | Register Type | Operand | Data                                                               | Notes |
|--------------|---------------|---------|--------------------------------------------------------------------|-------|
| PPR Resource | Read          | OP[7:0] | 0B: PPR Resource is not available<br>1B: PPR Resource is available |       |

### 1.3.27. MR26:31 Register Information (MA[5:0] = 1AH:1FH)

| OP[7]    | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------|-------|-------|-------|-------|-------|-------|-------|
| Reserved |       |       |       |       |       |       |       |

### 1.3.28. MR32 Register Information (MA[5:0] = 20H)

| OP[7]                                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQ Calibration Pattern "A" (default = 5AH) |       |       |       |       |       |       |       |

| Function                                  | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                | Notes |
|-------------------------------------------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Return DQ Calibration Pattern MR32 + MR40 | Write         | OP[7:0] | XB: An MPC command with OP[6:0]=0000011B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "5AH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information) |       |

### 1.3.29. MR33:39 Register Information (MA[5:0] = 21H:24H)

| OP[7]      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|------------|-------|-------|-------|-------|-------|-------|-------|
| Do Not Use |       |       |       |       |       |       |       |

### 1.3.30. MR40 Register Information (MA[5:0] = 28H)

| OP[7]                                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQ Calibration Pattern "B" (default = 3CH) |       |       |       |       |       |       |       |

| Function                                  | Register Type | Operand | Data                                                                                                                                                      | Notes   |
|-------------------------------------------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| Return DQ Calibration Pattern MR32 + MR40 | Write         | OP[7:0] | XB: A default pattern "3CH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information. | 1,2,3,4 |

#### Notes:

1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111B.
2. MR15 and MR22 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR22 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

### 1.3.31. MR51 Register Information (MA[5:0] = 33H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3]              | OP[2]             | OP[1]             | OP[0] |
|-------|-------|-------|-------|--------------------|-------------------|-------------------|-------|
| RFU   |       |       |       | Single Ended Clock | Single Ended WDQS | Single Ended RDQS | RFU   |

| Function           | Register Type | Operand | Data                                                                               | Notes     |
|--------------------|---------------|---------|------------------------------------------------------------------------------------|-----------|
| Single Ended RDQS  | Write Only    | OP[1]   | 0B: Differential Read DQS (Default)<br>1B: Single Ended Read DQS                   | 1,2,3,4,5 |
| Single Ended WDQS  |               | OP[2]   | 0B: Differential Write DQS (Default)<br>1B: Single Ended Write DQS                 | 1,2,3,4,6 |
| Single Ended Clock |               | OP[3]   | 0B: Differential Clock : CK_t/CK_c (Default)<br>1B: Single Ended Clock : CK_t only | 1,2,3,4,7 |

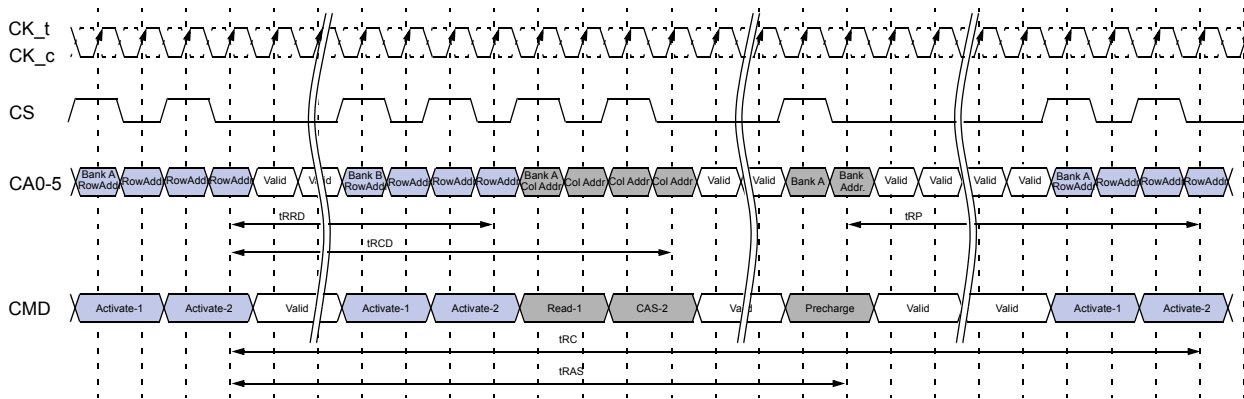
#### Notes :

1. The features described in MR51 are optional. Please check the vendor for the availability.
2. Device support for single ended mode features (MR51 OP[3:1]) is indicated in MR0 OP[5].
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
5. When single ended RDQS mode is enabled (MR51 OP[1] =1b), DRAM drives Read DQSB low or Hi-Z.
6. When single ended WDQS mode is enabled (MR51 OP[2] =1b), Write DQSB is required to be at a valid logic level. A valid Write DQSB signal will meet this requirement.
7. When single ended Clock mode is enabled (MR51 OP[3] =1b), CK\_c is required to be at a valid logic level. A valid CK\_c signal will meet this requirement.

## 2. LPDDR4 Command Definitions and Timing Diagrams

### 2.1. Activate Command

The ACTIVATE command is composed of two consecutive commands, Activate-1 command and Activate-2. Activate-1 command is issued by holding CS HIGH, CA0 HIGH and CA1 LOW at the first rising edge of the clock and Activate-2 command issued by holding CS HIGH, CA0 HIGH and CA1 HIGH at the first rising edge of the clock. The bank addresses BA0, BA1 and BA2 are used to select desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at  $t_{RCD}$  after the ACTIVATE command is issued. After a bank has been activated it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as  $t_{RAS}$  and  $t_{RP}$  respectively. The minimum time interval between ACTIVATE commands to the same bank is determined by the RAS cycle time of the device( $t_{RC}$ ). The minimum time interval between ACTIVATE commands to different banks is  $t_{RRD}$ .



**Figure - Activate Command Timing Example**

Note : A PRECHARGE command uses  $t_{RPab}$  timing for all-bank PRECHARGE and  $t_{RPpb}$  timing for single-bank PRECHARGE. In this figure,  $t_{RP}$  is used to denote either all-bank PRECHARGE or a single-bank PRECHARGE.

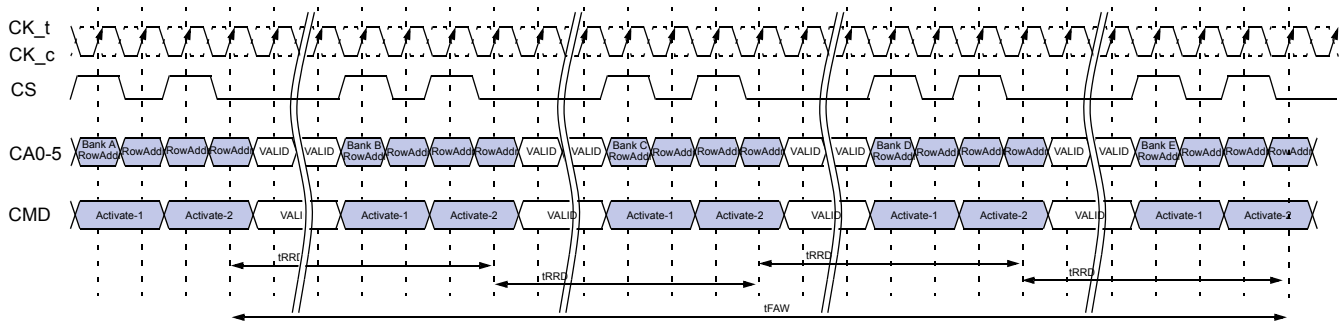
#### 2.1.1. 8-Bank Device Operation

Certain restrictions on operation of the 8-bank LPDDR4 devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

**8 bank device Sequential Bank Activation Restriction:** No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As

an example of the rolling window, if  $RU(tFAW/tCK)$  is 10 clocks, and an ACTIVATE command is issued in clock  $n$ , no more than three further ACTIVATE commands can be issued at or between clock  $n + 1$  and  $n + 9$ . REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous  $n$  clock cycles exceeds the tFAW time.

**The 8-Bank Device Precharge-All Allowance:** tRP for a PRECHARGE ALL command must equal tRPab, which is greater than tRPpb.



**Figure - tFAW Timing Example**



---

## 2.2. Read and Write Access Operations

After a bank has been activated, a read or write command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see Command Truth Table) at a rising edge of CK.

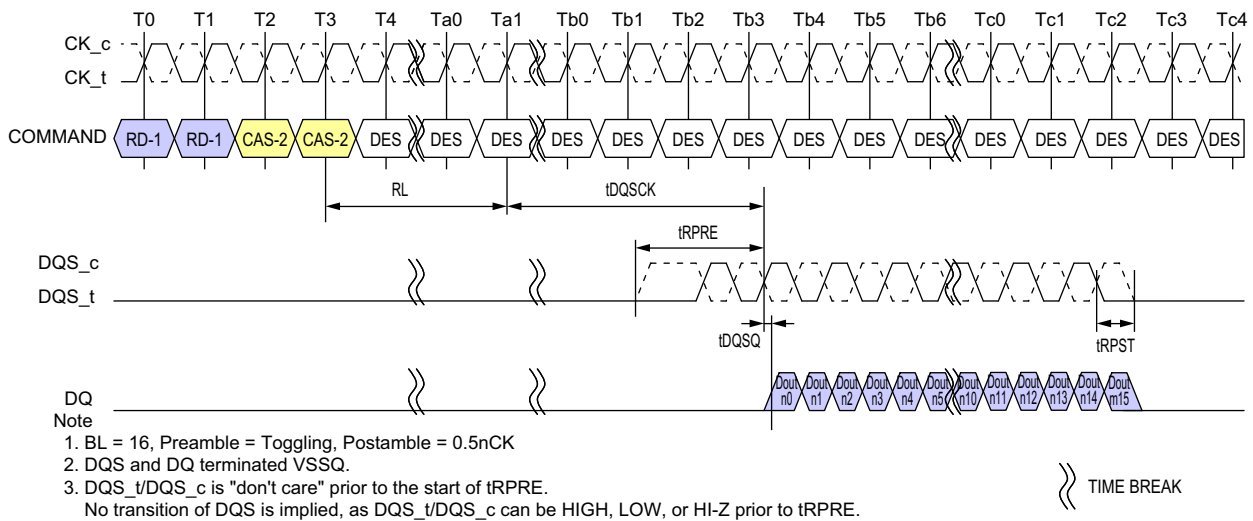
The LPDDR4-SDRAM provides a fast column access operation. A single Read or Write command will initiate a burst read or write operation, where data is transferred to/from the DRAM on successive clock cycles. Burst interrupts are not allowed, but the optimal burst length may be set on the fly (see command truth table).

### 2.3. Read Preamble and Postamble

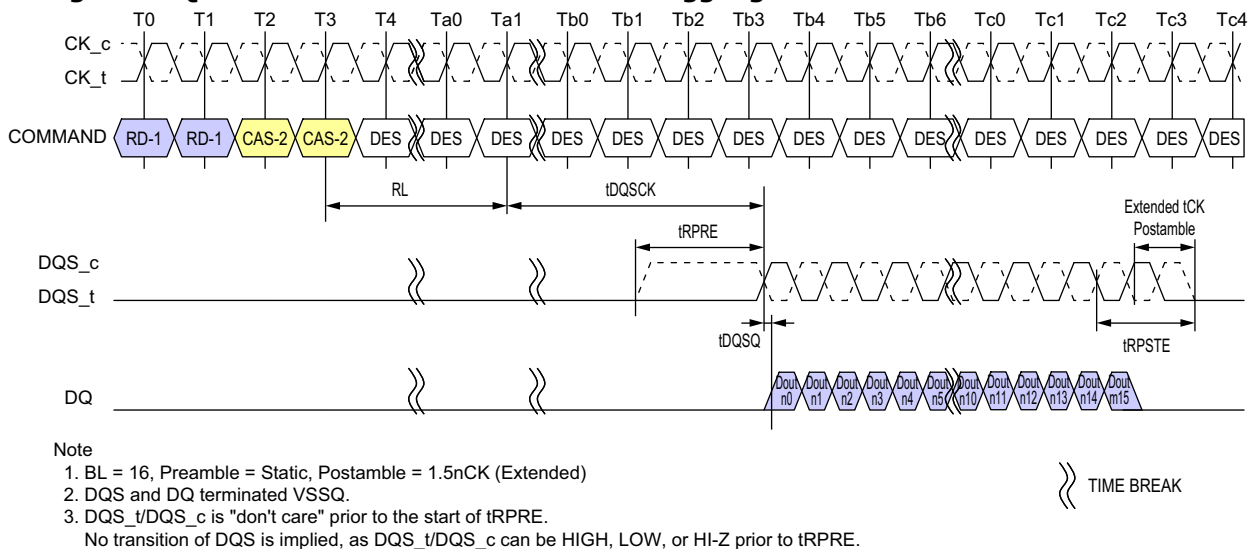
The DQS strobe for the LPDDR4-SDRAM requires a pre-amble prior to the first latching edge (the rising edge of DQS\_t with DATA "valid"), and it requires a post-ample after the last latching edge. The pre-ample and post-ample lengths are set via mode register writes (MRW).

For READ operations the pre-ample is  $2 \cdot t_{CK}$ , but the pre-ample is static (no-toggle) or toggling, selectable via mode register.

LPDDR4 will have a DQS Read post-ample of  $0.5 \cdot t_{CK}$  (or extended to  $1.5 \cdot t_{CK}$ ). Standard DQS postamble will be  $0.5 \cdot t_{CK}$  driven by the DRAM for Reads. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Read post-ample. The drawings below show examples of DQS Read post-ample for both standard (tRPST) and extended (tRPSTE) post-ample operation.



**Figure - DQS Read Preamble and Postamble: Toggling Preamble and  $0.5nCK$  Postamble**

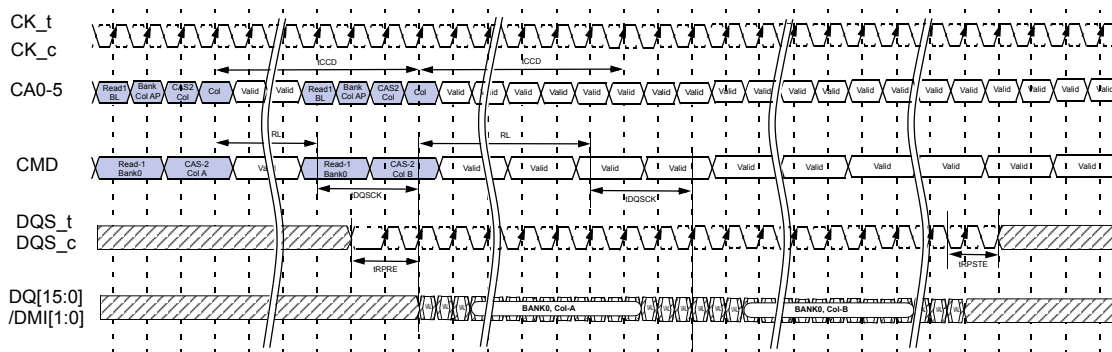


**Figure - DQS Read Preamble and Postamble: Static Preamble and  $1.5nCK$  Postamble**

## 2.4. Burst Read Operation

A burst Read command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be "0", so that the starting burst address is always a multiple of four (ex. 0x0, 0x4, 0x8, 0xC). The read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available  $RL * tCK + tDQSCK + tDQSQ$  after the rising edge of Clock that completes a read command. The data strobe output is driven tRPRE before the first valid rising strobe edge. The first data-bit of the burst is synchronized with the first valid (i.e. post-preamble) rising edge of the data strobe. Each subsequent dataout appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle postamble if the programmable post-amble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS\_t and DQS\_c.

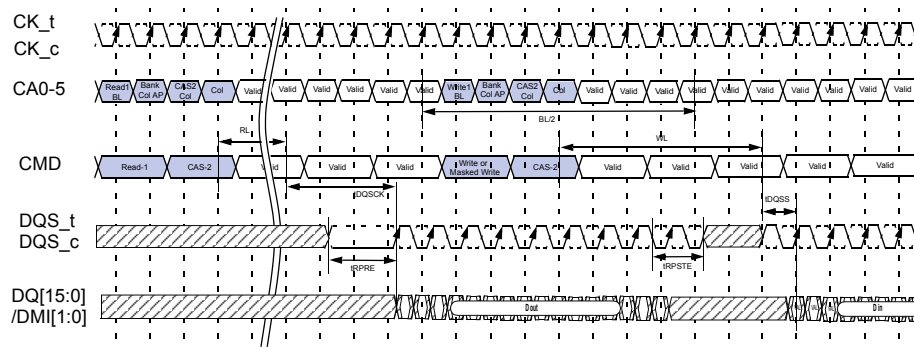
**Figure - Burst Read Timing. BL=16, Toggling tRPRE, Extended tRPST**



Notes:

1. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure - Burst Read followed by Burst Write. BL=16, Non-toggling tRPRE, Extended tRPST**



Notes:

1. DES commands are shown for ease of illustration; other commands may be valid at these times.

The minimum time from a Burst Read command to a Write or MASK WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE or MASK WRITE latency is defined with tRTW parameter and it is as following equation:

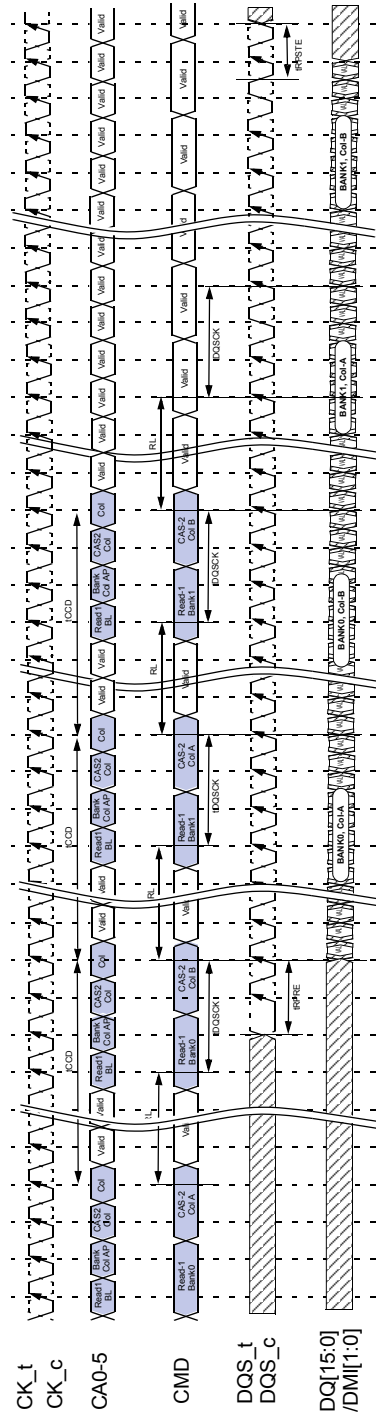
DQ ODT Disabled case; MR11 OP[2:0]=000b

$$t_{RTW} = RL + RU(t_{DQSCK(max)}/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$$

DQ ODT Enabled case; MR11 OP[2:0]≠000b

$$t_{RTW} = RL + RU(t_{DQSCK(max)}/t_{CK}) + BL/2 + RD(t_{RPST}) - ODTLon - RD(t_{ODTon,min}/t_{CK}) + 1$$

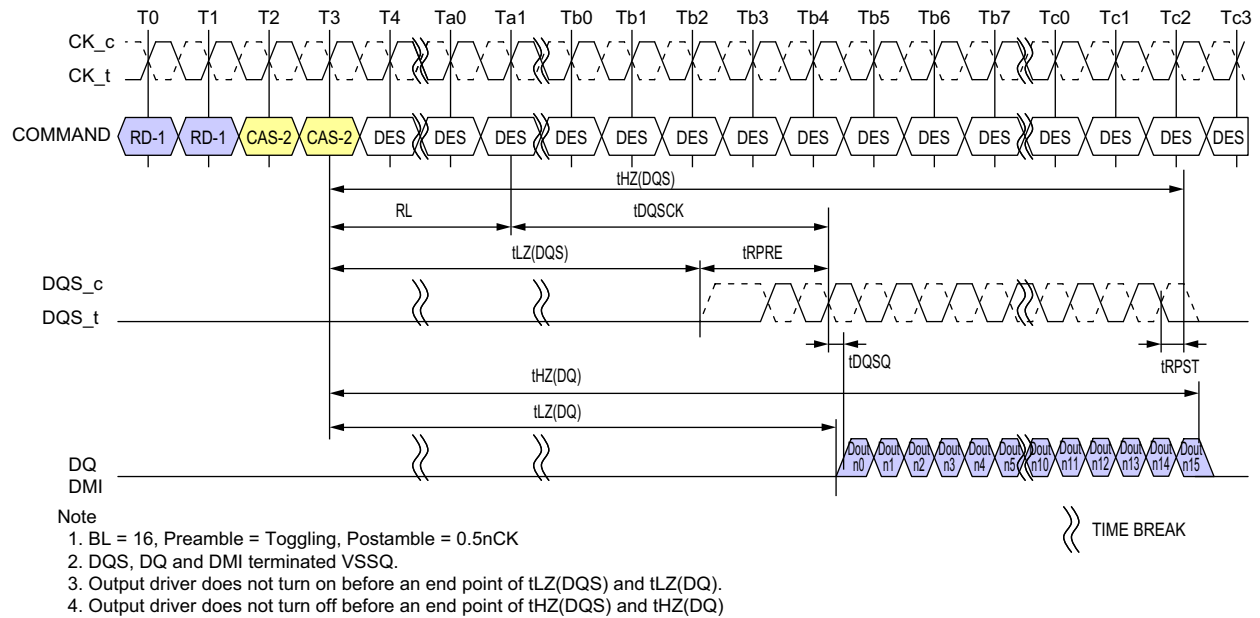
**Figure - Seamless Burst Read. BL=16, Toggling tRPRE, Extended tRPST**



The seamless Burst READ operation is supported by placing a READ command at every  $t_{CCD}(\min)$  interval for BL16 (or every  $2 \times t_{CCD}$  for BL32). The seamless Burst READ can access any open bank.

## 2.5. Read Timing

The read timing is shown in following figure:



**Figure - Read Timing**

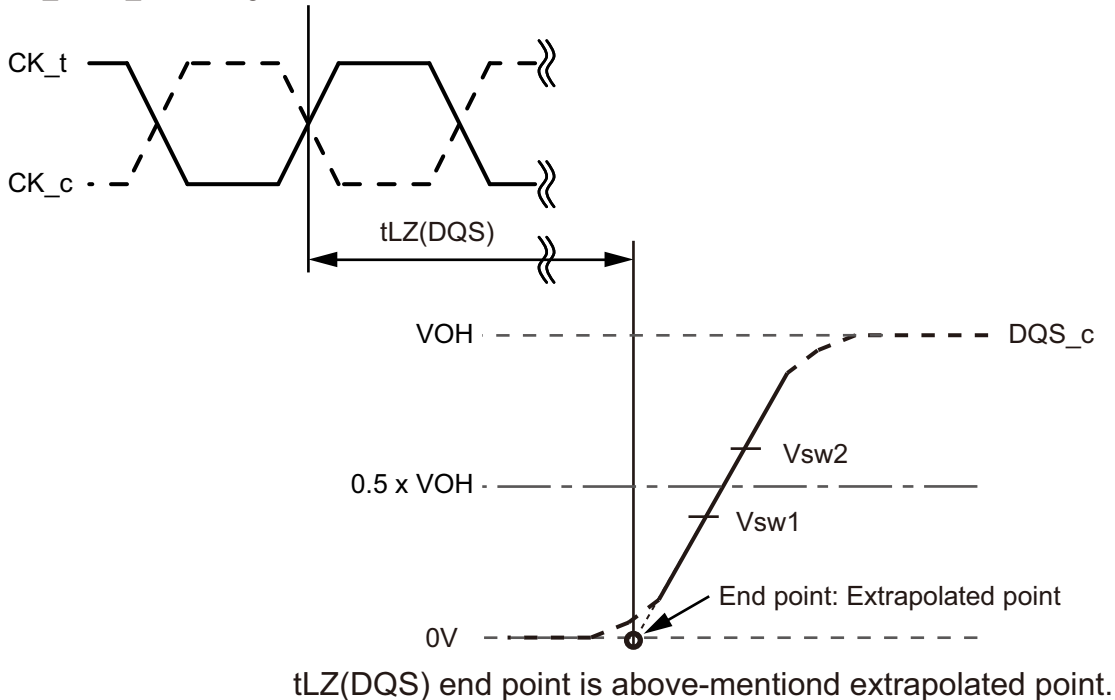
## 2.6. tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ).

This section shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.

### 2.6.1. tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment)

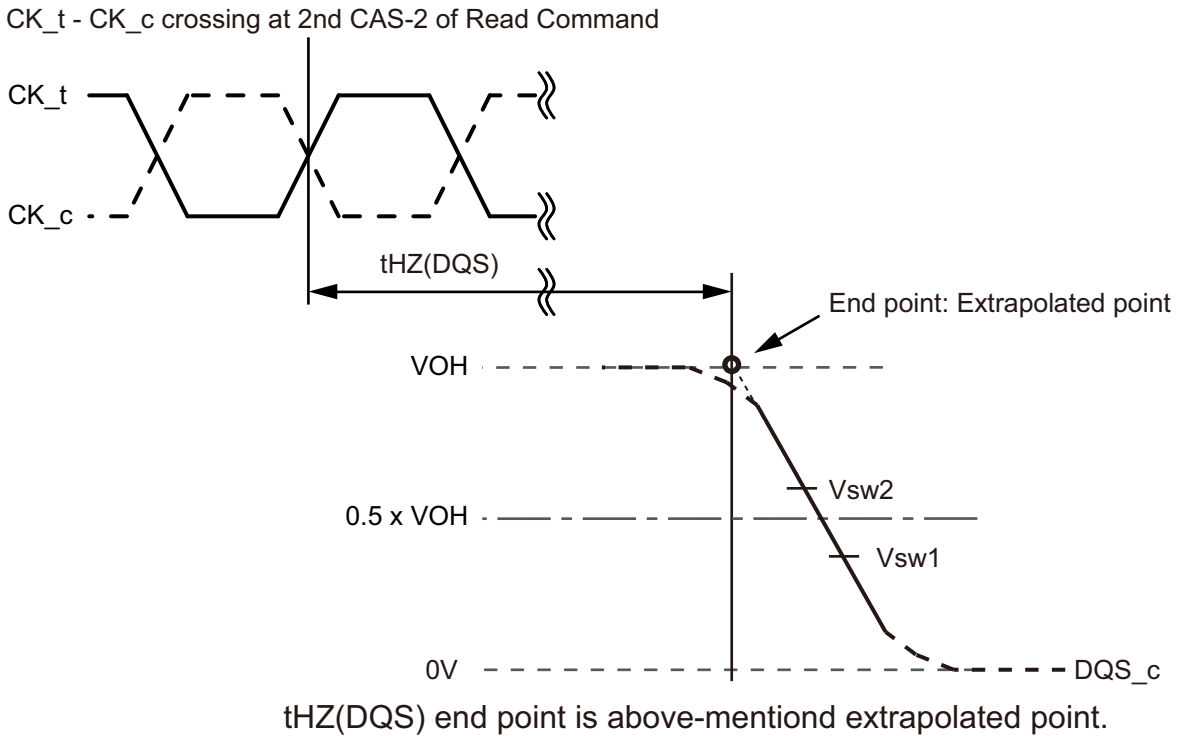
CK<sub>t</sub> - CK<sub>c</sub> crossing at 2nd CAS-2 of Read Command



Note

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3
2. Termination condition for DQS<sub>t</sub> and DQS<sub>c</sub> = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure - tLZ(DQS) method for calculating transitions and end point**



Note

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3
2. Termination condition for DQS<sub>t</sub> and DQS<sub>c</sub> = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure - tHZ(DQS) method for calculating transitions and end point**

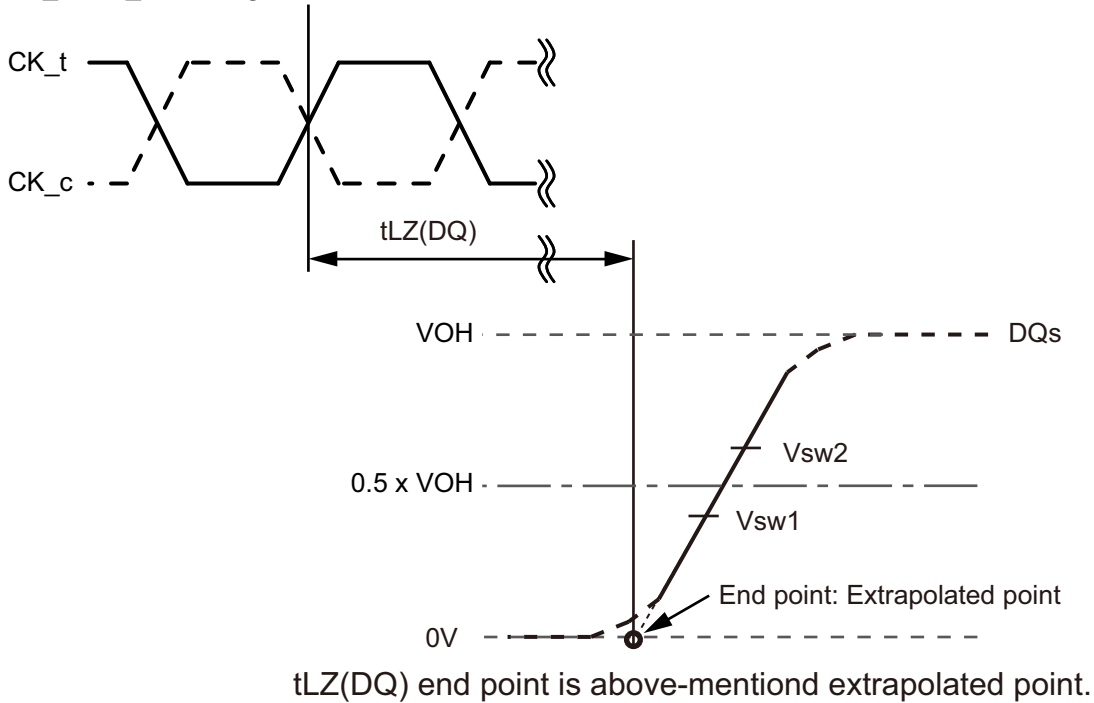
**Table - Reference voltage for tLZ(DQS), tHZ(DQS) Timing Measurements**

| Measured Parameter                                                          | Symbol   | Vsw1 [V]  | Vsw2 [V]  |
|-----------------------------------------------------------------------------|----------|-----------|-----------|
| DQS <sub>c</sub> low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>  | tLZ(DQS) | 0.4 x VOH | 0.6 x VOH |
| DQS <sub>c</sub> high impedance time from CK <sub>t</sub> , CK <sub>c</sub> | tHZ(DQS) | 0.4 x VOH | 0.6 x VOH |



## 2.6.2. tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment)

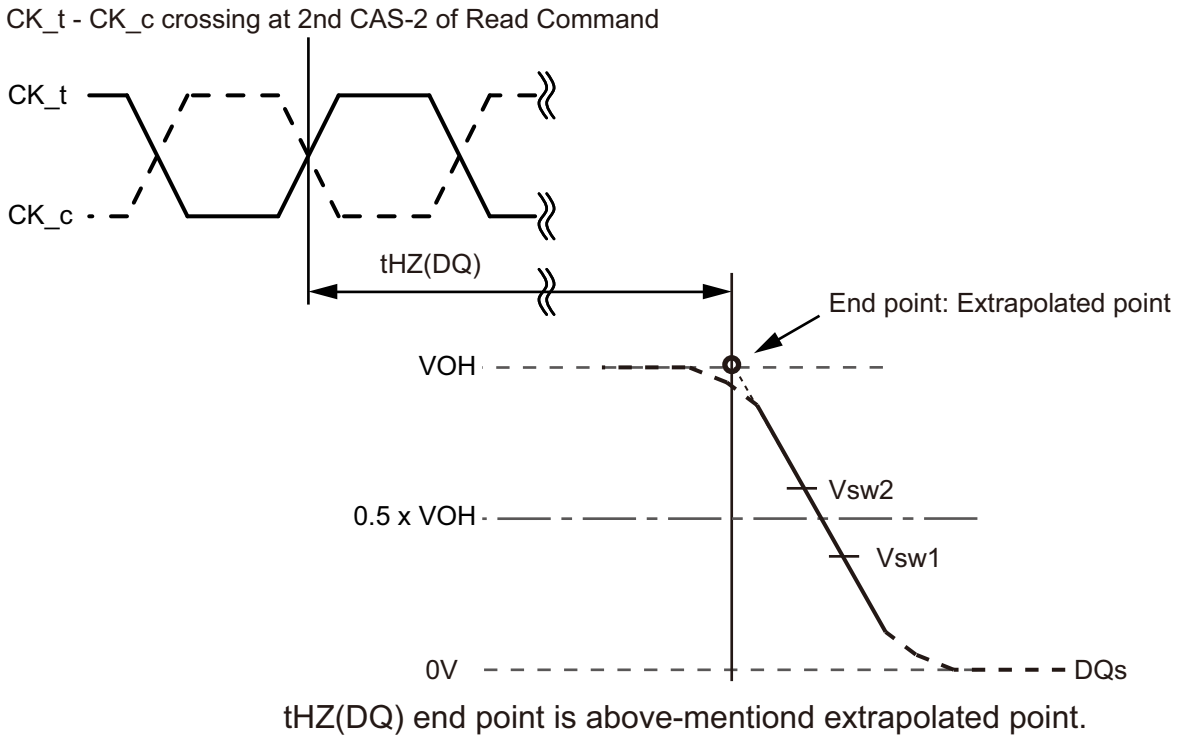
CK<sub>t</sub> - CK<sub>c</sub> crossing at 2nd CAS-2 of Read Command



Note

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

**Figure - tLZ(DQ) method for calculating transitions and end point**



Note

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure - tHZ(DQ) method for calculating transitions and end point**

**Table - Reference voltage for tLZ(DQS), tHZ(DQS) Timing Measurements**

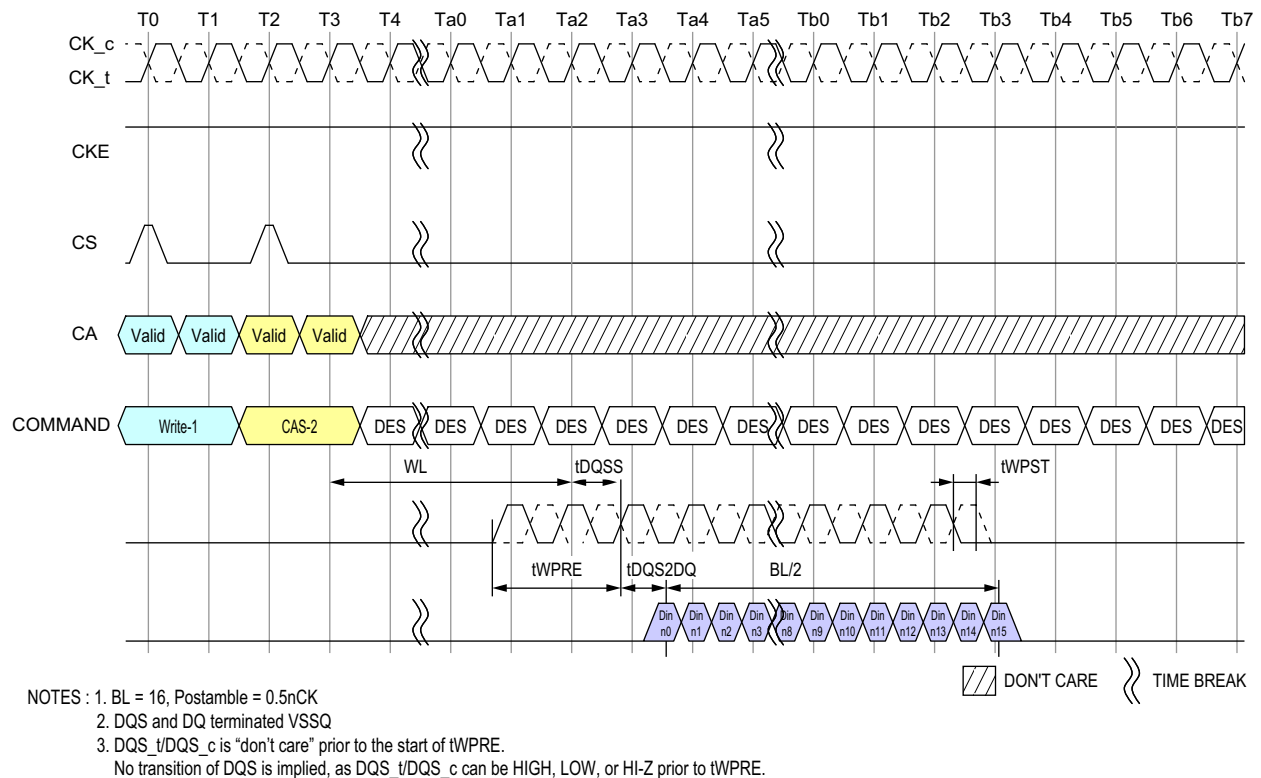
| Measured Parameter                                            | Symbol  | Vsw1 [V]  | Vsw2 [V]  |
|---------------------------------------------------------------|---------|-----------|-----------|
| DQ low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>  | tLZ(DQ) | 0.4 x VOH | 0.6 x VOH |
| DQ high impedance time from CK <sub>t</sub> , CK <sub>c</sub> | tHZ(DQ) | 0.4 x VOH | 0.6 x VOH |

## 2.7. Write Preamble and Postamble

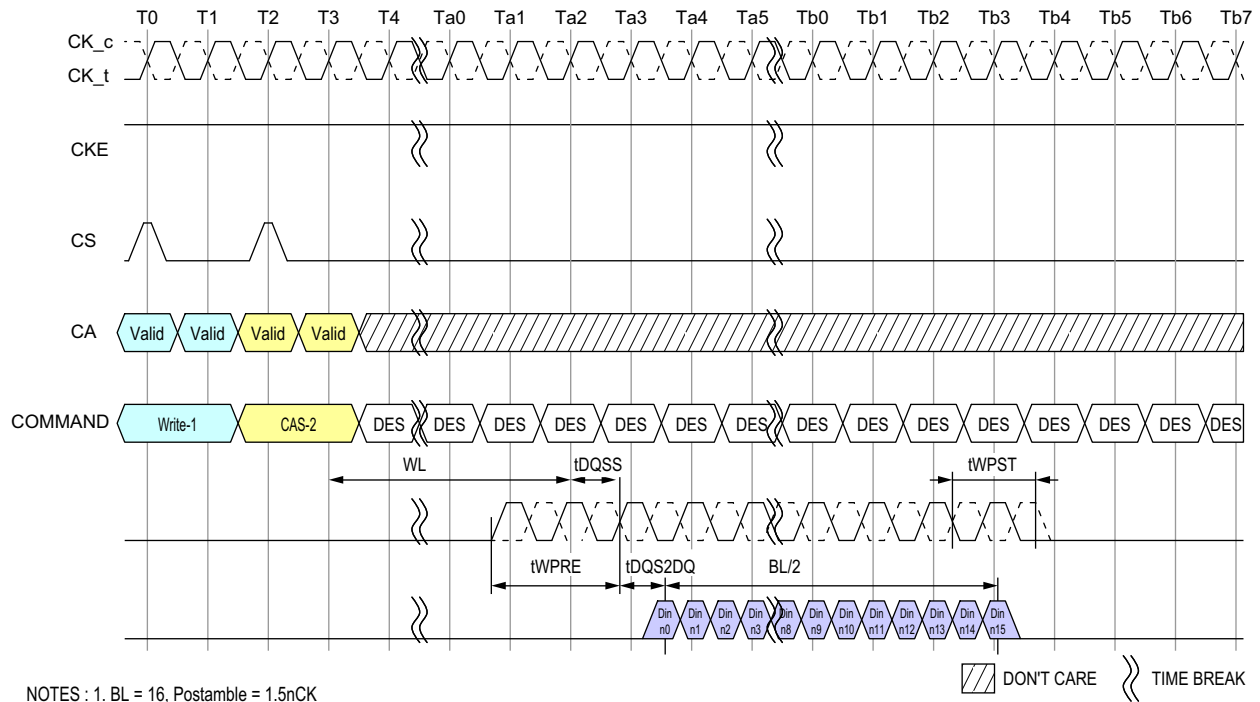
The DQS strobe for the LPDDR4-SDRAM requires a pre-amble prior to the first latching edge (the rising edge of DQS\_t with DATA "valid"), and it requires a post-ample after the last latching edge. The pre-ample and post-ample lengths are set via mode register writes (MRW).

For WRITE operations, a  $2 \cdot tCK$  pre-ample is required at all operating frequencies.

LPDDR4 will have a DQS Write post-ample of  $0.5 \cdot tCK$  or extended to  $1.5 \cdot tCK$ . Standard DQS post-ample will be  $0.5 \cdot tCK$  driven by the memory controller for Writes. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Write post-ample. The drawings below show examples of DQS Write post-ample for both standard ( $tWPST$ ) and extended ( $tWPSTE$ ) post-ample operation.



**Figure - DQS Write Preamble and Postamble;  $0.5nCK$  Postamble**



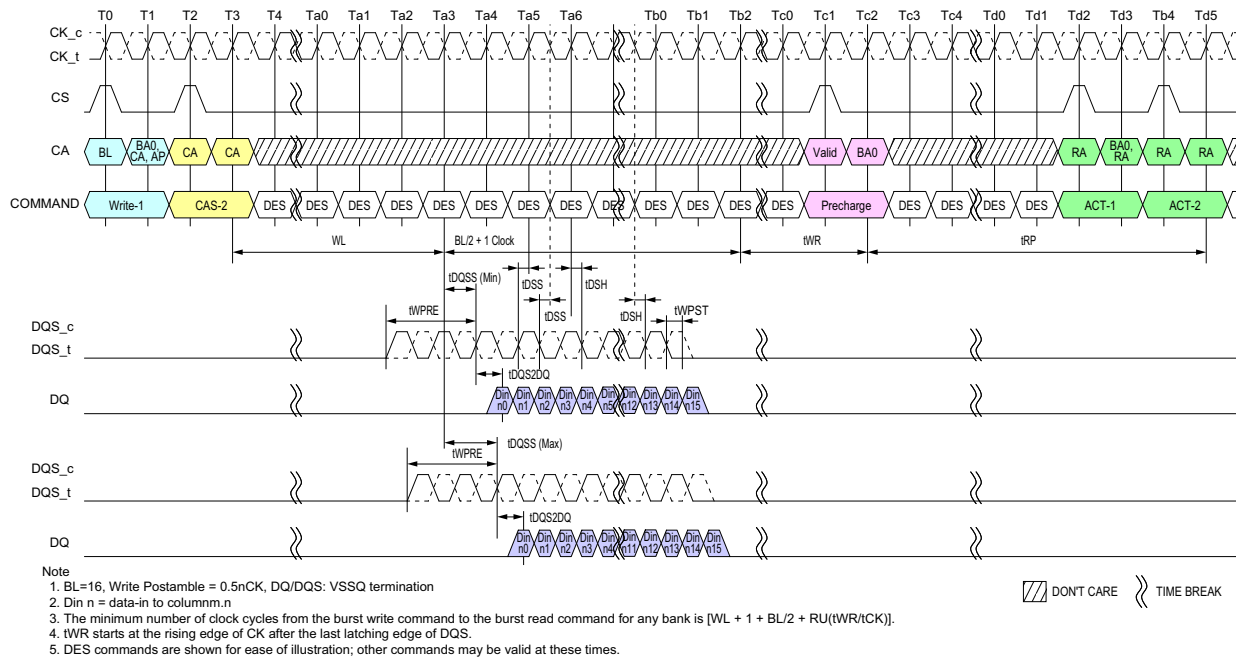
**Figure - DQS Write Preamble and Postamble: 1.5nCK Postamble**

## 2.8. Burst Write Operation

A burst WRITE command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. Column addresses C[3:2] should be driven LOW for Burst WRITE commands, and column addresses C[1:0] are not transmitted on the CA bus (and are assumed to be zero), so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the last rising edge of the clock that completes a write command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which tDQSS is measured. The first valid "latching" edge of DQS must be driven  $WL * tCK + tDQSS$  after the rising edge of Clock that completes a write command.

The LPDDR4-SDRAM uses an un-matched DQS-DQ path for lower power, so the DQS-strobe must arrive at the SDRAM ball prior to the DQ signal by the amount of tDQS2DQ. The DQS-strobe output is driven tWPRES before the first valid rising strobe edge. The tWPRES, write pre-ambler, is required to be 2 x tCK. The DQS-strobe must be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data must be held for tDIVW (data input valid window) and the DQS must be periodically trained to stay centered in the tDIVW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of DQS until the 16 or 32 bit data burst is complete. The DQS-strobe must remain active (toggling) for tWPST (WRITE post-ambler) after the completion of the burst WRITE. After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS<sub>t</sub> and DQS<sub>c</sub>.

**Figure - Burst Write Operation**

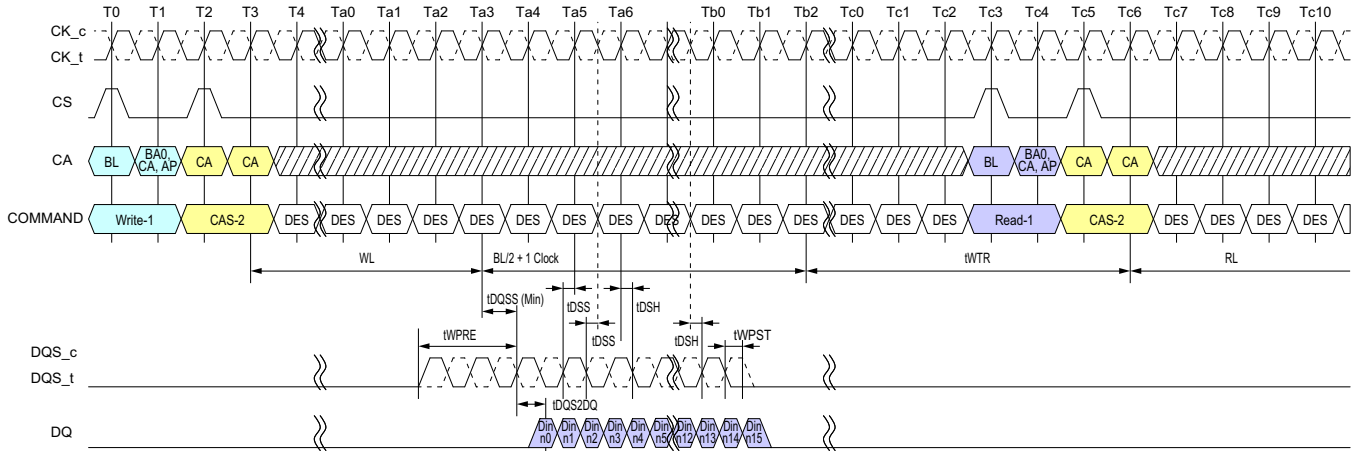


### Notes

1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to columnm.n

- The minimum number of clock cycles from the burst write command to the precharge command for any bank is  $[WL + 1 + BL/2 + RU(tWR/tCK)]$ .
- $tWR$  starts at the rising edge of CK after the last latching edge of DQS.
- DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure - Burst Write Followed by Burst Read**



**Note**

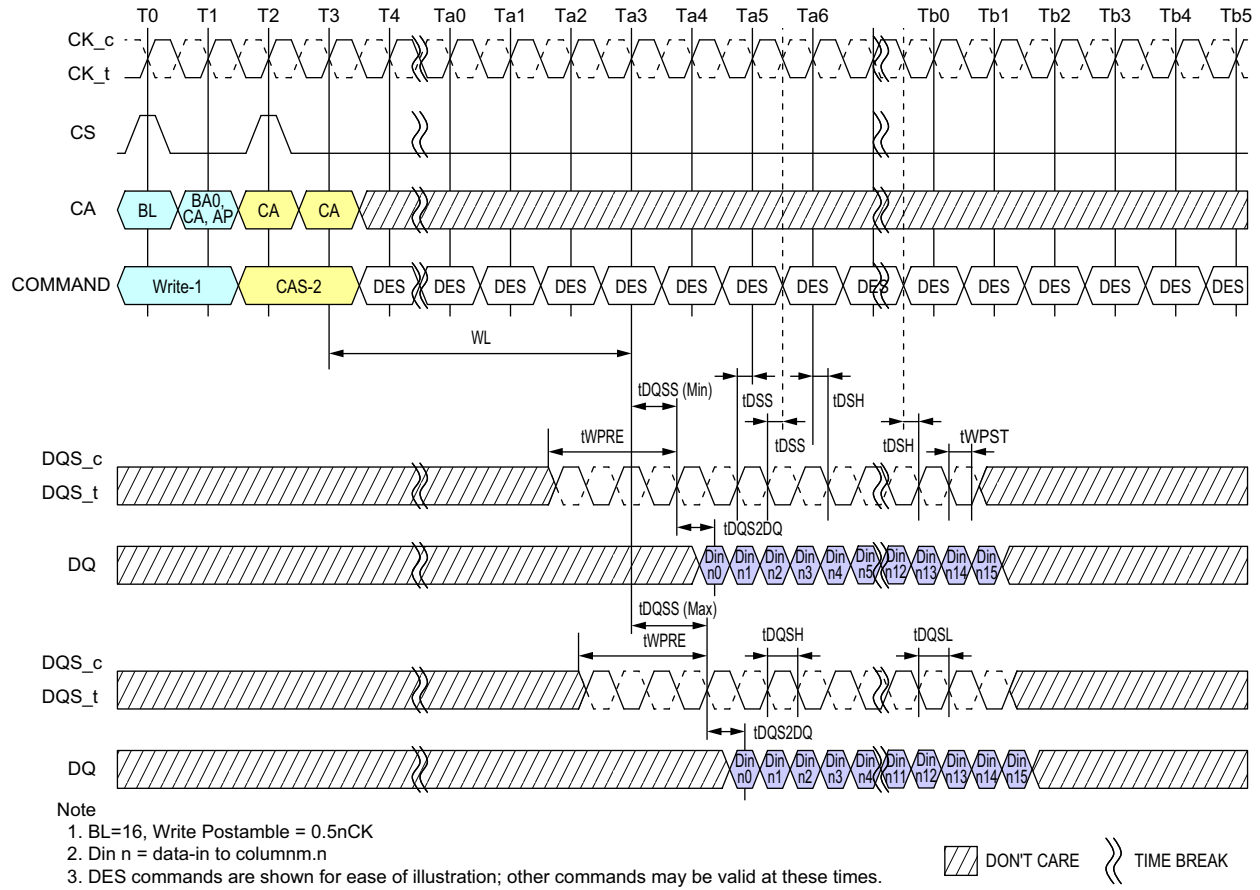
- BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
- Din n = data-in to columnm.n
- The minimum number of clock cycles from the burst write command to the burst read command for any bank is  $[WL + 1 + BL/2 + RU(tWTR/tCK)]$ .
- tWTR starts at the rising edge of CK after the last latching edge of DQS.
- DES commands are shown for ease of illustration; other commands may be valid at these times.

**Notes**

- BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
- Din n = data-in to columnm.n
- The minimum number of clock cycles from the burst write command to the burst read command for any bank is  $[WL + 1 + BL/2 + RU(tWTR/tCK)]$ .
- tWTR starts at the rising edge of CK after the last latching edge of DQS.
- DES commands are shown for ease of illustration; other commands may be valid at these times.

## 2.9. Write Timing

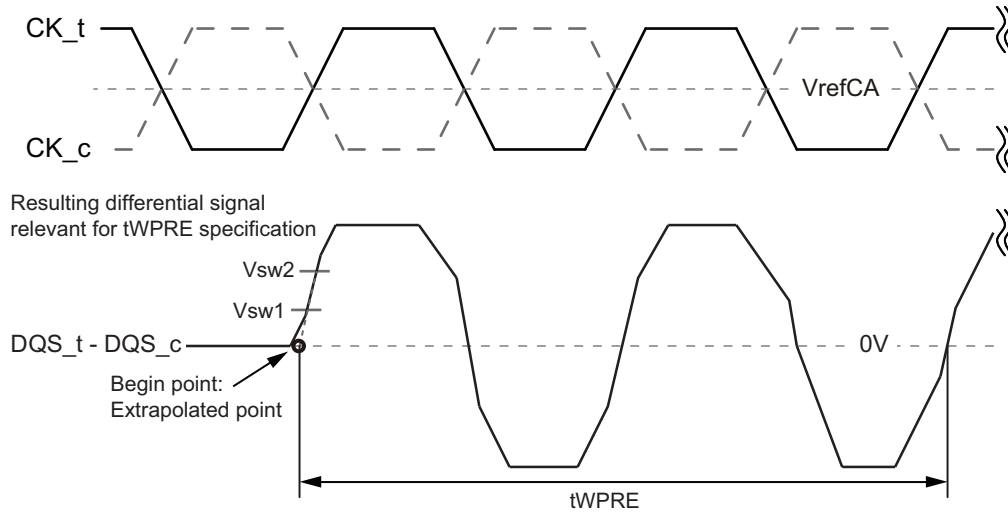
The write timing is shown in the following figure



**Figure - Write Timing**

### 2.9.1. tWPRE Calculation for ATE (Automated Test Equipment)

The method for calculating differential pulse widths for tWPRE is shown in the following figure



Note

1. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.

**Figure - Method for calculating tWPRE transitions and endpoints**

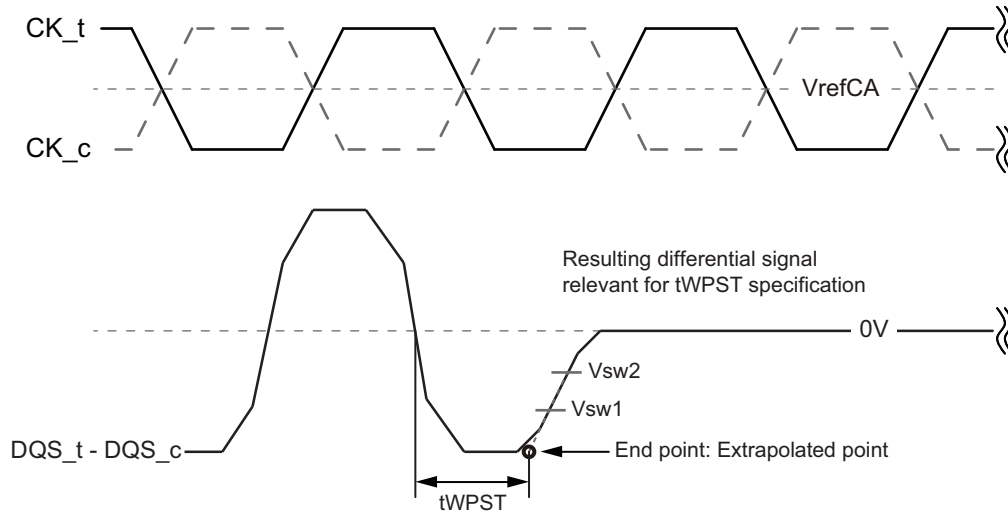
**Table - Reference Voltage for tWPRE Timing Measurements**

| Measured Parameter                       | Symbol | Vsw1 [V]      | Vsw2 [V]      |
|------------------------------------------|--------|---------------|---------------|
| DQS_t, DQS_c differential Write Preamble | tWPRE  | VIHL_AC x 0.3 | VIHL_AC x 0.7 |



### 2.9.2. tWPST Calculation for ATE (Automatic Test Equipment)

The method for calculating differential pulse widths for tWPST is shown in the following figure



Note

1. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.
2. Write Postamble: 0.5tCK
3. The method for calculating differential pulse widths for 1.5 tCK Postamble is same as 0.5 tCK Postamble.

**Figure - Method for calculating tWPST transitions and endpoints**

**Table - Reference Voltage for tWPST Timing Measurements**

| Measured Parameter                       | Symbol | Vsw1 [V]          | Vsw2 [V]          |
|------------------------------------------|--------|-------------------|-------------------|
| DQS_t, DQS_c differential Write Preamble | tWPST  | - (VIHL_AC x 0.7) | - (VIHL_AC x 0.3) |

## 2.10. Postamble and Preamble merging behavior

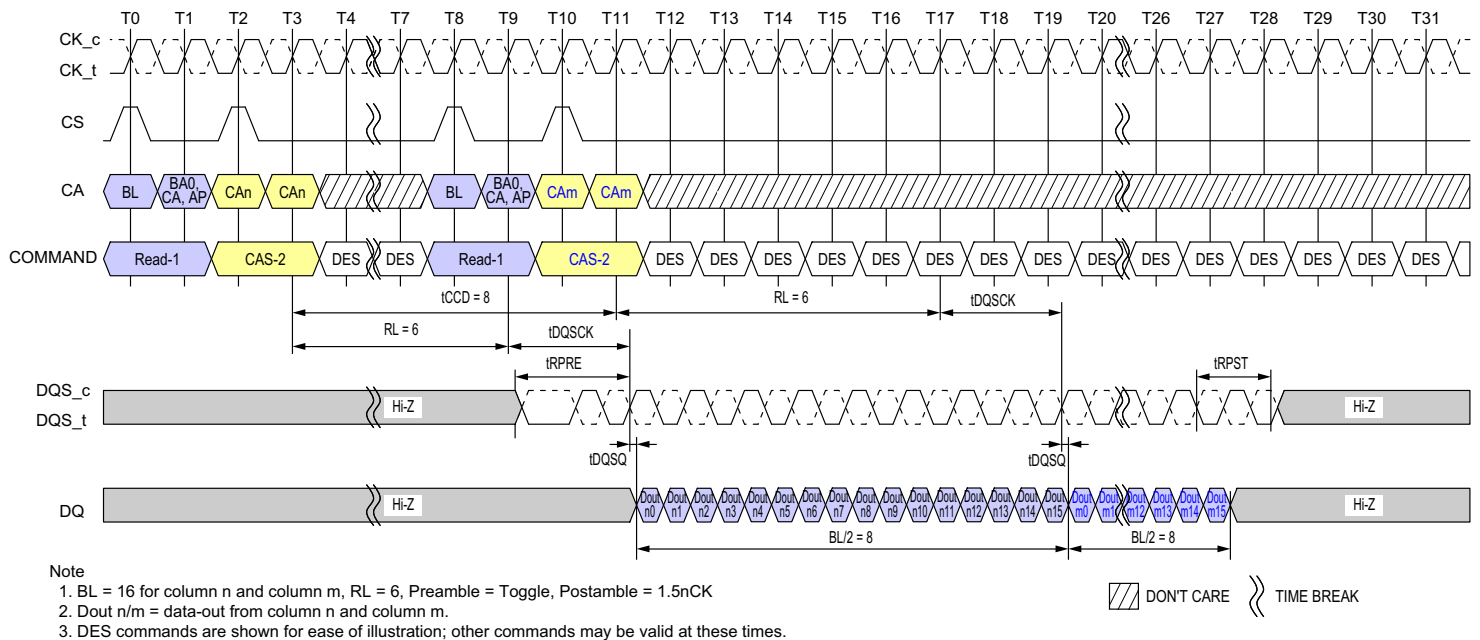
The DQS strobe for the device requires a preamble prior to the first latching edge (the rising edge of DQS\_t with data valid), and it requires a postamble after the last latching edge. The preamble and postamble options are set via Mode Register Write commands.

In Read to Read or Write to Write operations with  $t_{CCD}=BL/2$ , postamble for 1st command and preamble for 2nd command will disappear to create consecutive DQS latching edge for seamless burst operations.

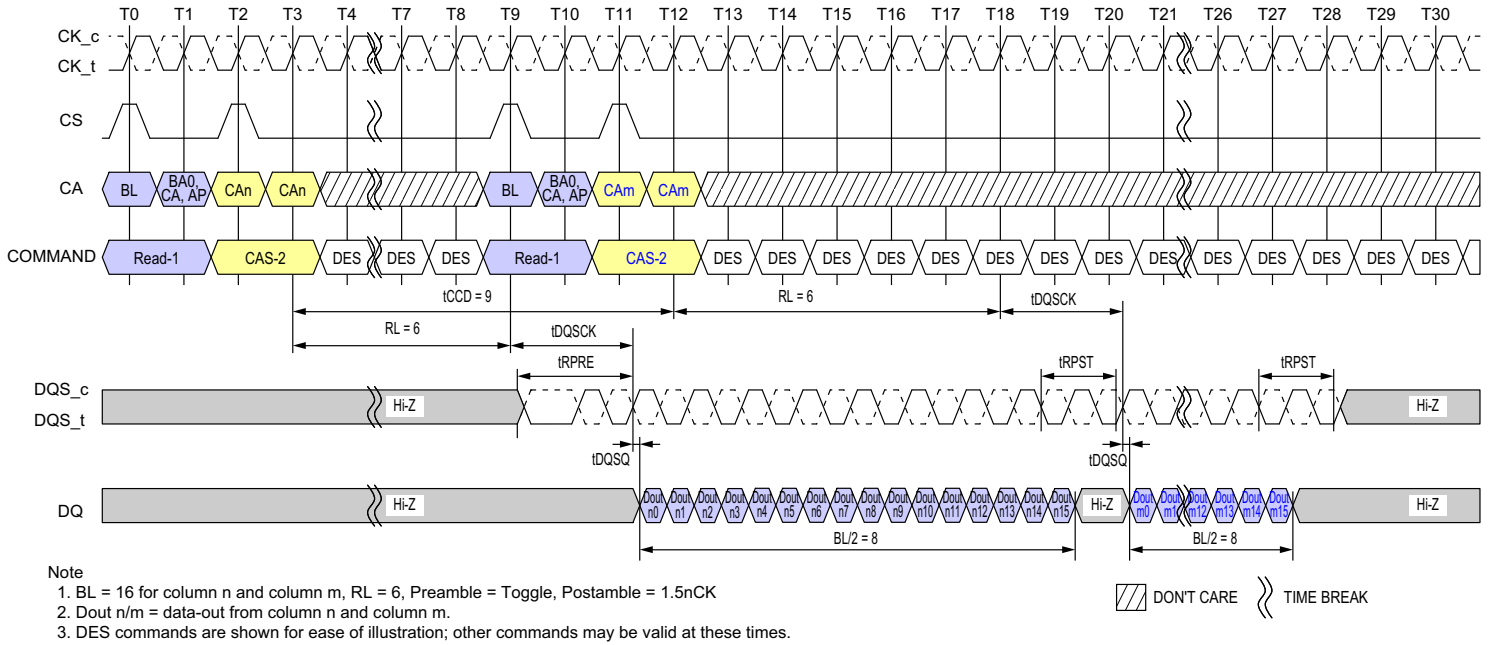
But in the case of Read to Read or Write to Write operations with command interval of  $t_{CCD}+1, t_{CCD}+2$ , etc., they will not completely disappear because it's not seamless burst operations.

Timing diagrams in this material describe Postamble and Preamble merging behavior in Read to Read or Write to Write operations with  $t_{CCD}+n$ .

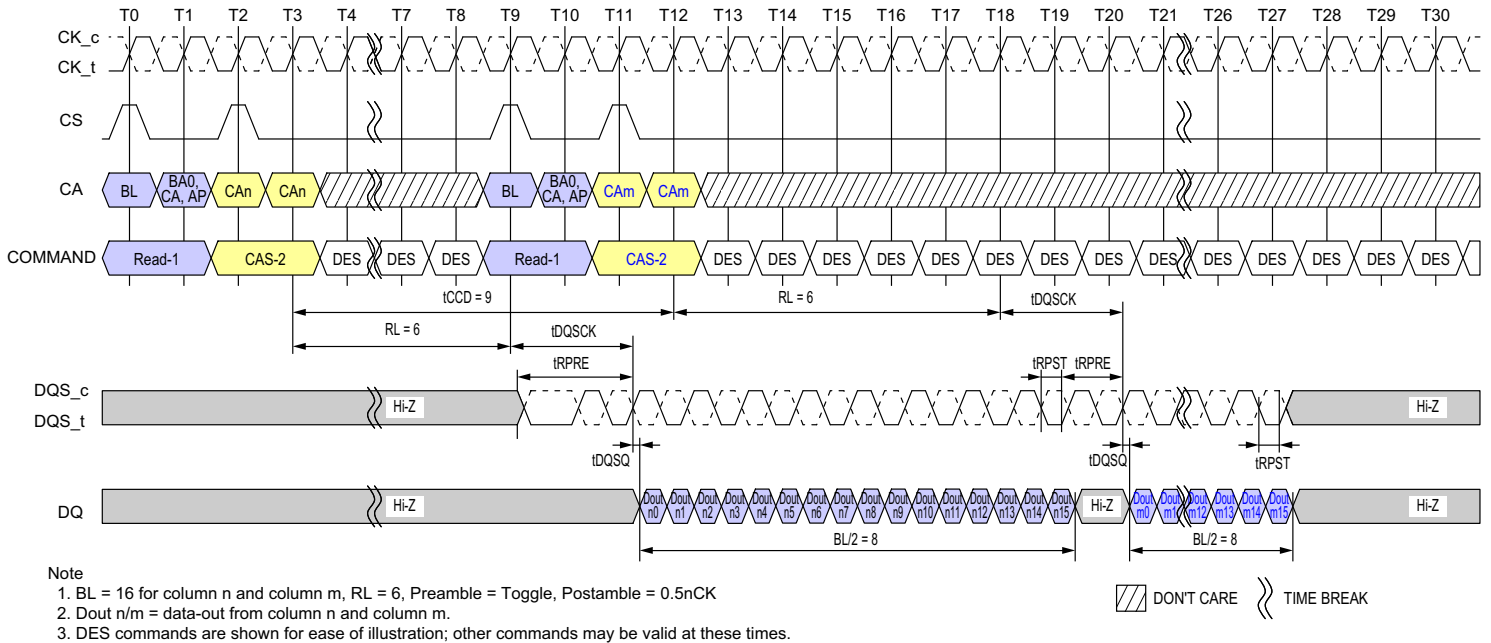
### 2.10.1. Read to Read Operation



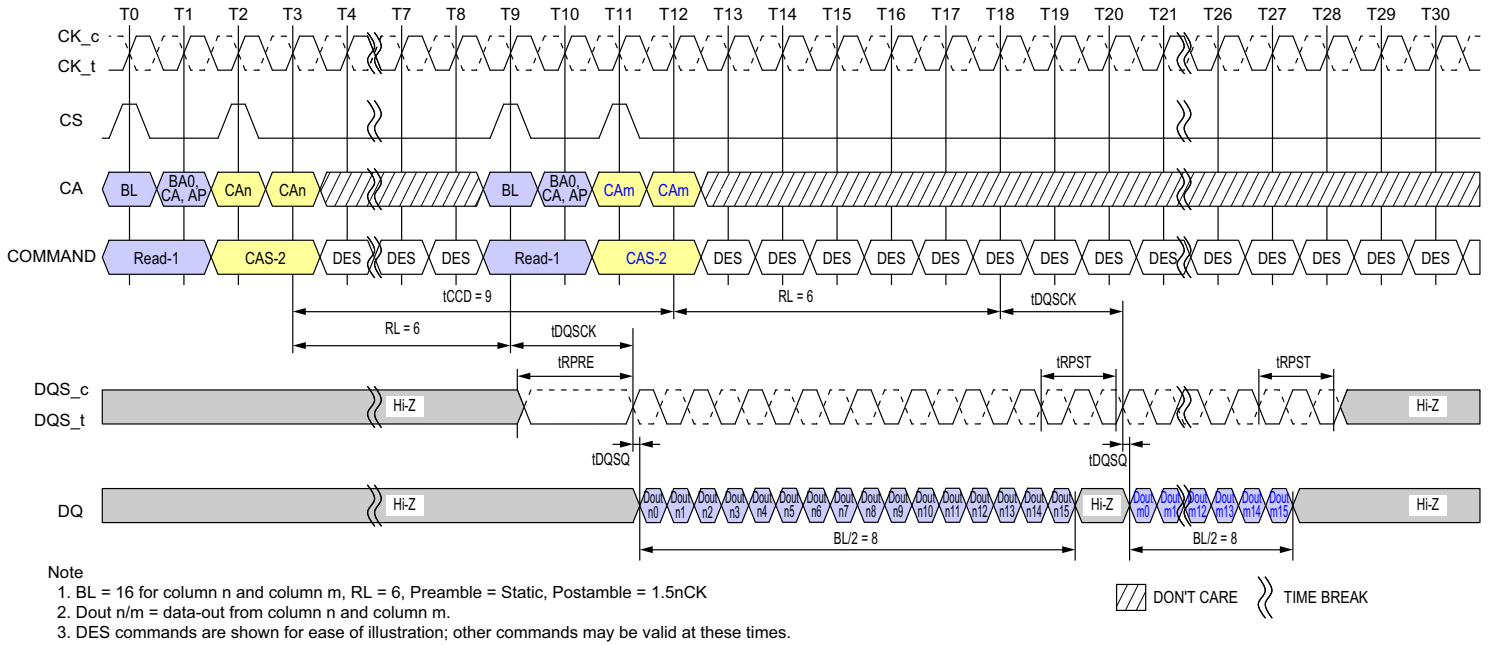
**Figure - Seamless Reads Operation:  $t_{CCD} = \text{Min}$ , Preamble = Toggle, 1.5nCK Postamble**



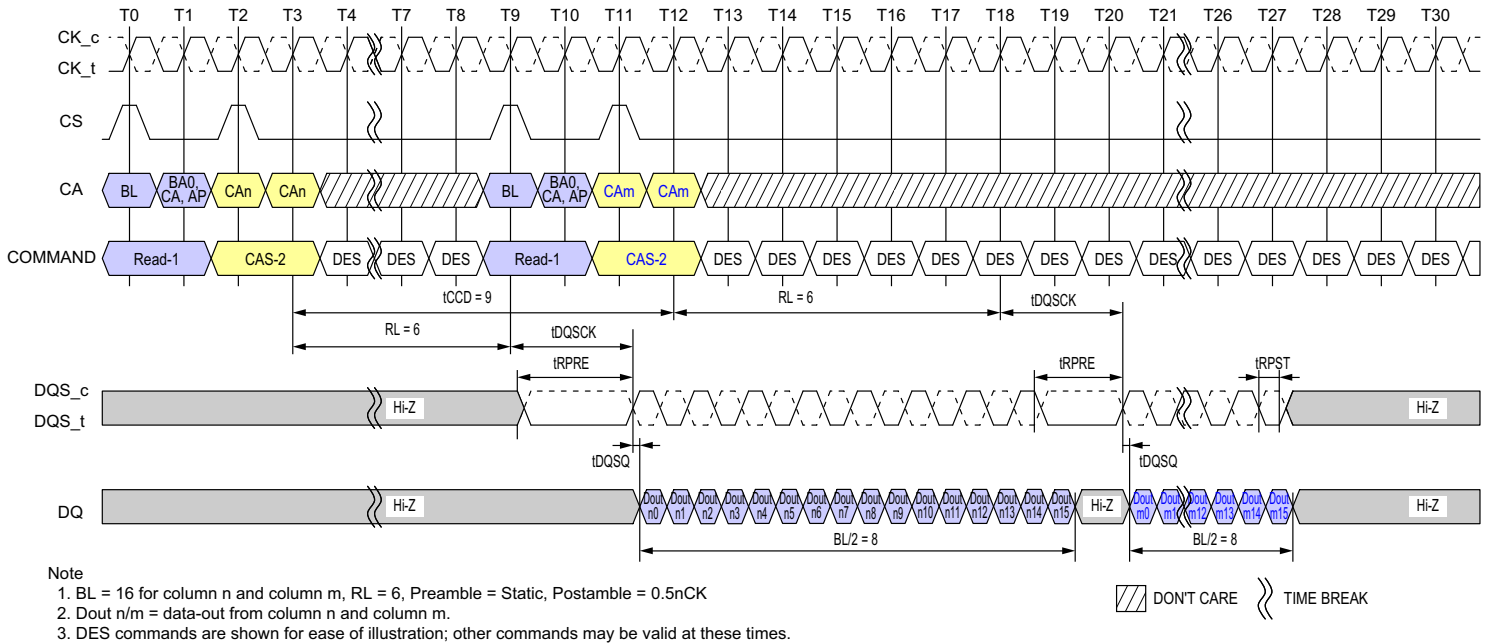
**Figure - Consecutive Reads Operation: tCCD = Min+1, Preamble=Toggle, 1.5nCK Postamble**



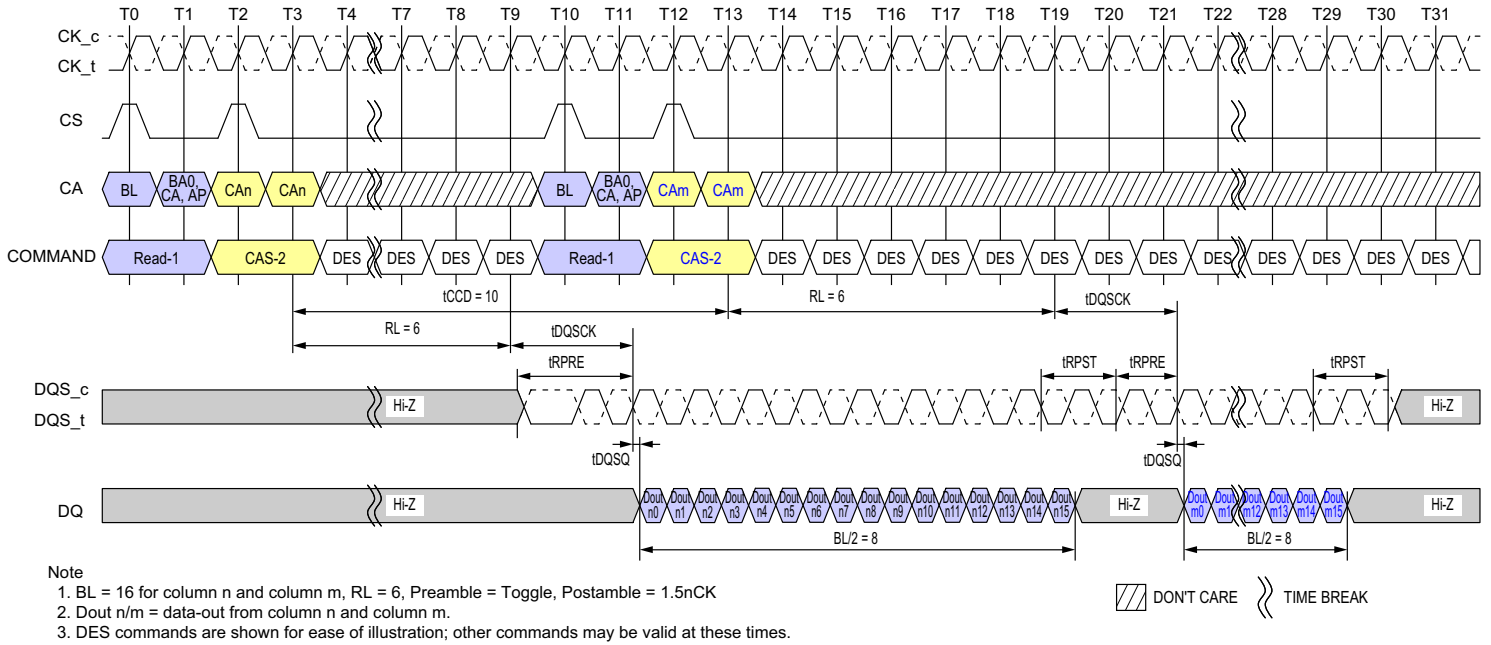
**Figure - Consecutive Reads Operation: tCCD=Min+1, Preamble=Toggle, 0.5nCK Postamble**



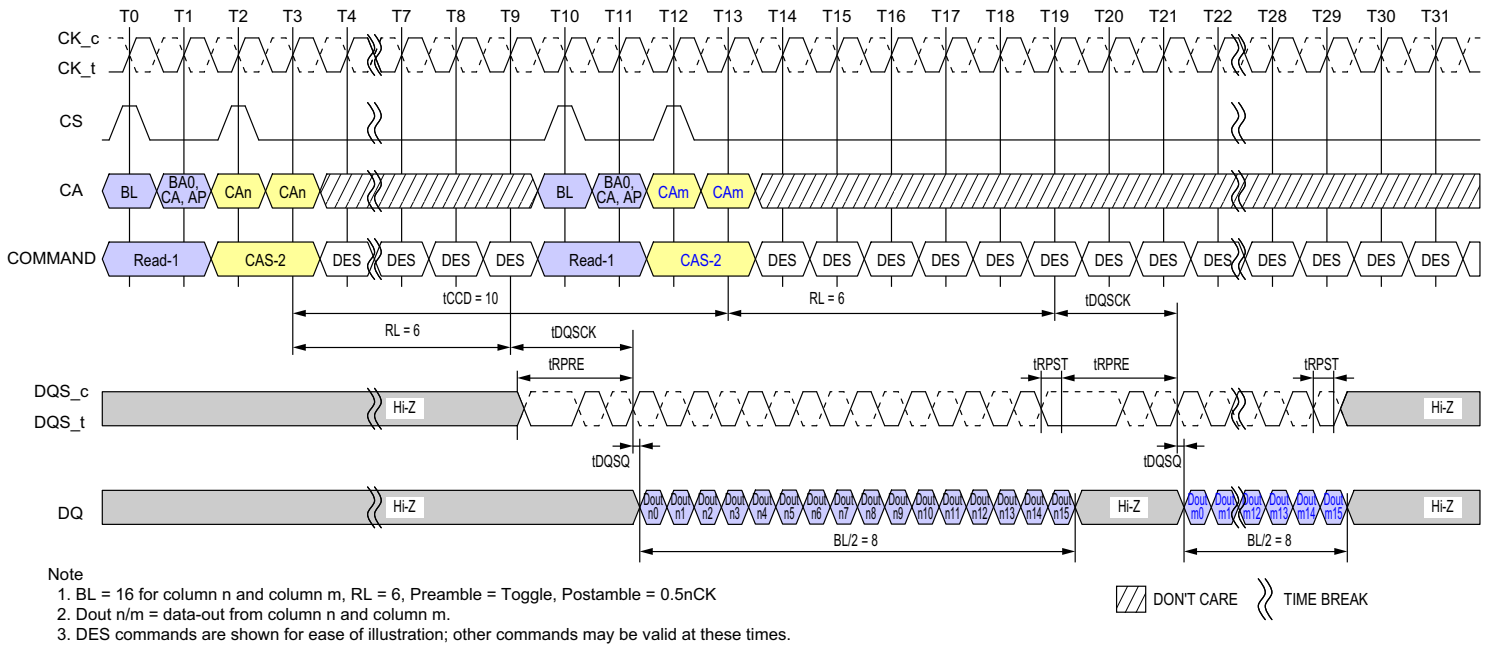
**Figure - Consecutive Reads Operation: tCCD = Min + 1, Preamble = Static, 1.5nCK Postamble**



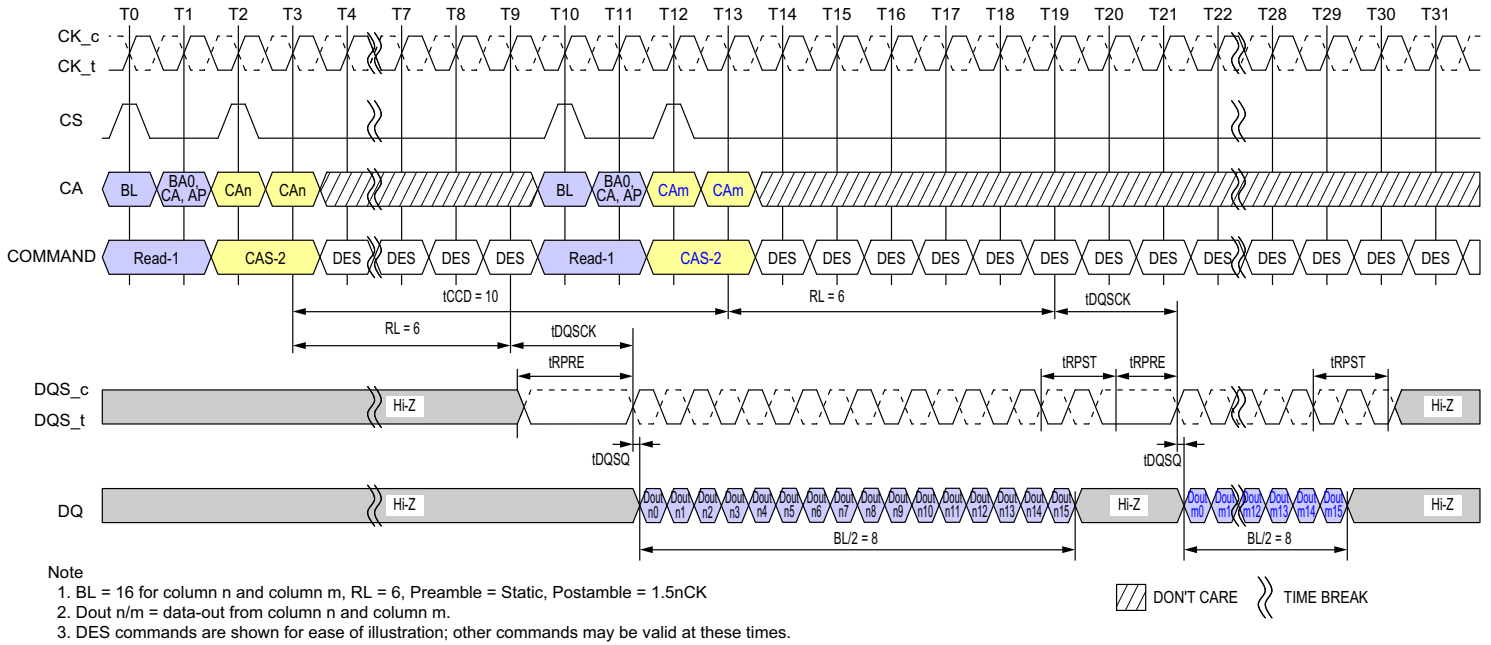
**Figure - Consecutive Reads Operation: tCCD = Min + 1, Preamble = Static, 0.5nCK Postamble**



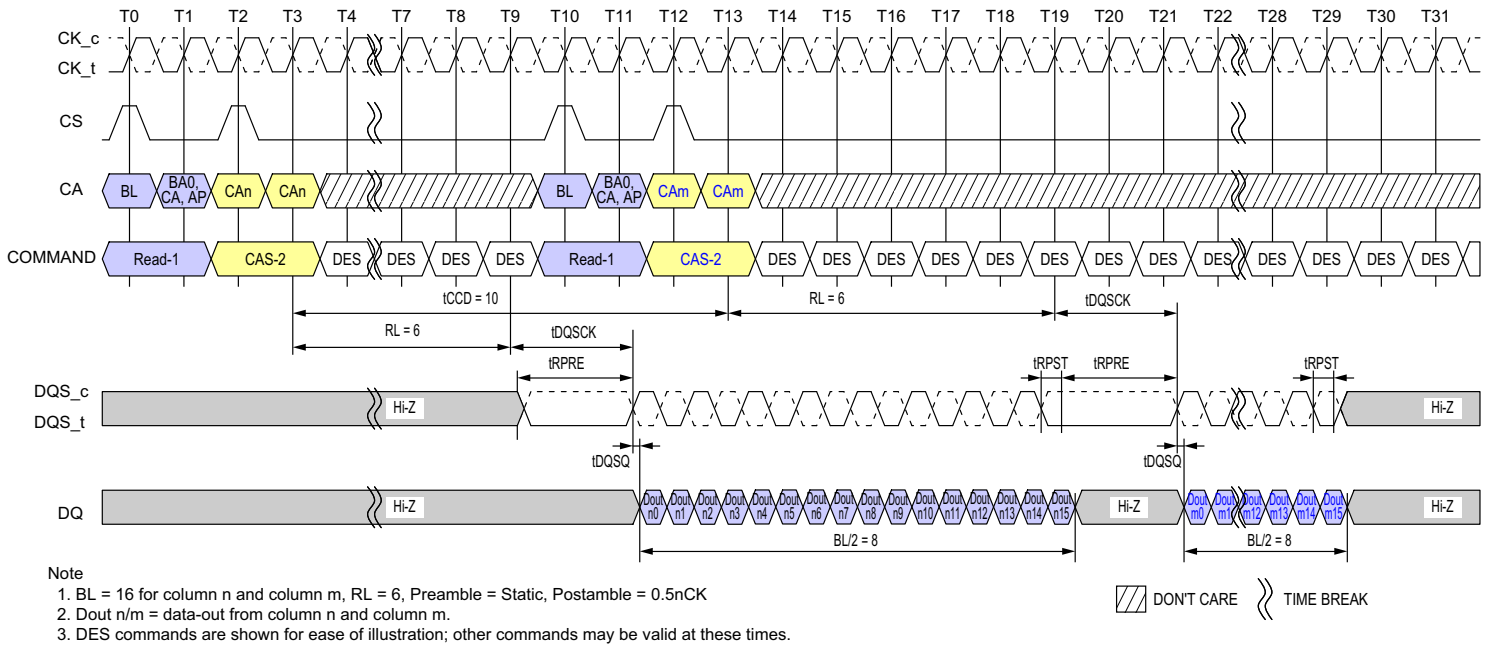
**Figure - Consecutive Reads Operation: tCCD = Min +2, Preamble = Toggle, 1.5nCK Postamble**



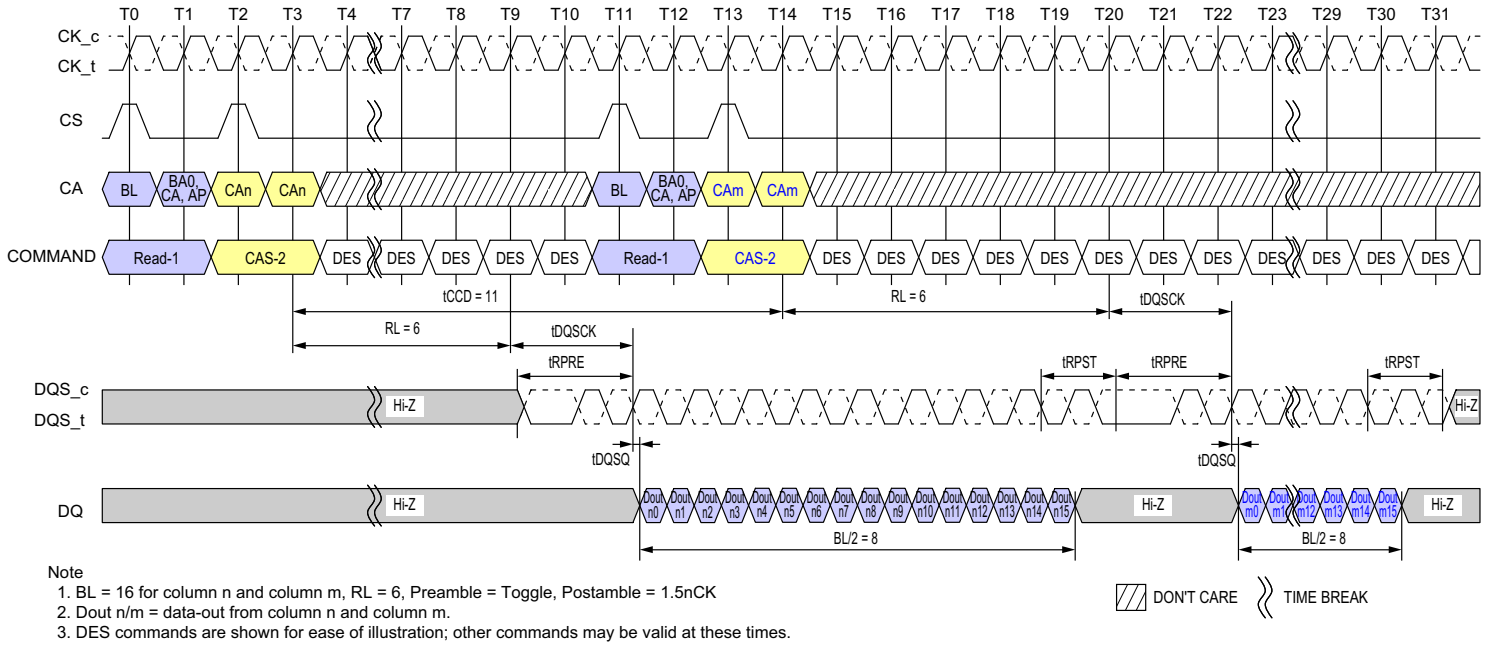
**Figure - Consecutive Reads Operation: tCCD = Min +2, Preamble = Toggle, 0.5nCK Postamble**



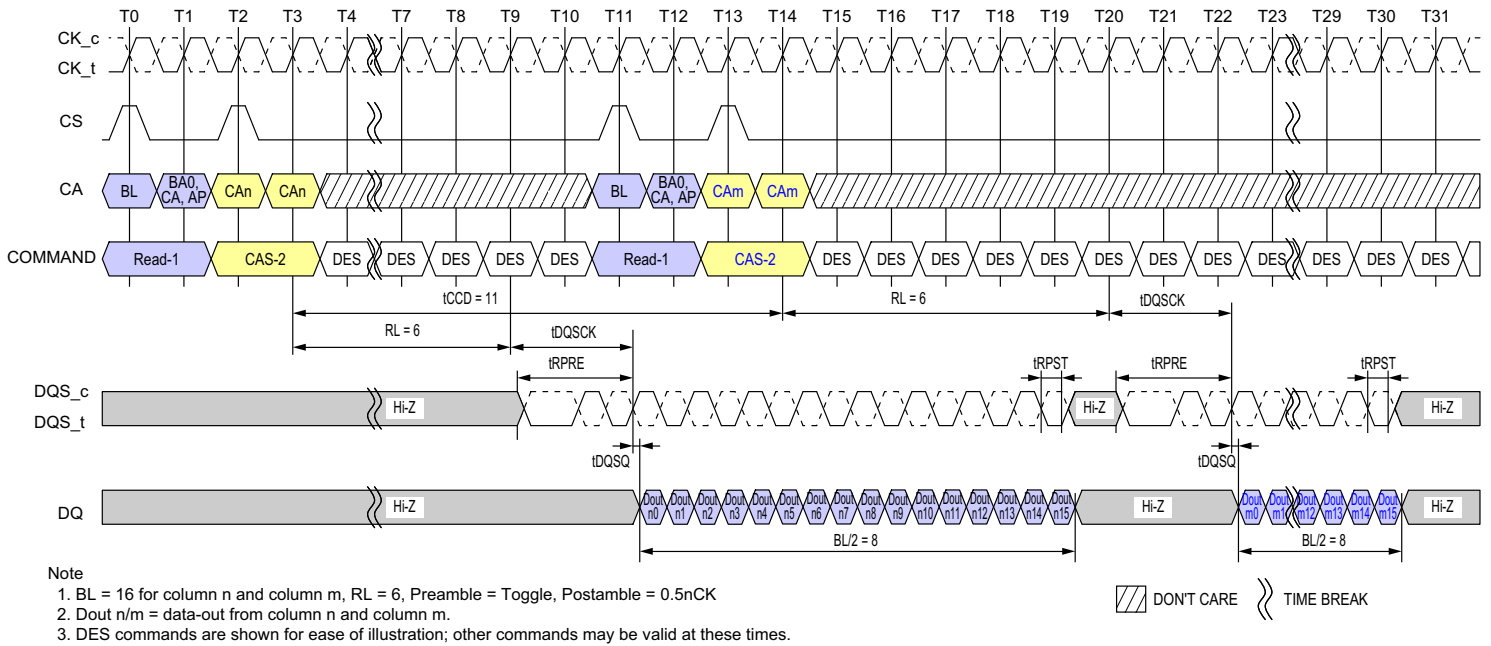
**Figure - Consecutive Reads Operation: tCCD = Min + 2, Preamble = Static, 1.5nCK Postamble**



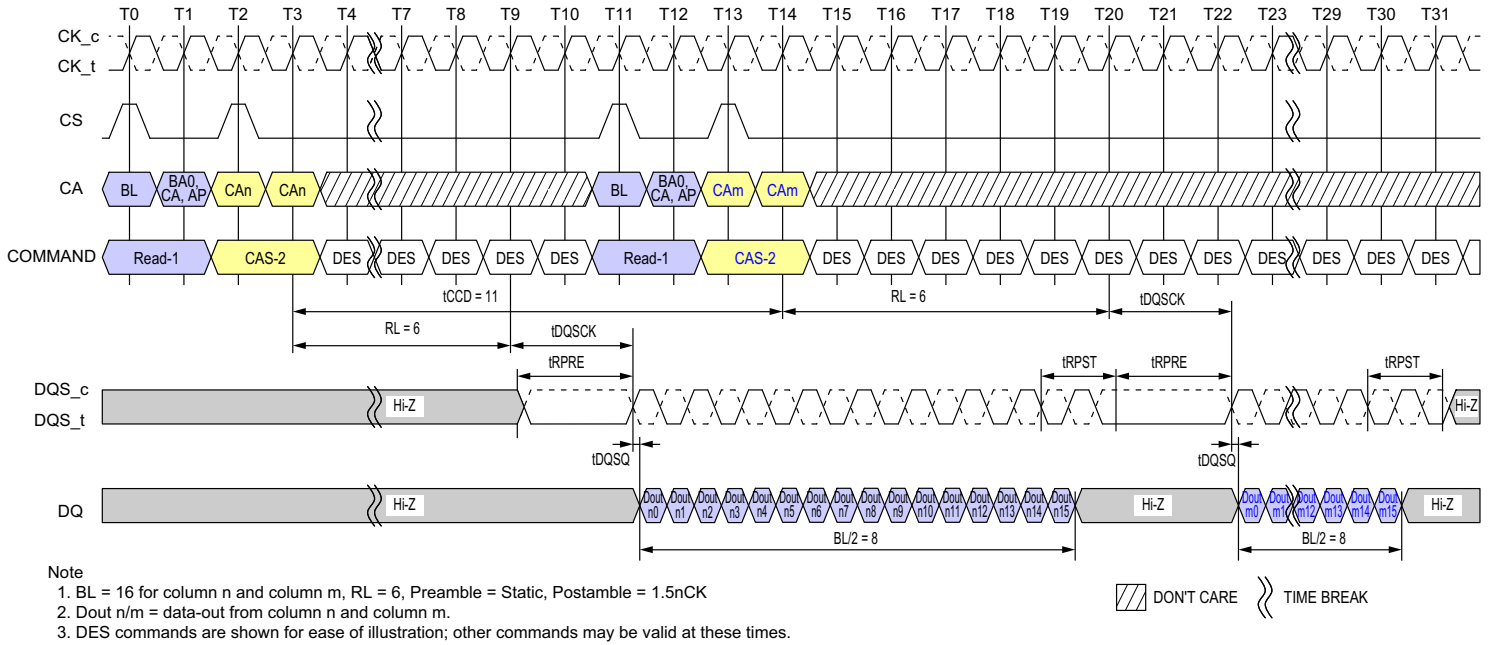
**Figure - Consecutive Reads Operation: tCCD = Min + 2, Preamble = Static, 0.5nCK Postamble**



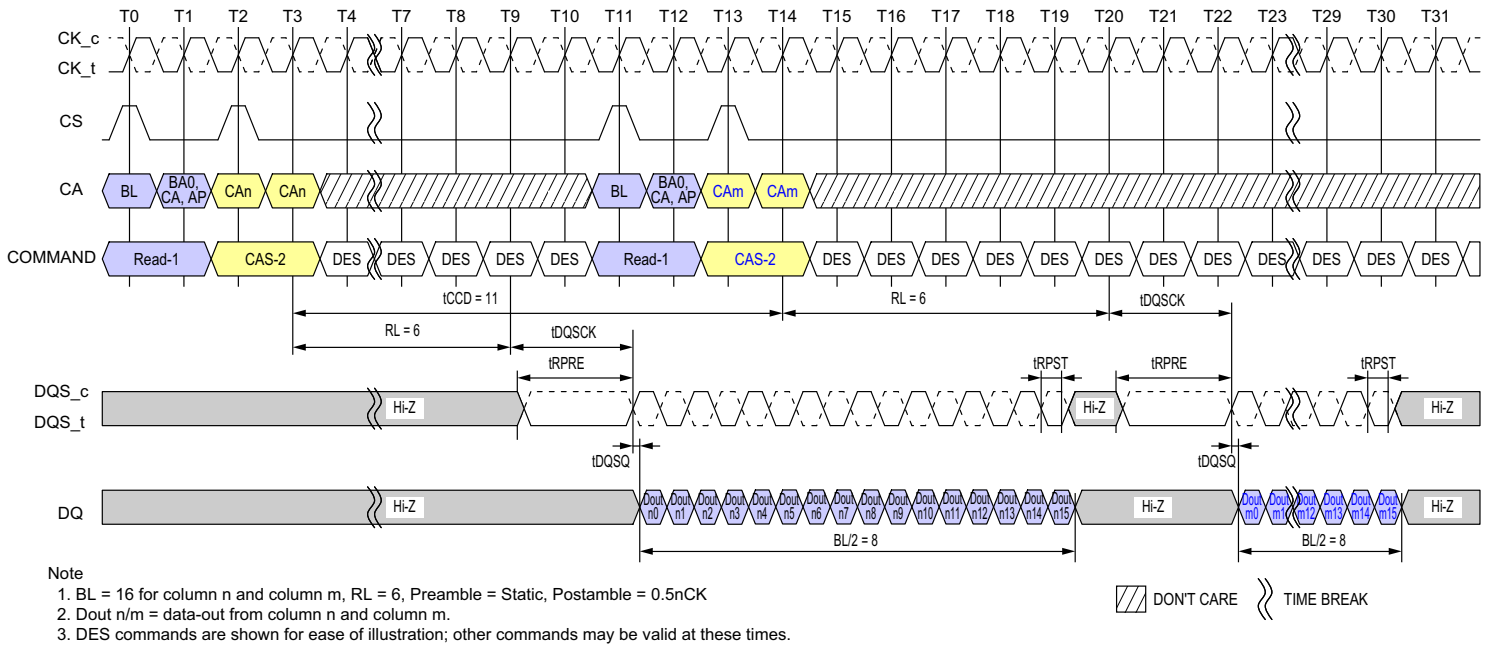
**Figure - Consecutive Reads Operation: tCCD = Min +3, Preamble = Toggle, 1.5nCK Postamble**



**Figure - Consecutive Reads Operation: tCCD = Min +3, Preamble = Toggle, 0.5nCK Postamble**



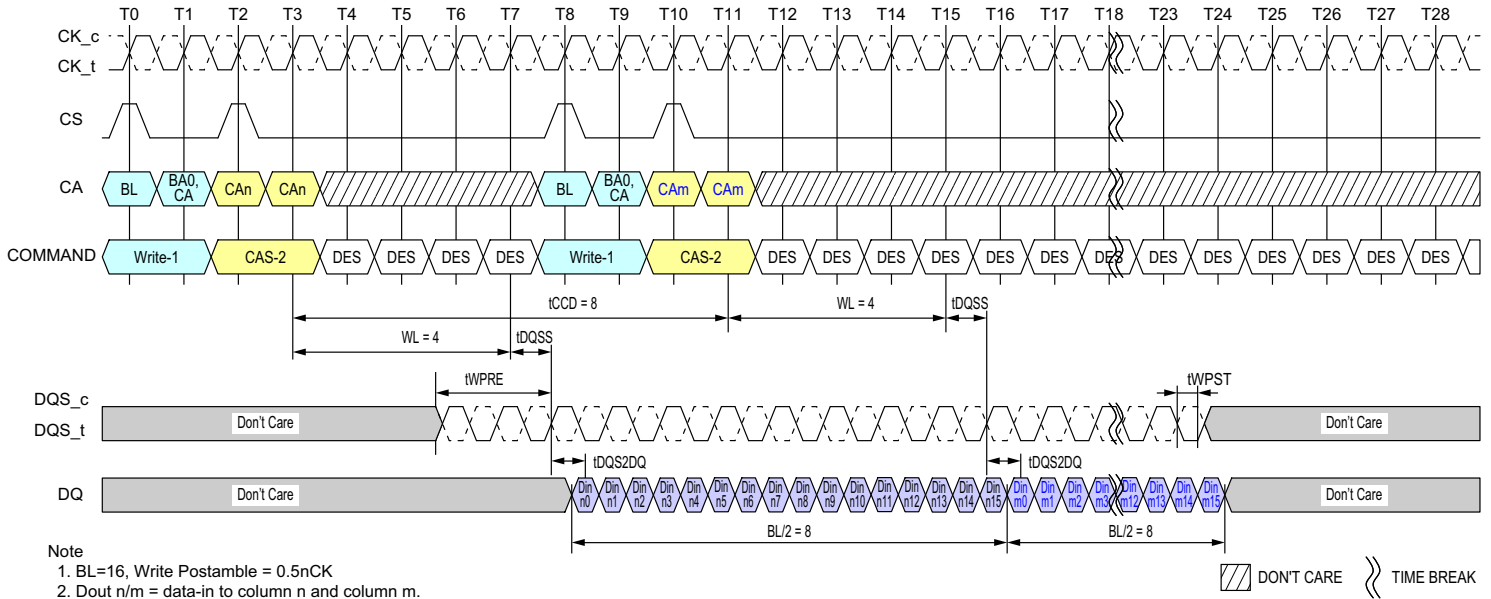
**Figure - Consecutive Reads Operation: tCCD = Min +3, Preamble = Static, 1.5nCK Postamble**



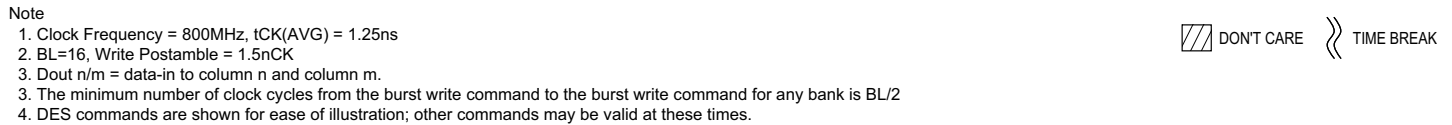
**Figure - Consecutive Reads Operation: tCCD = Min +3, Preamble = Static, 0.5nCK Postamble**



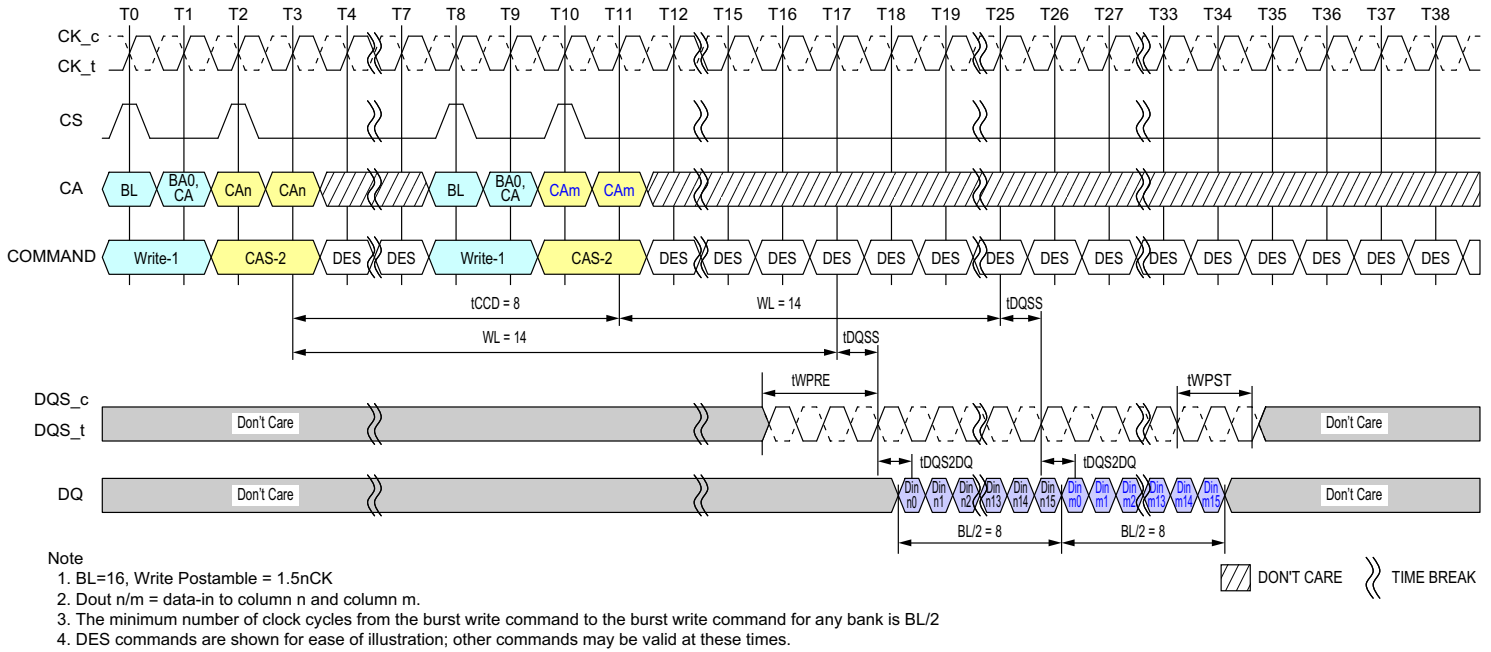
## 2.10.2. Write to Write operation



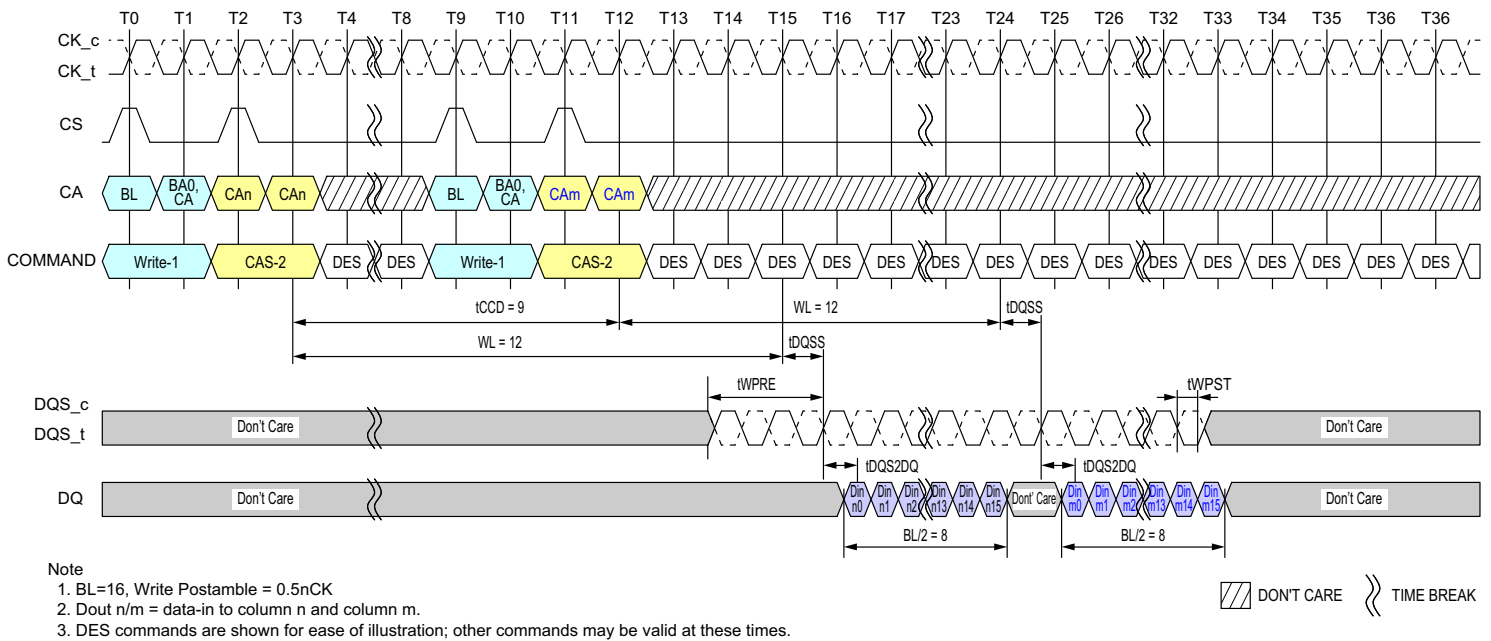
**Figure - Seamless Writes Operation: tCCD = Min, 0.5nCK Postamble**



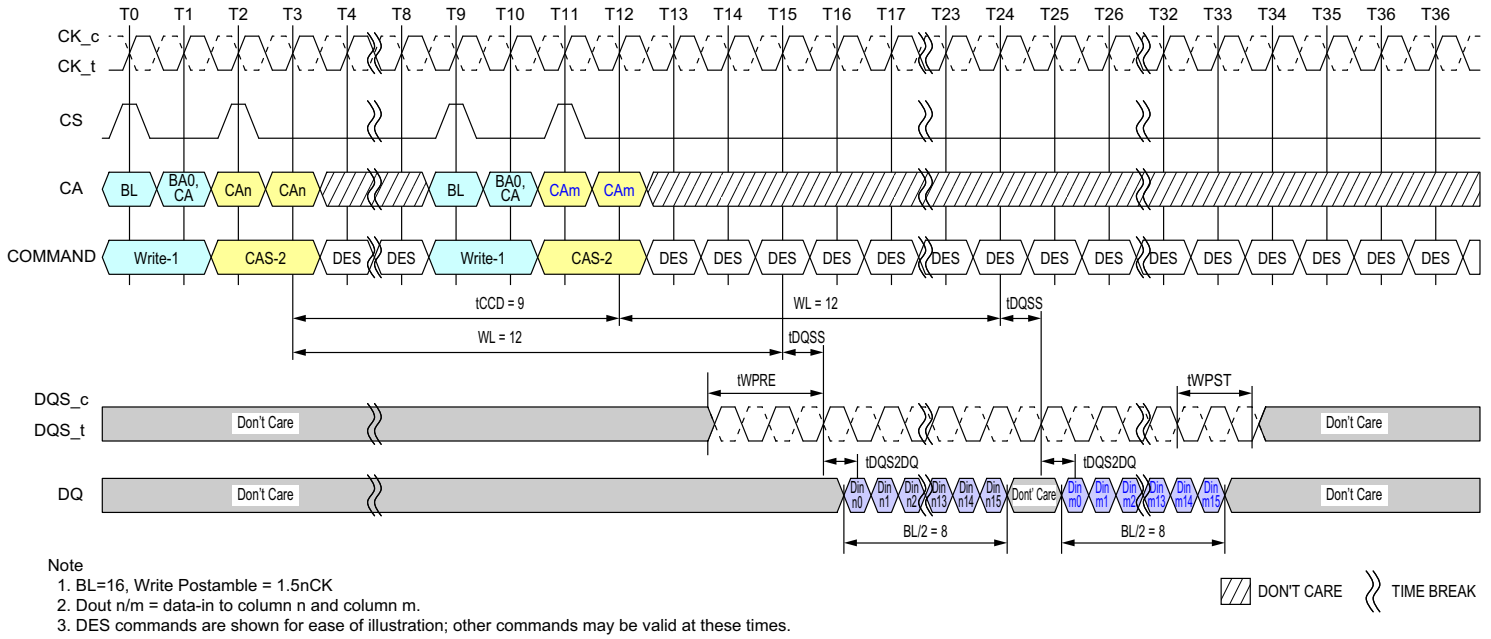
**Figure - Seamless Writes Operation: tCCD = Min, 1.5nCK Postamble, 533MHz < Clock Freq. ≤ 800MHz, ODT Worst Timing Case**



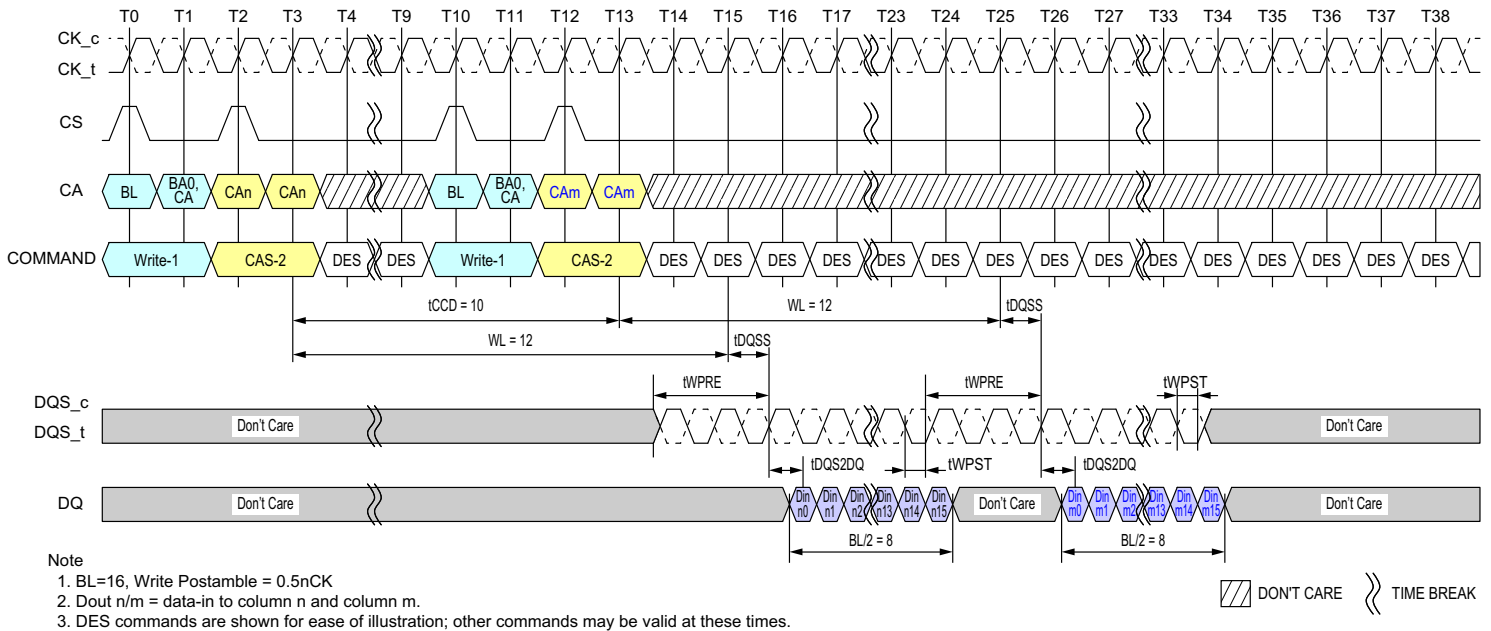
**Figure - Seamless Writes Operation:  $t_{CCD} = \text{Min}$ , 1.5nCK Postamble**



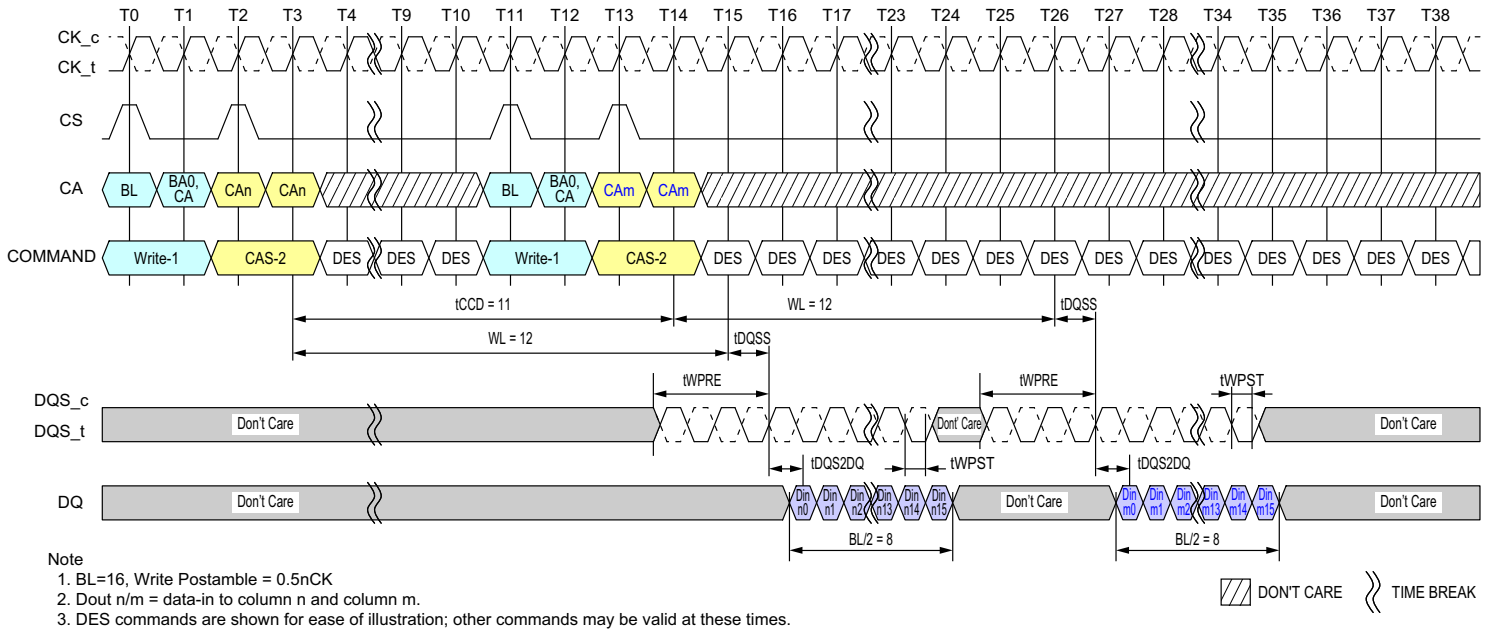
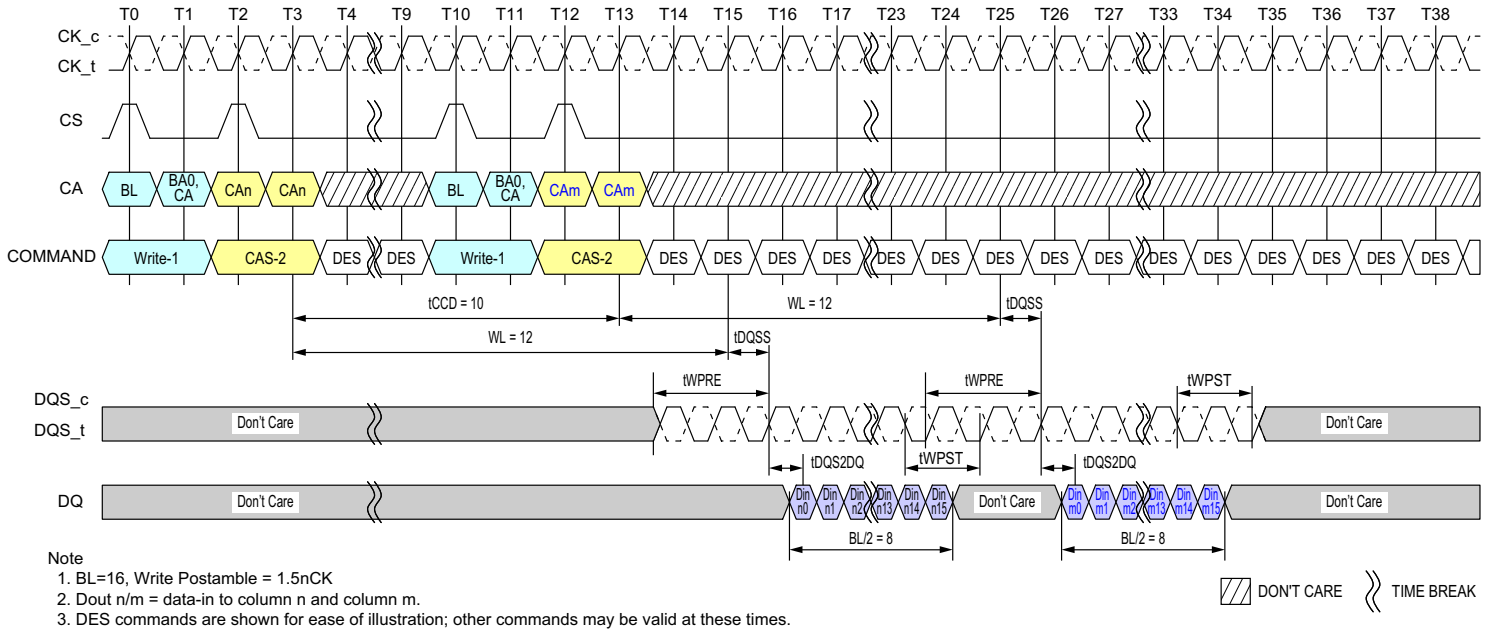
**Figure - Consecutive Writes Operation:  $t_{CCD} = \text{Min} + 1$ , 0.5nCK Postamble**



**Figure - Consecutive Writes Operation: tCCD = Min + 1, 1.5nCK Postamble**



**Figure - Consecutive Writes Operation: tCCD = Min + 2, 0.5nCK Postamble**

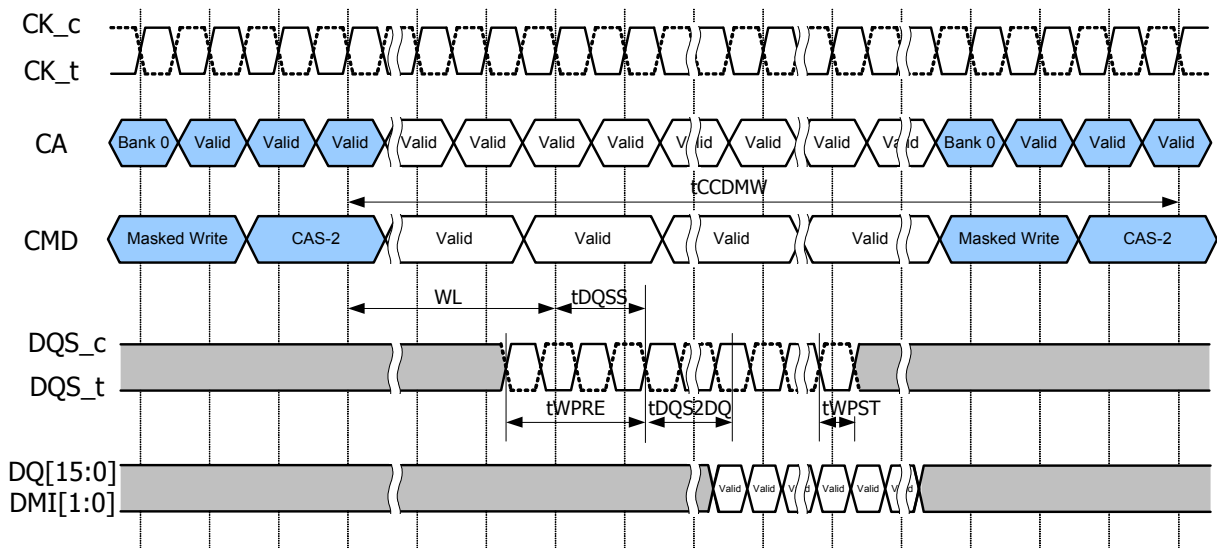




## 2.11. Masked Write Operation

The LPDDR4-SDRAM requires that Write operations which include a byte mask anywhere in the burst sequence must use the Masked Write command. This allows the DRAM to implement efficient data protection schemes based on larger data blocks. The Masked Write-1 command is used to begin the operation, followed by a CAS-2 command. A Masked Write command to the same bank cannot be issued until  $t_{CCDMW}$  is met, to allow the LPDDR4-SDRAM to finish the internal Read-Modify-Write. One Data Mask-Invert (DMI) pin is provided per byte lane, and the Data Mask-Invert timings match data bit (DQ) timing. See the section on "Data Mask Invert" for more information on the use of the DMI signal.

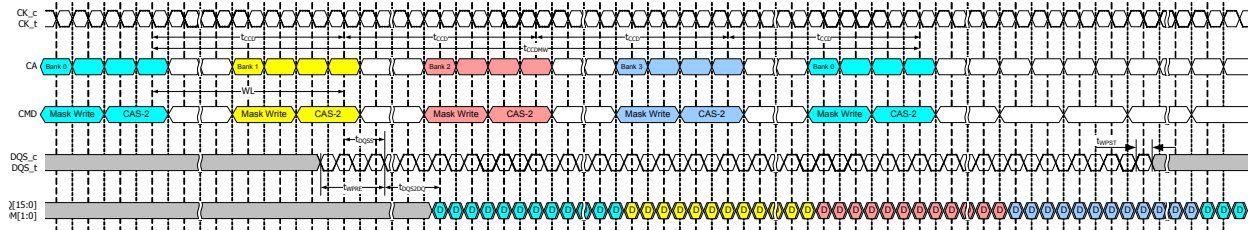
**Figure - Masked Write Command - Same Bank (Shown with BL16, 2tCK Preamble)**



Notes:

1. Masked Write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.

**Figure - Masked Write Command - Different Bank (shown with BL16, 2tCK Preamble)**



Notes:

1. Masked Write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.

### 2.11.1. Masked Write Timing constraints

**Table - Masked Write Timing constraints - Same bank**

| Next CMD<br>Current CMD | Activate                      | Read<br>(BL16 or 32)       | Write<br>(BL16 or 32)                                | Masked Write                                         | Precharge                         |
|-------------------------|-------------------------------|----------------------------|------------------------------------------------------|------------------------------------------------------|-----------------------------------|
| Activate                | Illegal                       | RU(tRCD/tCK)               | RU(tRCD/tCK)                                         | RU(tRCD/tCK)                                         | RU(tRAS/tCK)                      |
| Read (BL16)             | Illegal                       | 8 <sup>1)</sup>            | RL+RU(tDQSCCK(max)/<br>tCK) +BL/2-<br>WL+tWPRE+tRPST | RL+RU(tDQSCCK(max)/<br>tCK) +BL/2-<br>WL+tWPRE+tRPST | BL/2+max{(8, RU(tRTP/<br>tCK))}-8 |
| Read (BL32)             | Illegal                       | 16 <sup>2)</sup>           | RL+RU(tDQSCCK(max)/<br>tCK) +BL/2-<br>WL+tWPRE+tRPST | RL+RU(tDQSCCK(max)/<br>tCK) +BL/2-<br>WL+tWPRE+tRPST | BL/2+max{(8, RU(tRTP/<br>tCK))}-8 |
| Write (BL16)            | Illegal                       | WL+1+BL/2<br>+RU(tWTR/tCK) | 8 <sup>1)</sup>                                      | tCCDMW <sup>3)</sup>                                 | WL+ 1 + BL/2<br>+RU(tWR/tCK)      |
| Write (BL32)            | Illegal                       | WL+1+BL/2<br>+RU(tWTR/tCK) | 16 <sup>2)</sup>                                     | tCCDMW + 8 <sup>4)</sup>                             | WL+ 1 + BL/2<br>+RU(tWR/tCK)      |
| Masked Write            | Illegal                       | WL+1+BL/2<br>+RU(tWTR/tCK) | tCCD                                                 | tCCDMW <sup>3)</sup>                                 | WL+ 1 + BL/2<br>+RU(tWR/tCK)      |
| Precharge               | RU(tRP/tCK),<br>RU(tRPab/tCK) | Illegal                    | Illegal                                              | Illegal                                              | 4                                 |

Notes:

- 1) In the case of BL = 16, tCCD is 8\*tCK.
- 2) In the case of BL = 32, tCCD is 16\*tCK.
- 3) tCCDMW = 32\*tCK (4\*tCCD at BL=16)
- 4) Write with BL=32 operation has 8\*tCK longer than BL =16.
- 5) Units : tCK

**Table - Masked Write Timing constraints - Different bank**

| Next CMD<br>Current CMD | Activate     | Read<br>(BL16 or 32)       | Write<br>(BL16 or 32)                                | Masked Write<br>(BL16)                               | Precharge |
|-------------------------|--------------|----------------------------|------------------------------------------------------|------------------------------------------------------|-----------|
| Activate                | RU(tRRD/tCK) | 4                          | 4                                                    | 4                                                    | 2         |
| Read (BL16)             | 4            | 8 <sup>1)</sup>            | RL+RU(tDQSCCK(max)/<br>tCK) +BL/2-<br>WL+tWPRE+tRPST | RL+RU(tDQSCCK(max)/<br>tCK) +BL/2-<br>WL+tWPRE+tRPST | 2         |
| Read (BL32)             | 4            | 16 <sup>1)</sup>           | RL+RU(tDQSCCK(max)/<br>tCK) +BL/2-<br>WL+tWPRE+tRPST | RL+RU(tDQSCCK(max)/<br>tCK) +BL/2-<br>WL+tWPRE+tRPST | 2         |
| Write (BL16)            | 4            | WL+1+BL/2<br>+RU(tWTR/tCK) | 8 <sup>1)</sup>                                      | 8 <sup>1)</sup>                                      | 2         |
| Write (BL32)            | 4            | WL+1+BL/2<br>+RU(tWTR/tCK) | 16 <sup>1)</sup>                                     | 16 <sup>1)</sup>                                     | 2         |
| Masked Write            | 4            | WL+1+BL/2<br>+RU(tWTR/tCK) | 8 <sup>1)</sup>                                      | 8 <sup>1)</sup>                                      | 2         |
| Precharge               | 4            | 4                          | 4                                                    | 4                                                    | 4         |

Notes:

- 1) In the case of BL = 16, tCCD is 8\*tCK.
- 2) In the case of BL = 32, tCCD is 16\*tCK.
- 3) Units : tCK



## 2.12. LPDDR4 Data Mask (DM) and Data Bus Inversion (DBI<sub>dc</sub>) Function

LPDDR4 SDRAM supports the function of Data Mask and Data Bus inversion. Its details are shown below.

- LPDDR4 device supports Data Mask (DM) function for Write operation.
- LPDDR4 device supports Data Bus Inversion (DBI<sub>dc</sub>) function for Write and Read operation.
- LPDDR4 supports DM and DBI<sub>dc</sub> function with a byte granularity.
- DBI<sub>dc</sub> function during Write or Masked Write can be enabled or disabled through MR3 OP[7].
- DBI<sub>dc</sub> function during Read can be enabled or disabled through MR3 OP[6].
- DM function during Masked Write can be enabled or disabled through MR13 OP[5].
- LPDDR4 device has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals per channel.
- DMI signal is a bi-directional DDR signal and is sampled along with the DQ signals for Read and Write or Masked Write operation.

There are eight possible combinations for LPDDR4 device with DM and DBI<sub>dc</sub> function. Table below describes the functional behavior for all combinations.

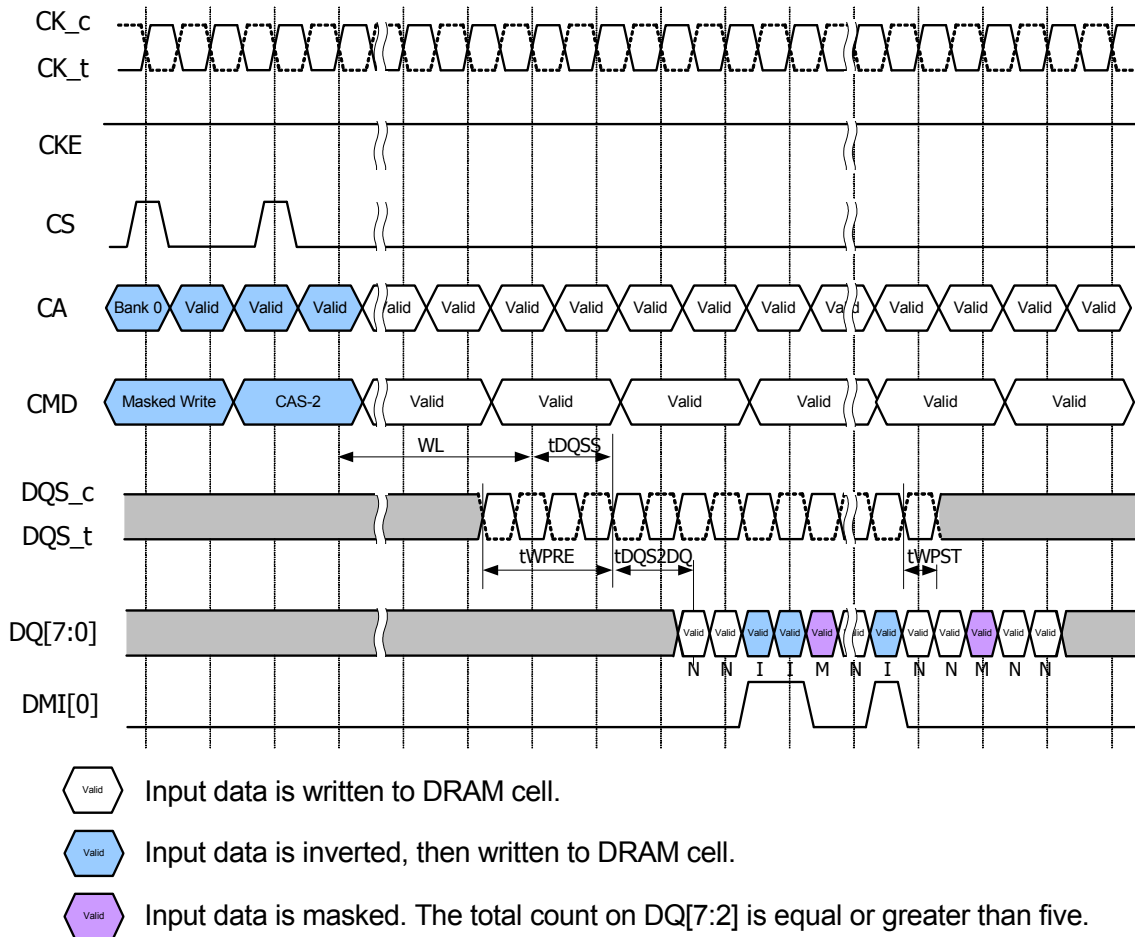
**Table - Function Behaviour of DMI Signal During Write, Masked Write and Read Operation**

| DM Fuction | Write DBI <sub>dc</sub> Fuction | Read DBI <sub>dc</sub> Fuction | DMI Signal during Write Command | DMI Signal during Masked Write Command | DMI Signal during Read | DMI Signal during MPC [WR FIFO] | DMI Signal during MPC [RD FIFO] | DMI Signal during MPC [DQ Read calibration] | DMI Signal during MRR Command |
|------------|---------------------------------|--------------------------------|---------------------------------|----------------------------------------|------------------------|---------------------------------|---------------------------------|---------------------------------------------|-------------------------------|
| Disable    | Disable                         | Disable                        | Note: 1                         | Note: 1, 3                             | Note: 2                | Note: 1                         | Note: 2                         | Note: 2                                     | Note: 2                       |
| Disable    | Enable                          | Disable                        | Note: 4                         | Note: 3                                | Note: 2                | Note: 9                         | Note: 10                        | Note: 11                                    | Note: 2                       |
| Disable    | Disable                         | Enable                         | Note: 1                         | Note: 3                                | Note: 5                | Note: 9                         | Note: 10                        | Note: 11                                    | Note: 12                      |
| Disable    | Enable                          | Enable                         | Note: 4                         | Note: 3                                | Note: 5                | Note: 9                         | Note: 10                        | Note: 11                                    | Note: 12                      |
| Enable     | Disable                         | Disable                        | Note: 6                         | Note: 7                                | Note: 2                | Note: 9                         | Note: 10                        | Note: 11                                    | Note: 2                       |
| Enable     | Enable                          | Disable                        | Note: 4                         | Note: 8                                | Note: 2                | Note: 9                         | Note: 10                        | Note: 11                                    | Note: 2                       |
| Enable     | Disable                         | Enable                         | Note: 6                         | Note: 7                                | Note: 5                | Note: 9                         | Note: 10                        | Note: 11                                    | Note: 12                      |
| Enable     | Enable                          | Enable                         | Note: 4                         | Note: 8                                | Note: 5                | Note: 9                         | Note: 10                        | Note: 11                                    | Note: 12                      |

1. DMI input signal is a don't care. DMI input receivers are turned OFF.
2. DMI output drivers are turned OFF.
3. Masked Write Command is not allowed and is considered an illegal command as DM function is disabled.
4. DMI signal is treated as DBI signal and it indicates whether DRAM needs to invert the Write data received on DQs within a byte. The LPDDR4 device inverts Write data received on the DQ inputs in case DMI was sampled HIGH, or leaves the Write data non-inverted in case DMI was sampled LOW.
5. The LPDDR4 DRAM inverts Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.
6. The LPDDR4 DRAM does not perform any mask operation when it receives Write command. During the Write burst associated with Write command, DMI signal must be driven LOW.
7. The LPDDR4 DRAM requires an explicit Masked Write command for all masked write operations. DMI signal is treated as DM signal and it indicates which bit time within the burst is to be masked. When DMI signal is HIGH, DRAM masks that bit time across all DQs associated within a byte. All DQ input signals within a byte are don't care (either HIGH or LOW) when DMI signal is HIGH. When DMI signal is LOW, the LPDDR4 DRAM does not perform mask operation and data received on DQ input is written to the array.
8. The LPDDR4 DRAM requires an explicit Masked Write command for all masked write operations. The LPDDR4 device masks the Write data received on the DQ inputs if the total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively) is equal to or greater than five and DMI signal is LOW. Otherwise the LPDDR4 DRAM does not perform mask operation and treats it as a legal DBI pattern; DMI signal is treated as DBI signal and data received on DQ input is written to the array.
9. DMI signal is treated as a training pattern. The LPDDR4 SDRAM does not perform any mask operation and does not invert Write data received on the DQ inputs.
10. DMI signal is treated as a training pattern. The LPDDR4 SDRAM returns DMI pattern written in WR-FIFO.

11. DMI signal is treated as a training pattern. For more details, see MPC RD DQ Calibration session.
12. DBI may apply or may not apply during normal MRR. It's vendor specific. If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DBI pin status should be low.  
 If read DBI is enable with MRS and vendor can support the DBI during MRR, the LPDDR4 DRAM inverts Mode Register Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.

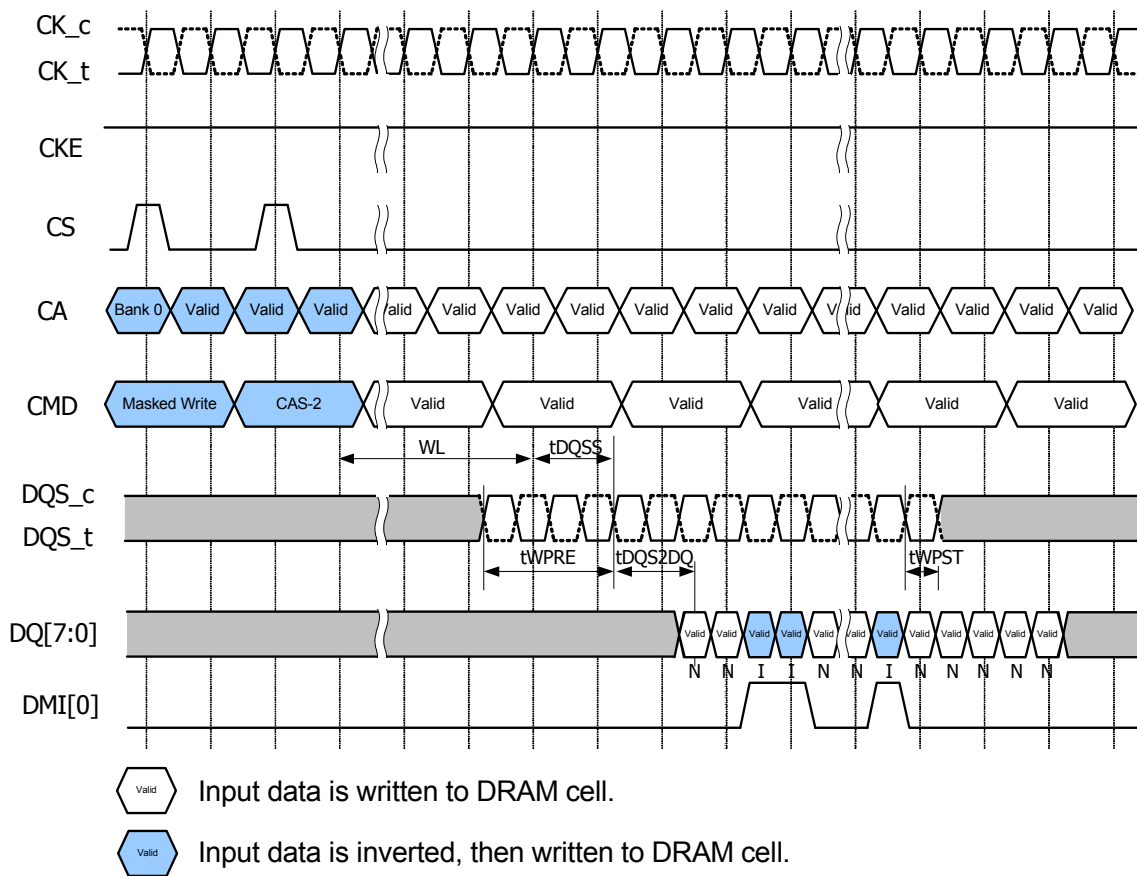
**Figure - Masked Write Operation w/ Write DBI Enabled; DM Enabled**



**Notes:**

1. Data Mask (DM) is Enabled; MR13 OP[5]=1, Data Bus Inversion (DBI) Write is Enabled; MR3 OP[7]=1.

**Figure - Write Command w/ Write DBI Enabled; DM Disabled**



**Notes:**

1. Data Mask (DM) is Disabled; MR13 OP[5]=0, Data Bus Inversion (DBI) Write is Enabled; MR3 OP[7]=1.

### 2.13. Precharge Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS, and CA[5:0] in the proper state as defined by the Command Truth Table. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access tRPab after an all-bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR4 devices can meet the instantaneous current demands, the row-precharge time for an all-bank PRECHARGE (tRPab) is longer than the perbank precharge time (tRPpb).

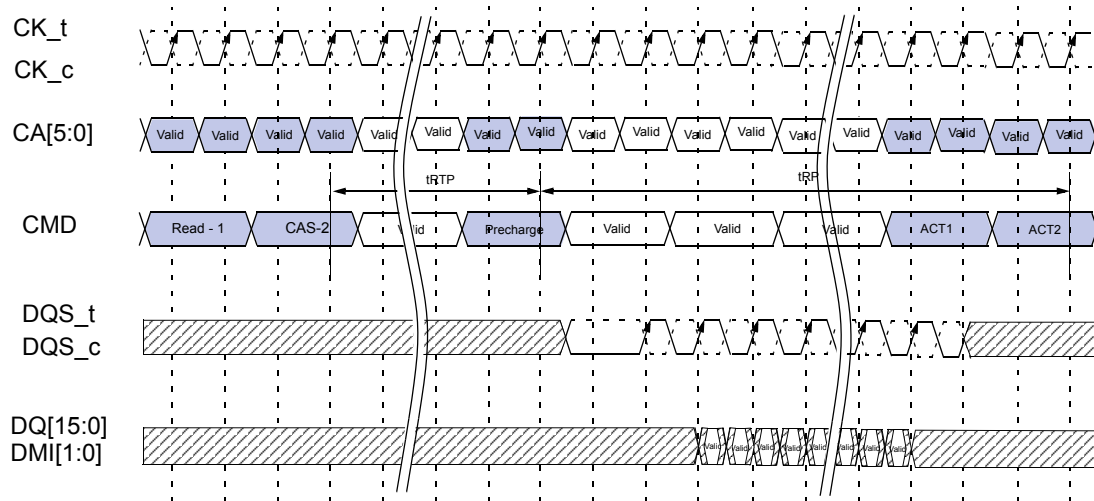
**Table - Precharge Bank Selection**

| <b>AB<br/>(CA[5], R1)</b> | <b>BA2<br/>(CA[2], R2)</b> | <b>BA1<br/>(CA[1], R2)</b> | <b>BA0<br/>(CA[0], R2)</b> | <b>Precharged<br/>Bank(s)</b> |
|---------------------------|----------------------------|----------------------------|----------------------------|-------------------------------|
| 0                         | 0                          | 0                          | 0                          | Bank 0 Only                   |
| 0                         | 0                          | 0                          | 1                          | Bank 1 Only                   |
| 0                         | 0                          | 1                          | 0                          | Bank 2 Only                   |
| 0                         | 0                          | 1                          | 1                          | Bank 3 Only                   |
| 0                         | 1                          | 0                          | 0                          | Bank 4 Only                   |
| 0                         | 1                          | 0                          | 1                          | Bank 5 Only                   |
| 0                         | 1                          | 1                          | 0                          | Bank 6 Only                   |
| 0                         | 1                          | 1                          | 1                          | Bank 7 Only                   |
| 1                         | Valid                      | Valid                      | Valid                      | All banks                     |

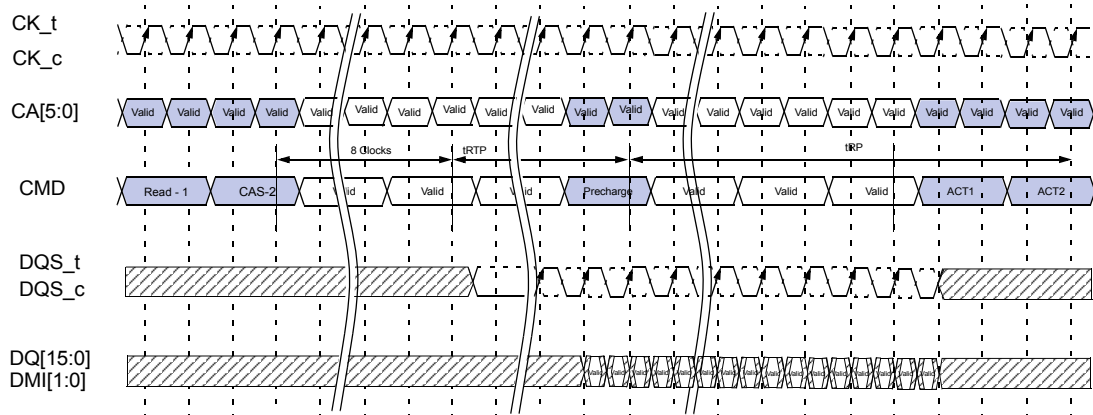
### 2.13.1. Burst Read Operation followed by Precharge

The PRECHARGE command can be issued as early as BL/2 clock cycles after a READ command, but PRECHARGE cannot be issued until after t<sub>RAS</sub> is satisfied. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (t<sub>RP</sub>) has elapsed. The minimum READ-to-PRECHARGE time must also satisfy a minimum analog time from the 2nd rising clock edge of the CAS-2 command. t<sub>RP</sub> begins BL/2 + 8 clock cycles after the READ command. For LPDDR4 READ-to-PRECHARGE timings see Table "Timing Between Commands (Precharge and Auto-Precharge)".

**Figure - Burst Read followed by Precharge (BL16, toggling pre-amble)**



**Figure - Burst Read followed by Precharge (BL32, Toggling Preamble)**

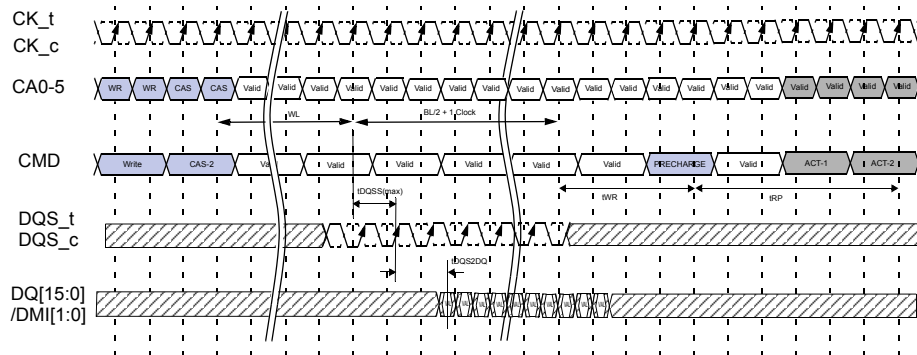


### 2.13.2. Burst Write followed by Precharge

A Write Recovery time ( $t_{WR}$ ) must be provided before a PRECHARGE command may be issued. This delay is referenced from the next rising edge of  $CK_t$  after the last latching DQS clock of the burst.

LPDDR4-SDRAM devices write data to the memory array in prefetch multiples (prefetch=16). An internal WRITE operation can only begin after a prefetch group has been clocked, so  $t_{WR}$  starts at the prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is  $WL + BL/2 + 1 + RU(t_{WR}/t_{CK})$  clock cycles.

**Figure - Burst Write followed by Precharge (BL16, 2tCK preamble)**



### 2.13.3. Auto Precharge operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the Auto-PRECHARGE function. When a READ, WRITE or Masked Write command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ, WRITE or Masked Write cycle.

If AP is LOW when the READ, WRITE or Masked Write command is issued, then the normal READ, WRITE or Masked Write burst operation is executed and the bank remains active at the completion of the burst.

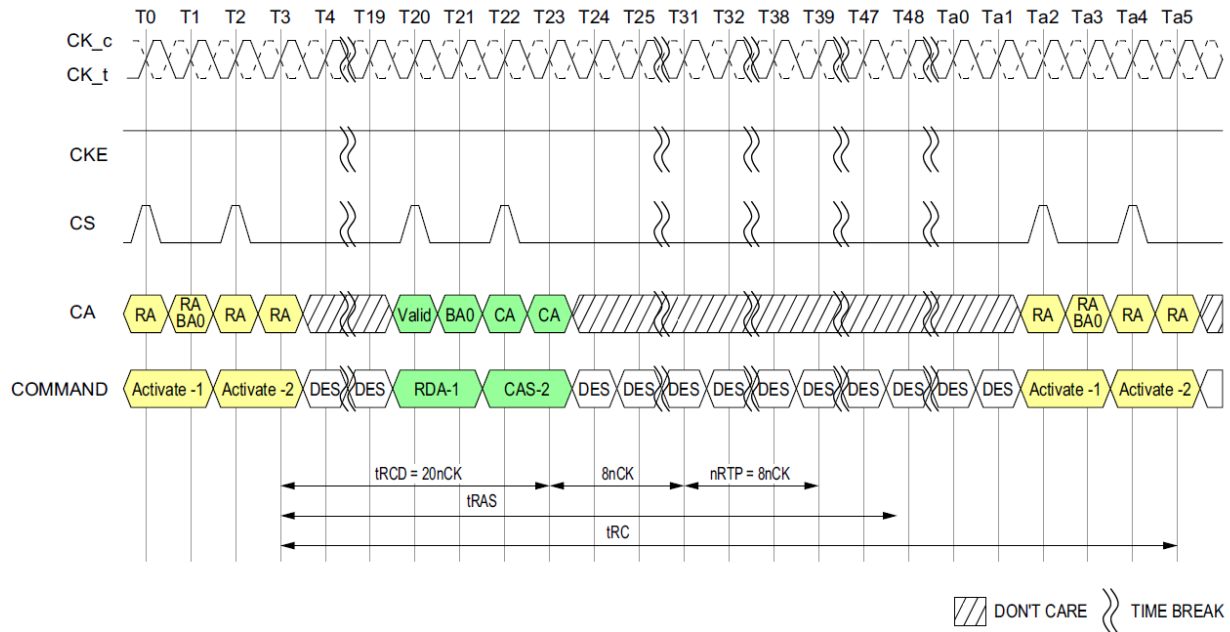
If AP is HIGH when the READ, WRITE or Masked Write command is issued, the Auto-PRECHARGE function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

Read with Auto Precharge or Write/Mask Write with Auto Precharge commands may be issued after  $t_{RCD}$  has been satisfied. The LPDDR4 SDRAM RAS Lockout feature will schedule the internal precharge to assure that  $t_{RAS}$  is satisfied.

$t_{RC}$  needs to be satisfied prior to issuing subsequent Activate commands to the same bank.

The figure below shows example of RAS lock function.

**Figure - Command Input Timing with RAS lock**



**Note**

1.  $t_{CK(AVG)} = 0.938ns$ , Data Rate = 2133Mbps,  $t_{RCD(Min)} = \text{Max}(18ns, 4nCK)$ ,  $t_{RAS(Min)} = \text{Max}(42ns, 3nCK)$ ,  $nRTP = 8nCK$ ,  $BL = 32$
2.  $t_{RCD} = 20nCK$  comes from Roundup( $18ns/0.938ns$ )
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

### 2.13.3.1. Burst Read with Auto-Precharge

If AP is HIGH when a READ command is issued, the READ with Auto-PRECHARGE function is engaged. An internal pre-charge procedure starts a following delay time after the READ command. And this delay time depends on BL setting.

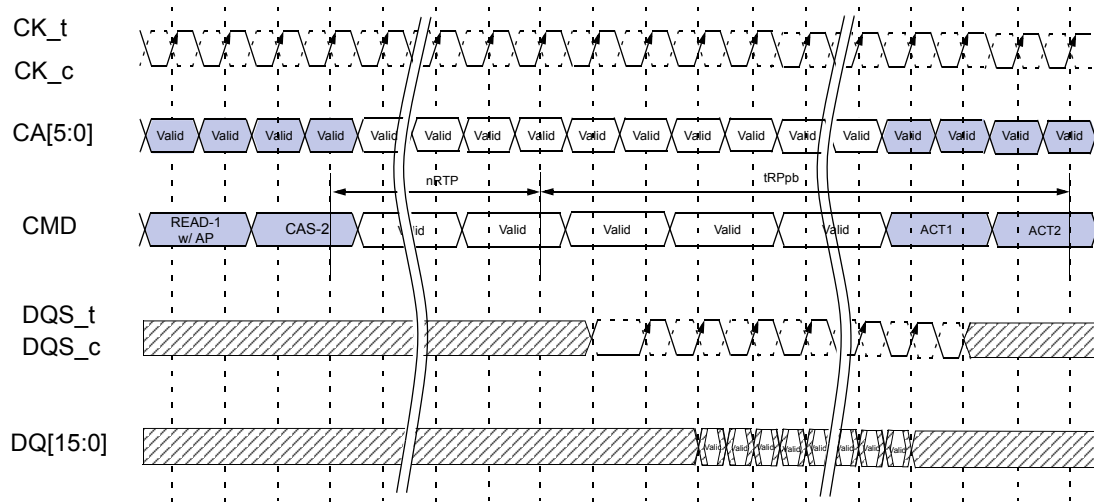
BL = 16:  $t_{RTP}$

BL = 32:  $8t_{CK} + t_{RTP}$

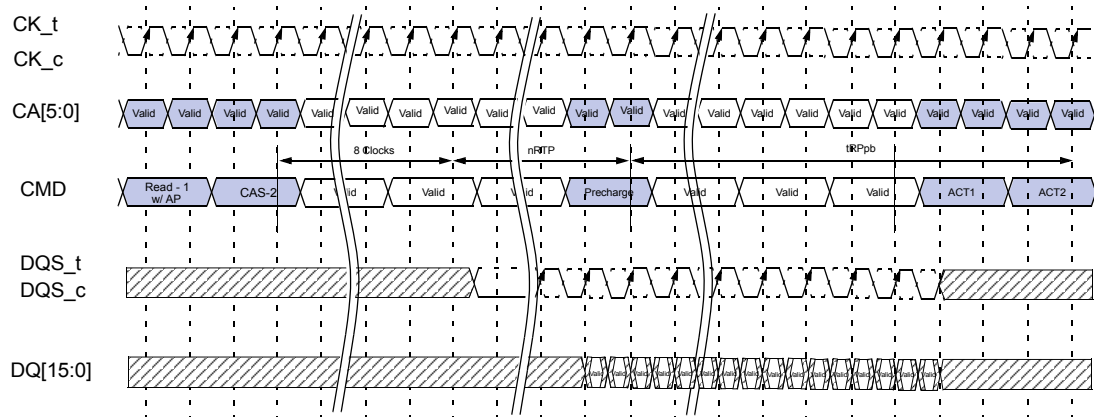
For LPDDR4 Auto-PRECHARGE calculations, see Table 2. Following an Auto-PRECHARGE operation, an ACTIVATE command can be issued to the same bank if the following two conditions are both satisfied:

- a. The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the Auto-PRECHARGE began, or
- b. The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.

**Figure - Burst Read with Auto-Precharge (BL16, Toggling preamble)**



**Figure - Burst Read with Auto-Precharge (BL32, Toggling preamble)**





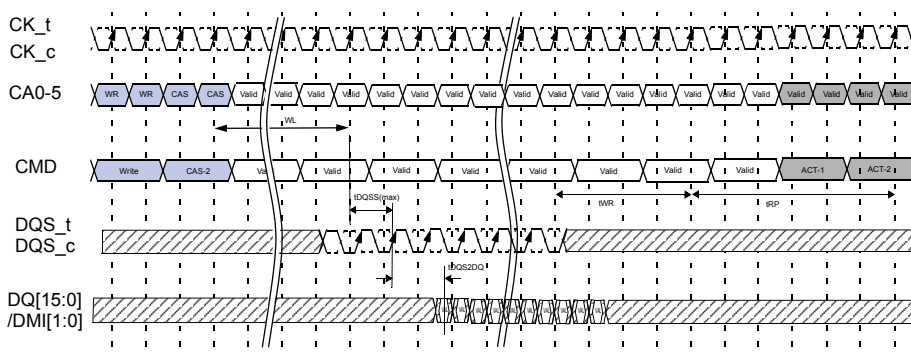
### 2.13.3.2. Burst Write with Auto-Precharge

If AP is HIGH when a WRITE command is issued, the WRITE with Auto-PRECHARGE function is engaged. The device starts an Auto-PRECHARGE on the rising edge tWR cycles after the completion of the Burst WRITE.

Following a WRITE with Auto-PRECHARGE, an ACTIVATE command can be issued to the same bank if the following conditions are met:

- a. The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the Auto-PRECHARGE began, and
- b. The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.

### Table - Burst Write with Auto-Precharge (BL16, 2tCK preamble)



### Table - Timing Between Commands (Precharge and Auto-Precharge) - DQ ODT is Disabled

| From Command      | To Command                                             | Minimum Delay between<br>"From Command" and "To Command" | Unit | Notes  |
|-------------------|--------------------------------------------------------|----------------------------------------------------------|------|--------|
| Read (BL16)       | Precharge<br>(to same bank as Read)                    | tRTP                                                     | tCK  | 1,6    |
|                   | Precharge All                                          | tRTP                                                     | tCK  | 1,6    |
| Read (BL32)       | Precharge<br>(to same bank as Read)                    | 8*tCK + tRTP                                             | tCK  | 1,6    |
|                   | Precharge All                                          | 8*tCK + tRTP                                             | tCK  | 1,6    |
| Read w/ AP (BL16) | Precharge<br>(to same bank as Read w/ AP)              | nRTP                                                     | tCK  | 1,10   |
|                   | Precharge All                                          | nRTP                                                     | tCK  | 1,10   |
|                   | Activate<br>(to same bank as Read w/ AP)               | nRTP + tRPpb                                             | tCK  | 1,8,10 |
|                   | Write or Write w/ AP<br>(same bank)                    | Illegal                                                  | -    | 3      |
|                   | Masked Write or Masked Write w/ AP<br>(same bank)      | Illegal                                                  | -    |        |
|                   | Write or Write w/ AP<br>(different bank)               | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRe           | tCK  | 3,4,5  |
|                   | Masked Write or Masked Write w/ AP<br>(different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRe           | tCK  | 3,4,5  |

| From Command        | To Command                                          | Minimum Delay between "From Command" and "To Command" | Unit | Notes  |
|---------------------|-----------------------------------------------------|-------------------------------------------------------|------|--------|
| Read w/ AP (BL16)   | Read or Read w/ AP (same bank)                      | Illegal                                               | -    |        |
|                     | Read or Read w/ AP (different bank)                 | BL/2                                                  | tCK  | 3      |
| Read w/ AP (BL32)   | Precharge (to same bank as Read w/ AP)              | 8*tCK + nRTP                                          | tCK  | 1,10   |
|                     | Precharge All                                       | 8*tCK + nRTP                                          | tCK  | 1,10   |
|                     | Activate (to same bank as Read w/ AP)               | 8*tCK + nRTP + tRPpb                                  | tCK  | 1,8,10 |
|                     | Write or Write w/ AP (same bank)                    | Illegal                                               | -    |        |
|                     | Masked Write or Masked Write w/ AP (same bank)      | Illegal                                               | -    |        |
|                     | Write or Write w/ AP (different bank)               | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE        | tCK  | 3,4,5  |
|                     | Masked Write or Masked Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE        | tCK  | 3,4,5  |
|                     | Read or Read w/ AP (same bank)                      | Illegal                                               | -    |        |
|                     | Read or Read w/ AP (different bank)                 | BL/2                                                  | tCK  | 3      |
| Write (BL16 & BL32) | Precharge (to same bank as Masked Write)            | WL + BL/2 + tWR + 1                                   | tCK  | 1,7    |
|                     | Precharge All                                       | WL + BL/2 + tWR + 1                                   | tCK  | 1,7    |
| Masked Write        | Precharge (to same bank as Masked Write)            | WL + BL/2 + tWR + 1                                   | tCK  | 1,7    |
|                     | Precharge All                                       | WL + BL/2 + tWR + 1                                   | tCK  | 1,7    |
| Write w/ AP         | Precharge (to same bank as Write w/ AP)             | WL + BL/2 + nWR + 1                                   | tCK  | 1,11   |
|                     | Precharge All                                       | WL + BL/2 + nWR + 1                                   | tCK  | 1,11   |
|                     | Activate (to same bank as Write w/ AP)              | WL + BL/2 + nWR + 1 + tRPpb                           | tCK  | 1,8,11 |
|                     | Write or Write w/ AP (same bank)                    | Illegal                                               | -    |        |
|                     | Write or Write w/ AP (different bank)               | BL/2                                                  | tCK  | 3      |
|                     | Masked-Write or Masked-Write w/ AP (different bank) | BL/2                                                  | tCK  | 3      |
|                     | Read or Read w/ AP (same bank)                      | Illegal                                               | -    |        |
|                     | Read or Read w/ AP (different bank)                 | WL + BL/2 + tWTR + 1                                  | tCK  | 3,9    |

| From Command       | To Command                                             | Minimum Delay between "From Command" and "To Command" | Unit | Notes  |
|--------------------|--------------------------------------------------------|-------------------------------------------------------|------|--------|
| Masked Write w/ AP | Precharge<br>(to same bank as Masked Write w/ AP)      | $WL + BL/2 + nWR + 1$                                 | tCK  | 1,11   |
|                    | Precharge all                                          | $WL + BL/2 + nWR + 1$                                 | tCK  | 1,11   |
|                    | Activate<br>(to same bank as Masked Write w/ AP)       | $WL + BL/2 + nWR + 1 + tRPpb$                         | tCK  | 1,8,11 |
|                    | Write or Write w/ AP<br>(same bank)                    | Illegal                                               | -    |        |
|                    | Masked Write or Masked Write w/ AP<br>(same bank)      | Illegal                                               | -    |        |
|                    | Write or Write w/ AP<br>(different bank)               | BL/2                                                  | tCK  | 3      |
|                    | Masked Write or Masked Write w/ AP<br>(different bank) | BL/2                                                  | tCK  | 3      |
|                    | Read or Read w/ AP (same bank)                         | Illegal                                               | -    |        |
|                    | Read or Read w/ AP (different bank)                    | $WL + BL/2 + tWTR + 1$                                | tCK  | 3,9    |
| Precharge          | Precharge<br>(to same bank as Precharge)               | 4                                                     | tCK  | 1      |
|                    | Precharge All                                          | 4                                                     | tCK  | 1      |
| Precharge All      | Precharge                                              | 4                                                     | tCK  | 1      |
|                    | Precharge All                                          | 4                                                     | tCK  | 1      |

#### Notes

- For a given bank, the precharge period should be counted from the latest precharge command, whether per-bank or all-bank, issued to that bank. The precharge period is satisfied tRP after that latest precharge command.
- Any command issued during the minimum delay time as specified in the table above is illegal.
- After READ w/AP, seamless read operations to different banks are supported. After WRITE w/AP or Masked Write w/AP, seamless write operations to different banks are supported. READ, WRITE, and Masked Write operations may not be truncated or interrupted.
- tRPST values depend on MR1 OP[7] respectively
- tWPST values depend on MR1 OP[2] respectively
- Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRTP(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRTP[ns] / tCK[ns])
- Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWR[ns] / tCK[ns])
- Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRPpb(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRPpb[ns] / tCK[ns])
- Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWTR(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWTR[ns] / tCK[ns])
- For Read w/AP the value is nRTP which is defined in Mode Register 2.
- For Write w/AP the value is nWR which is defined in Mode Register 1.

**Table - Timing Between Commands (Precharge and Auto-Precharge) - DQ ODT is Enabled**

| From Command         | To Command                                             | Minimum Delay between "From Command" and "To Command"                           | Unit | Notes |
|----------------------|--------------------------------------------------------|---------------------------------------------------------------------------------|------|-------|
| Read w/ AP<br>(BL16) | Write or Write w/ AP<br>(different bank)               | $RL + RU(tDQCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon, min/tCK) + 1$ | tCK  | 2,3   |
|                      | Masked Write or Masked Write w/ AP<br>(different bank) | $RL + RU(tDQCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon, min/tCK) + 1$ | tCK  | 2,3   |
| Read w/ AP<br>(BL32) | Write or Write w/ AP<br>(different bank)               | $RL + RU(tDQCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon, min/tCK) + 1$ | tCK  | 2,3   |
|                      | Masked Write or Masked Write w/ AP<br>(different bank) | $RL + RU(tDQCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon, min/tCK) + 1$ | tCK  | 2,3   |

#### Notes

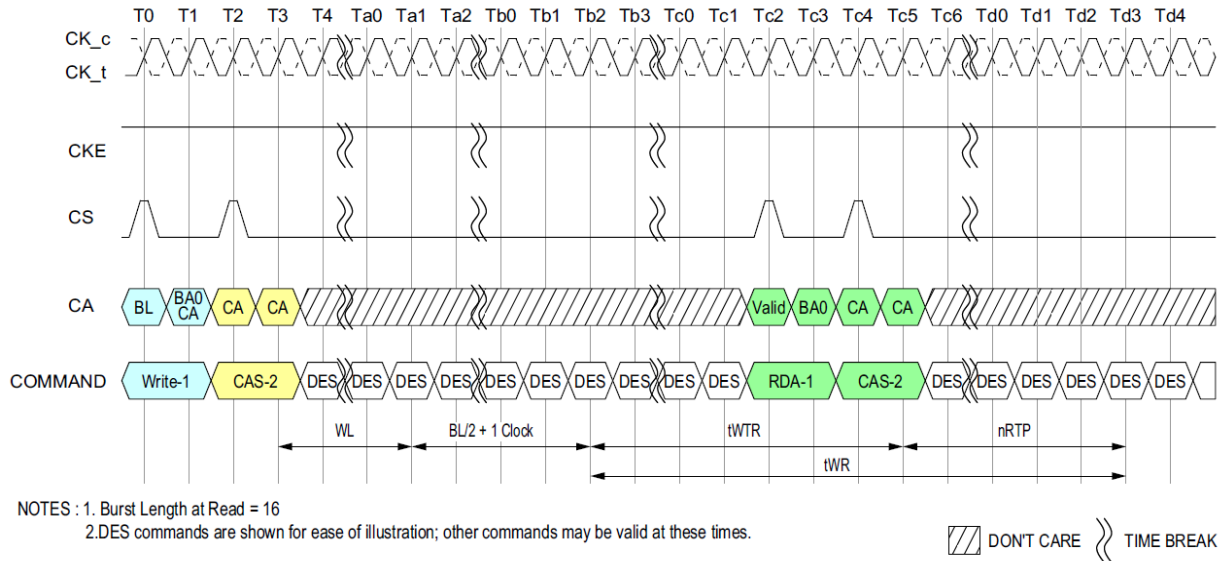
- The rest of Precharge and Auto-Precharge timings are as same as DQ ODT disabled case.
- After READ w/AP, seamless read operations to different banks are supported. READ, WRITE, and Masked Write operations may

not be truncated or interrupted.

3. tRPST values depend on MR1 OP[7] respectively.

### 2.13.3.3. Delay Time from Write to Read with Auto Precharge

In the case of write command followed by read with auto-precharge, controller must satisfy tWR for the write command before initiating the DRAM internal auto-precharge. It means that (tWTR + nRTP) should be equal or longer than (tWR) when BL setting is 16, as well as (tWTR + nRTP + 8nCK) should be equal or longer than (tWR) when BL setting is 32. Refer to the following figure for details.



### 2.14. Refresh command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of the clock. Per-bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. All-bank REFRESH is initiated with CA5 HIGH at the first rising edge of the clock.

A per-bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1 and CA2 at the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1 and bank address BA2 is transferred on CA2. A per-bank REFRESH command (REFpb) to the eight banks can be issued in any order. e.g. REFpb commands are issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per-bank REFRESH command the controller can send another set of per-bank REFRESH commands in the same order or a different order. e.g. REFpb commands are issued in the following order that is different from the previous order: 7-1-3-5-0-4-2-6. One of the possible order can also be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all eight banks have been refreshed using the per-bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. REFab command also synchronizes

the counter between the controller and SDRAM to zero. The SDRAM device can be placed in self-refresh or a REFab command can be issued at any time without cycling through all eight banks using per-bank REFRESH command. After the bank count is synchronized to zero the controller can issue per-bank REFRESH commands in any order as described in the previous paragraph.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the DRAM will perform refreshes to all banks as indicated by the row counter. If another refresh command (REFab or REFpb) is issued after the REFab command then it uses an incremented value of the row counter.

The table below shows examples of both bank and refresh counter increment behavior.

**Table - Bank and Refresh counter increment behavior**

| #    | Sub # | Command             | BA0 | BA1 | BA2 | Refresh Bank# | Bank Counter # | Ref Counter #<br>(Row Address #) |
|------|-------|---------------------|-----|-----|-----|---------------|----------------|----------------------------------|
| 0    | 0     | Reset, SRX or REFab |     |     |     |               | To 0           | -                                |
| 1    | 1     | REFpb               | 0   | 0   | 0   | 0             | 0 to 1         | n                                |
| 2    | 2     | REFpb               | 0   | 0   | 1   | 1             | 1 to 2         |                                  |
| 3    | 3     | REFpb               | 0   | 1   | 0   | 2             | 2 to 3         |                                  |
| 4    | 4     | REFpb               | 0   | 1   | 1   | 3             | 3 to 4         |                                  |
| 5    | 5     | REFpb               | 1   | 0   | 0   | 4             | 4 to 5         |                                  |
| 6    | 6     | REFpb               | 1   | 0   | 1   | 5             | 5 to 6         |                                  |
| 7    | 7     | REFpb               | 1   | 1   | 0   | 6             | 6 to 7         |                                  |
| 8    | 8     | REFpb               | 1   | 1   | 1   | 7             | 7 to 0         |                                  |
| 9    | 1     | REFpb               | 1   | 1   | 0   | 6             | 0 to 1         | n + 1                            |
| 10   | 2     | REFpb               | 1   | 1   | 1   | 7             | 1 to 2         |                                  |
| •    |       |                     |     |     |     |               |                |                                  |
| 15   | 7     | REFpb               | 0   | 0   | 0   | 0             | 6 to 7         |                                  |
| 16   | 8     | REFpb               | 1   | 0   | 0   | 4             | 7 to 0         |                                  |
| 17   | 1     | REFpb               | 0   | 0   | 0   | 0             | 0 to 1         | n + 2                            |
| 18   | 2     | REFpb               | 0   | 0   | 1   | 1             | 1 to 2         |                                  |
| 19   | 3     | REFpb               | 0   | 1   | 0   | 2             | 2 to 3         |                                  |
| 24   | 0     | REFab               | V   | V   | V   | 0~7           | To 0           | n + 2                            |
| 25   | 1     | REFpb               | 1   | 1   | 0   | 6             | 0 to 1         | n + 3                            |
| 26   | 2     | REFpb               | 1   | 1   | 1   | 7             | 1 to 2         |                                  |
| Snip |       |                     |     |     |     |               |                |                                  |

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after the prior PRECHARGE command to that bank
- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a dif-

ferent bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time ( $t_{RFCpb}$ ), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met:

- $t_{RFCpb}$  must be satisfied before issuing a REFab command
- $t_{RFCpb}$  must be satisfied before issuing an ACTIVATE command to the same bank
- $t_{RRD}$  must be satisfied before issuing an ACTIVATE command to a different bank
- $t_{RFCpb}$  must be satisfied before issuing another REFpb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- $t_{RFCab}$  has been satisfied following the prior REFab command
- $t_{RFCpb}$  has been satisfied following the prior REFpb command
- $t_{RP}$  has been satisfied following the prior PRECHARGE commands.

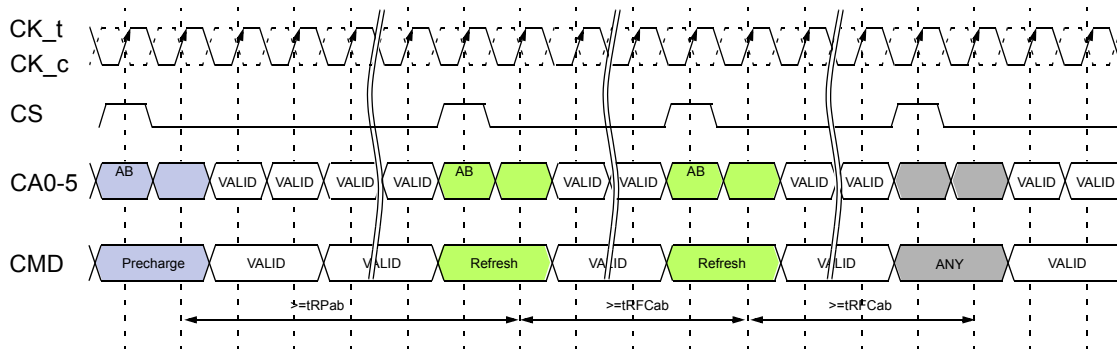
When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

- $t_{RFCab}$  latency must be satisfied before issuing an ACTIVATE command
- $t_{RFCab}$  latency must be satisfied before issuing a REFab or REFpb command.

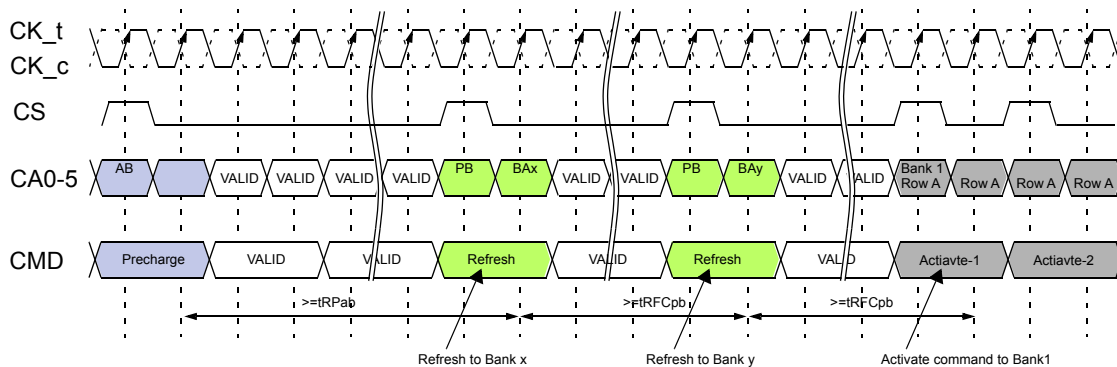
**Table - REFRESH Command Scheduling Separation requirements**

| Symbol                                                                                                                                                                                    | minimum delay from | to                                                             | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|----------------------------------------------------------------|-------|
| tRFCab                                                                                                                                                                                    | REFab              | REFab                                                          |       |
|                                                                                                                                                                                           |                    | Activate command to any bank                                   |       |
|                                                                                                                                                                                           |                    | REFpb                                                          |       |
| tRFCpb                                                                                                                                                                                    | REFpb              | REFab                                                          |       |
|                                                                                                                                                                                           |                    | Activate command to same bank as REFpb                         |       |
|                                                                                                                                                                                           |                    | REFpb                                                          |       |
| tRRD                                                                                                                                                                                      | REFpb              | Activate command to different bank than REFpb                  |       |
|                                                                                                                                                                                           | Activate           | REFpb                                                          | 1     |
|                                                                                                                                                                                           |                    | Activate command to different bank than prior Activate command |       |
| Note:                                                                                                                                                                                     |                    |                                                                |       |
| 1. A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state. |                    |                                                                |       |

**Figure - All-Bank REFRESH Operation**



**Figure - Per-Bank REFRESH Operation**



1. Operations to banks other than the bank being refreshed are supported during the tRFCpb period.

In general, a Refresh command needs to be issued to the LPDDR4 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR4 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed and maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in the table below. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to  $9 \times tREFI$ . A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to  $9 \times tREFI$ . At any given time, a maximum of 16 REF commands can be issued within  $2 \times tREFI$ .

Self-Refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

**Table - Legacy Refresh Command Timing Constraints**

| MR4 OP[2:0] | Refresh rate     | Max. No. of pulled in or postponed REFab | Max. interval between two REFab | Max. No. of REFab within $\max(2 \times t_{\text{REFI}} \times \text{Refresh rate multiplier}, 16 \times t_{\text{RFC}})$ | Per-bank Refresh |
|-------------|------------------|------------------------------------------|---------------------------------|---------------------------------------------------------------------------------------------------------------------------|------------------|
| 000B        | Low Temp. Limit  | N/A                                      | N/A                             | N/A                                                                                                                       | N/A              |
| 001B        | 4 x tREFI        | 8                                        | 9 x 4 x tREFI                   | 16                                                                                                                        | 1/8 of REFab     |
| 010B        | 2 x tREFI        | 8                                        | 9 x 2 x tREFI                   | 16                                                                                                                        | 1/8 of REFab     |
| 011B        | 1 x tREFI        | 8                                        | 9 x tREFI                       | 16                                                                                                                        | 1/8 of REFab     |
| 100B        | 0.5 x tREFI      | 8                                        | 9 x 0.5 x tREFI                 | 16                                                                                                                        | 1/8 of REFab     |
| 101B        | 0.25 x tREFI     | 8                                        | 9 x 0.25 x tREFI                | 16                                                                                                                        | 1/8 of REFab     |
| 110B        | 0.25 x tREFI     | 8                                        | 9 x 0.25 x tREFI                | 16                                                                                                                        | 1/8 of REFab     |
| 111B        | High Temp. Limit | N/A                                      | N/A                             | N/A                                                                                                                       | N/A              |

**Table - Modified Refresh Command Timing Constraints**

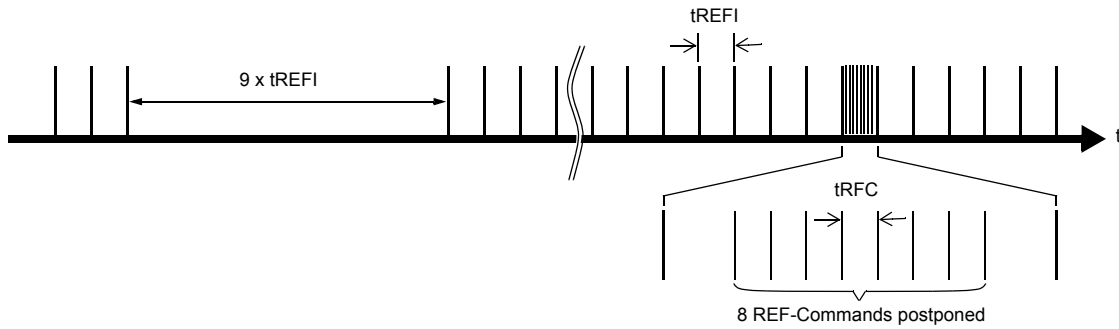
| MR4 OP[2:0] | Refresh rate     | Max. No. of pulled in or postponed REFab | Max. interval between two REFab | Max. No. of REFab within $\max(2 \times t_{\text{REFI}} \times \text{Refresh rate multiplier}, 16 \times t_{\text{RFC}})$ | Per-bank Refresh |
|-------------|------------------|------------------------------------------|---------------------------------|---------------------------------------------------------------------------------------------------------------------------|------------------|
| 000B        | Low Temp. Limit  | N/A                                      | N/A                             | N/A                                                                                                                       | N/A              |
| 001B        | 4 x tREFI        | 2                                        | 3 x 4 x tREFI                   | 4                                                                                                                         | 1/8 of REFab     |
| 010B        | 2 x tREFI        | 4                                        | 5 x 2 x tREFI                   | 8                                                                                                                         | 1/8 of REFab     |
| 011B        | 1 x tREFI        | 8                                        | 9 x tREFI                       | 16                                                                                                                        | 1/8 of REFab     |
| 100B        | 0.5 x tREFI      | 8                                        | 9 x 0.5 x tREFI                 | 16                                                                                                                        | 1/8 of REFab     |
| 101B        | 0.25 x tREFI     | 8                                        | 9 x 0.25 x tREFI                | 16                                                                                                                        | 1/8 of REFab     |
| 110B        | 0.25 x tREFI     | 8                                        | 9 x 0.25 x tREFI                | 16                                                                                                                        | 1/8 of REFab     |
| 111B        | High Temp. Limit | N/A                                      | N/A                             | N/A                                                                                                                       | N/A              |

**Notes:**

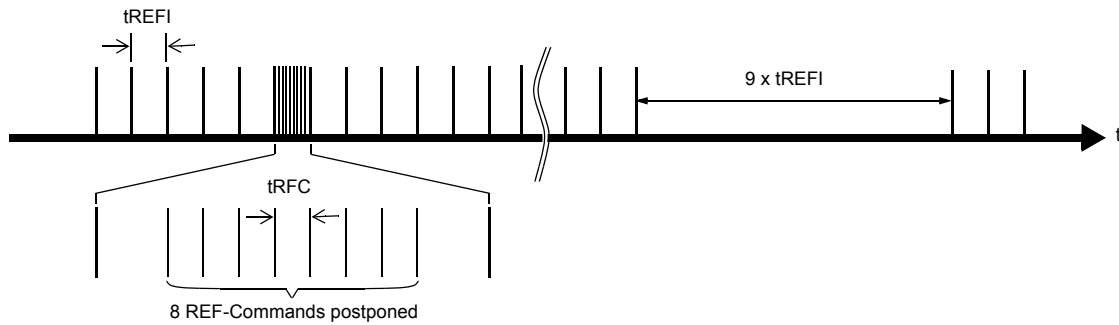
- For any thermal transition phase where Refresh mode is transitioned to either 2x tREFI or 4x tREFI, DRAM will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in refresh commands in previous thermal phase are not applied in new thermal phase. Entering new thermal phase the controller must count the number of pulled-in refresh commands as zero, regardless of remaining pulled-in refresh commands in previous thermal phase.
- LPDDR4 devices are refreshed properly if memory controller issues refresh commands with same or shorter refresh period than reported by MR4 OP[2:0]. If shorter refresh period is applied, the corresponding requirements from Table apply. For example, when MR4 OP[2:0]=001B, controller can be in any refresh rate from 4xtREFI to 0.25x tREFI. When MR4 OP[2:0]=010B, the only prohibited refresh rate is 4x tREFI.



**Figure - Postponing Refresh Commands (Example)**



**Figure - Pulling-in Refresh Commands (Example)**



## 2.15. LPDDR4 Refresh Requirements by Device Density

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the LPDDR4 DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

**Table - Refresh Requirement Parameters per die**

| Density                                  | Symbol | 4Gb     | 6Gb | 8Gb | 12Gb | 16Gb | Unit |
|------------------------------------------|--------|---------|-----|-----|------|------|------|
| Density per channel                      |        | 2Gb     | 3Gb | 4Gb | 6Gb  | 8Gb  | -    |
| Number of Banks                          |        | 8       |     |     |      |      | -    |
| Refresh Window<br>1 x tREFI              | tREFW  | 32      |     |     |      |      | ms   |
| Refresh Window<br>0.5 x tREFI            | tREFW  | 16      |     |     |      |      | ms   |
| Refresh Window<br>0.25 x tREFI           | tREFW  | 8       |     |     |      |      | ms   |
| Required number of REFRESH commands      | R      | 8,192   |     |     |      |      | -    |
| Average Refresh Interval<br>1 x tREFI    | REFab  | tREFI   |     |     |      |      | us   |
|                                          | REFpb  | tREFIpb |     |     |      |      | ns   |
| Average Refresh Interval<br>0.5 x tREFI  | REFab  | tREFI   |     |     |      |      | us   |
|                                          | REFpb  | tREFIpb |     |     |      |      | ns   |
| Average Refresh Interval<br>0.25 x tREFI | REFab  | tREFI   |     |     |      |      | us   |
|                                          | REFpb  | tREFIpb |     |     |      |      | ns   |
| Refresh Cycle Time (All Banks)           | tRFCab | 130     | 180 | 180 | 280  |      | ns   |
| Refresh Cycle Time (per Bank)            | tRFCpb | 60      | 90  | 90  | 140  |      | ns   |

Notes:

1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. Self refresh abort feature is available for higher density devices starting with 12 Gb device and tXSR\_abort(min) is defined as tRFCpb + 17.5ns.

## 2.16. Self Refresh Operation

### 2.16.1. Self Refresh Entry and Exit

The Self Refresh command can be used to retain data in the LPDDR4 SDRAM, the SDRAM retains data without external Refresh command. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh is entered by Self Refresh Entry Command defined by having CKE High, CS High, CA0 Low, CA1 Low, CA2 Low; CA3 High; CA4 High, CA5 Valid (Valid that means it is Logic Level, High or Low) for the first rising edge and CKE High, CS Low, CA0 Valid, CA1 Valid, CA2 Valid, CA3 Valid, CA4 Valid, CA5 Valid at the second rising edge of the clock. Self Refresh command is only allowed when SDRAM is idle state.

During Self Refresh mode, external clock input is needed and all input pin of SDRAM are activated.

SDRAM can accept the following commands, MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 except PASR Bank/Segment setting.

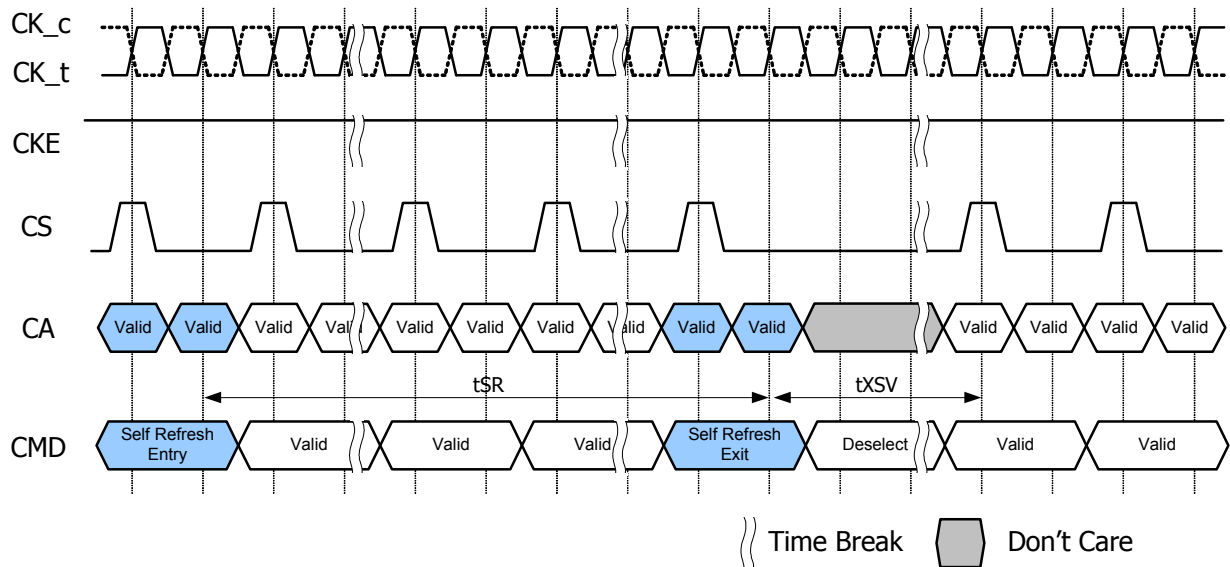
LPDDR4 SDRAM can operate in Self Refresh in both the standard or elevated temperature ranges. SDRAM will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperatures.

For proper Self Refresh operation, power supply pins (VDD1 and VDD2) must be at valid levels. VDDQ may be turned off during Self-Refresh after tESCKE is satisfied (Refer to Figure-Self Refresh Entry/Exit Timing with Power Down Entry/Exit for tESCKE).

Prior to exiting Self-Refresh VDDQ must be within specified limits. The minimum time that the SDRAM must remain in Self Refresh model is tSR,min.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when Self Refresh Exit is registered. Upon exit from Self Refresh, it is required that at least one REFRESH command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

**Figure - Self Refresh Entry/Exit Timing**

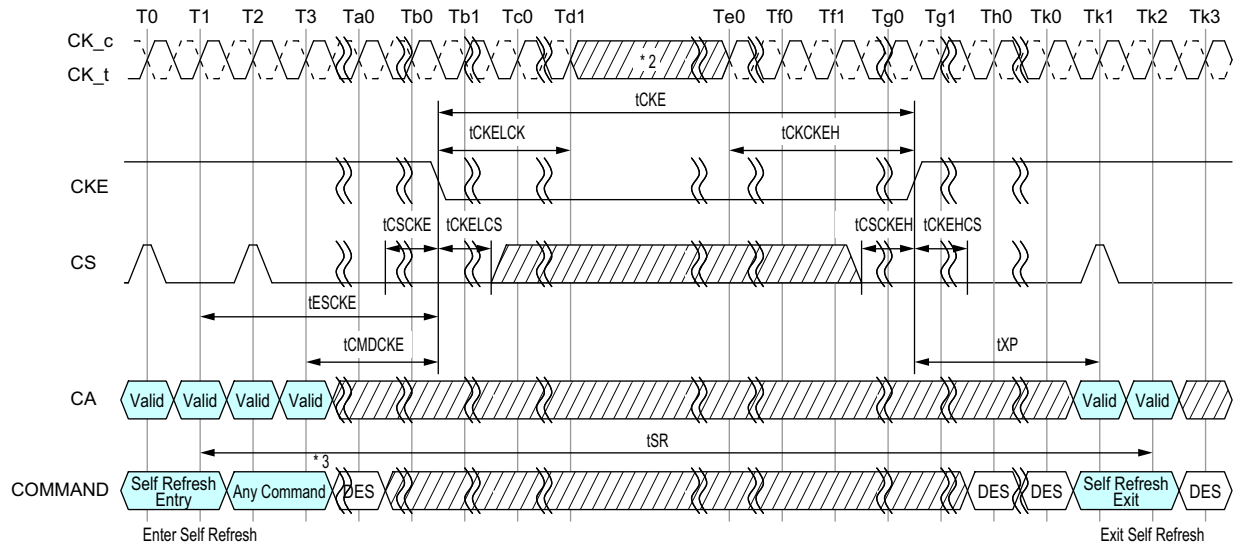


1. MRR-1, CAS-2, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. Address input may be don't care when input command is Deselect.

### 2.16.2. Power Down Entry and Exit during Self Refresh

Entering/Exiting Power Down Mode is allowed during Self Refresh mode in LPDDR4 SDRAM. The related timing parameters between Self Refresh Entry/Exit and Power Down Entry/Exit are shown in Figure-Self Refresh Entry/Exit Timing with Power Down Entry/Exit.

**Figure - Self Refresh Entry/Exit Timing with Power Down Entry/Exit**



**NOTES:**

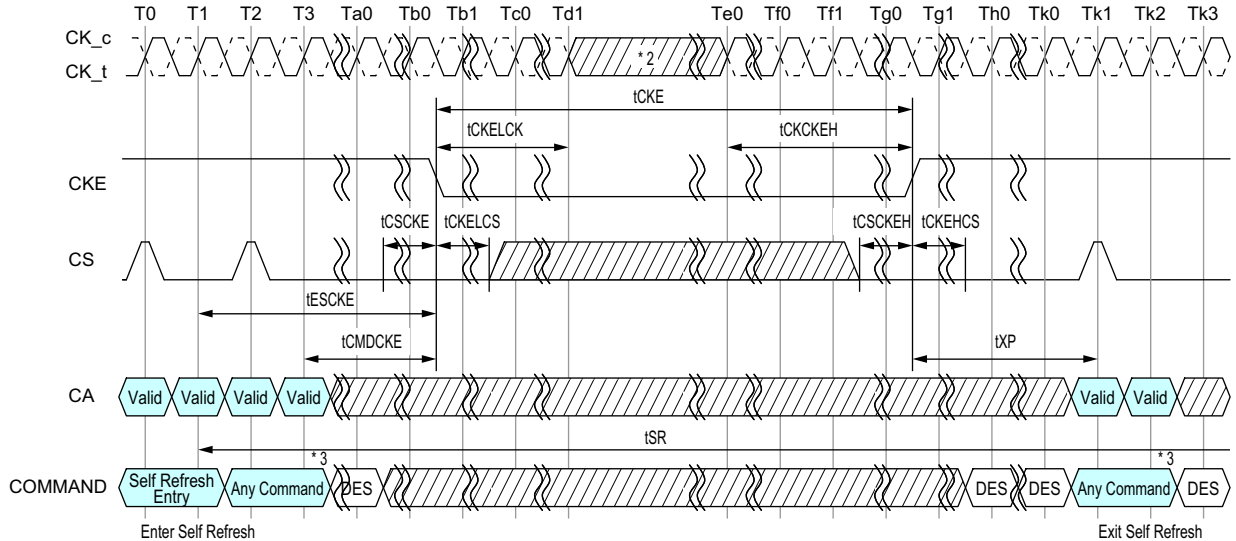
- MRR-1, CAS-2, DES, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
- Input clock frequency can be changed or the input clock can be stopped or floated after  $t_{CKELCK}$  satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of  $t_{CKCKEH}$  of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- 2 Clock command for example.

 DON'T CARE
  TIME BREAK

### 2.16.3. Command Input Timing after Power Down Exit

Command input timings after Power Down Exit during Self Refresh mode are shown in Figure-Command input timings after Power Down Exit during Self Refresh.

**Figure - Command input timings after Power Down Exit during Self Refresh**



**NOTES:**

1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. Input clock frequency can be changed or the input clock can be stopped or floated after tCKELCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
3. 2 Clock command for example.

 DON'T CARE
  TIME BREAK

### 2.16.4. Self Refresh Abort

If MR4 OP[3] is enabled then DRAM aborts any ongoing refresh during Self Refresh exit and does not increment the internal refresh counter. Controller can issue a valid command after a delay of tXSR\_abort instead of tXSR.

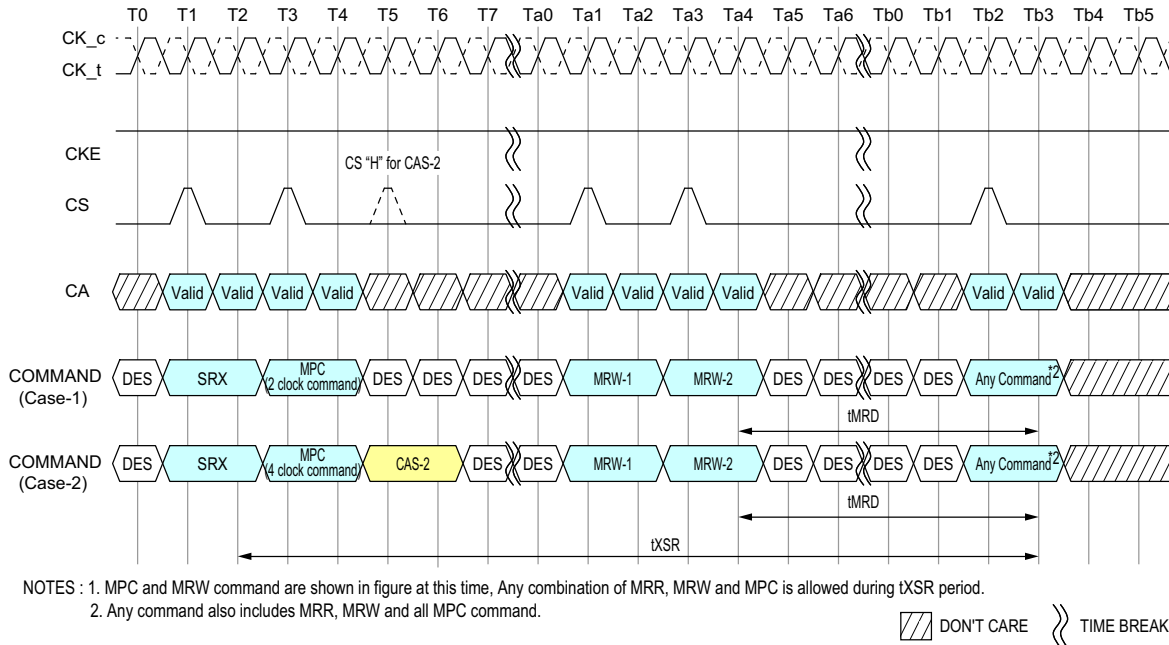
The value of tXSR\_abort(min) is defined as tRFCpb + 17.5 ns.

Upon exit from Self Refresh mode, the LPDDR4 SDRAM requires a minimum of one extra refresh (8 per bank or 1 all bank) before entry into a subsequent Self Refresh mode. This requirement remains the same irrespective of the setting of the MR bit for self refresh abort.

Self refresh abort feature is available for higher density devices starting with 12 Gb device.

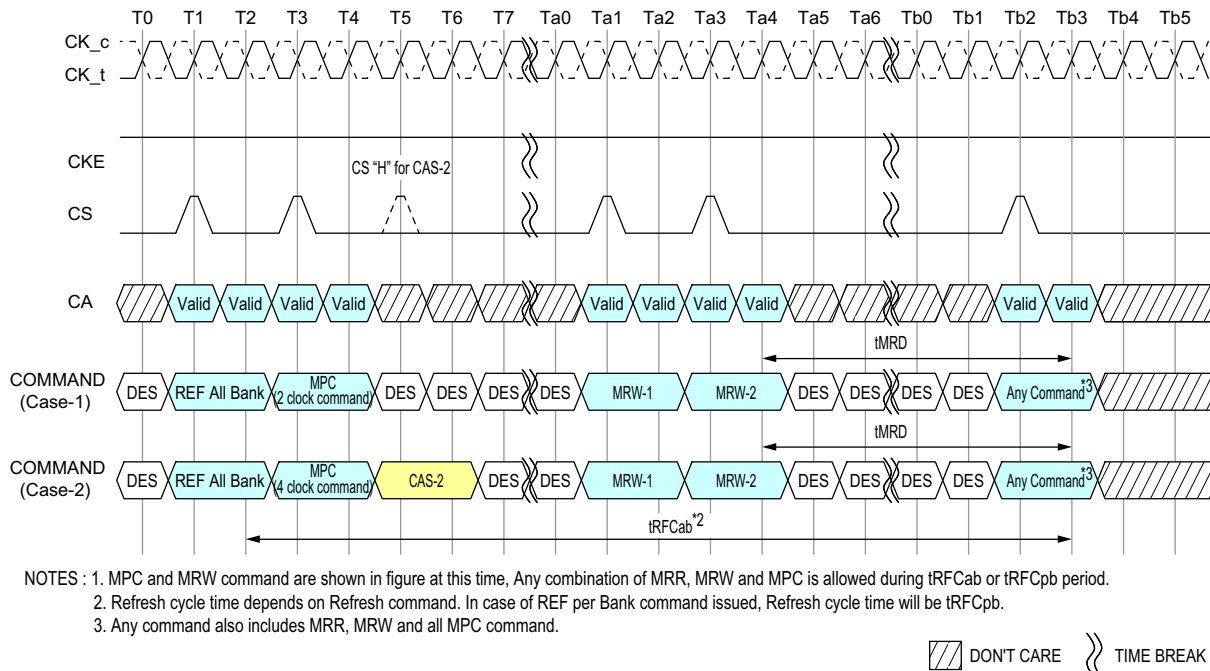
## 2.17. MRR, MRW, MPC Command during tXSR, tRFC

Mode Register Read (MRR), Mode Register Write (MRW) and Multi Purpose Command (MPC) can be issued during tXSR period.



**Figure - MRR, MRW and MPC Commands Issuing Timing during tXSR**

Mode Register Read (MRR), Mode Register Write (MRW) and Multi Purpose Command (MPC) can be issued during tRFC period.



**Figure - MRR, MRW and MPC Commands Issuing Timing during tRFC**

## 2.18. Mode Register Read (MRR) command

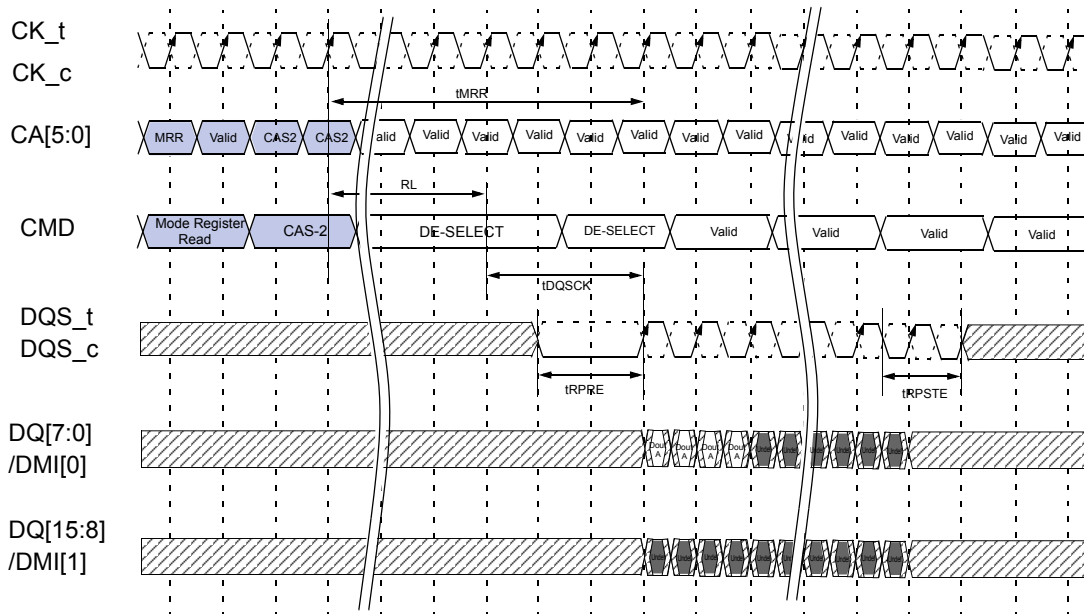
The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR4-SDRAM registers. The MRR command is initiated with CKE, CS and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) allow the user to select one of 64 registers. The mode register contents are available on the first 4UI's data bits of DQ[7:0] after  $RL \times t_{CK} + t_{DQSCK} + t_{DQSQ}$  following the MRR command. Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length 16. MRR operation must not be interrupted.

| BL  | 0 | 1   | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-----|---|-----|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| DQ0 |   | OP0 |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |
| DQ1 |   | OP1 |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |
| DQ2 |   | OP2 |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |
| DQ3 |   | OP3 |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |
| DQ4 |   | OP4 |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |
| DQ5 |   | OP5 |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |
| DQ6 |   | OP6 |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |
| DQ7 |   | OP7 |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |
| DMI |   |     |   |   |   |   |   |   |   |   | V  |    |    |    |    |    |

Notes:

1. MRR data are extended to first 4 UI's for DRAM controller to sample data easily.
2. DBI may apply or may not apply during normal MRR. It's vendor specific. If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DBI pin status should be low.
3. The read pre-amble and post-amble of MRR are same as normal read.

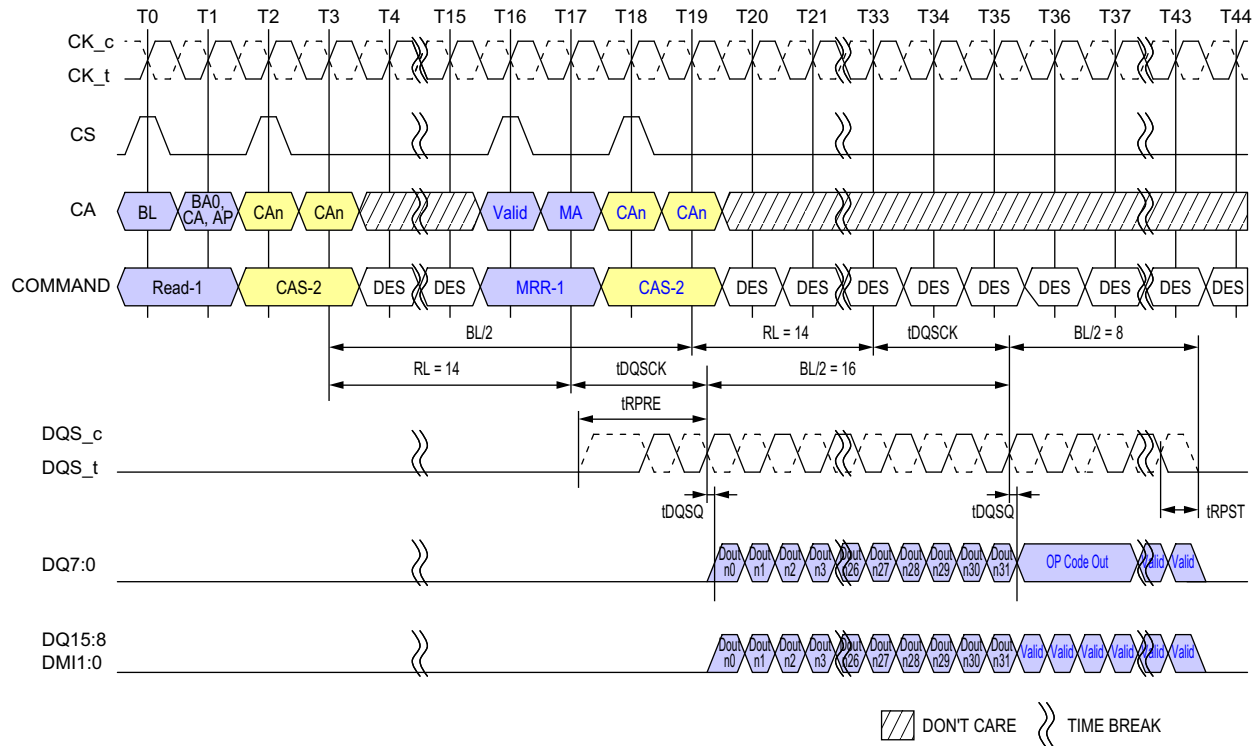
**Figure - Mode Register Read Operation**



1. Only BL=16 is supported.
2. Only De-Select is allowed during tMRR period.

### 2.18.1. MRR after Read and Write command

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, in a similar way WL + BL/2 + 1 + RU(tWTR/tCK) clock cycles after a prior Write, Write with AP, Mask Write, Mask Write with AP and MPC Write FIFO command in order to avoid the collision of Read and Write burst data on SDRAM's internal Data bus.

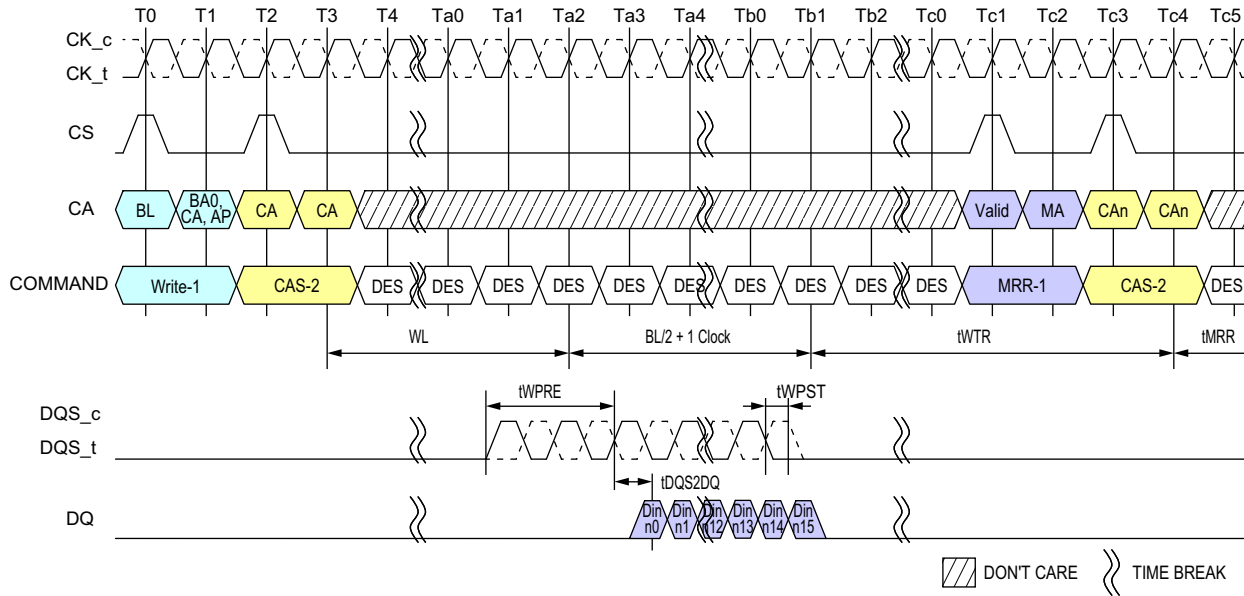


### Note

1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Read BL = 32, MRR BL = 16, RL = 14, Preamble = Toggle, Postamble = 0.5nCK, DBI = Disable, DQ/DQS: VSSQ termination
3. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

### Figure - Read to MRR Timing





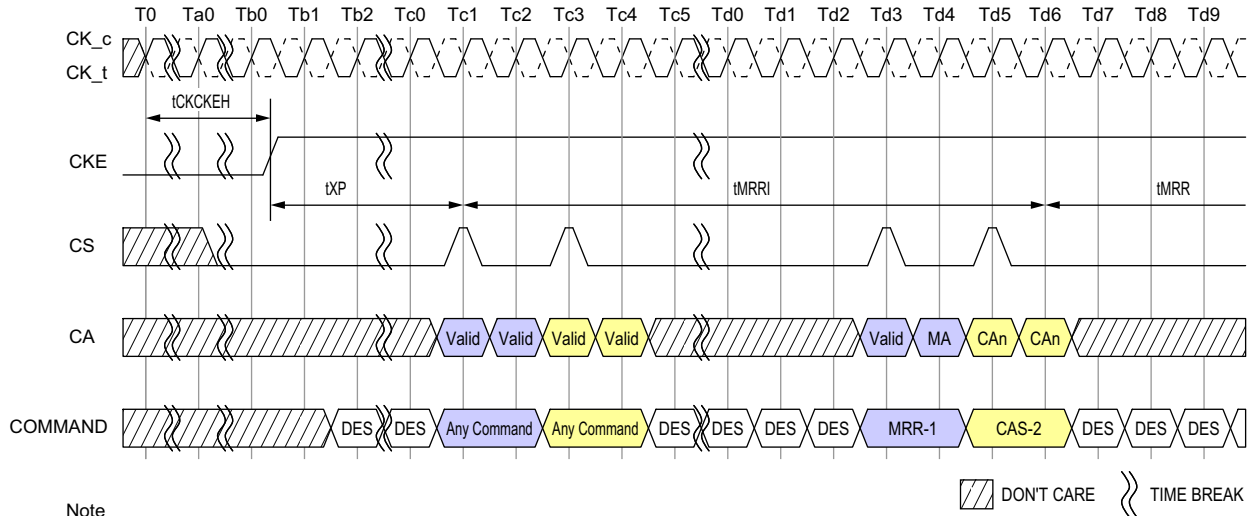
**Note**

1. Write BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Only DES is allowed during tMRR period.
3. Din n = data-in to columnm.n.
4. The minimum number of clock cycles from the burst write command to MRR command is  $WL + BL/2 + 1 + RU(tWTR/tCK)$ .
5. tWTR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

**Figure - Write to MRR Timing**

### 2.18.2. MRR after Power-Down Exit

Following the power-down state, an additional time,  $t_{MRRI}$ , is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to  $t_{RCD}$ ) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power-down mode.



#### Note

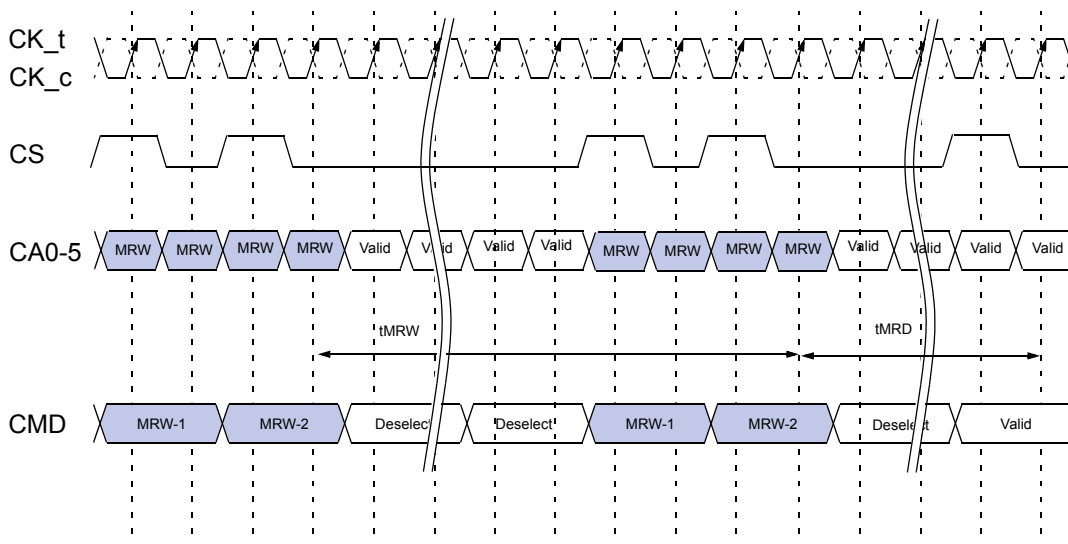
1. Only DES is allowed during  $t_{MRRI}$  period.
2. DES commands except  $t_{MRRI}$  period are shown for ease of illustration; other commands may be valid at these times.

**Figure - MRR Following Power-Down**

## 2.19. Mode Register Write (MRW) command

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CKE, CS, and CA[5:0] to valid levels at a rising edge of the clock (see Command Truth Table). The mode register address and the data written to the mode registers is contained in CA[5:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode register Writes to read-only registers have no impact on the functionality of the device.

**Figure - Mode Register Write Timing**



1. Only De-select command is allowed during tMRW and tMRD periods

### 2.19.1. Mode Register Write

MRW can be issued from either a Bank-Idle or Bank-Active state. Certain restrictions may apply for MRW from an Active state.

**Table - Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)**

| Current State  | Command | Intermediate State                        | Next State     |
|----------------|---------|-------------------------------------------|----------------|
| SDRAM          |         | SDRAM                                     | SDRAM          |
| All Banks Idle | MRR     | Mode Register Reading<br>(All Banks Idle) | All Banks Idle |
|                | MRW     | Mode Register Writing<br>(All Banks Idle) | All Banks Idle |
| Bank(s) Active | MRR     | Mode Register Reading                     | Bank(s) Active |
|                | MRW     | Mode Register Writing                     | Bank(s) Active |

**Table - MRR/MRW Timing Constraints : DQ ODT Disabled**

| From Command                  | To Command          | Minimum Delay between "From Command" and "To Command"                              | Unit | Notes |
|-------------------------------|---------------------|------------------------------------------------------------------------------------|------|-------|
| MRR                           | MRR                 | tMRR                                                                               | -    |       |
|                               | RD/RDA              | tMRR                                                                               | -    |       |
|                               | WR/WRA/<br>MWR/MWRA | $RL + RU(tDQSCK(max)/tCK) + BL/2 + 3 \cdot WL$                                     | nCK  |       |
|                               | MRW                 | $RL + RU(tDQSCK(max)/tCK) + BL/2 + 3$                                              | nCK  |       |
| RD/RDA                        | MRR                 | $BL/2$                                                                             | nCK  |       |
| WR/WRA/<br>MWR/MWRA           |                     | $WL + 1 + BL/2 + RU(tWTR/tCK)$                                                     | nCK  |       |
| MRW                           |                     | tMRD                                                                               | -    |       |
| Power Down Exit               |                     | tXP+tMRR                                                                           | -    |       |
| MRW                           | RD/RDA              | tMRD                                                                               | -    |       |
|                               | WR/WRA/<br>MWR/MWRA | tMRD                                                                               | -    |       |
|                               | MRW                 | tMRW                                                                               | -    |       |
| RD/<br>RD FIFO/<br>RD DQ CAL  | MRW                 | $RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + \max(RU(7.5ns/tCK), 8nCK)$            | nCK  |       |
| RD with<br>Auto-Precharge     |                     | $RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + \max(RU(7.5ns/tCK), 8nCK) + nRTP - 8$ | nCK  |       |
| WR/<br>MWR/<br>WR FIFO        |                     | $WL + 1 + BL/2 + \max(RU(7.5ns/tCK), 8nCK)$                                        | nCK  |       |
| WR/MWR with<br>Auto-Precharge |                     | $WL + 1 + BL/2 + \max(RU(7.5ns/tCK), 8nCK) + nWR$                                  | nCK  |       |

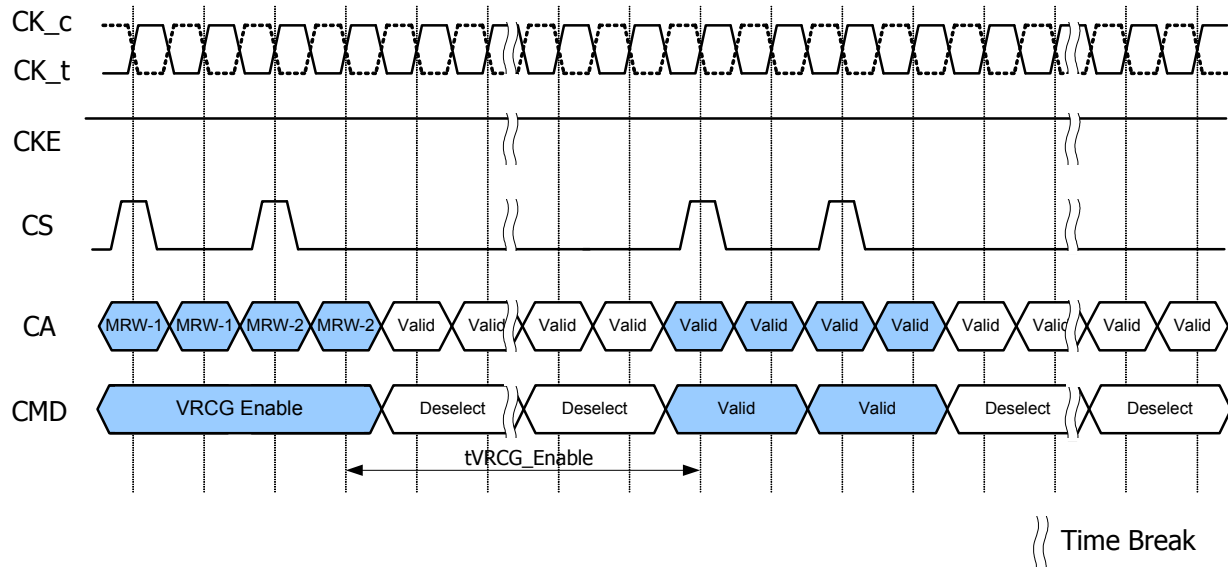
**Table - MRR/MRW Timing Constraints : DQ ODT Enabled**

| From Command                  | To Command              | Minimum Delay between "From Command" and "To Command"        | Unit | Notes |
|-------------------------------|-------------------------|--------------------------------------------------------------|------|-------|
| MRR                           | MRR                     | Same as ODT Disable Case                                     | -    |       |
|                               | RD/RDA                  |                                                              |      |       |
|                               | WR/WRA/<br>MWR/MWRA     | RL+RU(tDQSCK(max)/tCK)+BL/2+3<br>-ODTLon-RD(tODTon(min)/tCK) | nCK  |       |
|                               | MRW                     | Same as ODT Disable Case                                     | -    |       |
| RD/RDA                        | MRR                     | Same as ODT Disable Case                                     | -    |       |
| WR/WRA/<br>MWR/MWRA           |                         |                                                              |      |       |
| MRW                           |                         |                                                              |      |       |
| Power Down Exit               |                         |                                                              |      |       |
| MRW                           | RD/RDA                  | Same as ODT Disable Case                                     | -    |       |
|                               | WR/WRA/<br>MWR/<br>MWRA |                                                              |      |       |
|                               | MRW                     |                                                              |      |       |
| RD/<br>RD FIFO/<br>RD DQ CAL  | MRW                     | Same as ODT Disable Case                                     | -    |       |
| RD with<br>Auto-Precharge     |                         |                                                              |      |       |
| WR/<br>MWR/<br>WR FIFO        |                         |                                                              |      |       |
| WR/MWR with<br>Auto-Precharge |                         |                                                              |      |       |

## 2.20. Vref Current Generator (VRCG)

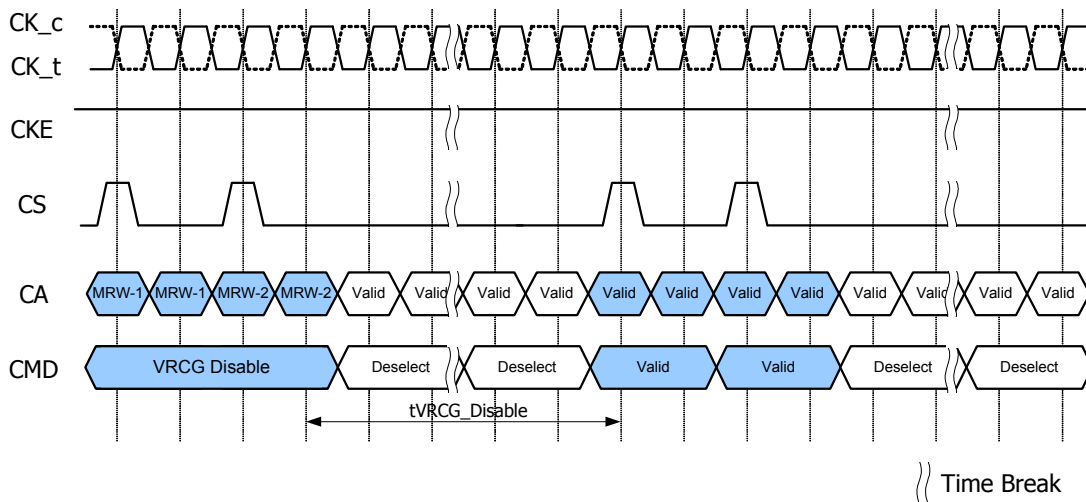
LPDDR4 SDRAM Vref current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal Vref(DQ) and Vref(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13[OP3] = 1. Only Deselect commands may be issued until tVRCG\_ENABLE is satisfied. tVRCG\_ENABLE timing is shown in figure below.

**Figure - VRCG Enable timing**



VRCG high current mode is disabled by setting MR13[OP3] = 0. Only Deselect commands may be issued until tVRCG\_DISABLE is satisfied. tVRCG\_DISABLE timing is shown in figure below.

**Figure - VRCG Disable timing**



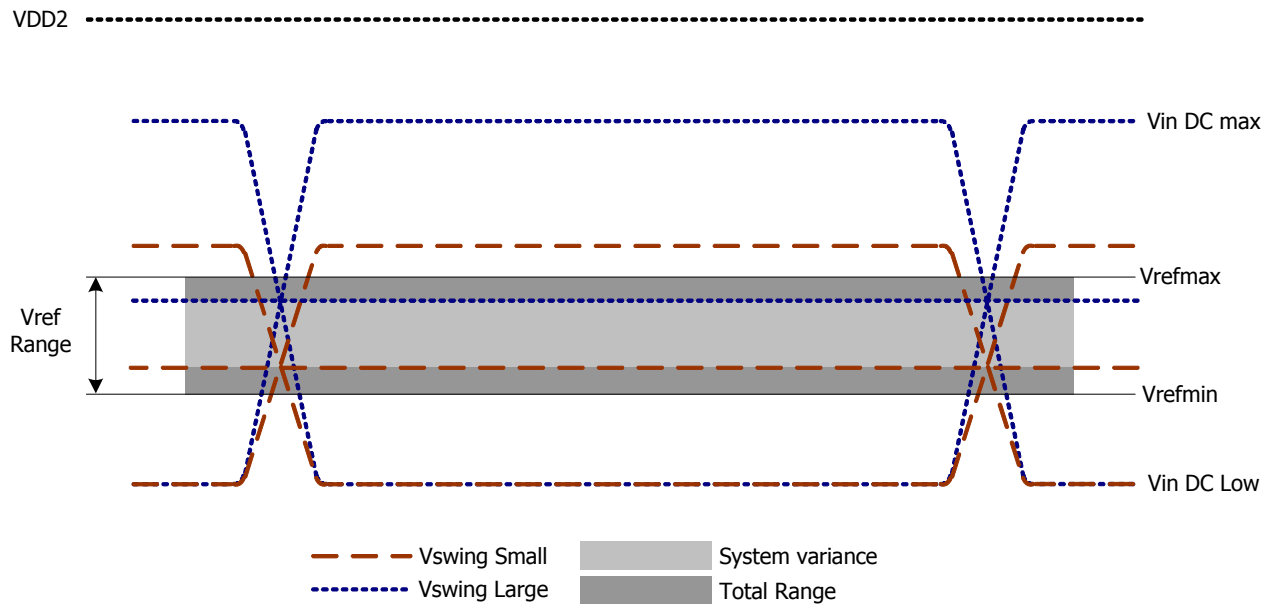
Note that LPDDR4 SDRAM devices support Vref(CA) and Vref(DQ) range and value changes without enabling VRCG high current mode.

## 2.21. CA Vref Training

The DRAM internal CA Vref specification parameters are voltage operating range, stepsize, Vref set tolerance, Vref step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for LPDDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure "Vref operating range (Vref.min, Vref.max)".

**Figure - Vref operating range (Vref.min, Vref.max)**

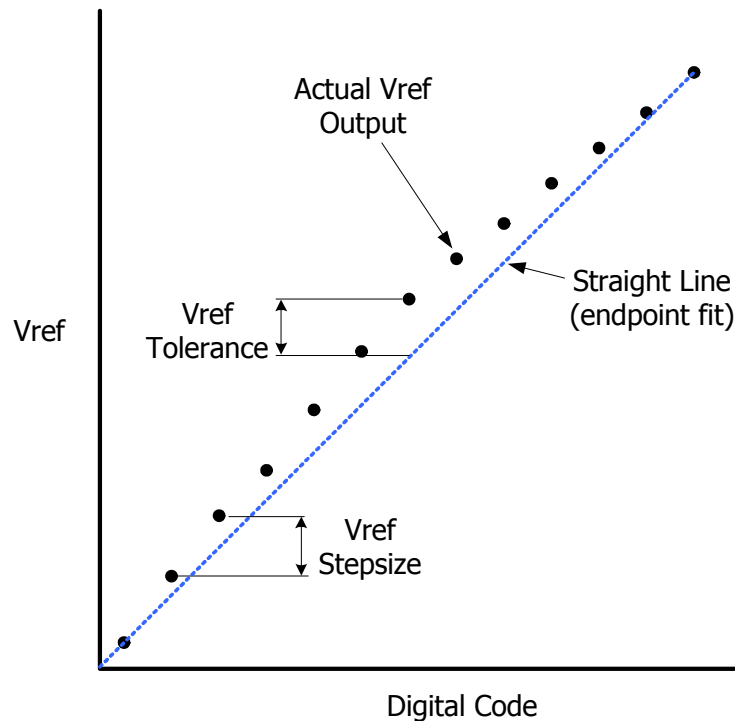


The Vref stepsize is defined as the stepsize between adjacent steps. Vref stepsize ranges from 0.3% VDD2 to 0.5%VDD2. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainty. The range of Vref set tolerance uncertainty is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

**Figure - Example of Vref set tolerance (max case only shown) and stepsize**



The Vref increment/decrement step times are defined by Vref\_time-short, middle and long. The Vref\_time-short, Vref\_time-middle and Vref\_time-long is defined from TS to TE as shown in the Figure "Vref\_time for short, middle and long timing diagram" below where TE is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance (Vref\_val\_tol).

The Vref valid level is defined by Vref\_val tolerance to qualify the step time TE as shown in Figure "Vref step single stepsize increment case". This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

Vref\_time-Short is for a single stepsize increment/decrement change in Vref voltage.

Vref\_time-Middle is at least 2 stepsizes increment/decrement change within the same VrefCA range in Vref voltage.

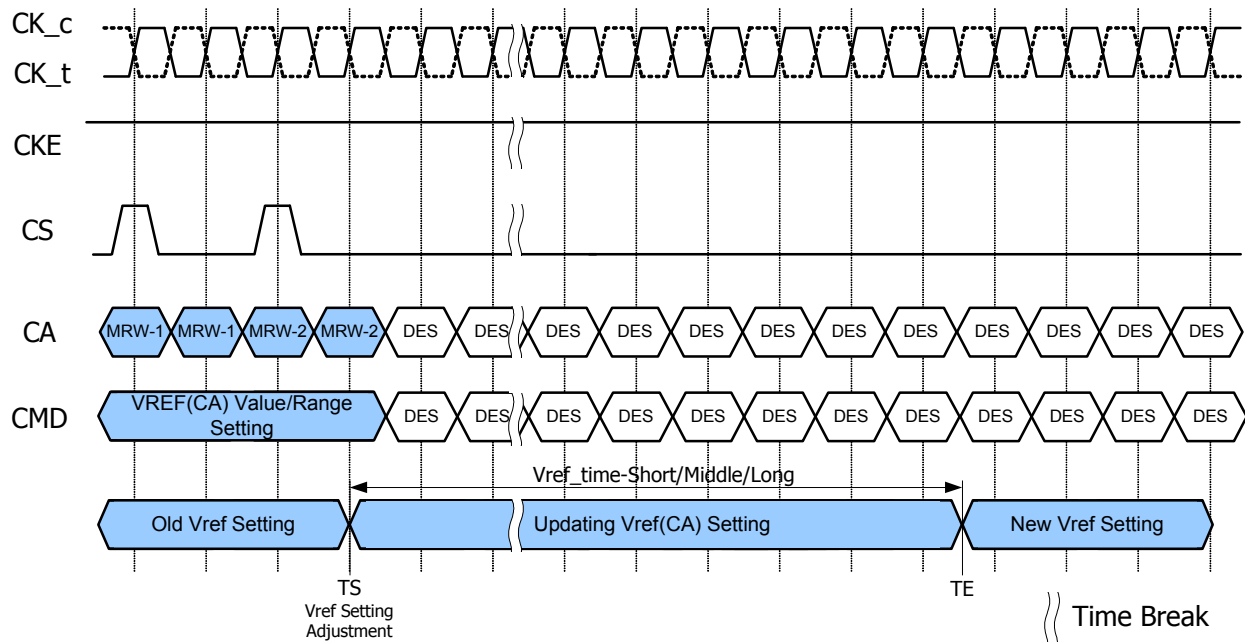
Vref\_time-Long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefCA Range in Vref voltage.

TS - is referenced to MRS command clock

TE - is referenced to the Vref\_val\_tol



**Figure - Vref\_time for short, middle and long timing diagram**

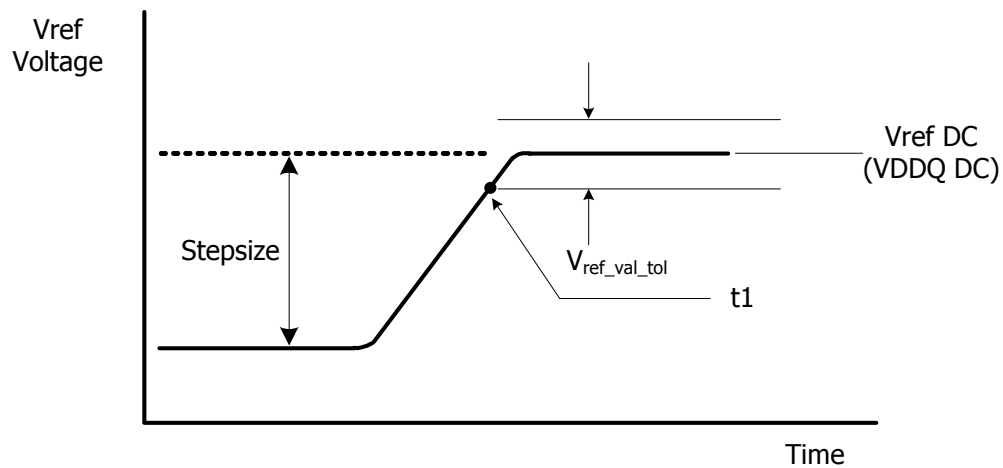


The MRW command to the mode register bits are as follows.

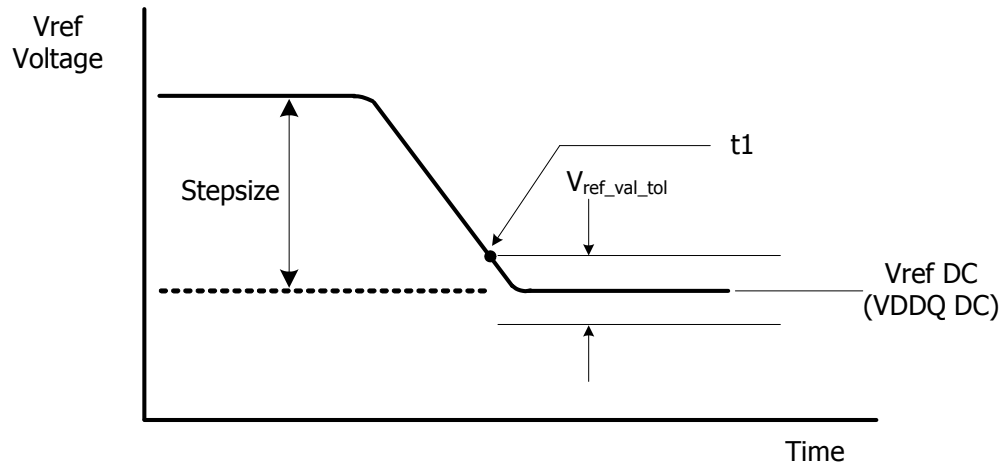
MR12 OP[5:0] : VREF(CA) Setting  
MR12 OP[6] : VREF(CA) Range

The minimum time required between two Vref MRS commands is Vref\_time-short for single step and Vref\_time-Middle for a full voltage range step.

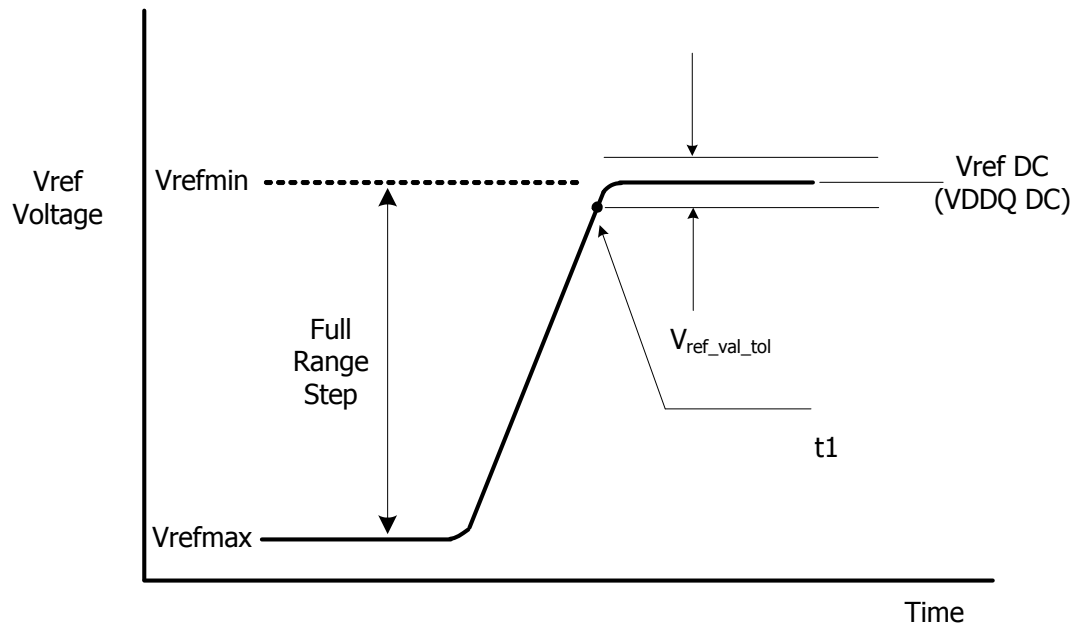
**Figure - Vref step single stepsize increment case**



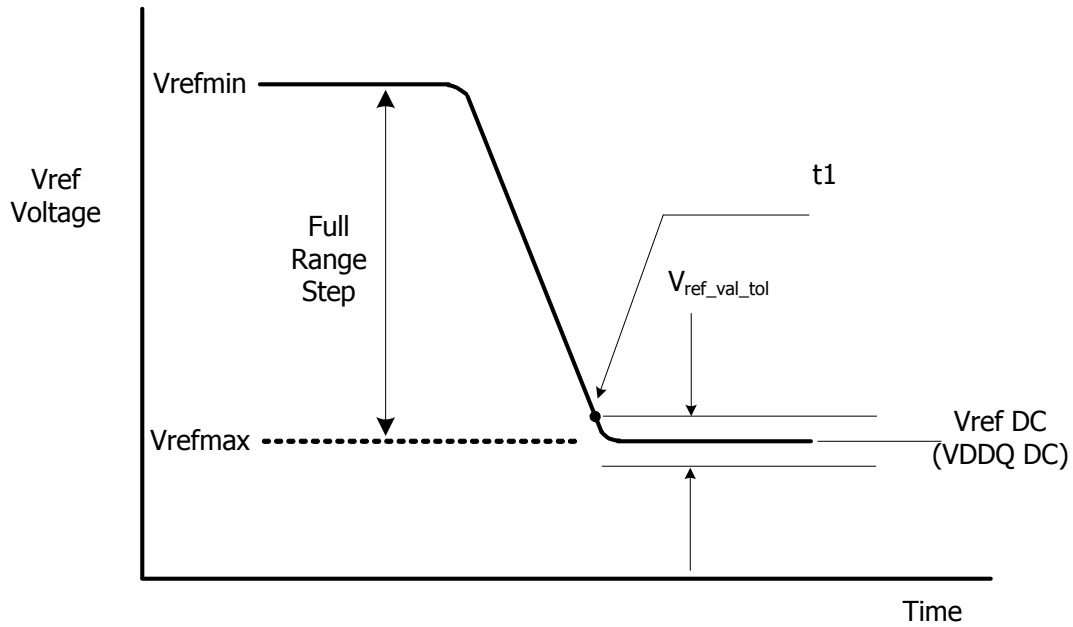
**Figure - Vref step single stepsize decrement case**



**Figure - Vref full step from Vrefmin to Vrefmax case**



**Figure - Vref full step from Vrefmax to Vrefmin case**



The table below contains the CA internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

**Table - CA Internal Vref Specifications**

| Parameter                         | Symbol           | Min.   | Typ.  | Max.  | Unit | Notes |
|-----------------------------------|------------------|--------|-------|-------|------|-------|
| Vref Max operating point Range[0] | Vref_max_R0      | -      | -     | 44.9% | VDDQ | 1,11  |
| Vref Min operating point Range[0] | Vref_min_R0      | 15%    | -     | -     | VDDQ | 1,11  |
| Vref Max operating point Range[1] | Vref_max_R1      | -      | -     | 62.9% | VDDQ | 1,11  |
| Vref Min operating point Range[1] | Vref_min_R1      | 32.9%  | -     | -     | VDDQ | 1,11  |
| Vref Stepsize                     | Vref_step        | 0.50%  | 0.60% | 0.70% | VDDQ | 2     |
| Vref Set Tolerance                | Vref_set_tol     | -11    | 0     | 11    | mV   | 3,4,6 |
|                                   |                  | -1.1   | 0     | 1.1   | mV   | 3,5,7 |
| Vref Step Time                    | Vref_time-short  | -      | -     | 100   | ns   | 8     |
|                                   | Vref_time-middle | -      | -     | 200   | ns   | 12    |
|                                   | Vref_time-Long   | -      | -     | 250   | ns   | 9     |
|                                   | Vref_time-weak   | -      | -     | 1     | ms   | 13,14 |
| Vref Valid tolerance              | Vref_val_tol     | -0.10% | 0.00% | 0.10% | VDDQ | 10    |

## Notes:

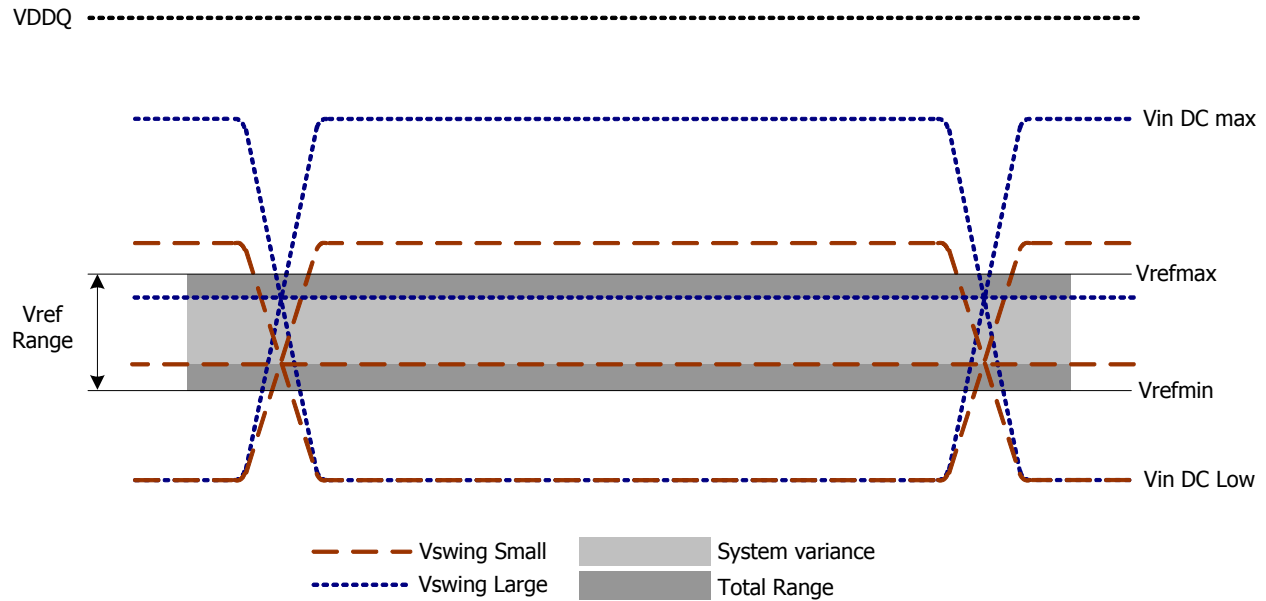
1. Vref DC voltage referenced to VDDQ\_DC.
2. Vref stepsize increment/decrement range. Vref at DC level.
3.  $Vref\_new = Vref\_old + n * Vref\_step$ ; n= number of steps; if increment use "+"; If decrement use "-".
4. The minimum value of Vref setting tolerance =  $Vref\_new - 11mV$ . The maximum value of Vref setting tolerance =  $Vref\_new + 11mV$ . For  $n > 4$
5. The minimum value of Vref setting tolerance =  $Vref\_new - 1.1mV$ . The maximum value of Vref setting tolerance =  $Vref\_new + 1.1mV$ . For  $n \leq 4$ .
6. Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.
7. Measured by recording the min and max values of the Vref output across 4 consecutive steps( $n=4$ ), drawing a straight line between those points and comparing all other Vref output settings to that line.
8. Time from MRS command to increment or decrement one step size for Vref.
9. Time from MRS command to increment or decrement Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefCA Range in Vref voltage.
10. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
11. DRAM range 0 or 1 set by MR12 OP[6].
12. Time from MRS command to increment or decrement more than one step size up a full range of Vref voltage within the same VrefCA range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 OP[3] = 0.
14. Vref\_time\_weak covers all Vref(CA) Range and Value change conditions are applied to Vref\_time\_Short/Middle/Long.

## 2.22. DQ Vref Training

The DRAM internal DQ Vref specification parameters are voltage operating range, stepsize, Vref set tolerance, Vref step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for LPDDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure "Vref operating range (Vref.min, Vref.max)".

**Figure - Vref operating range (Vref.min, Vref.max)**

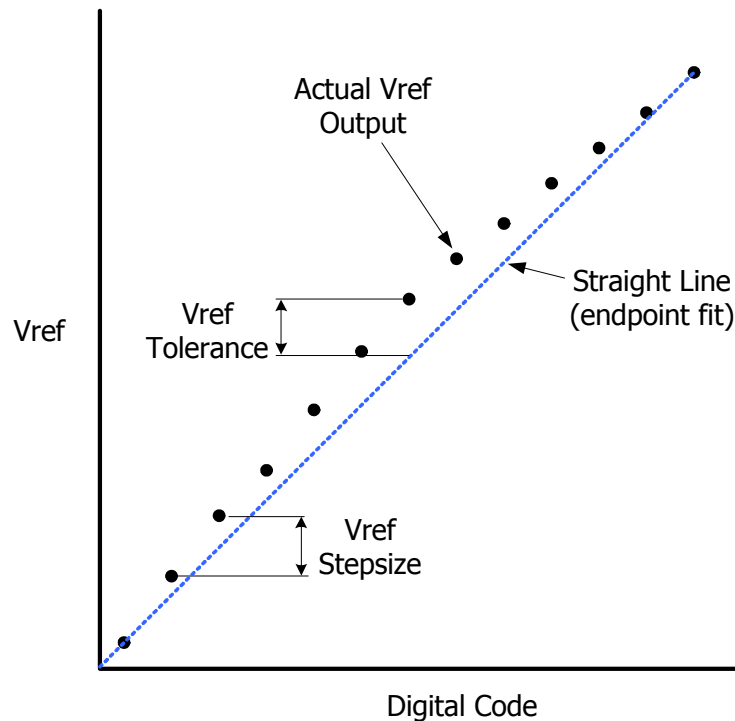


The Vref stepsize is defined as the stepsize between adjacent steps. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainty. The range of Vref set tolerance uncertainty is a function of number of steps  $n$ .

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

**Figure - Example of Vref set tolerance (max case only shown) and stepsize**



The Vref increment/decrement step times are defined by Vref\_time-short, middle and long. The Vref\_time-short, middle and Vref\_time-long is defined from TS to TE as shown in the Figure "Vref\_time for short and long timing diagram" below where TE is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance(Vref\_val\_tol).

The Vref valid level is defined by Vref\_val tolerance to qualify the step time TE as shown in Figure "Vref step single stepsize increment case". This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

Vref\_time-Short is for a single stepsize increment/decrement change in Vref voltage.

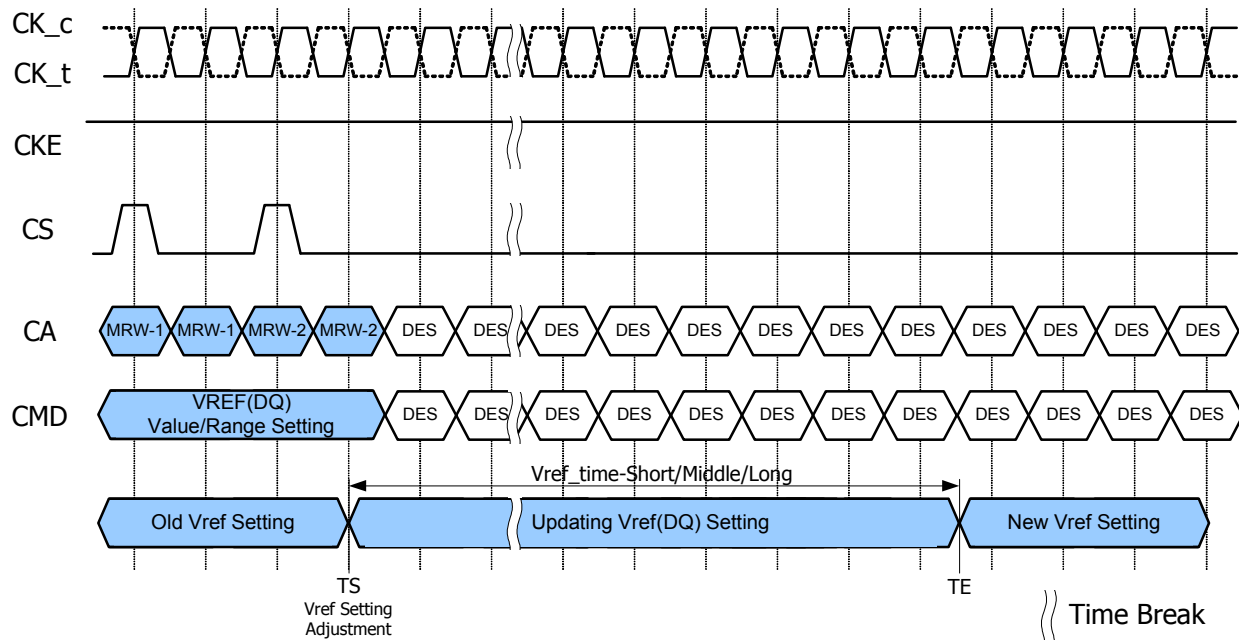
Vref\_time-Middle is at least 2 stepsizes increment/decrement change within the same VrefDQ range in Vref voltage.

Vref\_time-Long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefDQ Range in Vref voltage.

TS - is referenced to MRS command clock

TE - is referenced to the Vref\_val\_tol

**Figure - Vref\_time for short and long timing diagram**

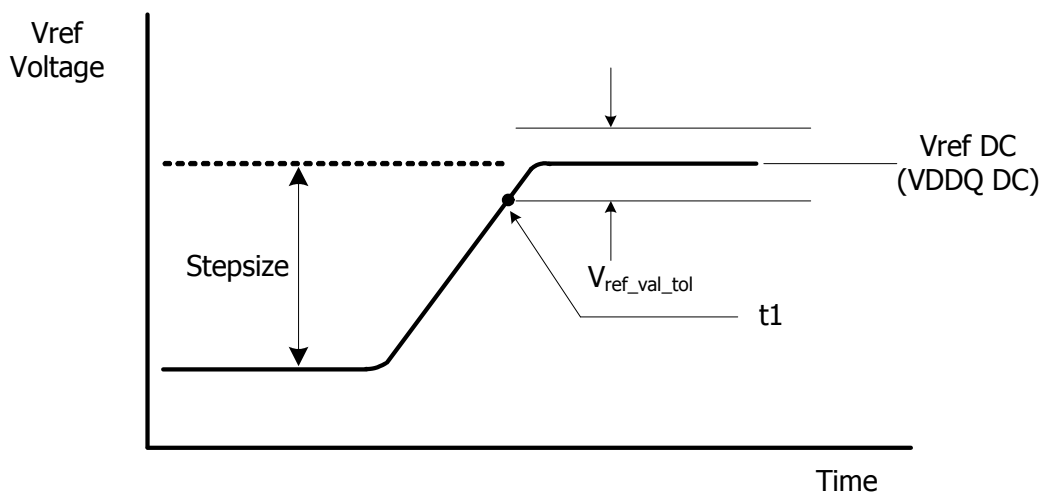


The MRW command to the mode register bits are as follows.

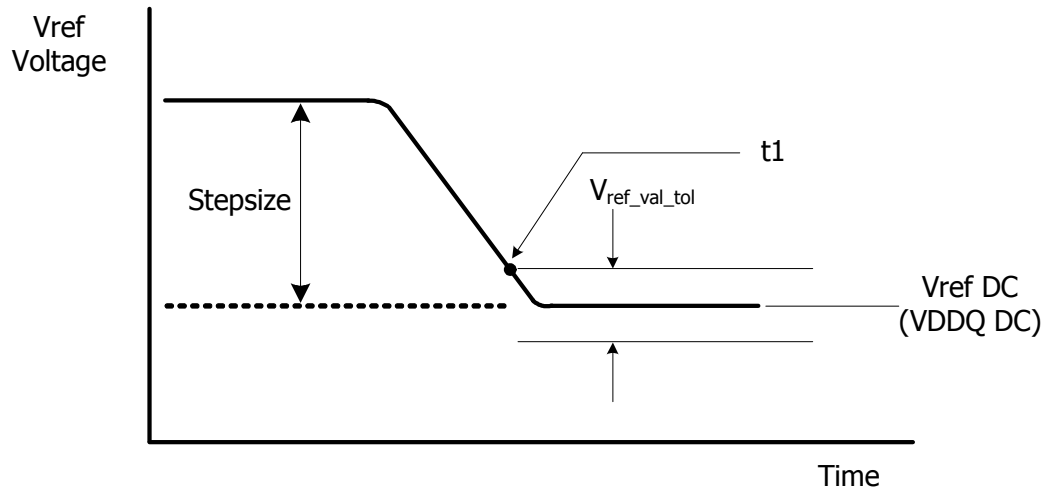
- MR14 OP[5:0] : VREF(DQ) Setting
- MR14 OP[6] : VREF(DQ) Range

The minimum time required between two Vref MRS commands is Vref\_time-short for single step and Vref\_time-Middle for a full voltage range step

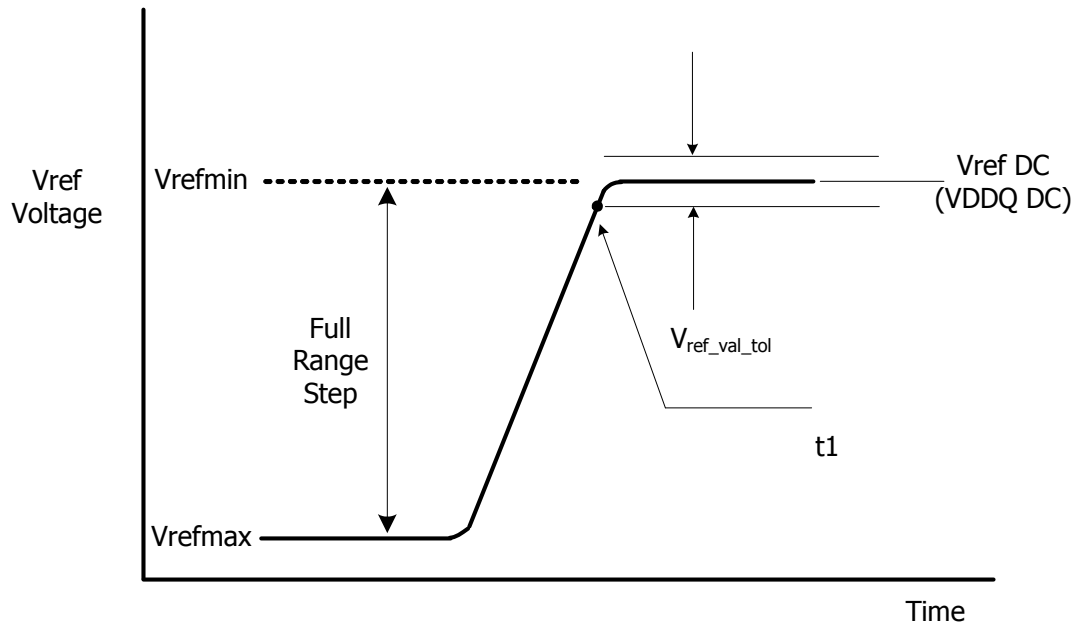
**Figure - Vref step single stepsize increment case**



**Figure - Vref step single stepsize decrement case**

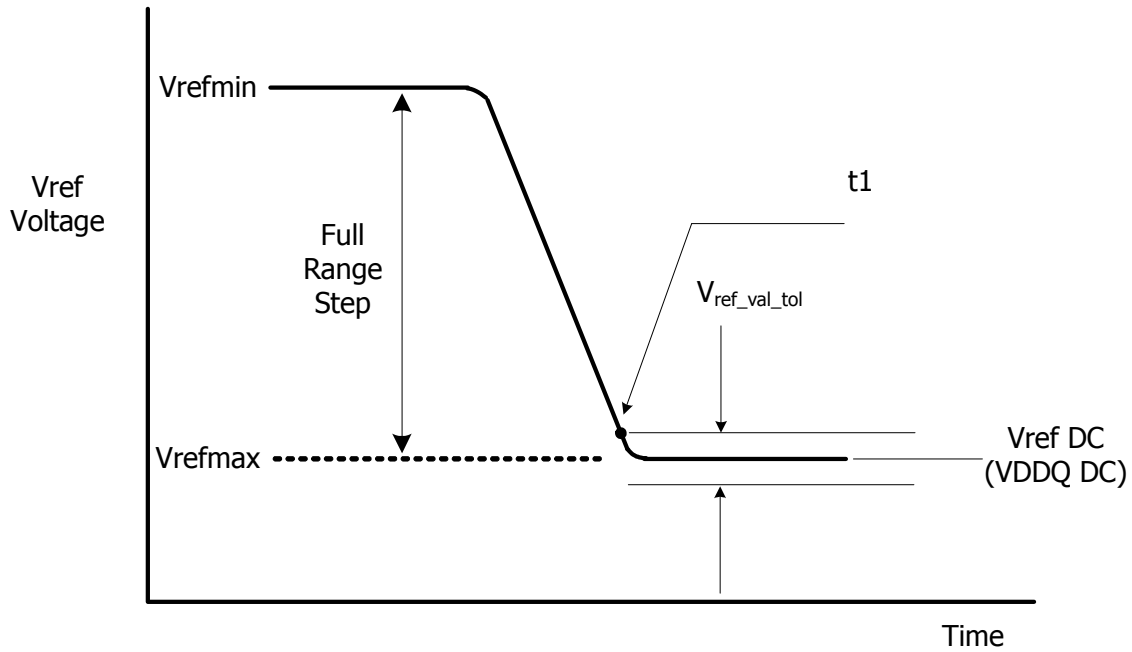


**Figure - Vref full step from Vrefmin to Vrefmax case**





**Figure - Vref full step from Vrefmax to Vrefmin case**



The table below contains the DQ internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

**Table - DQ Internal Vref Specifications**

| Parameter                         | Symbol           | Min.   | Typ.  | Max.  | Unit | Notes |
|-----------------------------------|------------------|--------|-------|-------|------|-------|
| Vref Max operating point Range[0] | Vref_max_R0      | -      | -     | 44.9% | VDDQ | 1,11  |
| Vref Min operating point Range[0] | Vref_min_R0      | 15%    | -     | -     | VDDQ | 1,11  |
| Vref Max operating point Range[1] | Vref_max_R1      | -      | -     | 62.9% | VDDQ | 1,11  |
| Vref Min operating point Range[1] | Vref_min_R1      | 32.9%  | -     | -     | VDDQ | 1,11  |
| Vref Stepsize                     | Vref_step        | 0.50%  | 0.60% | 0.70% | VDDQ | 2     |
| Vref Set Tolerance                | Vref_set_tol     | -11    | 0     | 11    | mV   | 3,4,6 |
|                                   |                  | -1.1   | 0     | 1.1   | mV   | 3,5,7 |
| Vref Step Time                    | Vref_time-short  | -      | -     | 100   | ns   | 8     |
|                                   | Vref_time-Middle | -      | -     | 200   | ns   | 12    |
|                                   | Vref_time-Long   | -      | -     | 250   | ns   | 9     |
|                                   | Vref_time-weak   | -      | -     | 1     | ms   | 13,14 |
| Vref Valid tolerance              | Vref_val_tol     | -0.10% | 0.00% | 0.10% | VDDQ | 10    |

**Notes:**

1. Vref DC voltage referenced to VDDQ\_DC.
2. Vref stepsize increment/decrement range. Vref at DC level.
3.  $Vref\_new = Vref\_old + n \cdot Vref\_step$ ; n= number of steps; if increment use "+"; If decrement use "-".
4. The minimum value of Vref setting tolerance =  $Vref\_new - 11mV$ . The maximum value of Vref setting tolerance =  $Vref\_new + 11mV$ . For  $n > 4$ .
5. The minimum value of Vref setting tolerance =  $Vref\_new - 1.1mV$ . The maximum value of Vref setting tolerance =  $Vref\_new + 1.1mV$ . For  $n \leq 4$ .

6. Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.
7. Measured by recording the min and max values of the Vref output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.
8. Time from MRS command to increment or decrement one step size for Vref.
9. Time from MRS command to increment or decrement Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefDQ Range in Vref voltage.
10. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
11. DRAM range 0 or 1 set by MR14 OP[6].
12. Time from MRS command to increment or decrement more than one step size up to a full range of Vref voltage within the same VrefDQ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.
14. Vref\_time\_weak covers all Vref(DQ) Range and Value change conditions are applied to Vref\_time\_Short/Middle/Long.

### 2.23. Command Bus Training

The LPDDR4-SDRAM command bus must be trained before enabling termination for high-frequency operation. LPDDR4 provides an internal VREF(ca) that defaults to a level suitable for un-terminated, low-frequency operation, but the VREF(ca) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation. The training mode described here centers the internal VREF(ca) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training mode.

Note: it is up to the system designer to determine what constitutes "low-frequency" and "high-frequency" based on the capabilities of the system. Low-frequency should then be defined as an operating frequency in which the system can reliably communicate with the SDRAM before Command Bus Training is executed.

The LPDDR4-SDRAM die has a bond-pad (ODT-CA) for multi-rank operation. In a multi-rank system, the terminating rank should be trained first, followed by the non-terminating rank(s). See the ODT section for more information.

The LPDDR4-SDRAM uses Frequency Set-Points to enable multiple operating settings for the die. The LPDDR4-SDRAM defaults to FSP-OP[0] at power-up, which has the default settings to operate in un-terminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR13 OP[6]=1B (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Prior to entering Command Bus Training, the SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when CKE is driven LOW, the LPDDR4-SDRAM will automatically switch to the alternate FSP register set (FSP-OP[y]) and use the alternate register settings during training (See note 6 in Figure "Entering Command Bus Training Mode and CA Training Pattern Input and Output with VrefCA Value Update" for more information on FSP-OP register sets). Upon training exit when CKE is driven HIGH, the LPDDR4-SDRAM will automatically switch back to the original FSP register set (FSP-OP[x]), returning to the "known-good" state that was operating prior to training. The training values for VREF(ca) are not retained by the DRAM in FSP-OP[y] registers, and must be written to the registers after training exit.

1. To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0]=1B (Command Bus Training Mode Enabled).

2. After time tMRD, CKE may be set LOW, causing the LPDDR4-SDRAM to switch from FSP-OP[x] to FSP-OP[y], and completing the entry into Command Bus Training mode.

A status of DQS\_t, DQS\_c, DQ and DMI are as follows, and DQ ODT state will be followed Frequency Set Point function except output pins.

- DQS\_t[0], DQS\_c[0] become input pins for capturing DQ[6:0] levels by its toggling.
- DQ[5:0] become input pins for setting VREF(ca) Level.
- DQ[6] becomes a input pin for setting VREF(ca) Range.
- DQ[7] and DMI[0] become input pins and their input level is Valid level or floating, either way is fine.
- DQ[13:8] become output pins to feedback its capturing value via command bus by CS signal.
- DQS\_t[1], DQS\_c[1], DMI[1] and DQ[15:14] become output pins or disable, it means that SDRAM may drive to a valid level or left floating.

3. At time tCAENT later, LPDDR4 SDRAM can accept to change its VREF(ca) Range and Value using input signals of DQS\_t[0], DQS\_c[0] and DQ[6:0] from existing value that's setting via MR12 OP[6:0]. The mapping between MR12 OP code and DQ signals is shown in the table below. At least one Vref CA setting is required before proceed to next training steps.

**Table - Mapping of MR12 OP Code and DQ Numbers**

|              | Mapping |     |     |     |     |     |     |
|--------------|---------|-----|-----|-----|-----|-----|-----|
| MR12 OP code | OP6     | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| DQ Number    | DQ6     | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |

- The new VREF(ca) value must "settle" for time tVREF\_LONG before attempting to latch CA information.
- To verify that the receiver has the correct VREF(ca) setting and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.
- To exit Command Bus Training mode, drive CKE HIGH, and after time tVREF\_LONG issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0]=0B. After time tMRW the LPDDR4-SDRAM is ready for normal operation. After training exit the LPDDR4-SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

Command Bus Training may be executed from IDLE, or Self Refresh states. When executing CBT within the Self Refresh state, the SDRAM must not be a power down state (i.e. CKE must be HIGH prior to training entry). Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

### 2.23.0.1. Training Sequence for single-rank systems:

Note that an example shown here is assuming an initial low-frequency, no-terminating operating point, training a high-frequency, terminating operating point. The **green text is low-frequency**, **magenta text is high-frequency**. Any operating point may be trained from any known good operating point)

- Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-OP[x], See note).
- Write FSP-WR[y] (or FSP-WR[x]) registers for all channels to set up high-frequency operating parameters.
- Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
- Drive CKE LOW, and change CK frequency to the high-frequency operating point.
- Perform Command Bus Training (VREFca, CS, and CA).
- Exit training by driving CKE HIGH, a change CK frequency to the low-frequency operating point prior to driving CKE HIGH, then issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
- Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the highfrequency operating point. At this point the Command Bus is trained and you may proceed to other training or normal operation.

### 2.23.0.2. Training Sequence for multi-rank systems:

(Example shown here is assuming an initial low-frequency operating point, training a high-frequency operating point. The **green text is low-frequency**, **magenta text is high-frequency**. Any operating point may be trained from any known good operating point)

- Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-WR[x], See Note).
- Write FSP-WR[y] (or FSP-WR[x]) registers for all channels and ranks to set up highfrequency operating parameters.

3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7]=1B.
4. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), and change CK frequency to the high-frequency operating point.
6. Perform Command Bus Training on the terminating rank (VREFca, CS, and CA).
7. Exit training by driving CKE HIGH, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[y] (or FSP-WR[x]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
8. Issue MRW-1 and MRW-2 command to enter training mode on the non-terminating rank (but keep CKE HIGH)
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the highfrequency operating point.
10. Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y] (or FSP-OP[x]).
11. Perform Command Bus Training on the non-terminating rank (VREFca, CS, and CA).
12. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] (or FSP-OP[y]) to turn off termination.
13. Exit training by driving CKE HIGH on the non-terminating rank, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
14. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the highfrequency operating point. At this point the Command Bus is trained for both ranks and you may proceed to other training or normal operation.

### 2.23.0.3. Relation between CA input pin and DQ output pin

The relation between CA input pin and DQ out pin is shown in the following table.

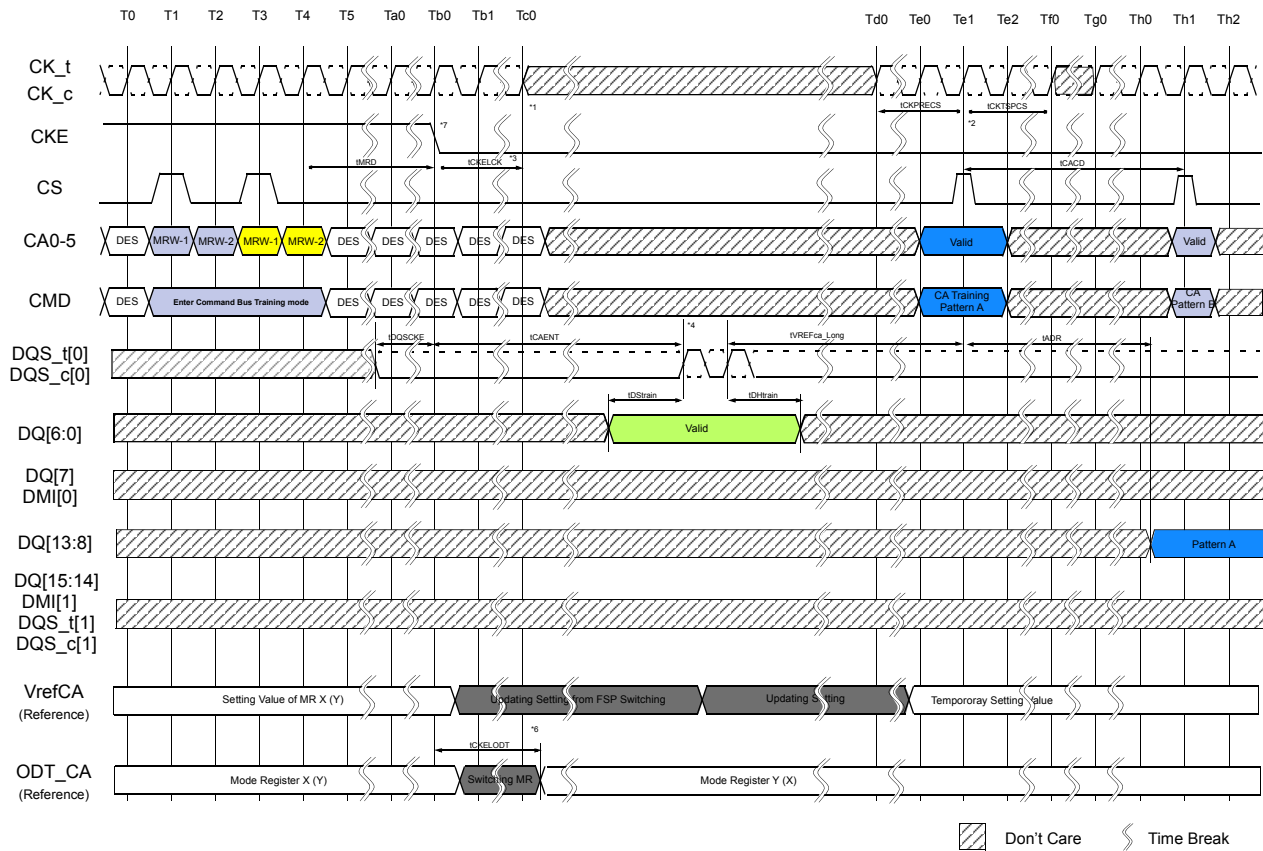
**Table - Mapping of CA input pin to DQ ouput pin**

|           | Mapping |      |      |      |     |     |
|-----------|---------|------|------|------|-----|-----|
| CA Number | CA5     | CA4  | CA3  | CA2  | CA1 | CA0 |
| DQ Number | DQ13    | DQ12 | DQ11 | DQ10 | DQ9 | DQ8 |

#### 2.23.0.4. Timing Diagram

The basic timing diagrams of Command Bus Training are shown in following figures.

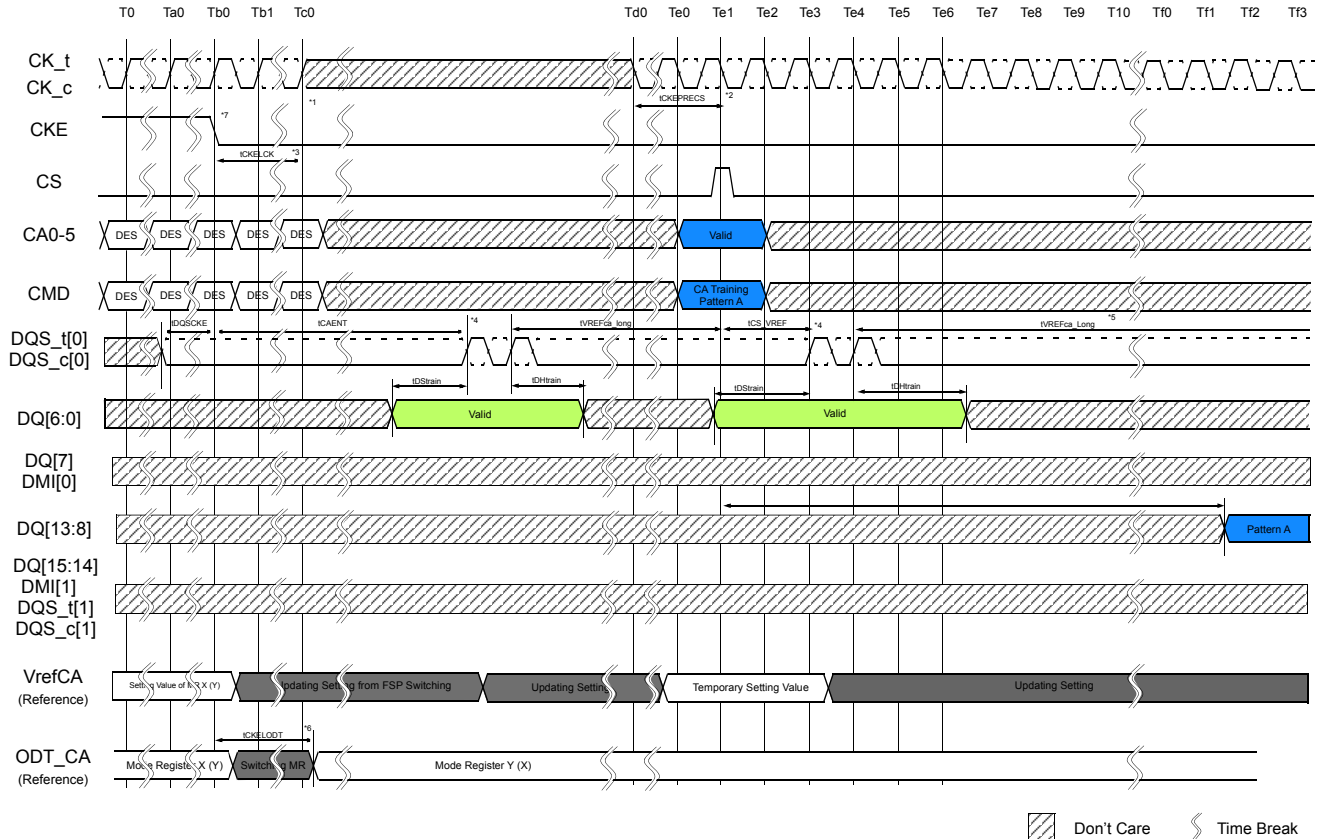
**Figure - Entering Command Bus Training Mode and CA Training Pattern Input and Output with VrefCA Value Update**



Notes:

1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS and tCKPSTCS.
3. Continue to Drive CK and Hold CA & CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. DRAM may or may not capture first rising/falling edge of DQS\_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ[6:0] signals.  
The captured value of DQ[6:0] signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFCa setting of MR12 temporary after time tVREFCa\_Long.
5. tVREF\_LONG may be reduced to tVREF\_SHORT if the following conditions are met: 1) The new Vref setting is a single step above or below the old Vref setting, and 2) The DQS pulses a single time, or the new Vref setting value on DQ[6:0] is static and meets tDSTRAIN/tDHTRAIN for every DQS pulse applied.
6. When CKE is driven LOW, the SDRAM will switch its FSP-OP registers to use the alternate (i.e. non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT\_CA disabled then termination will not enable in CA Bus Training mode. If the ODT\_CA pad is bonded to Vss or floating, ODT\_CA termination will never enable for that die.
7. When CKE is driven low in Command Bus Training mode, the LPDDR4-SDRAM will change operation to the alternate FSP, i.e. the inverse of the FSP programmed in the FSP-OP mode register.

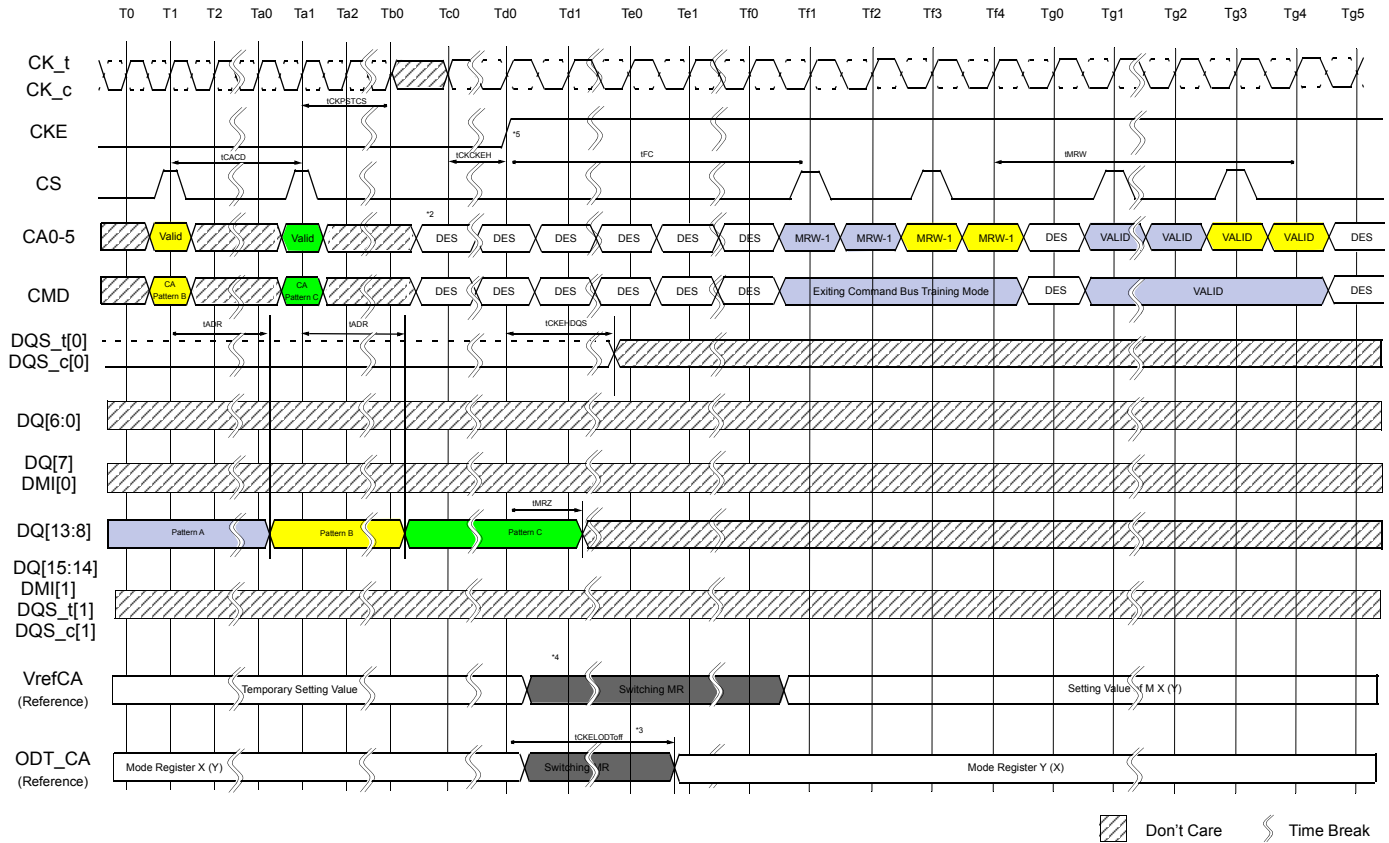
**Figure - Consecutive VrefCA Value Update**



**Notes:**

1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS.
3. Continue to Drive CK and Hold CA & CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. DRAM may or may not capture first rising/falling edge of DQS\_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ6:0 signals.  
The captured value of DQ[6:0] signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFca setting of MR12 temporary after time tvREFca\_Long.
5. tvREF\_LONG may be reduced to tvREF\_SHORT if the following conditions are met: 1) The new Vref setting is a single step above or below the old Vref setting, and 2) The DQS pulses a single time, or the new Vref setting value on DQ[6:0] is static and meets tDSTRAIN/tDHTRAIN for every DQS pulse applied.
6. When CKE is driven LOW, the SDRAM will switch its FSP-OP registers to use the alternate (i.e. non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT\_CA disabled then termination will not enable in CA Bus Training mode. If the ODT\_CA pad is bonded to Vss or floating, ODT\_CA termination will never enable for that die.
7. When CKE is driven low in Command Bus Training mode, the LPDDR4-SDRAM will change operation to the alternate FSP, i.e. the inverse of the FSP programmed in the FSP-OP mode register.

**Figure - Exiting Command Bus Training Mode with Valid Command**



**Notes:**

1. Clock can be stopped or frequency changed any time before  $t_{CKCKEH}$ . CK must meet  $t_{CKCKEH}$  before CKE is driven high. When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS and CA[5:0] must be Deselect (all low)  $t_{CKCKEH}$  before CKE is driven high.
3. When CKE is driven high, the SDRAM's ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).  
Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency.  
Example: VREF(ca) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4-SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.



1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high. When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS and CA[5:0] must be Deselect (all low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the SDRAM's ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).  
Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency.  
Example: VREF(ca) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4-SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

## 2.24. Frequency Set Point (FSP)

Frequency Set-Points allow the LPDDR4-SDRAM CA Bus to be switched between two differing operating frequencies, with changes in voltage swings and termination values, without ever being in an un-trained state which could result in a loss of communication to the DRAM. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the DRAM operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSP-WR bit allows MR parameters to be changed for an alternate Frequency Set-Point without affecting the LPDDR4-SDRAM's current operation. Once all necessary parameters have been written to the alternate Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have two physical registers controlled by FSP-WR and FSP-OP include:

**Table - Mode Register Function with two physical registers**

| MR#  | Operand | Function                                           | Note |
|------|---------|----------------------------------------------------|------|
| MR1  | OP[3]   | RD-PRE (RD Pre-amble Type)                         |      |
|      | OP[6:4] | nWR (Write-Recovery for Auto-Pre-charge commands)  |      |
|      | OP[7]   | RPST (RD Post-Ambles Length)                       |      |
| MR2  | OP[2:0] | RL (Read Latency)                                  |      |
|      | OP[5:3] | WL (Write Latency)                                 |      |
|      | OP[6]   | WLS (Write Latency Set)                            |      |
| MR3  | OP[0]   | PU-Cal (Pull-up Calibration Point)                 | 1    |
|      | OP[1]   | WR PST (WR Post-Ambles Length)                     |      |
|      | OP[5:3] | PDDS (Pull-down Drive Strength)                    |      |
|      | OP[6]   | DBI-RD (DBI Read Enable)                           |      |
|      | OP[7]   | DBI-WR (DBI Write Enable)                          |      |
| MR11 | OP[2:0] | DQ ODT (DQ Bus Receiver On-Die-Termination)        |      |
|      | OP[6:4] | CA ODT (CA Bus Receiver On-Die-Termination)        |      |
| MR12 | OP[5:0] | VREF(ca) (Vref(ca) Setting)                        |      |
|      | OP[6]   | VR-CA (Vref(ca) Range)                             |      |
| MR14 | OP[5:0] | Vref(dq) (Vref(dq) Setting)                        |      |
|      | OP[6]   | VR-DQ (Vref(dq) Range)                             |      |
| MR22 | OP[2:0] | SoC ODT (Controller ODT Value for VOH calibration) |      |
|      | OP[3]   | ODTE-CK (CK ODT Enabled for nonterminating rank)   |      |
|      | OP[4]   | ODTE-CS (CS ODT enable for non terminating rank)   |      |
|      | OP[5]   | ODTD-CA (CA ODT termination disable)               |      |

Note:

1. The synchronization MR3 OP[0] setting between Ch.0 and Ch.1 then the ZQ calibration is required in order to achieve a Driver strength and ODT tolerance to change MR3 OP[0] PU-CAL is changed through FSP.

See Mode Register Definition for more details.

Following table shows how the two mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

| Function | MR# & Operand | Data        | Operation                                                   | Note |
|----------|---------------|-------------|-------------------------------------------------------------|------|
| FSP-WR   | MR13 OP[6]    | 0 (Default) | Data write to Mode Register N for FSP-OP[0] by MRW command. | 1    |
|          |               | 1           | Data write to Mode Register N for FSP-OP[1] by MRW command. |      |
| FSP-OP   | MR13 OP[7]    | 0 (Default) | DRAM operates with Mode Register N for FSP-OP[0] setting.   | 2    |
|          |               | 1           | DRAM operates with Mode Register N for FSP-OP[1] setting.   |      |

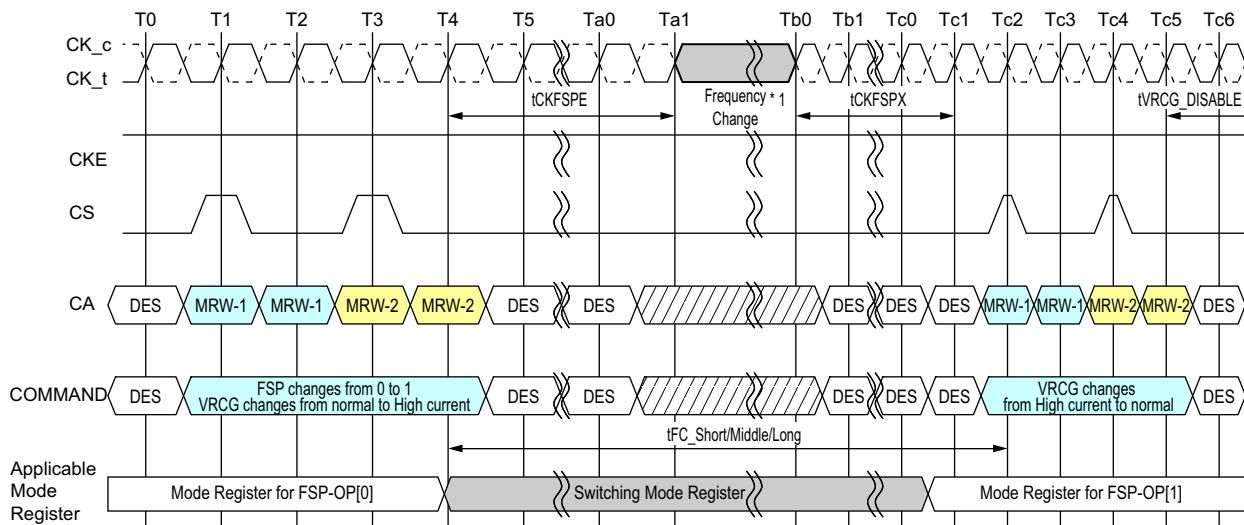
Notes:

1. FSP-WR stands for Frequency Set Point Write/Read.
2. FSP-OP stands for Frequency Set Point Operating Point.

### 2.24.0.1. Frequency Set Point update timing

The Frequency set point update timing is shown in the timing diagram below. When changing the frequency set point via MR13 OP[7], the VRCG setting: MR13 OP[3] have to be changed into VREF Fast Response (high current) mode at the same time. After Frequency change time( $t_{FC}$ ) is satisfied. VRCG can be changed into Normal Operation mode via MR13 OP[3].

**Figure - Frequency Set Point Switching Timing**



NOTES : 1. The definition that is Clock frequency change during CKE HIGH should be followed at the frequency change operation.  
For more information, refer to Section 4.42 Input Clock Stop and Frequency Change.

 DON'T CARE
  TIME BREAK

**Table -  $t_{FC}$  value mapping**

| Application      | Step size    |                                       | Range        |            |
|------------------|--------------|---------------------------------------|--------------|------------|
|                  | From FSP-OP0 | To FSP-OP1                            | From FSP-OP0 | To FSP-OP1 |
| $t_{FC\_Short}$  | Base         | A single step increment/decrement     | Base         | No Change  |
| $t_{FC\_Middle}$ | Base         | Two or more steps increment/decrement | Base         | No Change  |
| $t_{FC\_Long}$   | -            | -                                     | Base         | Change     |

Notes:

1. As well as from FSP-OP1 to FSP-OP0

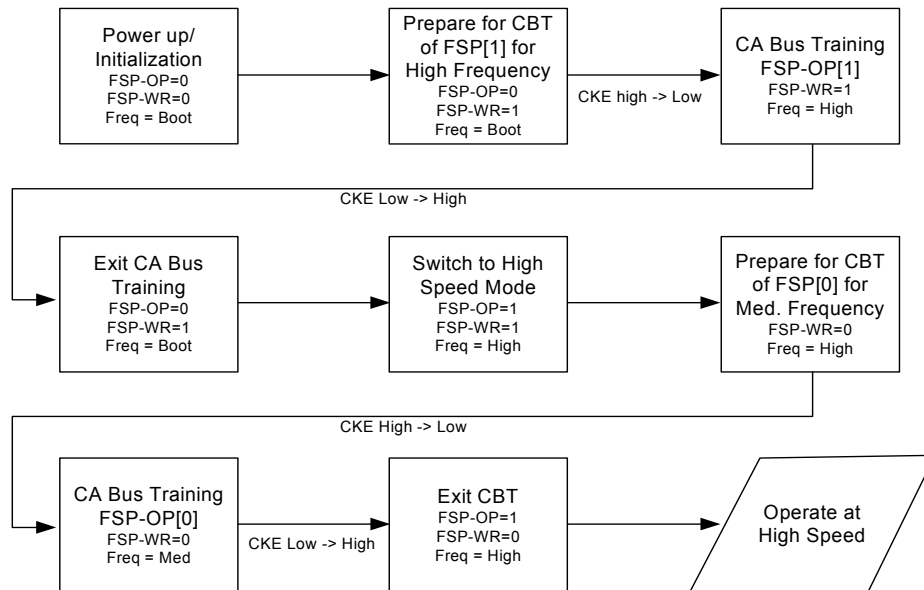
**Table - tFC value mapping example**

| Case | From/To | FSP-OP<br>MR13 OP[7] | Vref(ca) set-<br>ting:<br>MR12:<br>OP[5:0] | Vref(ca)<br>Range:<br>MR12<br>OP[6] | Application | Note |
|------|---------|----------------------|--------------------------------------------|-------------------------------------|-------------|------|
| 1    | From    | 0                    | 001100                                     | 0                                   | tFC_Short   | 1    |
|      | To      | 1                    | 001101                                     | 0                                   |             |      |
| 2    | From    | 0                    | 001100                                     | 0                                   | tFC_Middle  | 2    |
|      | To      | 1                    | 001110                                     | 0                                   |             |      |
| 3    | From    | 0                    | Don't care                                 | 0                                   | tFC_Long    | 3    |
|      | To      | 1                    | Don't care                                 | 1                                   |             |      |

Notes:

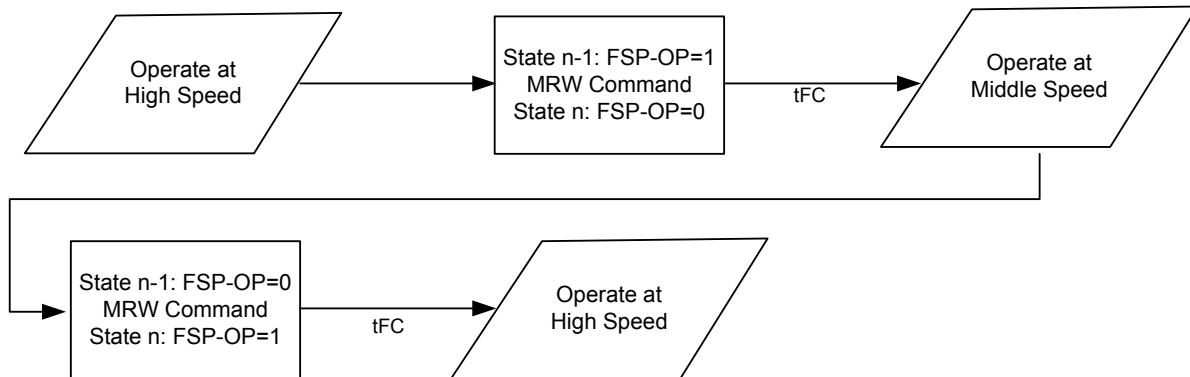
1. A single step size increment/decrement for Vref(ca) Setting Value.
2. Two or more step size increment/decrement for Vref(ca) Setting Value.
3. VREF(ca) Range is changed. In this case changing VREF(ca) Setting doesn't affect tFC value.

The LPDDR4-SDRAM defaults to FSP-OP[0] at power-up. Both Set-Points default to settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR4-SDRAM to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point (Figure "Training Two Frequency Set Points"). See the section Command Bus Training for more details on this training mode.

**Figure - Training Two Frequency Set Points**


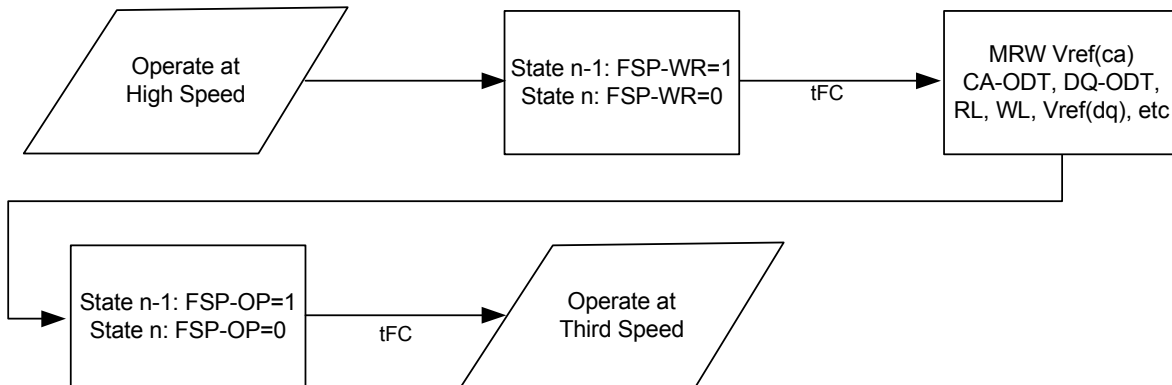
Once both Frequency Set Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (figure below)

**Figure - Switching between two trained Frequency Set Points**



Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously-trained values (in particular the Vref-CA calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure below).

**Figure - Switching to a third trained Frequency Set Point**



## 2.25. Write Leveling Mode

To improve signal-integrity performance, the LPDDR4 SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS<sub>t</sub>/DQS<sub>c</sub> signal pair.

All data bits (DQ[7:0] for DQS<sub>t</sub>/DQS<sub>c</sub>[0], and DQ[15:8] for DQS<sub>t</sub>/DQS<sub>c</sub>[1]) carry the training feedback to the controller. Both DQS signals in each channel must be leveled independently. Write-leveling entry/exit is independent between channels.

The LPDDR4 SDRAM enters into write-leveling mode when mode register MR2-OP[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only DESELECT commands are allowed, or a MRW command to exit the write-leveling operation. Depending on the absolute values of tQSL and tQSH in the application, the value of tDQSS may have to be better than the limits provided in the chapter "AC Timing Parameters" in order to satisfy the tDSS and tDSH specification. Upon completion of the write-leveling operation, the DRAM exits from write-leveling mode when MR2-OP[7] is reset LOW.

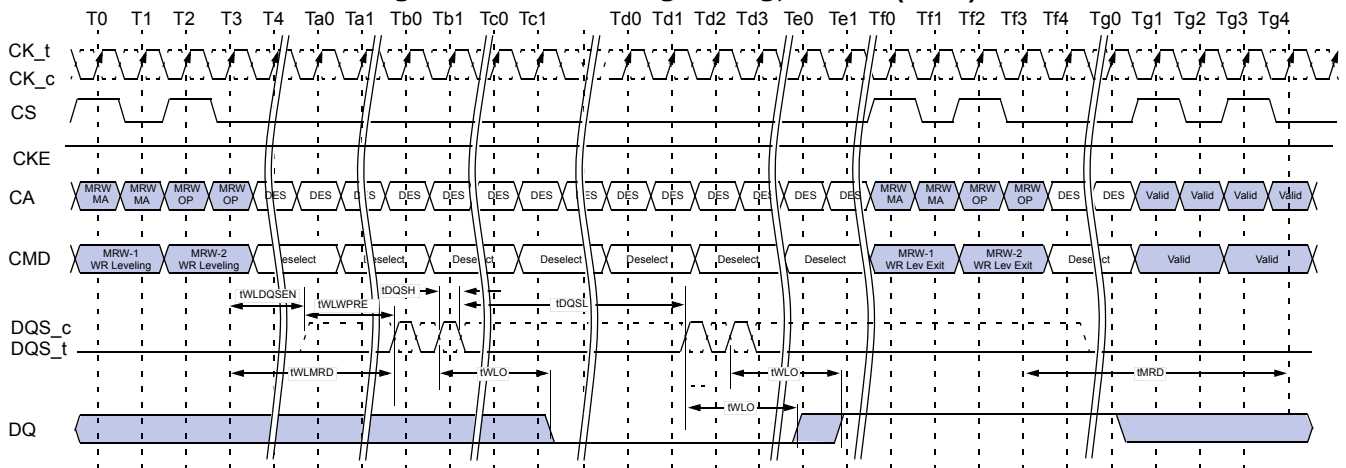
Write Leveling should be performed before Write Training (DQS2DQ Training).

### Write Leveling Procedure:

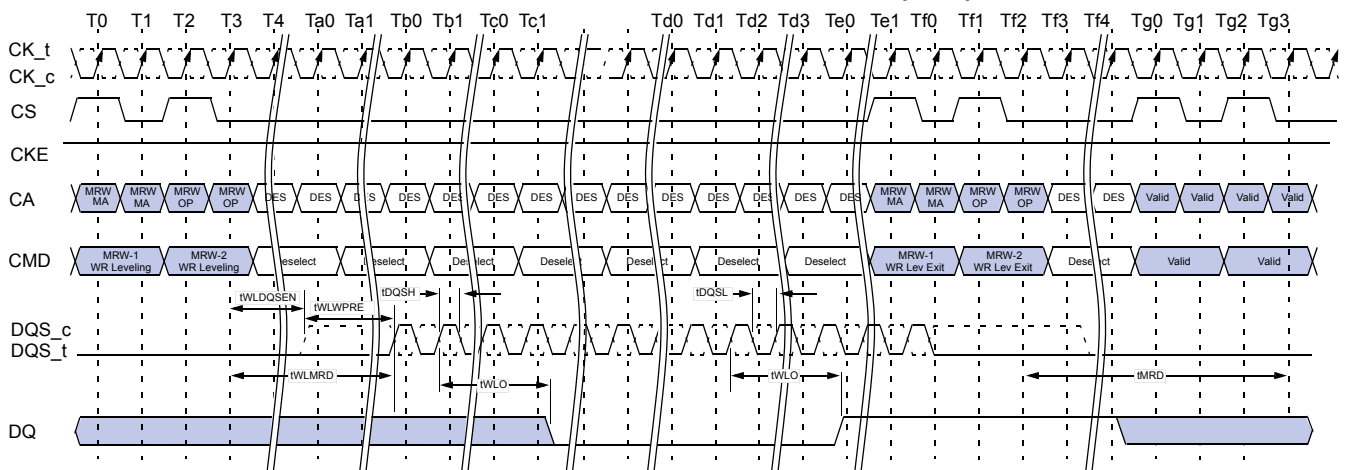
1. Enter into Write-leveling mode by setting MR2-OP[7]=1,
2. Once entered into Write-leveling mode, DQS<sub>t</sub> must be driven LOW and DQS<sub>c</sub> HIGH after a delay of tWLDQSEN.
3. Wait for a time tWLMRD before providing the first DQS signal input. The delay time tWLMRD(MAX) is controller-dependent.
4. DRAM may or may not capture first rising edge of DQS<sub>t</sub> due to an unstable first risign edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal during Write Training Mode.  
The captured clock level by each DQS edges are overwritten at any time and the DRAM provides asynchronous feedback on all the DQ bits after time tWLO.
5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS<sub>t</sub> and/or DQS<sub>c</sub> delay settings.
6. Repeat step 4 through step 5 until the proper DQS<sub>t</sub>/DQS<sub>c</sub> delay is established.
7. Exit from Write-leveling mode by setting MR2-OP[7]=0.

A Write Leveling timing example is shown in figure below.

**Figure - Write Leveling Timing,  $t_{DQSL}(\max)$**



**Figure - Write Leveling Timing,  $t_{DQSL}(\min)$**

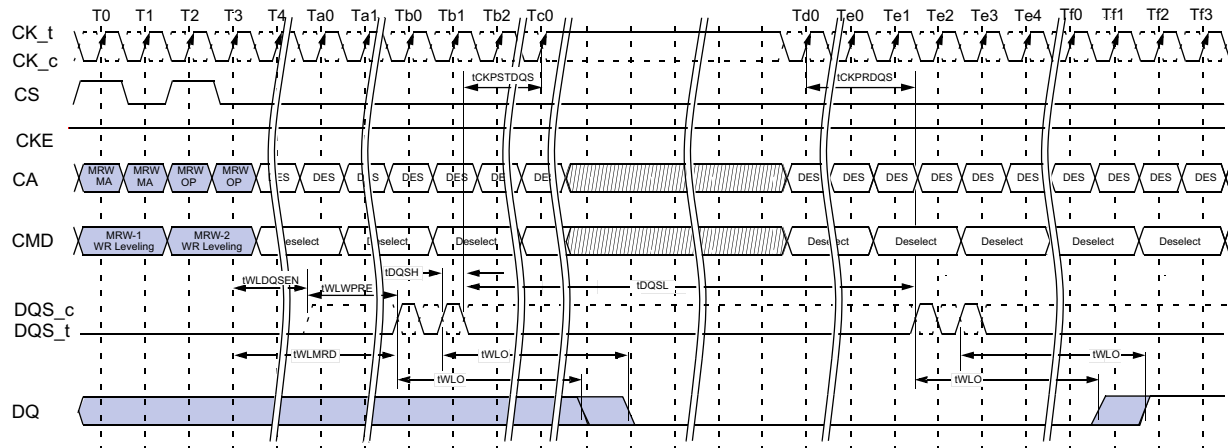


### 2.25.1. Input Clock Frequency Stop and Change

The input clock frequency can be stopped or changed from one stable clock rate to another stable clock rate during Write Leveling mode.

The Frequency stop or change timing is shown in Figure below

**Figure - Clock Stop and Timing during Write Leveling**



NOTES : 1. CK<sub>t</sub> is held LOW and CK<sub>c</sub> is held HIGH during clock stop.  
2. CS shall be held LOW during clock stop



## 2.26. MPC [RD DQ Calibration] Command

LPDDR4 devices feature a RD DQ Calibration training function that outputs a 16-bit user-defined pattern on the DQ pins. RD DQ Calibration is initiated by issuing a MPC [RD DQ Calibration] command followed by a CAS-2 command, cause the LPDDR4-SDRAM to drive the contents of MR32 followed by the contents of MR40 on each of DQ[15:0] and DMI[1:0]. The pattern can be inverted on selected DQ pins according to user-defined invert masks written to MR15 and MR20.

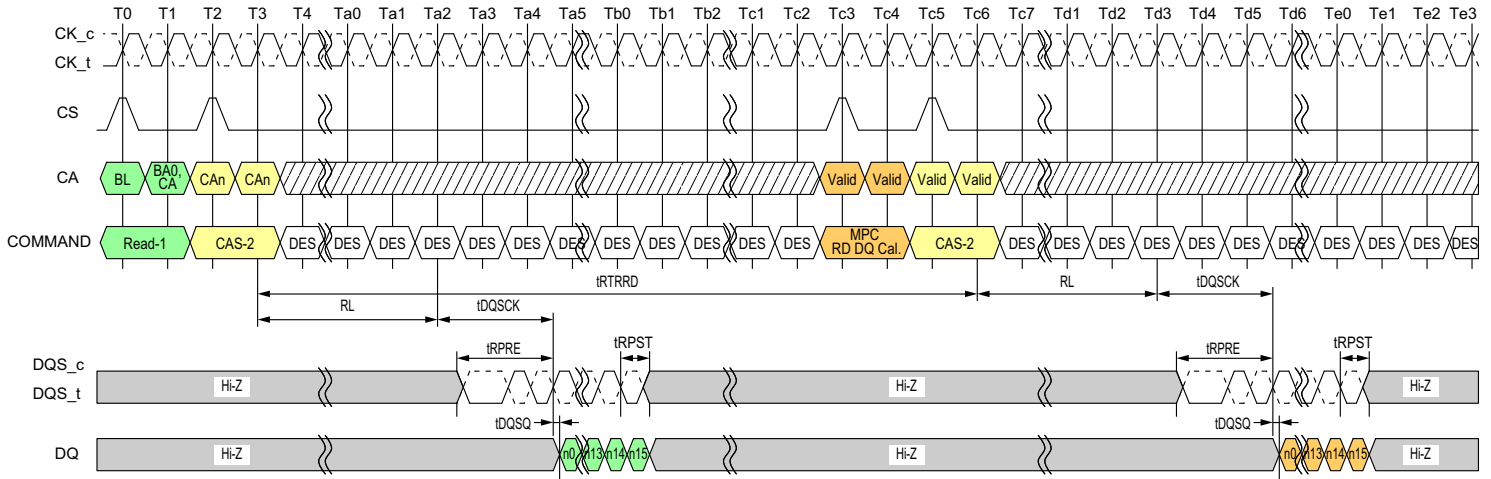
### RD DQ Calibration Training Procedure

The procedure for executing RD DQ Calibration is:

- Issue MRW commands to write MR32 (first eight bits), MR40 (second eight bits), MR15 (eight-bit invert mask for byte 0), and MR20 (eight-bit invert mask for byte 1)
  - o Optionally this step could be skipped to use the default patterns
    - MR32 default = 5Ah
    - MR40 default = 3Ch
    - MR15 default = 55h
    - MR20 default = 55h
- Issue an MPC [RD DQ Calibration] command followed immediately by a CAS-2 command
  - o Each time an MPC [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4 SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins
  - o The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit (see Table "Invert Mask Assignments")
  - o Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the DRAM mode register.
  - o The MPC-1 [RD DQ Calibration] command can be issued every tCCD seamlessly, and tRTRRD delay is required between Array Read command and the MPC-1 [RD DQ Calibration] command as well the delay required between the MPC-1 [RD DQ Calibration] command and an array read.
  - o The operands received with the CAS-2 command must be driven LOW
- DQ Read Training can be performed with any or no banks active, during Refresh, or during SREF with CKE high

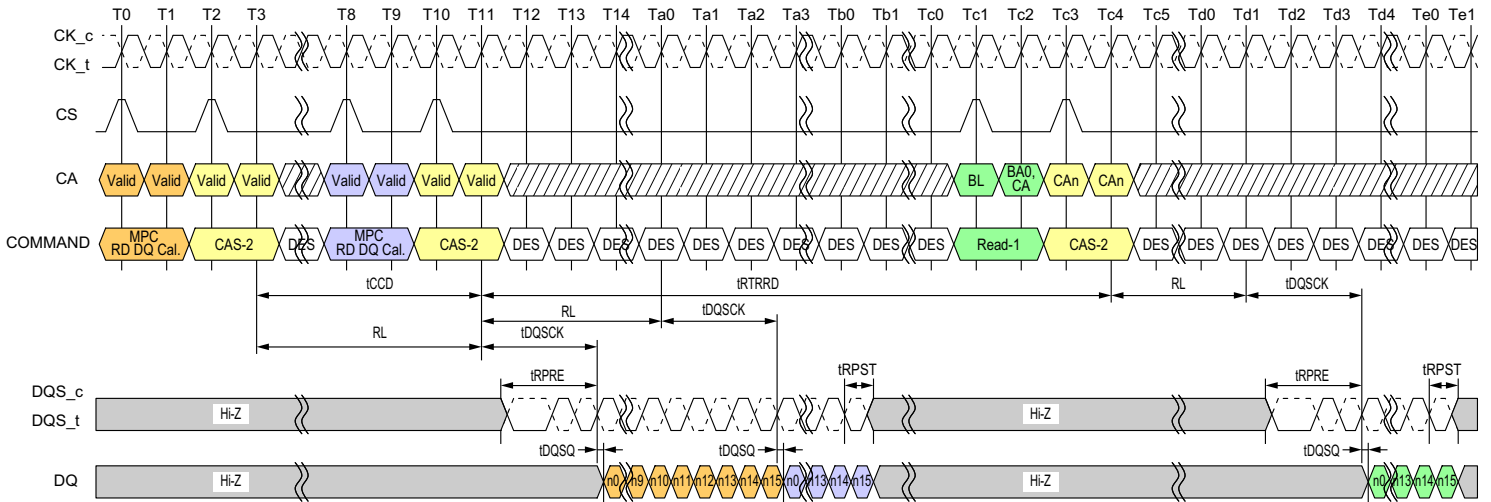
**Table - Invert Mask Assignments**

| Pin  | DQ8 | DQ9 | DQ10 | DQ11 | DMI1 | DQ12 | DQ13 | DQ14 | DQ15 |
|------|-----|-----|------|------|------|------|------|------|------|
| MR20 | OP0 | OP1 | OP2  | OP3  | N/A  | OP4  | OP5  | OP6  | OP7  |
| Pin  | DQ0 | DQ1 | DQ2  | DQ3  | DMI0 | DQ4  | DQ5  | DQ6  | DQ7  |
| MR15 | OP0 | OP1 | OP2  | OP3  | N/A  | OP4  | OP5  | OP6  | OP7  |

**Figure - DQ Read Training Timing: Read to Read DQ Calibration**


- NOTES : 1. Read-1 to MPC [RD DQ Calibration] Operation is shown as an example of command-to-command timing.  
Timing from Read-1 to MPC [RD DQ Calibration] command is tRTRRD.  
2. MPC [RD DQ Calibration] uses the same command-to-data timing relationship (RL, tDQSK, tDQSQ) as a Read-1 command.  
3. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK.  
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

⏏ DONT CARE ⏏ TIME BREAK

**Figure - DQ Read Training Timing: Read DQ Cal. to Read DQ Cal. / Read**


- NOTES : 1. MPC [RD DQ Calibration] to MPC [RD DQ Calibration] Operation is shown as an example of command-to-command timing.  
2. MPC [RD DQ Calibration] to Read-1 Operation is shown as an example of command-to-command timing.  
3. MPC [RD DQ Calibration] uses the same command-to-data timing relationship (RL, tDQSK, tDQSQ) as a Read-1 command.  
4. Seamless MPC [RD DQ Calibration] commands may be executed by repeating the command every tCCD time.  
5. Timing from MPC [RD DQ Calibration] command to Read-1 is tRTRRD.  
6. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK.  
7. DES commands are shown for ease of illustration; other commands may be valid at these times.

⏏ DONT CARE ⏏ TIME BREAK

### 2.26.1. MPC [RD DQ Calibration] Example

An example of MPC [RD DQ Calibration] output is shown in Table "MPC [RD DQ Calibration] Bit Ordering and Inversion Example". This shows the 16-bit data pattern that will be driven on each DQ when one DQ Read Training command is executed. This output assumes the following mode register values are used:

- MR32 = 1CH
- MR40 = 59H
- MR15 = 55H
- MR20 = 55H

**Table - MPC [RD DQ Calibration] Bit Ordering and Inversion Example**

| Pin  | Invert? | Bit sequence -> |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|---------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
|      |         | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DQ0  | Yes     | 1               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ1  | No      | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ2  | Yes     | 1               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ3  | No      | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DMI0 | Never   | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ4  | Yes     | 1               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ5  | No      | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ6  | Yes     | 1               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ7  | No      | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ8  | Yes     | 1               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ9  | No      | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ10 | Yes     | 1               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ11 | No      | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DMI1 | Never   | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ12 | Yes     | 1               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ13 | No      | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ14 | Yes     | 1               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ15 | No      | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

Notes:

1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when RD DQ Calibration is initiated via a MPC [RD DQ Calibration] command. The pattern transmitted serially on each data lane, organized "little endian" such that the low order bit in a byte is transmitted first. If the data pattern is 27H, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111.
2. MR15 and MR22 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. DMI [1:0] outputs status follows in the table below

Table - MR Setting vs. DMI Status

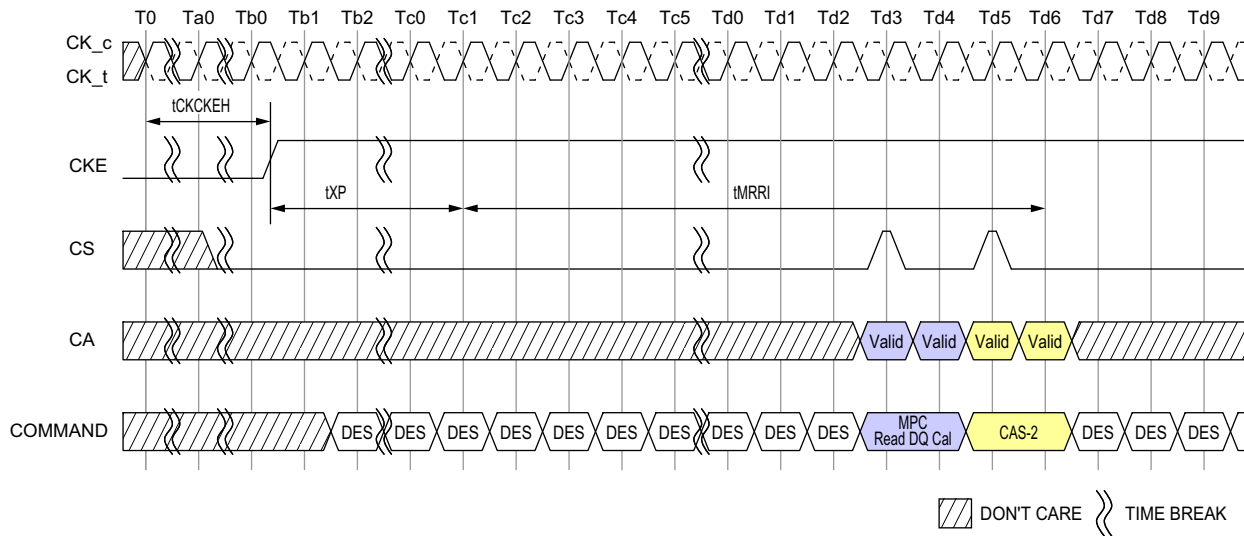
| DM Function<br>MR13 OP[5] | Write DBIdc Function<br>MR3 OP[7] | Read DBIdc Function<br>MR3 OP[6] | DMI Status                      |
|---------------------------|-----------------------------------|----------------------------------|---------------------------------|
| 1: Disable                | 0: Disable                        | 0: Disable                       | Hi-Z                            |
| 1: Disable                | 1: Enable                         | 0: Disable                       | The data pattern is transmitted |
| 1: Disable                | 0: Disable                        | 1: Enable                        | The data pattern is transmitted |
| 1: Disable                | 1: Enable                         | 1: Enable                        | The data pattern is transmitted |
| 0: Enable                 | 0: Disable                        | 0: Disable                       | The data pattern is transmitted |
| 0: Enable                 | 1: Enable                         | 0: Disable                       | The data pattern is transmitted |
| 0: Enable                 | 0: Disable                        | 1: Enable                        | The data pattern is transmitted |
| 0: Enable                 | 1: Enable                         | 1: Enable                        | The data pattern is transmitted |

4. No Data Bus Inversion (DBI) function is enacted during RD DQ Calibration, even if DBI is enabled in MR3-OP[6].

### 2.26.2. MPC of Read DQ Calibration after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the MPC of Read DQ Calibration command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the Read DQ data in MR32 and MR40 data path after exit from standby, power-down mode.

Figure - MPC Read DQ Calibration Following Power-Down State



## 2.27. MPC Write Training (DQS-DQ Training)

The LPDDR4-SDRAM uses an un-matched DQS-DQ path to enable high speed performance and save power in the DRAM. As a result, the DQS strobe must be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad, and has a shorter internal delay in the SDRAM than does the DQS signal. The SDRAM DQ receiver will latch the data present on the DQ bus when DQS reaches the latch, and training is accomplished by delaying the DQ signals relative to DQS such that the Data eye arrives at the receiver latch centered on the DQS transition.

Two modes of training are available in LPDDR4:

- Command-based FIFO WR/RD with user patterns
- A internal DQS clock-tree oscillator, to determine the need for, and the magnitude of, required training.

The command-based FIFO WR/RD uses the MPC command with operands to enable this special mode of operation. When issuing the MPC command, if OP6 is set LOW then the DRAM will perform a NOP command. When OP6 is set HIGH, then OP5:0 enable training functions or are reserved for future use (RFU). MPC commands that initiate a Read FIFO, READ DQ Calibration or Write FIFO to the SDRAM must be followed immediately by a CAS-2 command. See "Multi Purpose Command (MPC) Definition" for more information.

To perform Write Training, the controller can issue a MPC [Write DQ FIFO] command with OP[6:0] set as described in the MPC Definition section, followed immediately by a CAS-2 command (CAS-2 operands should be driven LOW) to initiate a Write DQ FIFO. Timings for MPC [Write DQ FIFO] are identical to a Write command, with WL (Write Latency) timed from the 2nd rising clock edge of the CAS-2 command. Up to 5 consecutive MPC [Write DQ FIFO] commands with user defined patterns may be issued to the SDRAM to store up to 80 values (BL16 x5) per pin that can be read back via the MPC [Read DQ FIFO] command. Write/Read FIFO Pointer operation is described later in this section.

After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compared with "expect" data to see if further training (DQ delay) is needed. MPC [Read DQ FIFO] is initiated by issuing a MPC command with OP[6:0] set as described in the MPC Definition section, followed immediately by a CAS-2 command (CAS-2 operands must be driven LOW). Timings for the MPC [Read DQ FIFO] command are identical to a Read command, with RL (Read Latency) timed from the 2nd rising clock edge of the CAS-2 command.

Read DQ FIFO is non-destructive to the data captured in the FIFO, so data may be read continuously until it is either overwritten by a Write DQ FIFO command or disturbed by CKE LOW or any of the following commands; Write, Masked Write, Read, Read DQ Calibration and a MRR. If fewer than 5 Write DQ FIFO commands were executed, then unwritten registers will have un-defined (but valid) data when read back.

The following command about MRW is only allowed from MPC [Write DQ FIFO] command to MPC [Read DQ FIFO]. Allowing MRW command is for OP[7]:FSP-OP, OP[6]:FSP-WR and OP[3]:VRCG of MR13 and MR14. And the rest of MRW command is prohibited.

For example: If 5 Write DQ FIFO commands are executed sequentially, then a series of Read DQ FIFO commands will read valid data from FIFO[0], FIFO[1]....FIFO[4], and will then wrap back to FIFO[0] on the next Read DQ FIFO.

On the other hand, if fewer than 5 Write DQ FIFO commands are executed sequentially (example=3), then a series of Read DQ FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], but the next two Read DQ FIFO commands will return un-defined data for FIFO[3] and FIFO[4] before wrapping back to the valid data in FIFO[0].

### 2.27.1. FIFO Pointer Reset and Synchronism

The Write DQ FIFO pointer is reset under the following conditions:

- Power-up initialization
- RESET\_n asserted
- Power-down entry
- Self Refresh Power-Down entry

The MPC [Write DQ FIFO] command advances the WR-FIFO pointer, and the MPC [Read DQ FIFO] advances the RD-FIFO pointer. Also any normal (non-FIFO) Read Operation (RD, RDA) advances both WR-FIFO pointer and RD-FIFO pointer. Issuing (non-FIFO) Read Operation command is inhibited during Write training period. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of Write training period:

$$b = a + (n * c)$$

Where:

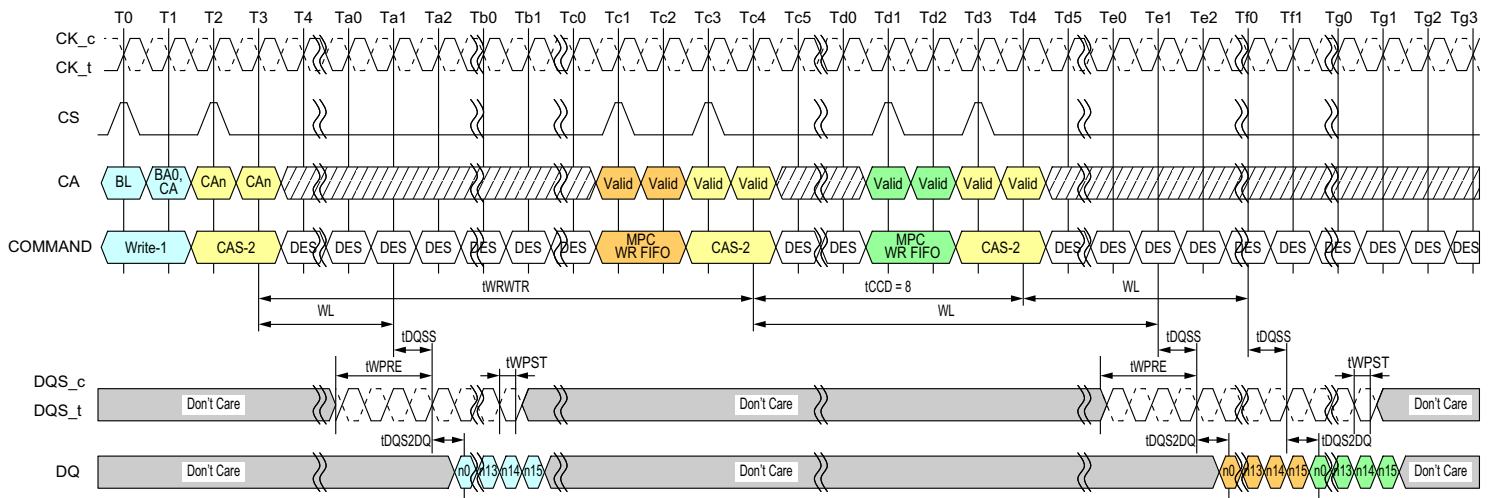
'a' is the number of MPC [Write DQ FIFO] commands

'b' is the number of MPC [Read DQ FIFO] commands

'c' is the FIFO depth (=5 for LPDDR4)

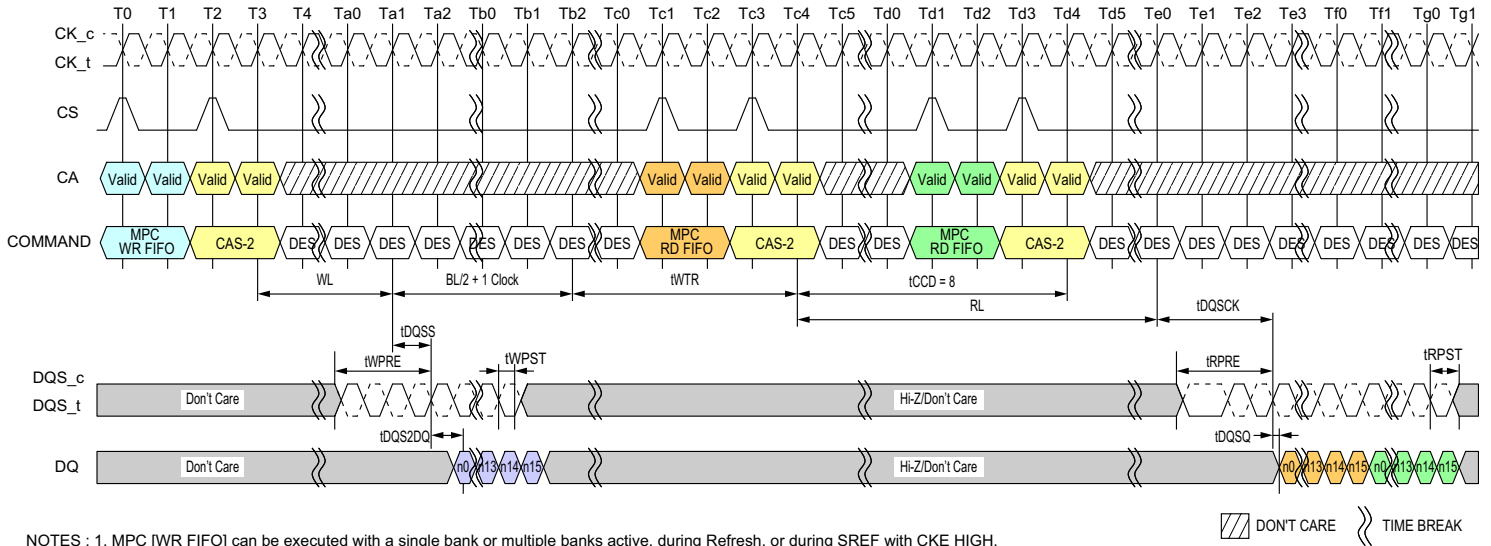
'n' is a positive integer,  $\geq 0$

**Figure - MPC [Write DQ FIFO] Operation Timing**



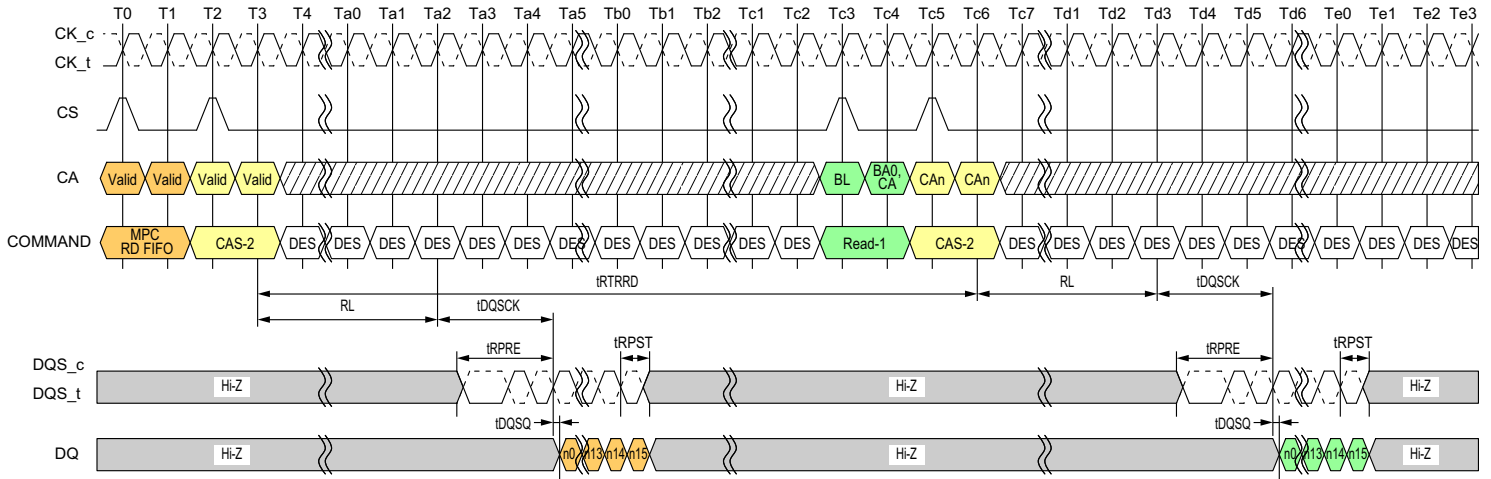
- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
  2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is tWRWTR.
  3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every tCCD time.
  4. MPC [WR-FIFO] uses the same command-to-data timing relationship (WL, tDQSS, tDQS2DQ) as a Write-1 command.
  5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data.  
The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
  6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW."
  7. To avoid corrupting the FIFO contents, MPC [RD-FIFO] must immediately follow MPC [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR.
  8. BL = 16, Write Postamble = 0.5nCK
  9. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure - MPC [Write FIFO] to MPC [Read FIFO] Timing**



- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
  2. MPC [WR-FIFO] to MPC [RD-FIFO] is shown as an example of command-to-command timing for MPC. Timing from MPC [WR-FIFO] to MPC [RD-FIFO] is specified in the command-to-command timing table.
  3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every  $t_{CCD}$  time.
  4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL,  $t_{DQSC}$ ,  $t_{DQSQ}$ ) as a Read-1 command.
  5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
  6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
  7. DM[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.
  8. BL = 16, Write Postamble = 0.5nCK, Read Preamble: Toggle, Read Postamble: 0.5nCK
  9. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure - MPC [Read FIFO] to Read Timing**

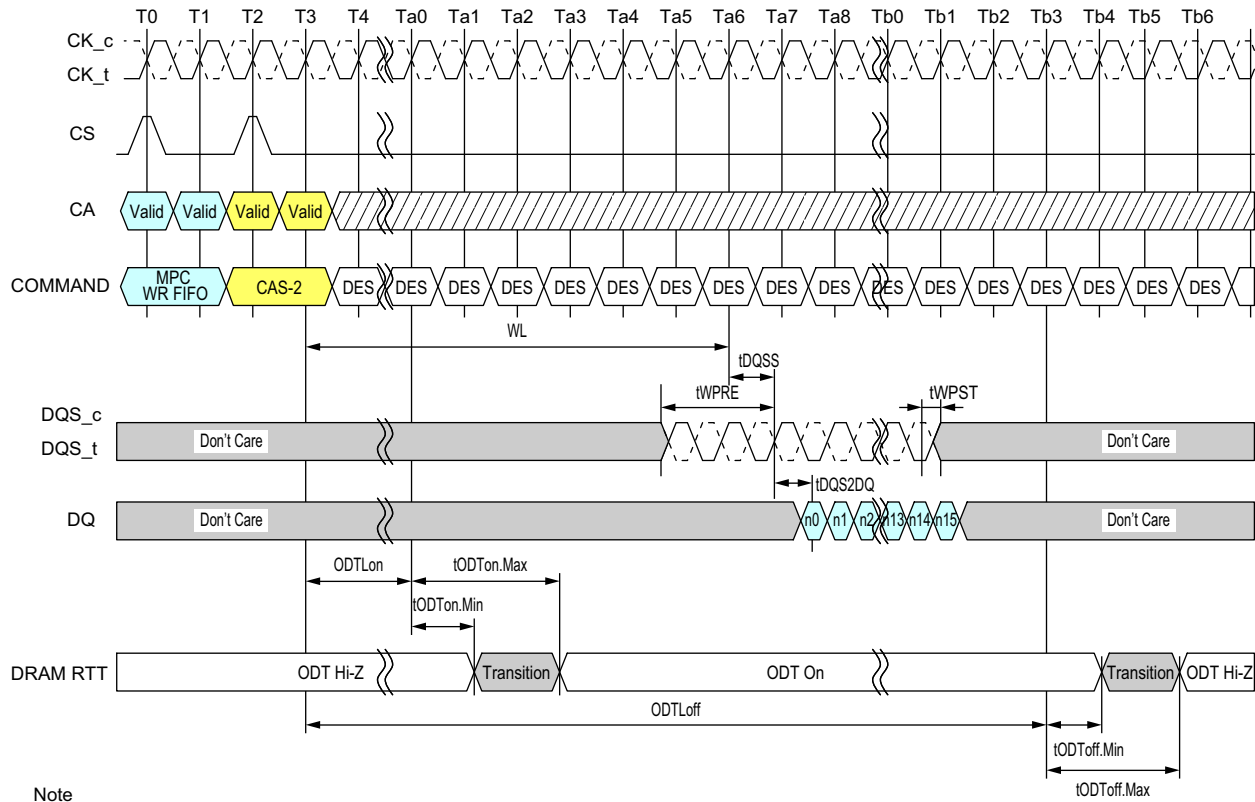


- NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
  2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC [RD-FIFO] command to Read is tRTRRD.
  3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
  4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSQ, tDQSQ) as a Read-1 command.
  5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
  6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
  7. DM[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.
  8. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK
  9. DES commands are shown for ease of illustration; other commands may be valid at these times.

 DONT CARE
  TIME BREAK



**Figure - MPC [Write FIFO] with DQ ODT Timing**

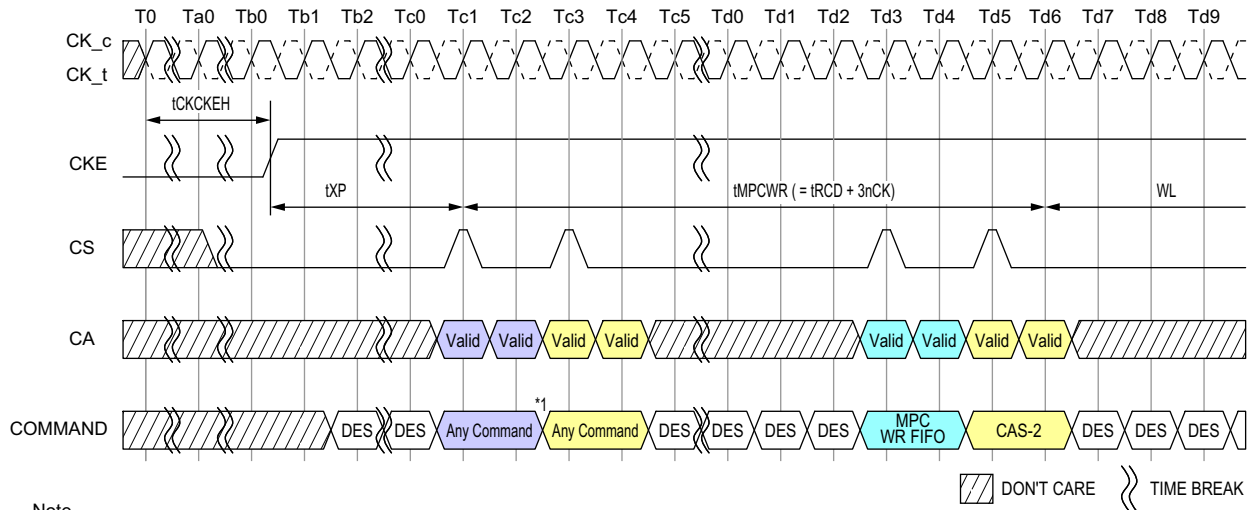


**Note**

1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [WR-FIFO] uses the same command-to-data/ODT timing relationship (WL, tDQSS, tDQS2DQ, ODTLon, ODTLoff, tODTon, tODToff) as a Write-1 command.
3. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
4. BL = 16, Write Postamble = 0.5nCK
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

 DON'T CARE
  TIME BREAK

**Figure - Power Down Exit to MPC [Write FIFO] Timing**



**Note**

1. Any commands except MPC WR FIFO and other exception commands defined other section in this document (i.e. MPC Read DQ Cal).
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

## 2.28. DQS Interval Oscillator

As voltage and temperature change on the SDRAM die, the DQS clock tree delay will shift and may require re-training. The LPDDR4-SDRAM includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error.

The DQS Interval Oscillator is started by issuing a MPC [Start DQS Osc] command with OP[6:0] set as described in the MPC Operation section, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator may be stopped by issuing a MPC [Stop DQS Osc] command with OP[6:0] set as described in the MPC Operation section, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR23 for more information). If MR23 is set to automatically stop the DQS Oscillator, then the MPC [Stop DQS Osc] command should not be used (illegal). When the DQS Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR18 and MR19.

The controller may adjust the accuracy of the result by running the DQS Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\text{DQS Oscillator Granularity Error} = 2 * (\text{DQS delay}) / \text{run time}$$

Where:

Run Time = total time between start and stop commands

DQS delay = the value of the DQS clock tree delay (tDQS2DQ min/max)

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific.

Therefore, the total accuracy of the DQS Oscillator counter is given by:

$$\text{DQS Oscillator Accuracy} = 1 - \text{Granularity Error} - \text{Matching Error}$$

**For example:** If the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 800ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\text{DQS Oscillator Granularity Error} = 2 * (0.8\text{ns}) / 100\text{ns} = 1.6\%$$

This equates to a granularity timing error or 12.8ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\text{DQS Oscillator Accuracy} = 1 - [(12.8 + 5.5) / 800] = 97.7\%$$

**For example:** running the DQS oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 500ns, and the maximum DQS clock tree delay is 800ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\text{DQS Oscillator Granularity Error} = 2 * (0.8\text{ns}) / 500\text{ns} = 0.32\%$$

This equates to a granularity timing error or 2.56ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\text{DQS Oscillator Accuracy} = 1 - [(2.56 + 5.5) / 800] = 99.0\%$$

The result of the DQS Interval Oscillator is defined as the number of DQS Clock Tree Delays that can be counted within the "run time," determined by the controller. The result is stored in MR18-OP[7:0] and MR19-OP[7:0]. MR18 contains the least significant bits (LSB) of the result, and MR19 contains the most significant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAM when a MPC-1 [Stop DQS Osc] command is received. The SDRAM counter will count to its maximum value ( $=2^{16}$ ) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest "run time" for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest Run Time Interval} = 2^{16} * t_{\text{DQS2DQ}}(\text{min}) = 2^{16} * 0.2\text{ns} = 13.1\mu\text{s}$$

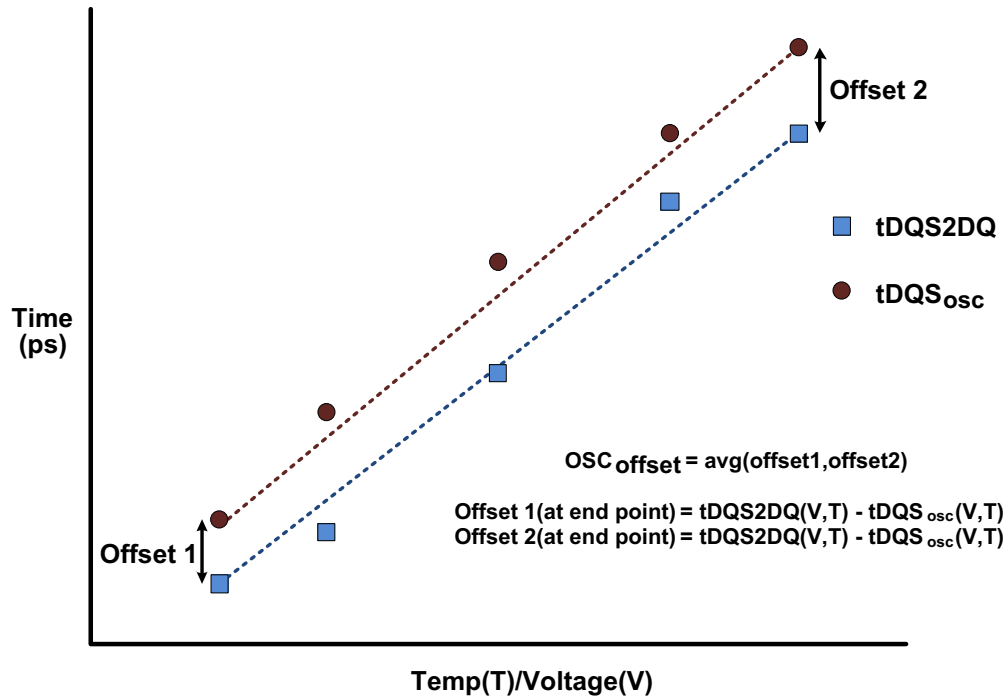
### 2.28.1. Interval Oscillator matching error

The interval oscillator matching error is defined as the difference between the DQS training ckt(interval oscillator) and the actual DQS clock tree across voltage and temperature.

#### Parameters:

- $t_{DQS2DQ}$ : Actual DQS clock tree delay
- $t_{DQSOSC}$ : Training ckt(interval oscillator) delay
- $OSC_{offset}$ : Average delay difference over voltage and temp(shown in the figure below)
- $OSC_{Match}$ : DQS oscillator matching error

**Figure - Interval oscillator offset ( $OSC_{offset}$ )**



$OSC_{Match}$  :

$$OSC_{Match} = [t_{DQS2DQ}(V,T) - t_{DQS_{OSC}}(V,T) - OSC_{offset}]$$

$t_{DQS_{OSC}}$  :

$$t_{DQS_{OSC}}(V,T) = \text{Runtime} / 2 * \text{Count}$$

**Table - DQS Oscillator Matching Error Specification**

| Parameter                     | Symbol         | Min  | Max | Units | Notes         |
|-------------------------------|----------------|------|-----|-------|---------------|
| DQS Oscillator Matching Error | $OSC_{Match}$  | -20  | 20  | ps    | 1,2,3,4,5,6,7 |
| DQS Oscillator Offset         | $OSC_{offset}$ | -100 | 100 | ps    | 2,4,7         |

Note

1. The  $OSC_{Match}$  is the matching error per between the actual DQS and DQS interval oscillator over voltage and temp.
2. This parameter will be characterized or guaranteed by design.

3. The  $OSC_{Match}$  is defined as the following:

$$OSC_{Match} = [tDQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

Where  $tDQS2DQ_{(V,T)}$  and  $tDQS_{OSC(V,T)}$  are determined over the same voltage and temp conditions.

4. The runtime of the oscillator must be at least 200ns for determining  $tDQS_{OSC(V,T)}$

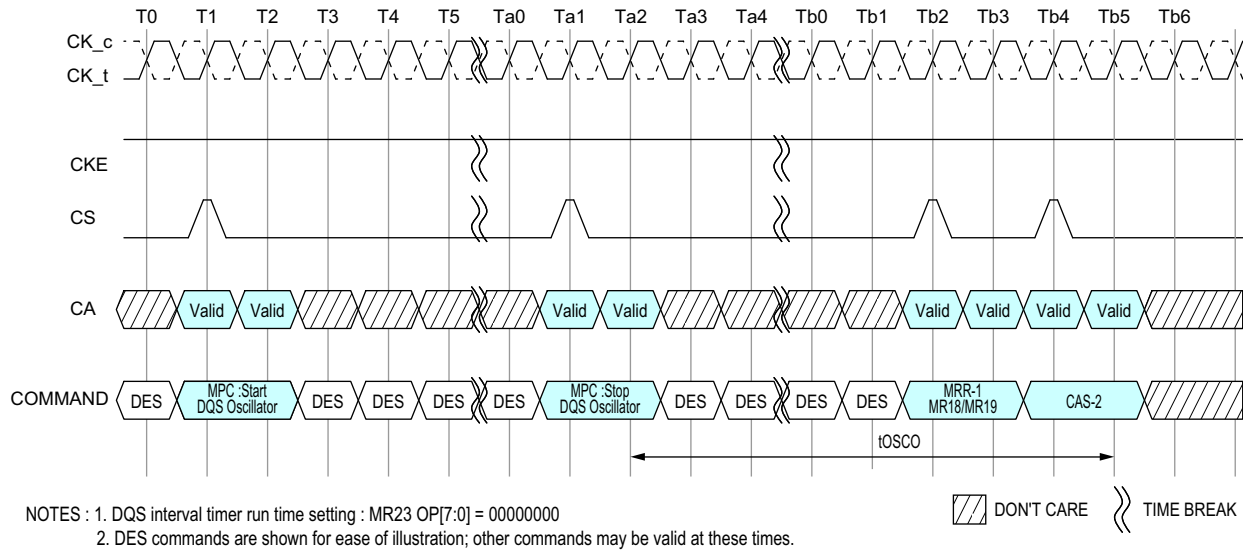
$$tDQS_{OSC(V,T)} = Runtime / 2 * Count$$

- 5. The input stimulus for  $tDQS2DQ$  will be consistent over voltage and temp conditions.
- 6. The  $OSC_{offset}$  is the average difference of the endpoints across voltage and temp.
- 7. These parameters are defined per channel.
- 8.  $tDQS2DQ(V,T)$  delay will be the average of DQS to DQ delay over the runtime period.

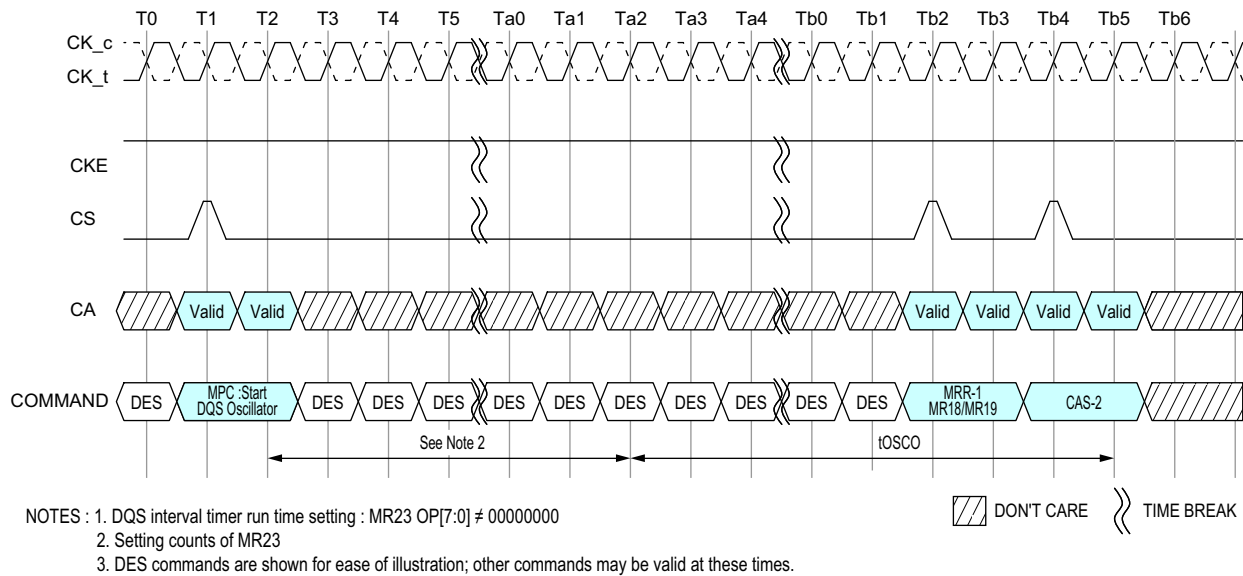
## 2.28.2. DQS Interval Oscillator Readout Timing

OSC Stop to its counting value readout timing is shown in following figures:

**Figure - In case of DQS Interval Oscillator is stopped by MPC Command**



**Figure - In case of DQS Interval Oscillator is stopped by DQS interval timer**



## 2.29. Read Preamble Training

LPDDR4 READ Preamble Training is supported through the MPC function.

This mode can be used to train or read level the DQS receivers. Once READ Preamble Training is enabled by MR13[OP1] = 1, the LPDDR4 DRAM will drive DQS\_t LOW, DQS\_c HIGH within tSDO and remain at these levels until an MPC DQ READ Training command is issued.

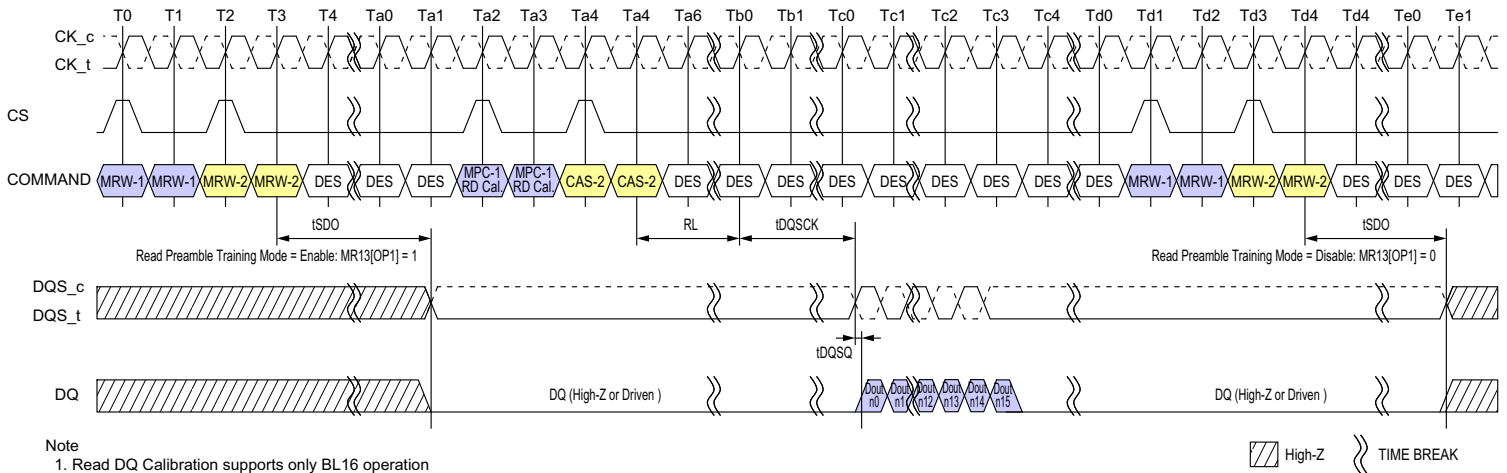
During READ Preamble Training the DQS preamble provided during normal operation will not be driven by the DRAM. Once the MPC DQ READ Training command is issued, the DRAM will drive DQS\_t/DQS\_c like a normal READ burst after RL. DRAM may or may not drive DQ[15:0] in this mode.

While in READ Preamble Training Mode, only READ DQ Calibration commands may be issued.

- Issue an MPC [RD DQ Calibration] command followed immediately by a CAS-2 command.
- Each time an MPC [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4 SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
- The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit.
- Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the DRAM mode register.
- This command can be issued every tCCD seamlessly.
- The operands received with the CAS-2 command must be driven LOW.

READ Preamble Training is exited within tSDO after setting MR13[OP1] = 0.

**Figure - Read Preamble Training**





### 2.30. Multi Purpose Command (MPC)

LPDDR4-SDRAMs use the MPC command to issue a NOP and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6]=0 then the SDRAM executes a NOP (no operation) command, and when OP[6]=1 then the SDRAM further decodes one of several training commands.

When OP[6]=1 and when the training command includes a Read or Write operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as any normal Read or Write command. The operands of the CAS-2 command following a MPC Read/Write command must be driven LOW. The following MPC commands must be followed by a CAS-2 command:

- Write FIFO
- Read FIFO
- Read DQ Calibration

All other MPC commands do not require a CAS-2 command, including:

- NOP
- Start DQS Interval Oscillator
- Stop DQS Interval Oscillator
- Start ZQ Calibration
- Latch ZQ Calibration

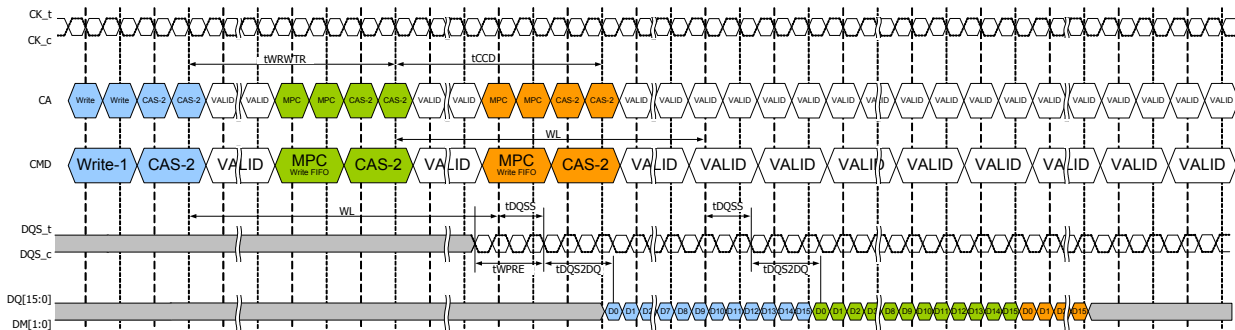
**Table - MPC Command Definition**

| Command                     | SDR Command Pins (2) |         |    | SDR CA Pins (10) |     |     |     |     |     | CK_t edge | Notes |
|-----------------------------|----------------------|---------|----|------------------|-----|-----|-----|-----|-----|-----------|-------|
|                             | CKE                  |         | CS | CA0              | CA1 | CA2 | CA3 | CA4 | CA5 |           |       |
|                             | CK_t(n-1)            | CK_t(n) |    |                  |     |     |     |     |     |           |       |
| Multi Purpose Command (MPC) | H                    | H       | H  | L                | L   | L   | L   | L   | OP6 | R1        | 1,2   |
|                             |                      |         | L  | OP0              | OP1 | OP2 | OP3 | OP4 | OP5 | R2        |       |

| Function       | Operand | Data                                                                                                                                                                                                                                                                | Notes   |
|----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| Training Modes | OP[6:0] | 0XXXXXXB: NOP<br>1000001B: RD FIFO<br>1000011B: RD DQ Calibration (MR32/MR40)<br>1000101B: RFU<br>1000111B: WR FIFO<br>1001001B: RFU<br>1001011B: Start DQS Osc<br>1001101B: Stop DQS Osc<br>1001111B: ZQCal Start<br>1010001B: ZQCal Latch<br>All Others: Reserved | 1,2,3,4 |

**Notes:**

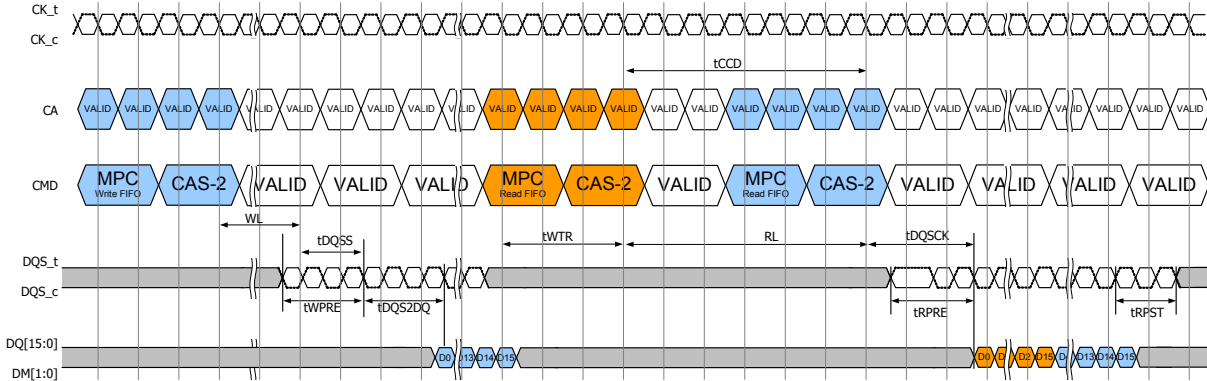
- See command truth table for more information
- MPC commands for Read or Write training operations must be immediately followed by CAS-2 command consecutively without any other commands in between. MPC command must be issued first before issuing the CAS-2 command.

**Figure - MPC [WR FIFO] Operation**

**Notes:**

- MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
- Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is tWRWTR.
- Seamless MPC [WR-FIFO] commands may be executed by repeating the command every tCCD time.
- MPC [WR-FIFO] uses the same command-to-data timing relationship (WL, tDQSS, tDQS2DQ) as a Write-1 command.
- A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data. The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
- For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW."
- To avoid corrupting the FIFO contents, MPC [RD-FIFO] must immediately follow MPC [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR. See Write Training session for more information on FIFO pointer behavior.

**Figure - MPC [RD FIFO] Read Operation**

(Shown with  $t_{WPRE}=2nCK$ ,  $t_{WPST}=0.5nCK$ ,  $t_{RPRE}=toggling$ ,  $t_{RPST}=1.5nCK$ )

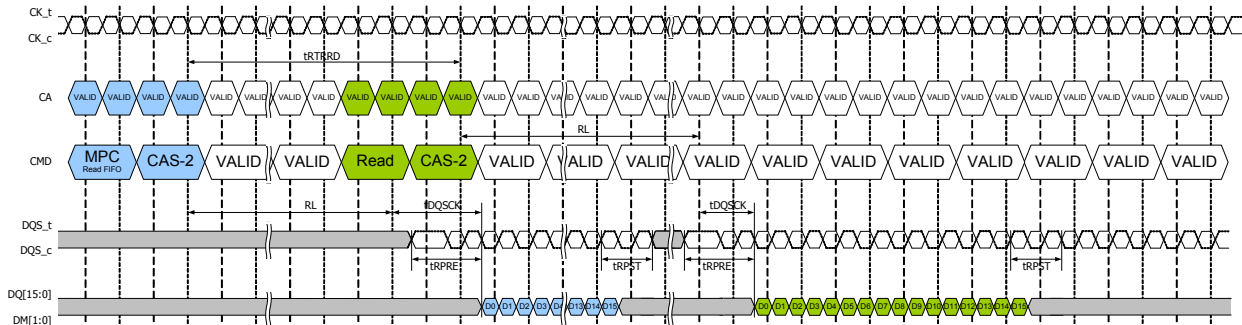


**Notes:**

1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [WR FIFO] to MPC [RD FIFO] is shown as an example of command-to-command timing for MPC.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every  $t_{CCD}$  time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL,  $t_{DQCK}$ ) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

**Figure - MPC [RD FIFO] Operation**

(Shown with  $t_{RPRE}=toggling$ ,  $t_{RPST}=1.5nCK$ )



**Notes:**

1. MPC [RD FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC [RD-FIFO] command to Read is  $t_{RTRRD}$ .
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every  $t_{CCD}$  time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL,  $t_{DQCK}$ ) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on

the FIFO pointer behavior.

6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."

7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

**Table - Timing Constraints for Training Commands**

| Previous Command        | Next Command            | Minimum Delay                           | Unit | Notes |
|-------------------------|-------------------------|-----------------------------------------|------|-------|
| WR/MWR                  | MPC [WR FIFO]           | tWRWTR                                  | nCK  | 1     |
|                         | MPC [RD FIFO]           | Not Allowed                             | -    | 2     |
|                         | MPC [RD DQ Calibration] | WL+RU(tDQSS(max)/tCK)+BL/2+RU(tWTR/tCK) | nCK  |       |
| RD/MRR                  | MPC [WR FIFO]           | tRTW                                    | nCK  | 4     |
|                         | MPC [RD FIFO]           | Not Allowed                             |      | 2     |
|                         | MPC[RD DQ Calibration]  | tRTRRD                                  | nCK  | 3     |
| MPC [WR FIFO]           | WR/MWR                  | Not Allowed                             |      | 2     |
|                         | MPC [WR FIFO]           | tCCD                                    | nCK  |       |
|                         | RD/MRR                  | Not Allowed                             |      | 2     |
|                         | MPC [RD FIFO]           | WL+RU(tDQSS(max)/tCK)+BL/2+RU(tWTR/tCK) | nCK  |       |
|                         | MPC [RD DQ Calibration] | Not Allowed                             |      | 2     |
| MPC [RD FIFO]           | WR/MWR                  | tRTW                                    | nCK  | 4     |
|                         | MPC [WR FIFO]           | tRTW                                    | nCK  | 4     |
|                         | RD/MRR                  | tRTRRD                                  | nCK  | 3     |
|                         | MPC [RD FIFO]           | tCCD                                    | nCK  |       |
|                         | MPC [RD DQ Calibration] | tRTRRD                                  | nCK  | 3     |
| MPC [RD DQ Calibration] | WR/MWR                  | tRTW                                    | nCK  | 4     |
|                         | MPC [WR FIFO]           | tRTW                                    | nCK  | 4     |
|                         | RD/MRR                  | tRTRRD                                  | nCK  | 3     |
|                         | MPC [RD FIFO]           | Not Allowed                             |      | 2     |
|                         | MPC [RD DQ Calibration] | tCCD                                    | nCK  |       |

Notes:

- $tWRWTR = WL + BL/2 + RU(tDQSS(max)/tCK) + \max(RU(7.5ns/tCK), 8nCK)$
- No commands are allowed between MPC [WR FIFO] and MPC [RD FIFO] except MRW commands related to training parameters.
- $tRTRRD = RL + RU(tDQSS(max)/tCK) + BL/2 + RD(tRPST) + \max(RU(7.5ns/tCK), 8nCK)$
- tRTW (DQ ODT Disabled case; MR11 OP[2:0]=000b)**  
 $= RL + RU(tDQSS(max)/tCK) + BL/2 - WL + tWPRES + RD(tRPST)$   
**tRTW (DQ ODT Enabled case; MR11 OP[2:0]≠000b)**  
 $= RL + RU(tDQSS(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTmin/tCK) + 1$

---

### 2.31. Thermal offset

Because of their tight thermal coupling with the LPDDR4 device, hot spots on an SOC can induce thermal gradients across the LPDDR4 device. As these hot spots may not be located near the device thermal sensor, the devices' temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through MR4(6:5) to either or to both the channels. This temperature offset may modify refresh behavior for the channel to which the offset is provided. It will take a max of 200us to have the change reflected in MR4(2:0) for the channel to which the offset is provided. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is larger than 15 degrees C, then self-refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the LPDDR4 memory controller.

Support of thermal offset function is optional. Please refer to vendor datasheet to figure out if the function is supported or not.

### 2.32. Temperature Sensor

LPDDR4 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

LPDDR4 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4[2:0] equals 'b011. LPDDR4 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + \text{tTSI} + \text{SysRespDelay}) \leq 2^\circ\text{C}$$

**Table - Temperature Sensor**

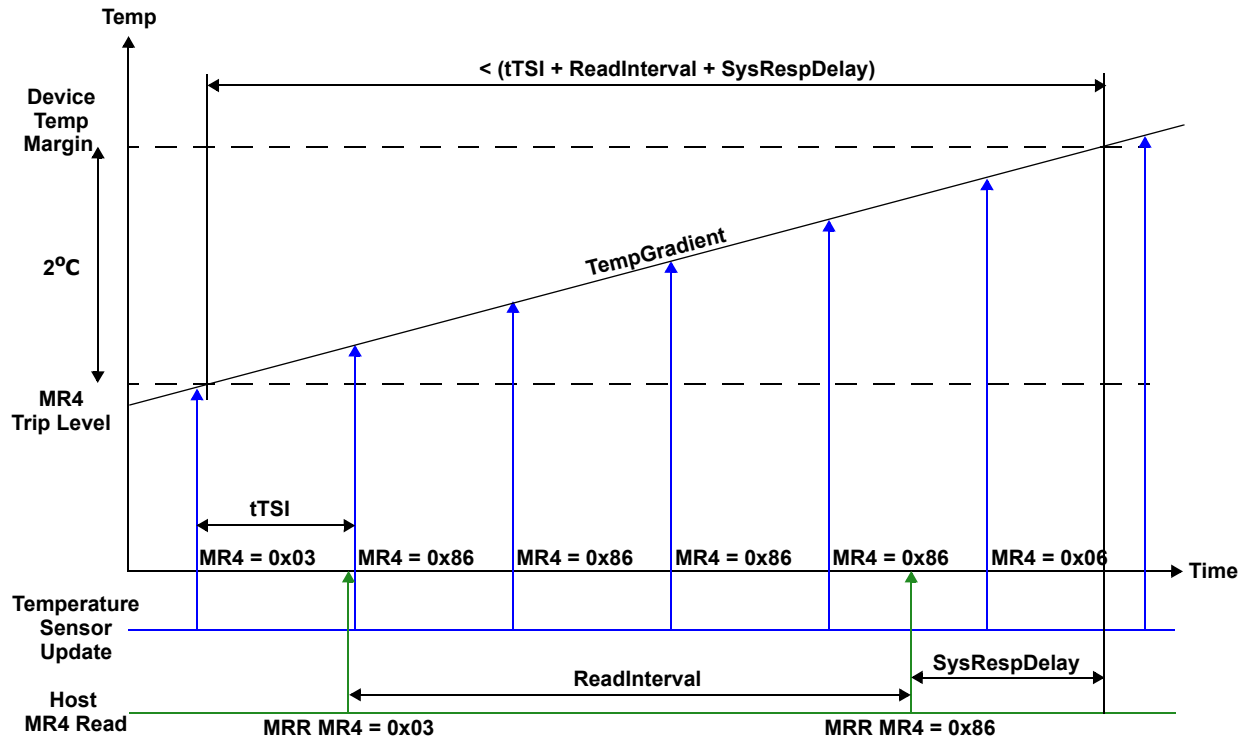
| Parameter                   | Symbol       | Max/Min | Value            | Unit | Notes |
|-----------------------------|--------------|---------|------------------|------|-------|
| System Temperature Gradient | TempGradient | Max     | System Dependent | °C/s |       |
| MR4 Read Interval           | ReadInterval | Max     | System Dependent | ms   |       |
| Temperature Sensor Interval | tTSI         | Max     | 32               | ms   |       |
| System Response Delay       | SysRespDelay | Max     | System Dependent | ms   |       |
| Device Temperature Margin   | TempMargin   | Max     | 2                | °C   |       |

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

$$(10^\circ\text{C/s}) \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2^\circ\text{C}$$

In this case, ReadInterval shall be no greater than 167ms.

Figure - Temp sensor Timing



### 2.33. ZQ Calibration

The MPC command is used to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation, and is designed to eliminate any need for coordination between channels (i.e. it allows for channel independence).

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the SDRAM's calibration procedure, and ZQCal Latch captures the result and loads it into the SDRAM's drivers.

A ZQCal Start command may be issued anytime the LPDDR4-SDRAM is not in a power-down state. A ZQCal Latch Command may be issued anytime outside of power-down after tZQCAL has expired and all DQ bus operations have completed. The CA Bus must maintain a Deselect state during tZQLAT to allow CA ODT calibration settings to be updated. The following mode register fields that modify I/O parameters cannot be changed following a ZQCal Start command and before tZQCAL has expired:

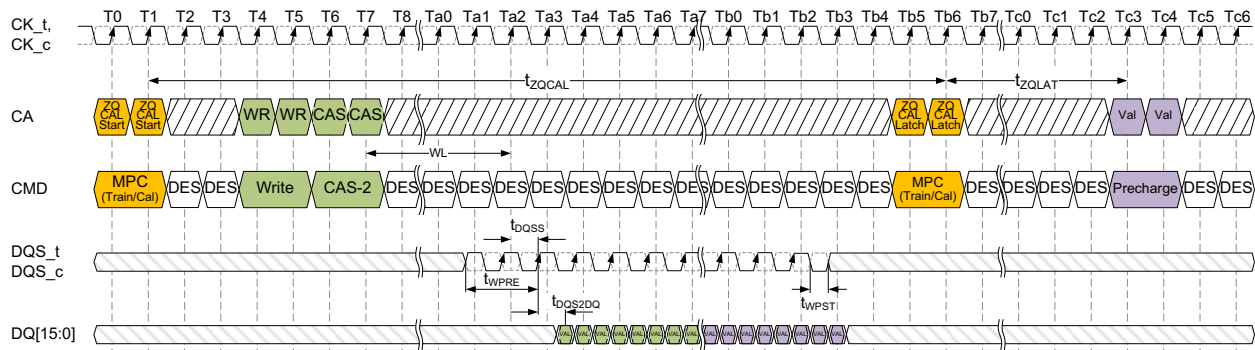
- PU-Cal (Pull-up Calibration VOH Point)
- PDDS (Pull Down Drive Strength and Rx Termination)
- DQ-ODT (DQ ODT Value)
- CA-ODT (CA ODT Value)

#### 2.33.1. ZQCal Reset

The ZQCal Reset command resets the output impedance calibration to a default accuracy of +/- 30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to +/- 30% when ZQCal Start and ZQCal Latch commands are not used.

The ZQCal Reset command is executed by writing MR10-OP[0]=1B.

**Figure - ZQCal Timing**



Note

1. Write and Precharge operations shown for illustrative purposes. Any single or multiple valid commands may be executed within the tZQCAL time and prior to latching the results.
2. Before the ZQ-Latch command can be executed, any prior commands utilizing the DQ bus must have completed. Write commands with DQ Termination must be given enough time to turn off the DQ-ODT before issuing the ZQ-Latch command. See the ODT section for ODT timing.



### 2.33.2. Multi-Channel Considerations

The LPDDR4-SDRAM includes a single ZQ pin and associated ZQ Calibration circuitry. Calibration values from this circuit will be used by both channels according to the following protocol:

1. ZQCal Start commands may be issued to either or both channels.
2. ZQCal Start commands may be issued when either or both channels are executing other commands and other commands may be issued during tZQCAL.
3. ZQCal Start commands may be issued to both channels simultaneously.
4. The ZQCal Start command will begin the calibration unless a previously requested ZQ calibration is in progress.
5. If a ZQCal Start command is received while a ZQ calibration is in progress on the SDRAM, the ZQCal Start command will be ignored and the in-progress calibration will not be interrupted.
6. ZQCal Latch commands are required for each channel.
7. ZQCal Latch commands may be issued to both channels simultaneously.
8. ZQCal Latch commands will latch results of the most recent ZQCal Start command provided tZQCAL has been met.
9. ZQCal Latch commands which do not meet tZQCAL will latch the results of the most recently completed ZQ calibration.
10. ZQ Reset MRW commands will only reset the calibration values for the channel issuing the command.

In compliance with complete channel independence, either channel may issue ZQCal Start and ZQCal Latch commands as needed without regard to the state of the other channel.

#### 2.33.2.1. ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and VDDQ.

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQ pin of each die's x16 channel shall use a separate ZQCal resistor.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQ Cal's don't overlap.

The total capacitive loading on the ZQ pin must be limited to 25pF.

Example: If a system configuration shares a CA bus between 'n' channels to form a n \* 16 wide bus, and no means are available to control the ZQCal separately for each channel (i.e. separate CS, CKE, or CK), then each x16 channel must have a separate ZQCal resistor.

Example: For a x32, two rank system, each x16 channel must have its own ZQCal resistor, but the ZQCal resistor can be shared between ranks on each x16 channel. In this configuration, the CS signal can be used to ensure that the ZQCal commands for Rank[0] and Rank[1] don't overlap.

#### 2.33.2.2. ZQ Wiring for Byte-mode PKG including mixed configuration

Standard LPDDR4 package ballmaps allocate one ZQ ball per die. Byte-mode packages potentially support more die for higher package memory density. In order to use ballmaps developed for Standard LPDDR4, an alternate ZQ ball wiring strategy is employed when packages contain Byte-mode devices as shown in Figure in section 2.1.

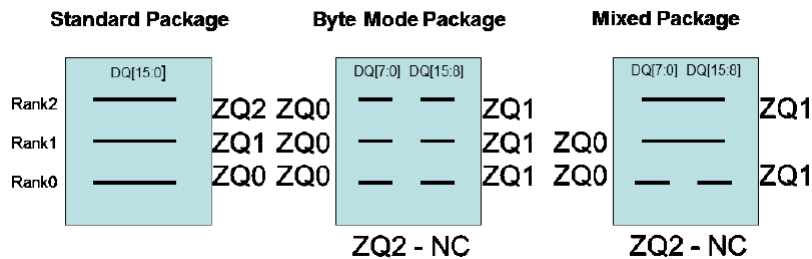
Since the wiring strategy for Byte-mode and Mixed packages shares a single ZQ resistor among ranks, applications must

ensure that the ZQ cal's do not overlap. (See section 4.33.2.1)

Below are specific wiring notes for dual channel (x32) LPDDR4 packages

1. For packages using only standard devices
  - ZQ0 is connected to rank 0 DRAM
  - ZQ1 is connected to rank 1 DRAM (if present)
  - ZQ2 is connected to rank 2 DRAM (if present)
2. For packages using only byte-mode devices
  - ZQ0 is connected to all lower byte[7:0] or upper byte [15:8] DRAM(s)
  - ZQ1 is connected to opposite byte of all DRAM(s) from those connected to ZQ0
  - ZQ2 is NC
3. For packages using both standard and byte-mode devices
  - ZQ0 is connected to all lower byte[7:0] or upper byte [15:8] DRAM(s)
  - ZQ1 is connected to opposite byte of all DRAM(s) from those connected to ZQ0
  - Standard DRAM(s) may be connected to either ZQ0 or ZQ1
  - ZQ2 is NC

Multi-rank packages containing Byte-mode devices place additional loading on the I/O and power topologies and therefore may not be appropriate for all application environments.



## 2.34. Pull-down and Pull-up Driver Characteristics and Calibration Point

**Table - Pull-down Driver Characteristics, with ZQ Calibration**

| <b>R<sub>ONPD,nom</sub></b> | <b>Resistor</b>      | <b>Min</b> | <b>Nom</b> | <b>Max</b> | <b>Unit</b> |
|-----------------------------|----------------------|------------|------------|------------|-------------|
| 40 Ohm                      | R <sub>ON40PD</sub>  | 0.90       | 1.0        | 1.10       | RZQ/6       |
| 48 Ohm                      | R <sub>ON48PD</sub>  | 0.90       | 1.0        | 1.10       | RZQ/5       |
| 60 Ohm                      | R <sub>ON60PD</sub>  | 0.90       | 1.0        | 1.10       | RZQ/4       |
| 80 Ohm                      | R <sub>ON80PD</sub>  | 0.90       | 1.0        | 1.10       | RZQ/3       |
| 120 Ohm                     | R <sub>ON120PD</sub> | 0.90       | 1.0        | 1.10       | RZQ/2       |
| 240 Ohm                     | R <sub>ON240PD</sub> | 0.90       | 1.0        | 1.10       | RZQ/1       |

Notes:

1. All values are after ZQ calibration. Without ZQ Calibration R<sub>ONPD</sub> values are +/- 30%

**Table - Pull-up Driver Characteristics, with ZQ Calibration**

| <b>VOH<sub>PU,nom</sub></b> | <b>VOH,nom(mV)</b> | <b>Min</b> | <b>Nom</b> | <b>Max</b> | <b>Unit</b> |
|-----------------------------|--------------------|------------|------------|------------|-------------|
| VDDQ*0.5                    | 300                | 0.90       | 1.0        | 1.10       | VOH,nom     |
| VDDQ*0.6                    | 360                | 0.90       | 1.0        | 1.10       | VOH,nom     |

Notes:

1. All values are after ZQ calibration. Without ZQ Calibration VOH,nom values are +/- 30%
2. VOH,nom (mV) values are based on a nominal VDDQ=0.6V.

**Table - Valid Calibration Points**

| <b>VOH<sub>PU,nom</sub></b> | <b>ODT Values</b> |            |           |           |           |           |
|-----------------------------|-------------------|------------|-----------|-----------|-----------|-----------|
|                             | <b>240</b>        | <b>120</b> | <b>80</b> | <b>60</b> | <b>48</b> | <b>40</b> |
| VDDQ*0.5                    | Valid             | Valid      | Valid     | Valid     | Valid     | Valid     |
| VDDQ*0.6                    | DNU               | Valid      | DNU       | Valid     | DNU       | DNU       |

Notes:

1. Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.
2. If the VOH(nom) calibration point is changed, then re-calibration is required.
3. DNU = Do Not Use

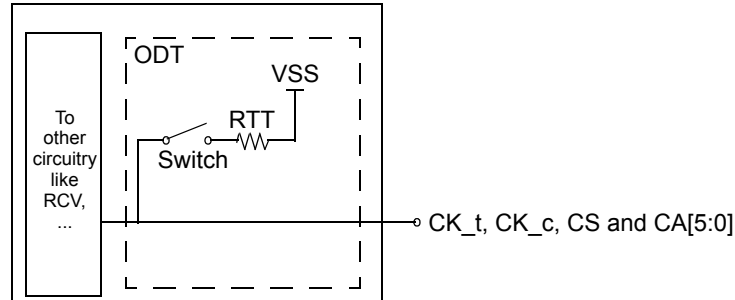
### 2.35. Command/Address Bus On Die Termination

ODT (On-Die Termination) is a feature of the LPDDR4 SDRAM that allows the SDRAM to turn on/off termination resistance for CK<sub>t</sub>, CK<sub>c</sub>, CS and CA[5:0] signals without the ODT control pin.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting.

A simple functional representation of the DRAM ODT feature is shown in the Figure below

**Figure - Functional Representation of CA ODT**



#### 2.35.1. ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK<sub>t</sub>, CK<sub>c</sub>, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK<sub>t</sub>, CK<sub>c</sub>, CS and CA[5:0] signals. Only one termination load will be present even if multiple devices are sharing the command signals. In a multirank system, the terminating rank should be trained first, followed by the non-terminating rank(s).

**Table - Command Bus ODT State**

| ODTE-CA<br>MR11[6:4]  | ODTD-CA<br>MR22[5] | ODTF-CK<br>MR22[3] | ODTF-CS<br>MR22[4] | ODT State<br>for CA | ODT State<br>for CK <sub>t</sub> /CK <sub>c</sub> | ODT State<br>for CS |
|-----------------------|--------------------|--------------------|--------------------|---------------------|---------------------------------------------------|---------------------|
| Disabled <sup>1</sup> | Valid <sup>2</sup> | Valid <sup>2</sup> | Valid <sup>2</sup> | Off                 | Off                                               | Off                 |
| Valid <sup>2</sup>    | 0                  | 0                  | 0                  | On                  | On                                                | On                  |
| Valid <sup>2</sup>    | 0                  | 0                  | 1                  | On                  | On                                                | Off                 |
| Valid <sup>2</sup>    | 0                  | 1                  | 0                  | On                  | Off                                               | On                  |
| Valid <sup>2</sup>    | 0                  | 1                  | 1                  | On                  | Off                                               | Off                 |
| Valid <sup>2</sup>    | 1                  | 0                  | 0                  | Off                 | On                                                | On                  |
| Valid <sup>2</sup>    | 1                  | 0                  | 1                  | Off                 | On                                                | Off                 |
| Valid <sup>2</sup>    | 1                  | 1                  | 0                  | Off                 | Off                                               | On                  |
| Valid <sup>2</sup>    | 1                  | 1                  | 1                  | Off                 | Off                                               | Off                 |

Notes:

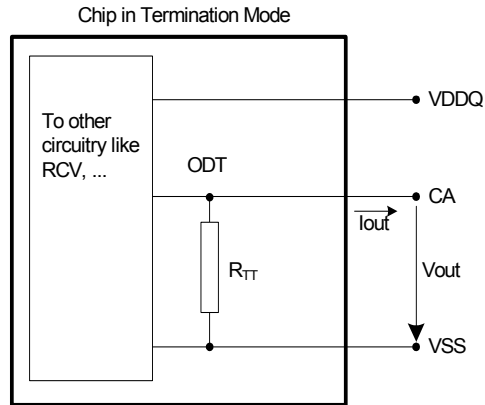
1. Default value
2. "Valid" means "0 or 1"
2. The state of ODT<sub>CA</sub> is not changed when the DRAM enters power-down mode. This maintains termination for alternate ranks in multi-rank systems.

## 2.35.2. ODT Mode Register and ODT characteristics

A functional representation of the on-die termination is shown in the figure below.

$$RTT = V_{out} / |I_{out}|$$

**Figure - CA On Die Termination**



**Table - ODT DC Electrical Charanteristics, assuming RZQ=240Ω +/- 1% over the entire operating temperature range after a proper ZQ calibration up to 3200Mbps**

| MR11 OP[6:4]               | RTT  | Vout            | Min | Nom | Max | Unit  | Notes |
|----------------------------|------|-----------------|-----|-----|-----|-------|-------|
| 001                        | 240Ω | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ   | 1,2,3 |
|                            |      | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|                            |      | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 010                        | 120Ω | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/2 | 1,2,3 |
|                            |      | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|                            |      | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 011                        | 80Ω  | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/3 | 1,2,3 |
|                            |      | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|                            |      | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 100                        | 60Ω  | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/4 | 1,2,3 |
|                            |      | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|                            |      | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 101                        | 48Ω  | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/5 | 1,2,3 |
|                            |      | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|                            |      | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 110                        | 40Ω  | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/6 | 1,2,3 |
|                            |      | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|                            |      | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| Mismatch CA-CA within byte |      | 0.50*VDDQ       | -   |     | 2   | %     | 1,2,4 |

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-dn ODT resistors are recommended to be calibrated at 0.50\*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.75\*VDD2 and 0.2\*VDD2.
3. Measurement definition for RTT: **TBD**
4. CA to CA mismatch within clock group (CA,CS) variation for a given component including CK\_t and CK\_c (characterized).

$$CA - CA_{mismatch} = \frac{RODT(max) - RODT(min)}{RODT(avg)}$$

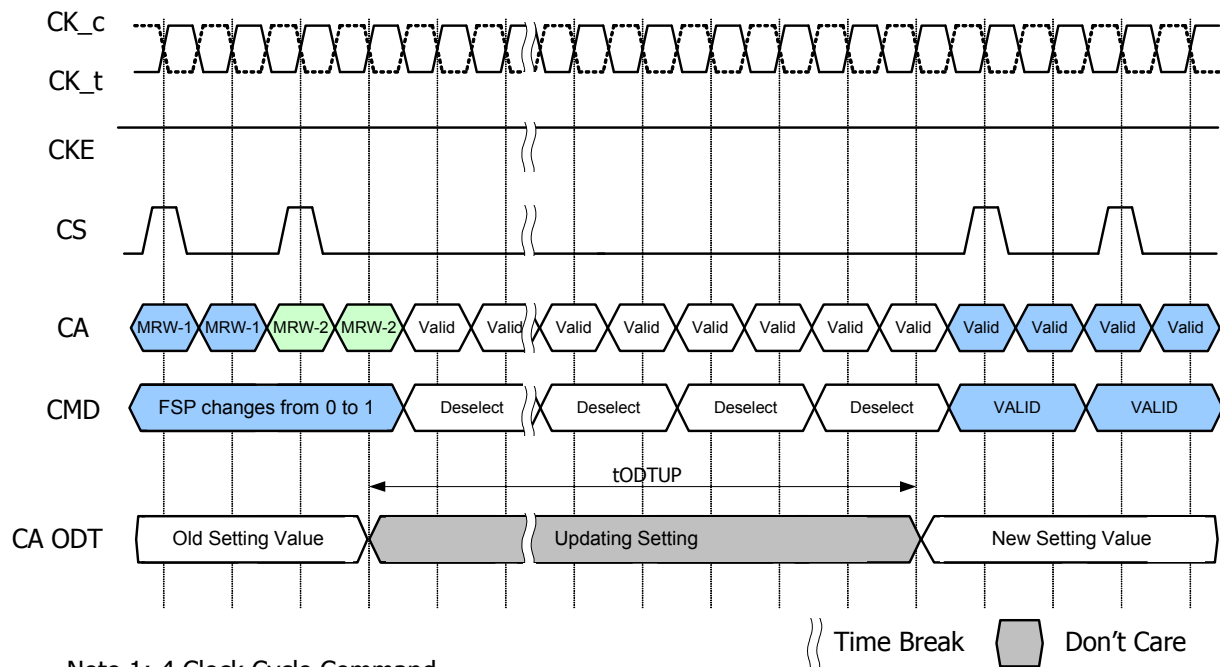
Notes:

1. As of publication of this document, under discussion by the formulating committee.

### 2.35.3. ODT for Command/Address update time

ODT for Command/Address update time after Mode Register set are shown in the figure below

**Figure - CA ODT setting update timing in 4 Clock Cycle Command**



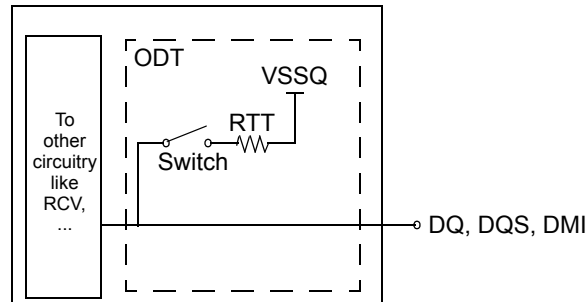
Note 1: 4 Clock Cycle Command

## 2.36. DQ On-die Termination

ODT (On-Die Termination) is a feature of the LPDDR4 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS<sub>t</sub>, DQS<sub>c</sub> and DMI signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during Write operation.

The ODT feature is off and cannot be supported in Power Down and Self-Refresh modes.

A simple functional representation of the DRAM ODT feature is shown in following Figure.



**Figure - Functional Representation of DQ ODT**

The switch is enabled by the internal ODT control logic, which uses the Write-1 command and other mode register control information. The value of RTT is determined by the settings of Mode Register bits.

### 2.36.1. ODT Mode Register

The ODT Mode is enabled if MR11 OP[2:0] are non zero. In this case, the value of RTT is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP[2:0] = 000b.

### 2.36.2. Asynchronous ODT

When ODT Mode is enabled in MR11 OP[2:0], DRAM ODT is always Hi-Z. DRAM ODT feature is automatically turned ON asynchronously based on the Write-1 or Mask Write-1 command that DRAM samples. After the write burst is complete, DRAM ODT featured is automatically turned OFF asynchronously.

Following timing parameters apply when DRAM ODT mode is enabled::

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODToff,min, tODToff,max

ODTLon is a synchronous parameter and it is the latency from CAS-2 command to tODTon reference. ODTLon latency is a fixed latency value for each speed bin. Each speed bin has a different ODTLon latency. Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on.

Maximum RTT turn on time (tODT<sub>on,max</sub>) is the point in time when the ODT resistance is fully on. tODT<sub>on,min</sub> and tODT<sub>on,max</sub> are measured once ODT<sub>Lon</sub> latency is satisfied from CAS-2 command. ODT<sub>Loff</sub> is a synchronous parameter and it is the latency from CAS-2 command to tODT<sub>off</sub> reference. ODT<sub>Loff</sub> latency is a fixed latency value for each speed bin. Each speed bin has a different ODT<sub>Loff</sub> latency. Minimum RTT turn-off time (tODT<sub>off,min</sub>) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (tODT<sub>off,max</sub>) is the point in time when the on-die termination has reached high impedance. tODT<sub>off,min</sub> and tODT<sub>off,max</sub> are measured once ODT<sub>Loff</sub> latency is satisfied from CAS-2 command.

**Table - ODT Timings**

| ODT <sub>Lon</sub> Latency <sup>a)</sup> |            | ODT <sub>Loff</sub> Latency <sup>b)</sup> |            | Lower Frequency Limit (>) | Upper Frequency Limit (≤) |
|------------------------------------------|------------|-------------------------------------------|------------|---------------------------|---------------------------|
| WL Set "A"                               | WL Set "B" | WL Set "A"                                | WL Set "B" |                           |                           |
| N/A                                      | N/A        | N/A                                       | N/A        | 10                        | 266                       |
| N/A                                      | N/A        | N/A                                       | N/A        | 266                       | 533                       |
| N/A                                      | 6          | N/A                                       | 22         | 533                       | 800                       |
| 4                                        | 12         | 20                                        | 28         | 800                       | 1066                      |
| 4                                        | 14         | 22                                        | 32         | 1066                      | 1333                      |
| 6                                        | 18         | 24                                        | 36         | 1333                      | 1600                      |
| 6                                        | 20         | 26                                        | 40         | 1600                      | 1866                      |
| 8                                        | 24         | 28                                        | 44         | 1866                      | 2133                      |
| nCK                                      | nCK        | nCK                                       | nCK        | MHz                       | MHz                       |

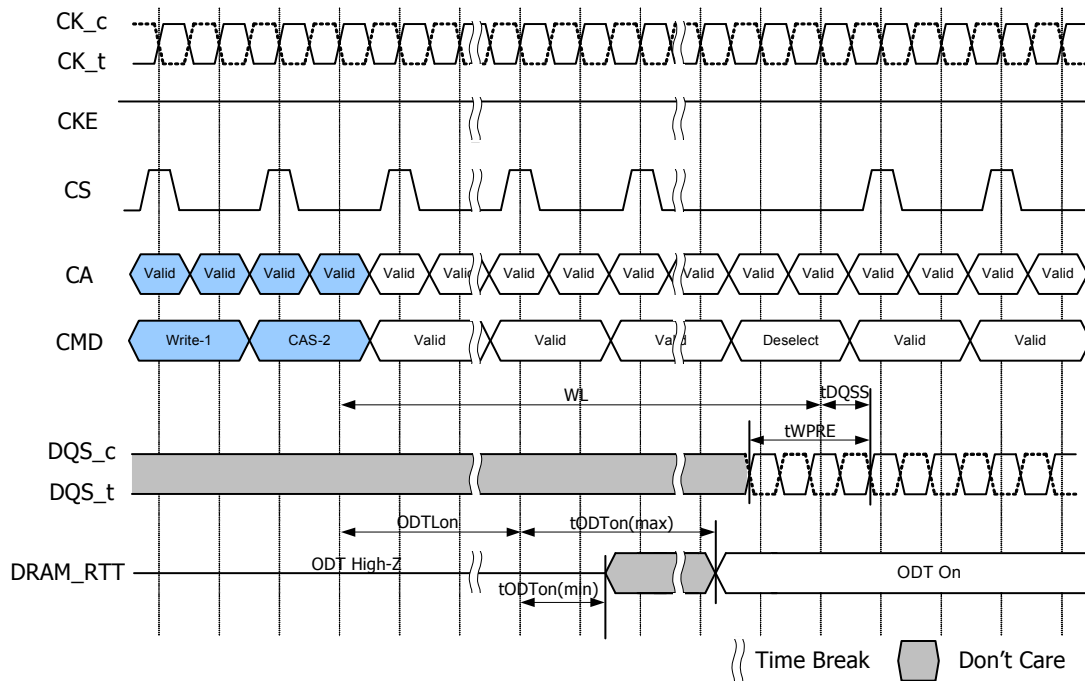
- a. ODT<sub>Lon</sub> is referenced from CAS-2 command. See timing diagram examples below.  
b. ODT<sub>Loff</sub> is shown in table assumes BL=16. For BL32, 8 tCK should be added.

**Table - Asynchronous ODT turn on and turn off timing**

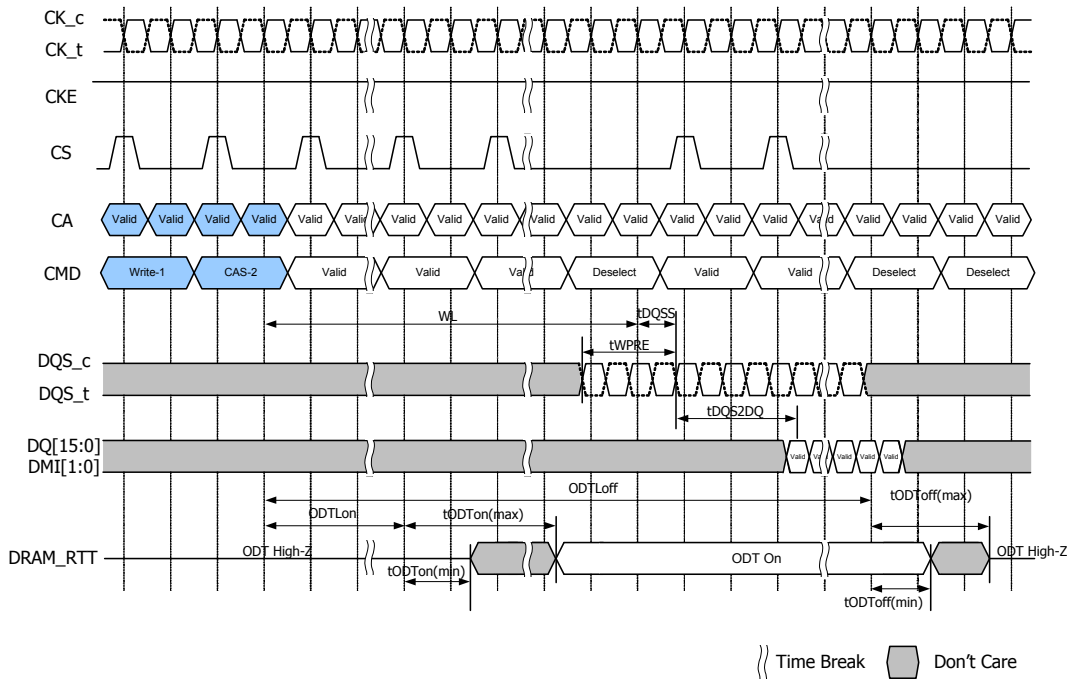
| Parameter               | 800~2133MHz | Unit |
|-------------------------|-------------|------|
| tODT <sub>on,min</sub>  | 1.5         | ns   |
| tODT <sub>on,max</sub>  | 3.5         | ns   |
| tODT <sub>off,min</sub> | 1.5         | ns   |
| tODT <sub>off,max</sub> | 3.5         | ns   |



**Figure - Asynchronous ODT<sub>ON</sub> Timing Example;  $t_{WPRE} = 2 t_{CK}$ ,  $t_{DQSS} = \text{Nominal}$**



**Figure - Asynchronous ODT<sub>OFF</sub> Timing Example,  $t_{WPRE} = 2 nCK$ ,  $t_{DQSS} = \text{Nominal}$**



### 2.36.3. ODT during Write Leveling

If ODT is enabled in MR11 OP[2:0], in Write Leveling mode, DRAM always provides the termination on DQS\_t/DQS\_c signals. DQ termination is always off in Write Leveling mode regardless.

**Table - DRAM Termination Function in Write Leveling Mode**

| ODT Enabled in MR11 | DQS_t/DQS_c termination | DQ termination |
|---------------------|-------------------------|----------------|
| Disabled            | OFF                     | OFF            |
| Enabled             | ON                      | OFF            |

### 2.37. On Die Termination for DQ, DQS and DMI

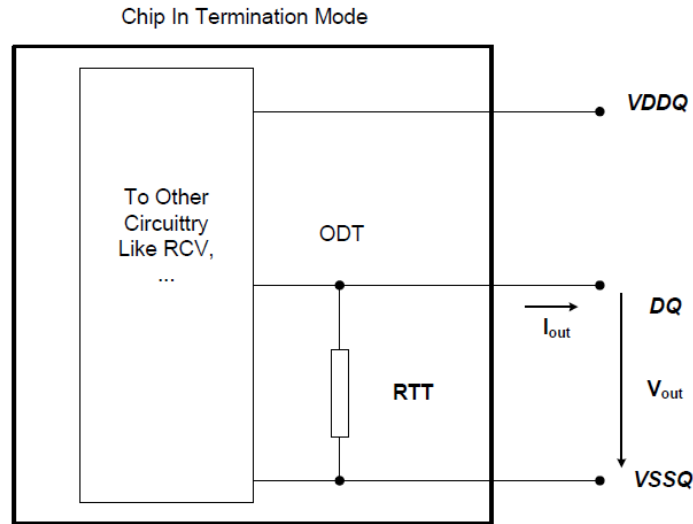
On-Die Termination effective resistance  $RTT$  is defined by MR bits MR11 OP[2:0].

ODT is applied to the DQ, DMI, DQS\_t and DQS\_c pins.

A functional representation of the on-die termination is shown in the figure below.

$$RTT = V_{out} / |I_{out}|$$

**Figure - DQ On Die Termination**



**Table - ODT DC Electrical Characteristics, assuming  $RZQ=240\Omega \pm 1\%$  over the entire operating temperature range after a proper ZQ calibration for up to 3200Mbps.**

| MR11 OP[2:0] | RTT          | Vout            | Min | Nom | Max | Unit  | Notes |
|--------------|--------------|-----------------|-----|-----|-----|-------|-------|
| 001          | 240 $\Omega$ | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ   | 1,2,3 |
|              |              | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|              |              | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 010          | 120 $\Omega$ | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/2 | 1,2,3 |
|              |              | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|              |              | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 011          | 80 $\Omega$  | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/3 | 1,2,3 |
|              |              | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|              |              | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 100          | 60 $\Omega$  | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/4 | 1,2,3 |
|              |              | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|              |              | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 101          | 48 $\Omega$  | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/5 | 1,2,3 |
|              |              | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|              |              | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |
| 110          | 40 $\Omega$  | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/6 | 1,2,3 |
|              |              | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 |       | 1,2,3 |
|              |              | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 |       | 1,2,3 |

| MR11 OP[2:0]               | RTT | Vout      | Min | Nom | Max | Unit | Notes |
|----------------------------|-----|-----------|-----|-----|-----|------|-------|
| Mismatch CA-CA within byte |     | 0.50*VDDQ | -   |     | 2   | %    | 1,2,4 |

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-dn ODT resistors are recommended to be calibrated at 0.50\*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.75\*VDDQ and 0.2\*VDDQ.
3. Measurement definition for RTT: TBD
4. DQ to DQ mismatch within byte variation for a given component including DQS\_t and DQS\_c (characterized).

$$DQ - DQ_{mismatch} = \frac{RODT(max) - RODT(min)}{RODT(avg)}$$

Notes:

1. As of publication of this document, under discussion by the formulating committee.

## 2.38. Output Driver and Termination Register Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

**Table - Output Driver and Termination Register Sensitivity Definition**

| Resistor      | Definition Point   | Min                                                              | Max                                                               | Unit | Notes |
|---------------|--------------------|------------------------------------------------------------------|-------------------------------------------------------------------|------|-------|
| $R_{ONPD}$    | $0.50 \times VDDQ$ | $90-(dR_{on}dT \times  \Delta T )-(dR_{on}dV \times  \Delta V )$ | $110+(dR_{on}dT \times  \Delta T )+(dR_{on}dV \times  \Delta V )$ | %    | 1,2   |
| $VOH_{PU}$    | $0.50 \times VDDQ$ | $90-(dVOHdT \times  \Delta T )-(dVOHdV \times  \Delta V )$       | $110+(dVOHdT \times  \Delta T )+(dVOHdV \times  \Delta V )$       | %    | 1,2,5 |
| $R_{TT(I/O)}$ | $0.50 \times VDDQ$ | $90-(dR_{on}dT \times  \Delta T )-(dR_{on}dV \times  \Delta V )$ | $110+(dR_{on}dT \times  \Delta T )+(dR_{on}dV \times  \Delta V )$ | %    | 1,2,3 |
| $R_{TT(In)}$  | $0.50 \times VDDQ$ | $90-(dR_{on}dT \times  \Delta T )-(dR_{on}dV \times  \Delta V )$ | $110+(dR_{on}dT \times  \Delta T )+(dR_{on}dV \times  \Delta V )$ | %    | 1,2,4 |

Note.

1.  $\Delta T = T - T(@ \text{Calibration})$ ,  $\Delta V = V - V(@ \text{Calibration})$
2.  $dR_{on}dT$ ,  $dR_{on}dV$ ,  $dVOHdT$ ,  $dVOHdV$ ,  $dR_{TT}dV$ , and  $dR_{TT}dT$  are not subject to production test but are verified by design and characterization.
3. This parameter applies to Input/Output pin such as DQS, DQ and DMI.
4. This parameter applies to Input pin such as CK, CA and CS.
5. Refer to 4.36 Pull Up/Pull Down Driver Characteristics for  $VOH_{PU}$ .

**Table - Output Driver and Termination Register Temperature and Voltage Sensitivity**

| Symbol      | Parameter                        | Min  | Max  | Unit |
|-------------|----------------------------------|------|------|------|
| $dR_{on}dT$ | $R_{ON}$ Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| $dR_{on}dV$ | $R_{ON}$ Voltage Sensitivity     | 0.00 | 0.20 | %/mV |
| $dVOHdT$    | VOH Temperature Sensitivity      | 0.00 | 0.75 | %/°C |
| $dVOHdV$    | VOH Voltage Sensitivity          | 0.00 | 0.35 | %/mV |
| $dR_{TT}dT$ | $R_{TT}$ Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| $dR_{TT}dV$ | $R_{TT}$ Voltage Sensitivity     | 0.00 | 0.20 | %/mV |

## 2.39. Power Down Mode

### 2.39.1. Power Down Entry and Exit

Power-down is asynchronously entered when CKE is driven LOW and CS is LOW. CKE must not go LOW while the following operations are in progress:

- Mode Register Read
- Mode Register Write
- Read
- Write
- Vref(CA) Range and Value setting via MRW
- Vref(DQ) Range and Value setting via MRW
- Command Bus Training mode Entering/Exiting via MRW
- VRCG High Current mode Entering/Exiting via MRW

And the LPDDR4 DRAM cannot be placed in power-down state during "Start DQS Interval Oscillator" operation.

CKE can go LOW while any other operations such as row activation, Precharge, Auto Precharge, or Refresh are in progress. The power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figure "Basic Power-Down Entry and Exit Timing".

Entering power-down deactivates the input and output buffers, excluding CKE and Reset\_n. To ensure that there is enough time to account for internal delay on the CKE signal path, CS input is required stable Low level and CA input level is don't care after CKE is driven LOW, this timing period is defined as tCKELCS.

Clock input is required after CKE is driven LOW, this timing period is defined as tCKELCK. CKE LOW will result in deactivation of all input receivers except Reset\_n after tCKELCK has expired. In power-down mode, CKE must be held LOW; all other input signals except Reset\_n are "Don't Care". CKE LOW must be maintained until tCKE,min is satisfied.

VDDQ can be turned off during power-down. Prior to exiting power-down, VDDQ must be within its minimum/maximum operating ranges.

No refresh operations are performed in power-down mode except Self-Refresh power-down. The maximum duration in non-Self-Refresh power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH must be maintained until tCKE,min is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

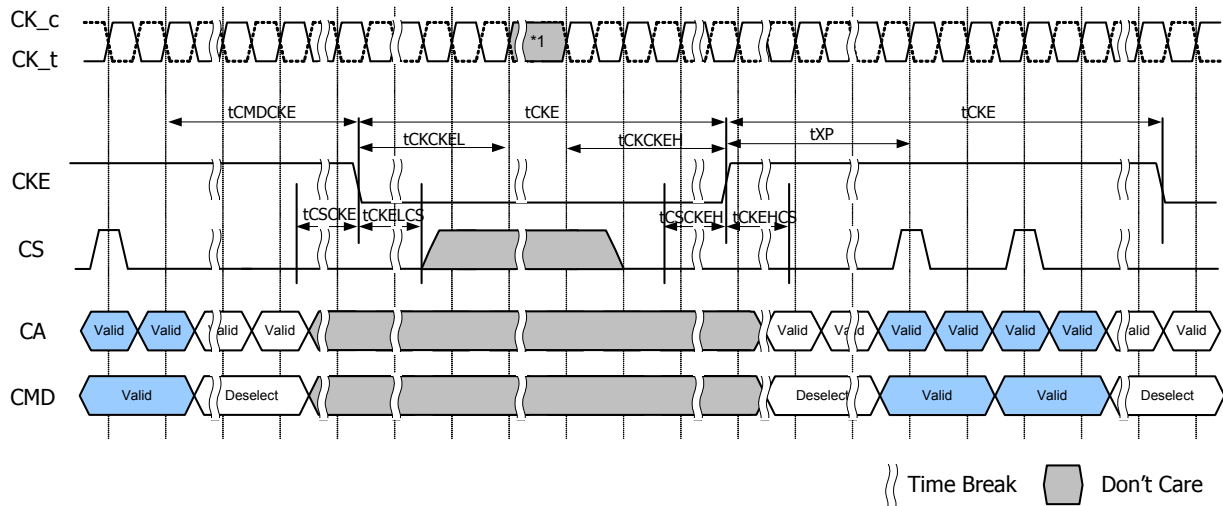
Clock frequency change or Clock Stop is inhibited during tCMDCKE, tCKELCK, tCKCKEH, tXP, tMRWCKEL and tZQCKE periods.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. And If power-down occurs when Self Refresh is in progress, this mode is referred to as Self Refresh power-down in which the internal refresh is continuing in the same way as Self Refresh mode.

When CA, CK and/or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing

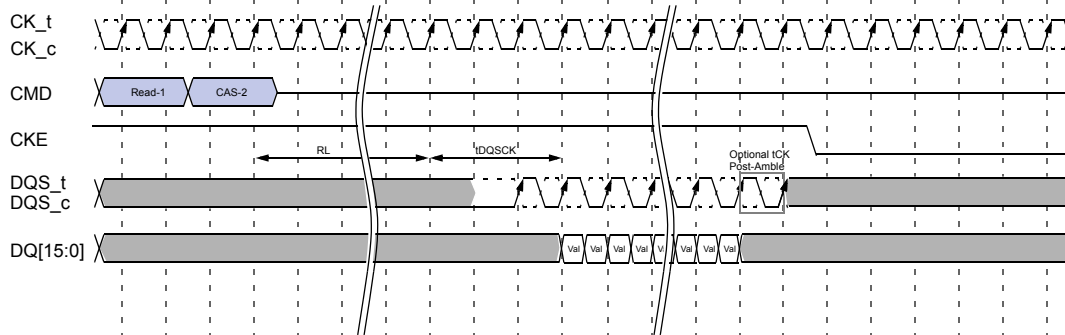
ODT will continue to terminate the command bus in all DRAM states including power-down.

**Figure - Basic Power-down Entry and Exit Timing**



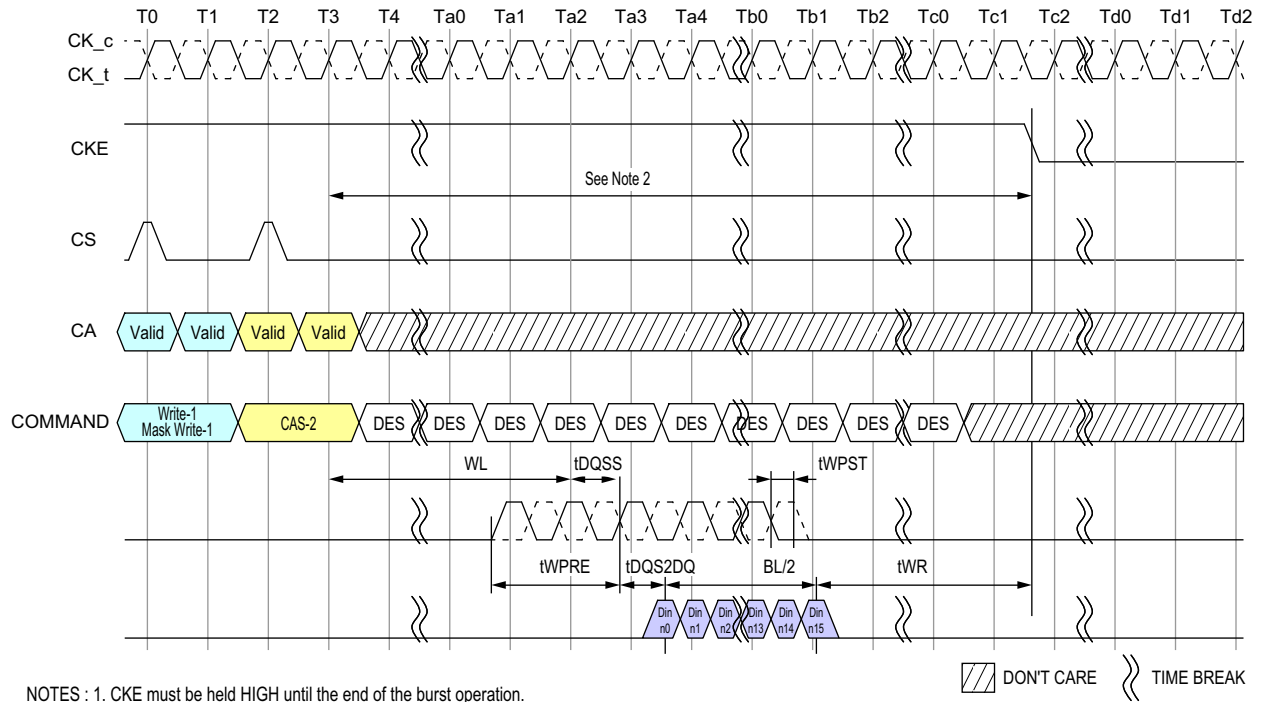
1. Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of  $RU(t_{CKCKEH}/t_{CKE})$  of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

**Figure - Read and Read with Auto-precharge to Power-Down Entry**



1. CKE must be held HIGH until the end of the burst operation.
2. Minimum Delay time from Read Command or Read with Auto Precharge Command to falling edge of CKE signal is as follows.
  - Read Post-amble = 0.5nCK : MR1 OP[7]=[0] :  $(RL \times t_{CK}) + t_{DQCK}(\text{Max}) + ((BL/2) \times t_{CK}) + 1t_{CK}$
  - Read Post-amble = 1.5nCK : MR1 OP[7]=[1] :  $(RL \times t_{CK}) + t_{DQCK}(\text{Max}) + ((BL/2) \times t_{CK}) + 2t_{CK}$

**Figure - Write and Mask Write to Power-Down Entry**



- NOTES : 1. CKE must be held HIGH until the end of the burst operation.  
2. Minimum Delay time from Write Command or Mask Write Command to falling edge of CKE signal is as follows.  
 $(WL \times t_{CK}) + t_{DQSS}(\text{Max}) + t_{DQS2DQ}(\text{Max}) + ((BL/2) \times t_{CK}) + t_{WR}$   
3. This timing is applied regardless of DQ ODT Disable/Enable setting: MR11[OP2:0].  
4. This timing diagram only applies to the Write and Mask Write Commands without Auto Precharge.

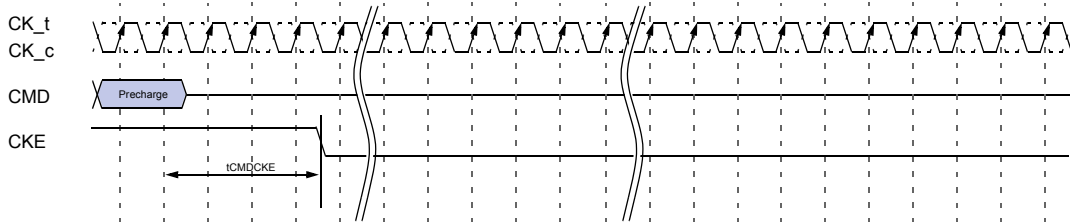


[illegible]

-  DON'T CARE       TIME BREAK

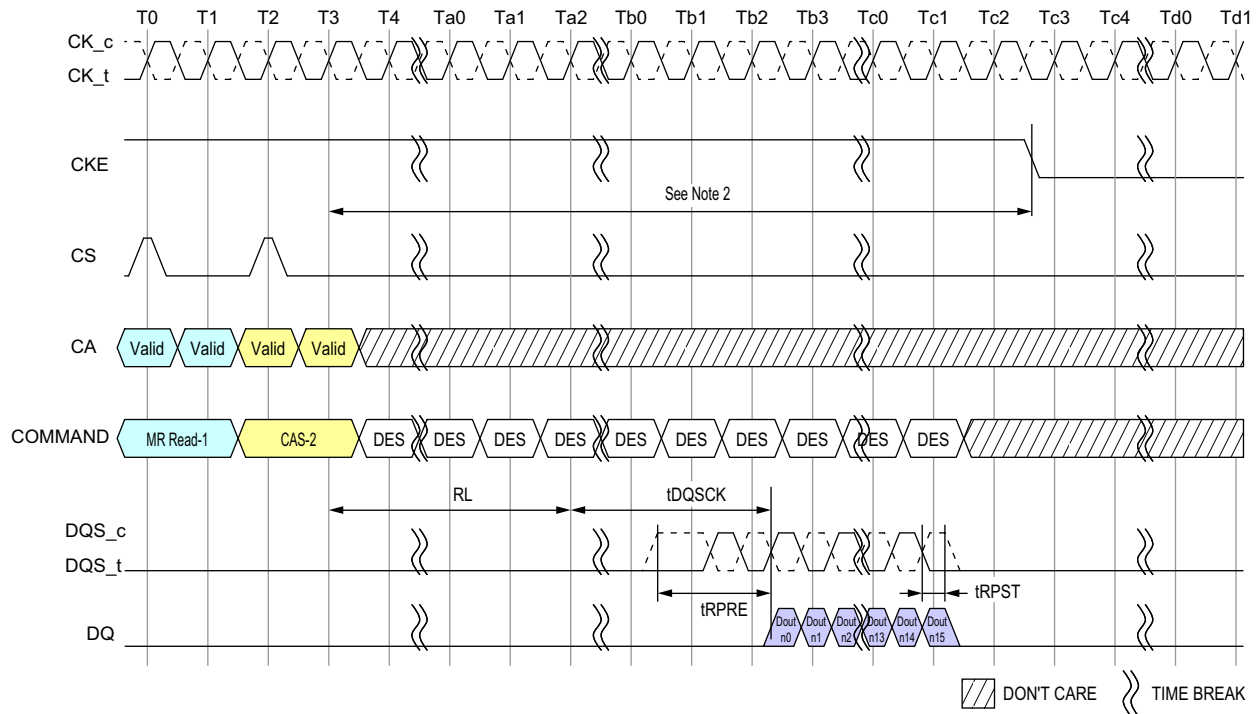
237

**Figure - Precharge Command to Power-Down Entry**



Notes: 1. CKE must be held HIGH until t<sub>CMDCKE</sub> is satisfied.

**Figure - Mode Register Read to Power-Down Entry**



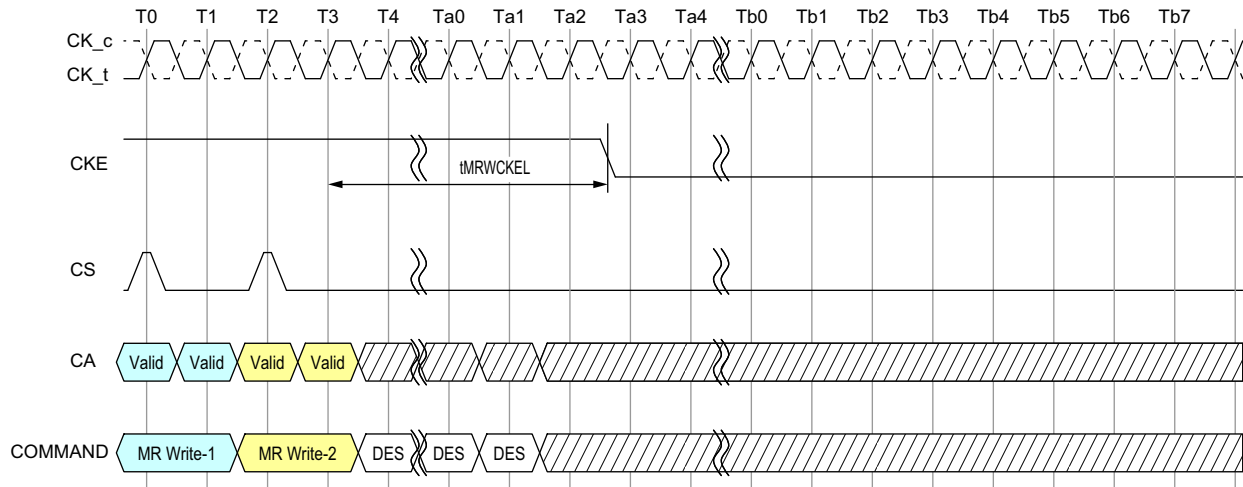
NOTES : 1. CKE must be held HIGH until the end of the burst operation.

2. Minimum Delay time from Mode Register Read Command to falling edge of CKE signal is as follows:

Read Post-amble = 0.5nCK : MR1 OP[7]=0] : (RL x tCK) + t<sub>DQSCK</sub>(Max) + ((BL/2) x tCK) + 1tCK

Read Post-amble = 1.5nCK : MR1 OP[7]=1] : (RL x tCK) + t<sub>DQSCK</sub>(Max) + ((BL/2) x tCK) + 2tCK

**Figure - MRW to Power-Down Entry**



NOTES : 1. CKE must be held HIGH until tMRWCKEL is satisfied.

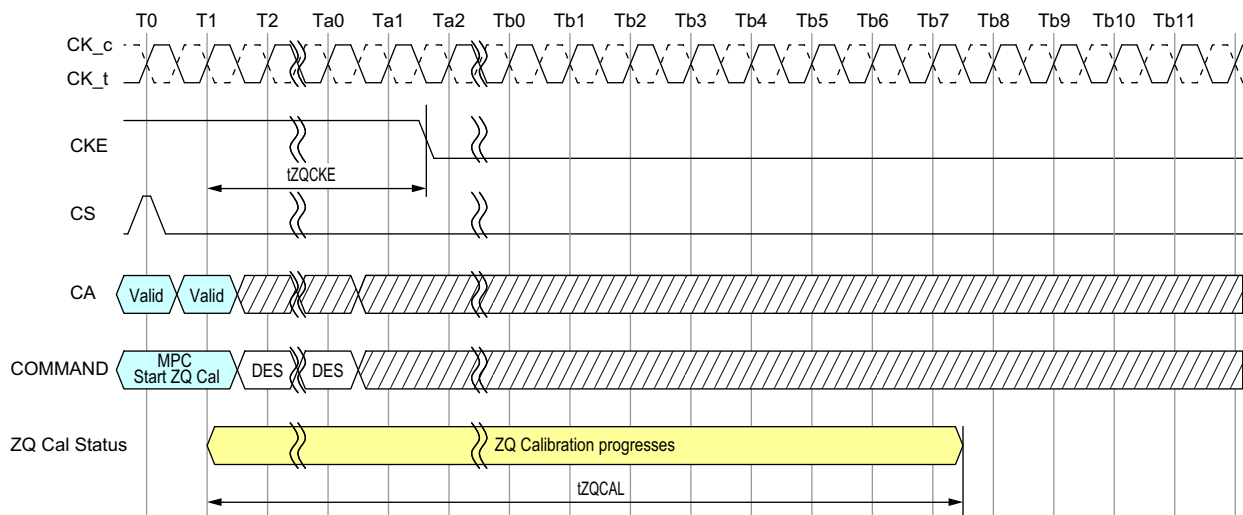
2. This timing is the general definition for Power Down Entry after Mode Register Write Command.

When a Mode Register Write Command changes a parameter or starts an operation that requires special timing longer than tMRWCKEL, that timing must be satisfied before CKE is driven low.

Changing the Vref(DQ) value is one example, in this case the appropriate Vref\_time-Short/Middle/Long must be satisfied.

▨ DON'T CARE    ≡≡ TIME BREAK

**Figure - MPC ZQCAL\_start to Power-Down Entry**



NOTES : 1. ZQ Calibration continues if CKE goes low after tZQCKE is satisfied.

▨ DON'T CARE    ≡≡ TIME BREAK

## 2.40. Input clock stop and frequency change

LPDDR4 SDRAMs support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(ABS)min}$  is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions ( $t_{RCD}$ ,  $t_{RP}$ ) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 4 clock cycles after CKE goes LOW;
- The clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR4 devices support clock stop during CKE LOW under the following conditions:

- CK\_t is held LOW and CK\_c is held HIGH or both are floated during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions ( $t_{RCD}$ ,  $t_{RP}$ ) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 4 clock cycles after CKE goes LOW;
- The clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR4 devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK(ABS)min}$  is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions ( $t_{RCD}$ ,  $t_{WR}$ ,  $t_{WRA}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ , etc.) have been met prior to changing the frequency;
- CS shall be held LOW during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR4 SDRAM is ready for normal operation after the clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2 \cdot t_{CK} + t_{XP}$ .

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR4 devices support clock stop during CKE HIGH under the following conditions:

- CK\_t is held LOW and CK\_c is held HIGH during clock stop;
- CS shall be held LOW during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions ( $t_{RCD}$ ,  $t_{WR}$ ,  $t_{WRA}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ , etc.) have been met prior to stopping the clock;
- The LPDDR4 SDRAM is ready for normal operation after the clock is restarted and satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2 \cdot t_{CK} + t_{XP}$ .

## 2.41. Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

### 2.41.1. Command Truth Table

| Command                                            | SDR Command Pins | SDR CA Pins (10) |     |     |     |     |     | CK t edge | Notes       |
|----------------------------------------------------|------------------|------------------|-----|-----|-----|-----|-----|-----------|-------------|
|                                                    | CS               | CA0              | CA1 | CA2 | CA3 | CA4 | CA5 |           |             |
| Deselect (DES)                                     | L                | X                |     |     |     |     |     | R1        | 1,2         |
| Multi Purpose Command (MPC)                        | H                | L                | L   | L   | L   | L   | OP6 | R1        | 1,2,9       |
|                                                    | L                | OP0              | OP1 | OP2 | OP3 | OP4 | OP5 | R2        |             |
| Precharge (Per Bank, All Bank)                     | H                | L                | L   | L   | L   | H   | AB  | R1        | 1,2,3,4     |
|                                                    | L                | BA0              | BA1 | BA2 | V   | V   | V   | R2        |             |
| Refresh (Per Bank, All Bank)                       | H                | L                | L   | L   | H   | L   | AB  | R1        | 1,2,3,4     |
|                                                    | L                | BA0              | BA1 | BA2 | V   | V   | V   | R2        |             |
| Self Refresh Entry                                 | H                | L                | L   | L   | H   | H   | V   | R1        | 1,2         |
|                                                    | L                | V                |     |     |     |     |     | R2        |             |
| Write-1                                            | H                | L                | L   | H   | L   | L   | BL  | R1        | 1,2,3,6,7,9 |
|                                                    | L                | BA0              | BA1 | BA2 | V   | C9  | AP  | R2        |             |
| Self Refresh Exit                                  | H                | L                | L   | H   | L   | H   | V   | R1        | 1,2         |
|                                                    | L                | V                |     |     |     |     |     | R2        |             |
| Mask Write-1                                       | H                | L                | L   | H   | H   | L   | L   | R1        | 1,2,3,5,6,9 |
|                                                    | L                | BA0              | BA1 | BA2 | V   | C9  | AP  | R2        |             |
| RFU                                                | H                | L                | L   | H   | H   | H   | V   | R1        | 1,2         |
|                                                    | L                | V                |     |     |     |     |     | R2        |             |
| Read-1                                             | H                | L                | H   | L   | L   | L   | BL  | R1        | 1,2,3,6,7,9 |
|                                                    | L                | BA0              | BA1 | BA2 | V   | C9  | AP  | R2        |             |
| CAS-2 (Write-2 or Mask Write-2 or Read-2 or MRR-2) | H                | L                | H   | L   | L   | H   | C8  | R1        | 1,8,9       |
|                                                    | L                | C2               | C3  | C4  | C5  | C6  | C7  | R2        |             |
| RFU                                                | H                | L                | H   | L   | H   | L   | V   | R1        | 1,2         |
|                                                    | L                | V                |     |     |     |     |     | R2        |             |
| RFU                                                | H                | L                | H   | L   | H   | H   | V   | R1        | 1,2         |
|                                                    | L                | V                |     |     |     |     |     | R2        |             |
| MRW-1                                              | H                | L                | H   | H   | L   | L   | OP7 | R1        | 1,2,11      |
|                                                    | L                | MA0              | MA1 | MA2 | MA3 | MA4 | MA5 | R2        |             |
| MRW-2                                              | H                | L                | H   | H   | L   | H   | OP6 | R1        | 1,2,11      |
|                                                    | L                | OP0              | OP1 | OP2 | OP3 | OP4 | OP5 | R2        |             |
| MRR-1                                              | H                | L                | H   | H   | H   | L   | V   | R1        | 1,2,12      |
|                                                    | L                | MA0              | MA1 | MA2 | MA3 | MA4 | MA5 | R2        |             |
| RFU                                                | H                | L                | H   | H   | H   | H   | V   | R1        | 1,2         |
|                                                    | L                | V                |     |     |     |     |     | R2        |             |
| Activate-1                                         | H                | H                | L   | R12 | R13 | R14 | R15 | R1        | 1,2,3,10    |
|                                                    | L                | BA0              | BA1 | BA2 | V   | R10 | R11 | R2        |             |
| Activate-2                                         | H                | H                | H   | R6  | R7  | R8  | R9  | R1        | 1,10        |
|                                                    | L                | R0               | R1  | R2  | R3  | R4  | R5  | R2        |             |

#### Notes

1. All LPDDR4 commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge

- of clock. Deselect command is 1 clock cycle long.
2. "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CS, CK\_t, CK\_c and CA[5:0] can be floated.
  3. Bank addresses BA[2:0] determine which bank is to be operated upon.
  4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
  5. Mask Write-1 command supports only BL 16. For Mask Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
  6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an auto-precharge will occur to the bank associated with the Write, Mask Write or Read command.
  7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
  8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
  9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
  10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
  11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
  12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

## 2.42. Post Package Repair - PPR

LPDDR4 supports Fail Row address repair as an optional feature and it is readable through MR25 OP[7:0]. PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With PPR, LPDDR4 can correct 1Row per Bank.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the PPR mode entry and repair.

### 2.42.1. Fail Row Address Repair

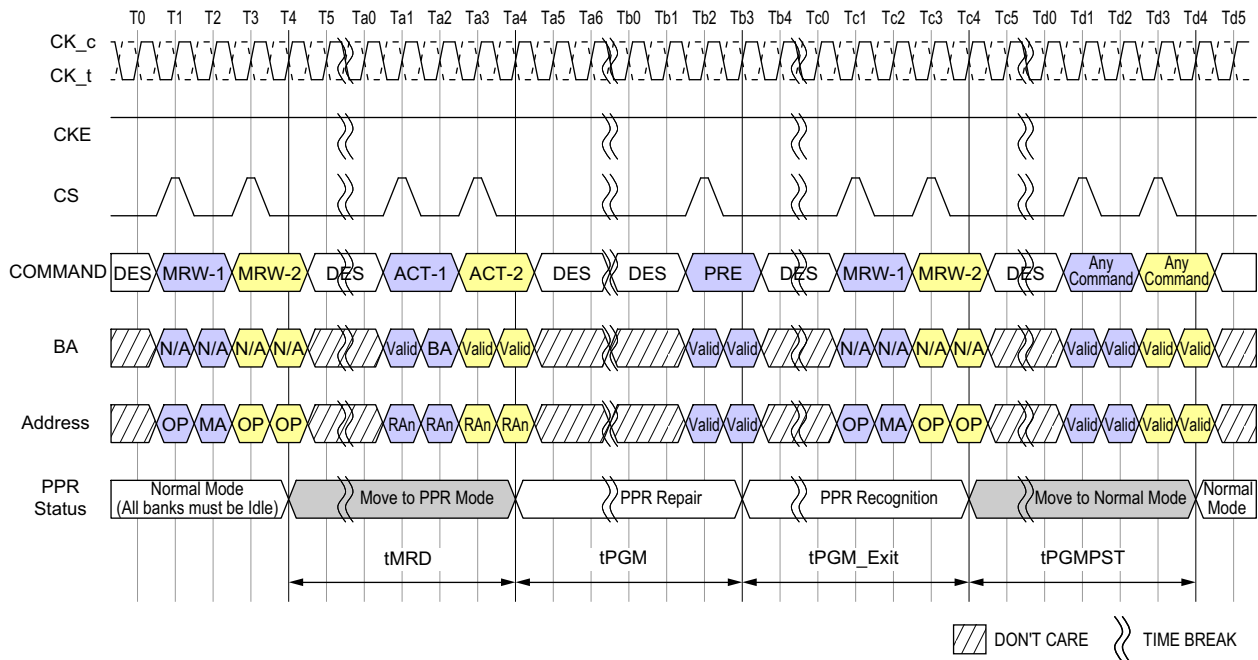
The following is procedure of PPR.

1. Before entering 'PPR' mode, All banks must be Precharged
2. Enable PPR using MR4 bit "OP4=1" and wait tMRD
3. Issue ACT command with Fail Row address
4. Wait tPGM to allow DRAM repair target Row Address internally and issue PRE
5. Wait tPGM\_Exit after PRE which allow DRAM to recognize repaired Row address
6. Exit PPR with setting MR4 bit "OP4=0"
7. LPDDR4 will accept any valid command after tPGMPST
8. In More than one fail address repair case, Repeat Step 2 to 7

Once PPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after PPR exit with MR4 [OP4=0] and tPGMPST.

The following Timing diagram show PPR related MR bits and its operation.

**Figure - PPR Timing**



### 3. Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Parameter                            | Symbol    | Min  | Max | Unit | Notes |
|--------------------------------------|-----------|------|-----|------|-------|
| VDD1 supply voltage relative to VSS  | VDD1      | -0.4 | 2.1 | V    | 1     |
| VDD2 supply voltage relative to VSS  | VDD2      | -0.4 | 1.5 | V    | 1     |
| VDDQ supply voltage relative to VSSQ | VDDQ      | -0.4 | 1.5 | V    | 1     |
| Voltage on Any Pin relative to VSS   | VIN, VOUT | -0.4 | 1.5 | V    |       |
| Storage Temperature                  | TSTG      | -55  | 125 | °C   | 2     |

Notes:

1. See the section "Power-up, Initialization, and Power-off" for information about relationships between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, please refer to JESD51-2 standard.



## 4. AC and DC Operating Conditions

### 4.1. Recommended DC Operating Conditions

| Parameter               | Symbol | Min  | Typ  | Max  | Unit | Notes |
|-------------------------|--------|------|------|------|------|-------|
| Core Power 1            | VDD1   | 1.70 | 1.80 | 1.95 | V    | 1,2   |
| Core Power 2 & CA Power | VDD2   | 1.06 | 1.10 | 1.17 | V    | 1,2,3 |
| I/O Buffer Power        | VDDQ   | 0.57 | 0.60 | 0.65 | V    | 2,3   |

- VDD1 uses significantly less current than VDD2.
- The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
- The voltage noise tolerance from DC to 20MHz exceeding a pk-pk tolerance of 45mV at the DRAM ball is not included in the TdIVW.

### 4.2. Input Leakage Current

| Parameter             | Symbol | Min | Max | Unit | Notes |
|-----------------------|--------|-----|-----|------|-------|
| Input Leakage current | $I_L$  | -4  | 4   | uA   | 1,2   |

Notes:

- For CK\_t, CK\_c, CKE, CS, CA, ODT\_CA and RESET\_n. Any input  $0V \leq V_{IN} \leq VDD2$  (All other pins not under test = 0V).
- CA ODT is disabled for CK\_t, CK\_c, CS, and CA.

### 4.3. Input/Output Leakage Current

| Parameter                    | Symbol   | Min | Max | Unit | Notes |
|------------------------------|----------|-----|-----|------|-------|
| Input/Output Leakage current | $I_{OZ}$ | -5  | 5   | uA   | 1,2   |

Notes:

- For DQ, DQS\_t, DQS\_c and DMI. Any I/O  $0V \leq V_{OUT} \leq VDDQ$ .
- I/Os status are disabled: High Impedance and ODT Off.

### 4.4. Operating Temperature

| Parameter             | Symbol   | Min        | Max | Unit | Note |
|-----------------------|----------|------------|-----|------|------|
| Operating Temperature | Standard | $T_{OPER}$ | -25 | °C   | 1    |
|                       | Extended |            | 85  |      | 1    |

- Operating Temperature is the case surface temperature on the center-top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2 standard.
- Some applications require operation of LPDDR4 in the maximum temperature conditions in the Elevated Temperature Range between 85°C and 105°C case temperature. For LPDDR4 devices, derating may be necessary to operate in this range. See MR4 on the section "Mode Register".
- Either the device case temperature rating or the temperature sensor (See the section of "Temperature Sensor") may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

## 5. AC and DC Input Measurement Levels

### 5.1. 1.1V High speed LVCMOS (HS\_LLVC MOS)

#### 5.1.1. Standard specifications

All voltages are referenced to ground except where noted.

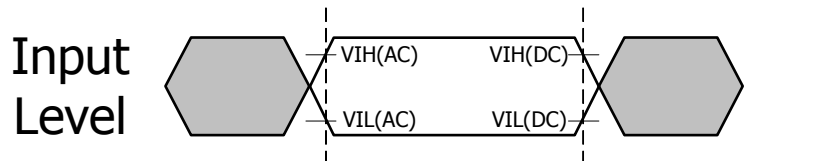
**Table - LPDDR4 Input level for CKE**

| Parameter             | Symbol  | Min               | Max               | Unit | Notes |
|-----------------------|---------|-------------------|-------------------|------|-------|
| Input high level (AC) | VIH(AC) | $0.75 \cdot VDD2$ | $VDD2 + 0.2$      | V    | 1     |
| Input low level (AC)  | VIL(AC) | -0.2              | $0.25 \cdot VDD2$ | V    | 1     |
| Input high level (DC) | VIH(DC) | $0.65 \cdot VDD2$ | $VDD2 + 0.2$      | V    |       |
| Input low level (DC)  | VIL(DC) | -0.2              | $0.35 \cdot VDD2$ | V    |       |

Notes:

1. Refer to LPDDR4 AC Over/Undershoot section.

**Figure - Input AC timing definition for CKE**



Note:

1. AC level is guaranteed transition point
2. DC level is hysteresis

 Don't Care

#### 5.1.2. LPDDR4 Input Level for Reset\_n and ODT\_CA

This definition applies to Reset\_n and ODT\_CA.

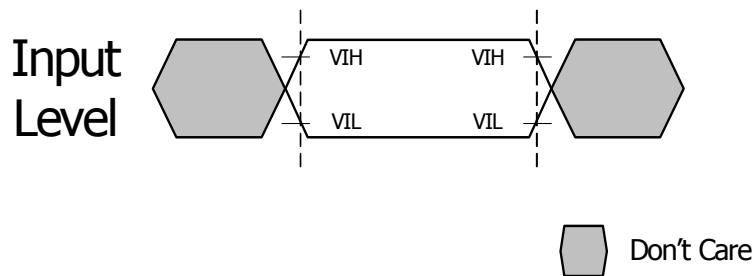
**Table - LPDDR4 Input level for Reset\_n and ODT\_CA**

| Parameter        | Symbol | Min              | Max               | Unit | Notes |
|------------------|--------|------------------|-------------------|------|-------|
| Input high level | VIH    | $0.8 \cdot VDD2$ | $VDD2 + 0.2$      | V    | 1     |
| Input low level  | VIL    | -0.2             | $0.20 \cdot VDD2$ | V    | 1     |

Notes:

1. Refer to LPDDR4 AC Over/Undershoot section.

**Figure - Input AC timing definition**



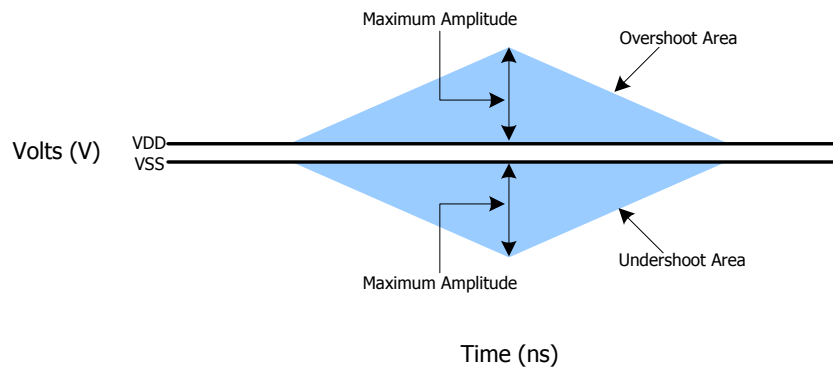
### 5.1.3. AC Over/Undershoot

#### 5.1.3.1. LPDDR4 AC Over/Undershoot

**Table - LPDDR4 AC Over/Undershoot**

| Parameter                                          | Specification | Units |
|----------------------------------------------------|---------------|-------|
| Maximum peak amplitude allowed for overshoot area  | 0.3           | V     |
| Maximum peak amplitude allowed for undershoot area | 0.3           | V     |
| Maximum overshoot area above VDD/VDDQ              | 0.8           | V-ns  |
| Maximum undershoot area below VSS/VSSQ             | 0.8           | V-ns  |

**Figure - AC Overshoot and Undershoot Definition for Address and Control Pins**

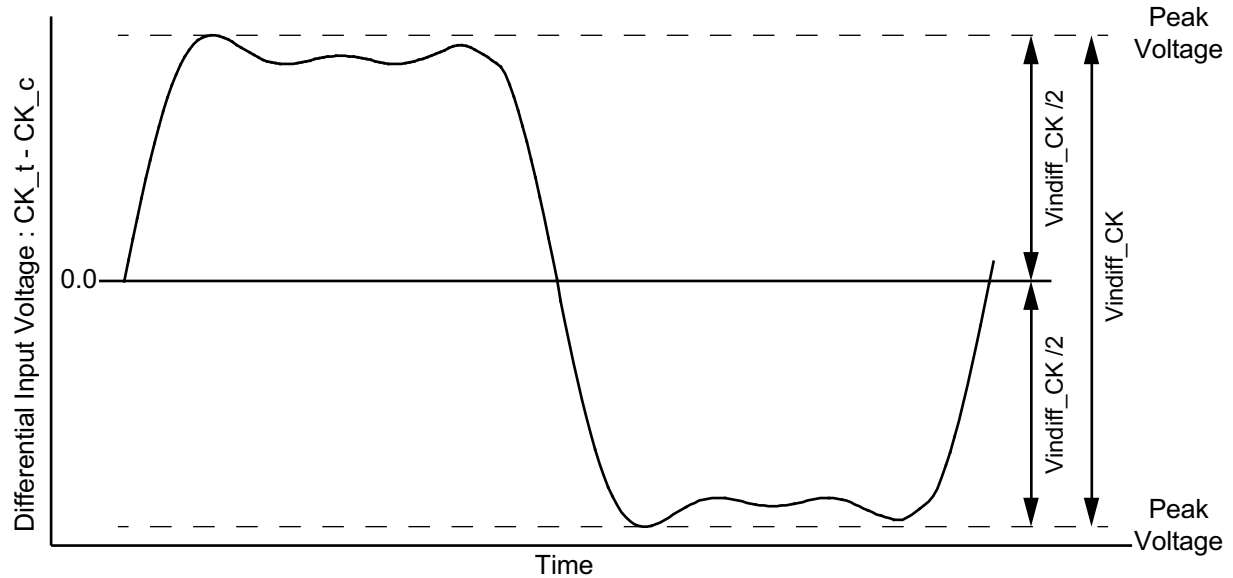


## 5.2. Differential Input Voltage

### 5.2.1. Differential Input Voltage for CK

The minimum input voltage need to satisfy both  $V_{\text{indiff\_CK}}$  and  $V_{\text{indiff\_CK}}/2$  specification at input receiver and their measurement period is  $1t_{\text{CK}}$ .  $V_{\text{indiff\_CK}}$  is the peak to peak voltage centered on 0 volts differential and  $V_{\text{indiff\_CK}}/2$  is max and min peak voltage from 0V.

**Figure - CK Differential Input Voltage**



**Table - CK differential input voltage**

| Parameter                     | Symbol     | Data Rate              |     |                |     |      |     | Unit | Notes |
|-------------------------------|------------|------------------------|-----|----------------|-----|------|-----|------|-------|
|                               |            | 1600/1867 <sup>a</sup> |     | 2133/2400/3200 |     | 4266 |     |      |       |
|                               |            | Min                    | Max | Min            | Max | Min  | Max |      |       |
| CK differential input voltage | Vindiff_CK | 420                    | -   | 380            | -   | 360  | -   | mV   | 1     |

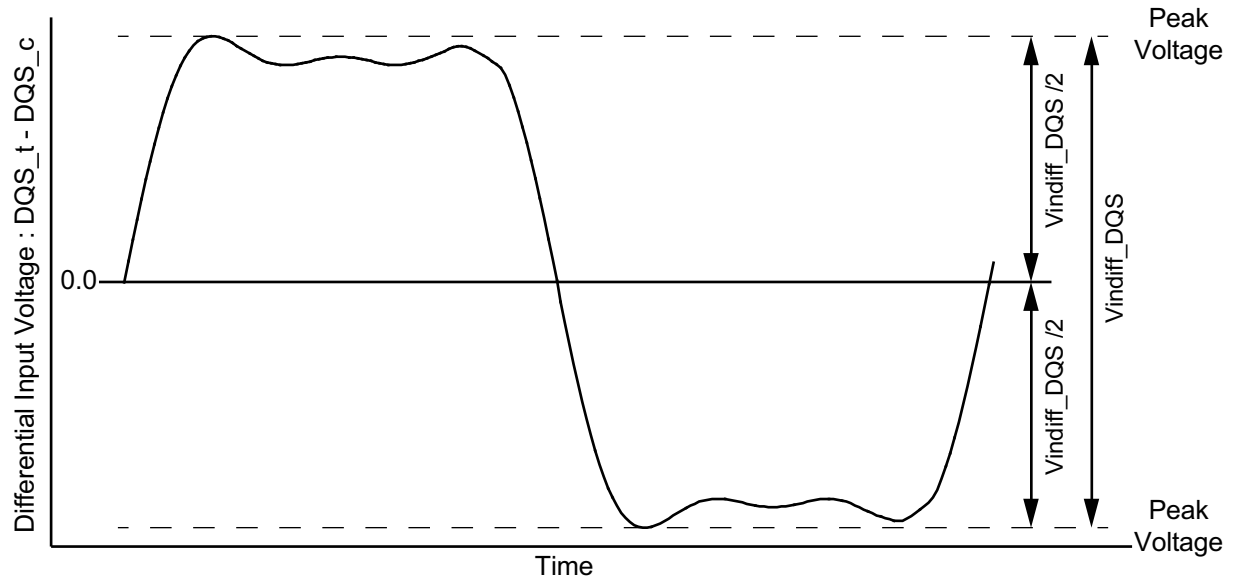
Notes:

1. The peak voltage of Differential CK signals is calculated in a following equation.  
 $V_{\text{indiff\_CK}} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$   
 $\text{Max Peak Voltage} = \text{Max}(f(t))$   
 $\text{Min Peak Voltage} = \text{Min}(f(t))$   
 $f(t) = V_{\text{CK\_t}} - V_{\text{CK\_c}}$
- a. The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1867.

### 5.2.2. Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff\_DQS and Vindiff\_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff\_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff\_DQS /2 is max and min peak voltage from 0V.

**Figure - DQS Differential Input Voltage**



**Table - CK differential input voltage**

| Parameter              | Symbol      | Data Rate              |     |                |     |      |     | Unit | Notes |
|------------------------|-------------|------------------------|-----|----------------|-----|------|-----|------|-------|
|                        |             | 1600/1867 <sup>a</sup> |     | 2133/2400/3200 |     | 4266 |     |      |       |
|                        |             | Min                    | Max | Min            | Max | Min  | Max |      |       |
| DQS differential input | Vindiff_DQS | 360                    | -   | 360            | -   | 340  | -   | mV   | 1     |

Notes:

1. The peak voltage of Differential CK signals is calculated in a following equation.  

$$\text{Vindiff\_DQS} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

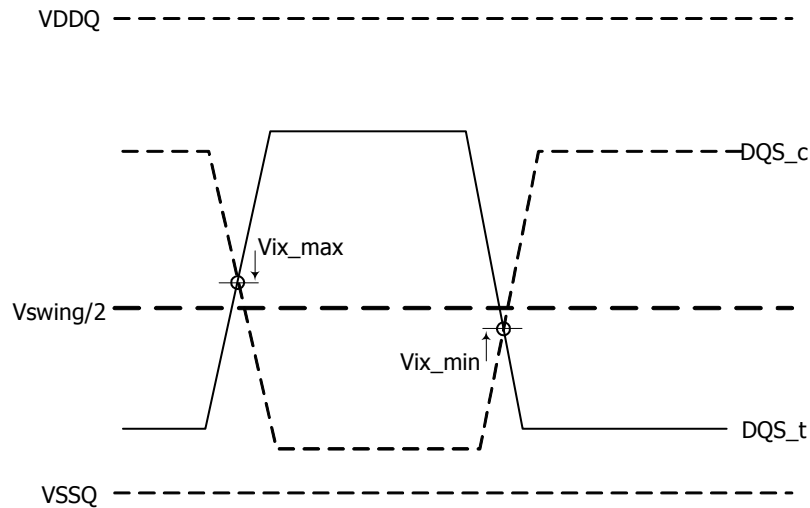
$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = \text{VDQS\_t} - \text{VDQS\_c}$$
- a. The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1867.

### 5.2.3. Differential Input Cross Point Voltage

**Figure - DQS input crosspoint voltage (Vix)**



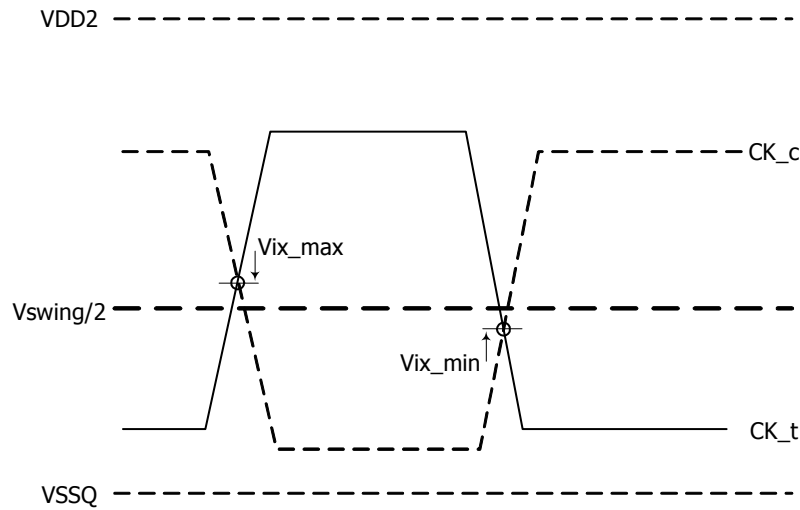
**Table - DQS input voltage crosspoint (Vix) ratio**

| Parameter                                       | Symbol        | min/max | LPDDR4<br>2133 | LPDDR4<br>3200 | LPDDR4<br>4200 | Units | Notes |
|-------------------------------------------------|---------------|---------|----------------|----------------|----------------|-------|-------|
| DQS Differential input crosspoint voltage ratio | Vix_DQS_ratio | max     | 20             | 20             | 20             | %     | 1,2   |

Notes:

1. The Vix voltage is referenced to  $V_{swing}/2(avg) = 0.5(V_{DQS\_t} + V_{DQS\_c})$  where the average is over tbd UI.
2. The ratio of the Vix pk voltage divided by  $V_{diff\_DQS}$  :  $Vix\_DQS\_Ratio = 100 * (Vix\_DQS / V_{diff\_DQS} \text{ pk-pk})$  where  $V_{diff\_DQS} \text{ pk-pk} = 2 * |V_{DQS\_t} - V_{DQS\_c}|$

**Figure - CK input crosspoint voltage (Vix)**



**Table - CK input voltage crosspoint (Vix) ratio**

| Parameter                                      | Symbol       | min/max | LPDDR4<br>2133 | LPDDR4<br>3200 | LPDDR4<br>4200 | Units | Notes |
|------------------------------------------------|--------------|---------|----------------|----------------|----------------|-------|-------|
| CK Differential input crosspoint voltage ratio | Vix_CK_ratio | max     | 25             | 25             | 25             | %     | 1,2   |

Notes:

1. The Vix voltage is referenced to  $V_{swing}/2(avg) = 0.5(V_{CK\_t} + V_{CK\_c})$  where the average is over tbd UI.
2. The ratio of the Vix pk voltage divided by Vdiff\_CK :  $Vix\_CK\_Ratio = 100 * (Vix\_CK / V_{diff\_CK\_pk-pk})$  where  $V_{diff\_CK\_pk-pk} = 2 * |V_{CK\_t} - V_{CK\_c}|$

### 5.3. AC and DC Logic Input Levels for ODT input

**Table - LPDDR4 Input level**

| Parameter             | Symbol  | Min                  | Max                  | Unit | Notes |
|-----------------------|---------|----------------------|----------------------|------|-------|
| Input high level (AC) | VIH(AC) | $0.75 \cdot V_{DD2}$ | $V_{DD2} + 0.2$      | V    | 1     |
| Input low level (AC)  | VIL(AC) | -0.2                 | $0.25 \cdot V_{DD2}$ | V    | 1     |
| Input high level (DC) | VIH(DC) | $0.65 \cdot V_{DD2}$ | $V_{DD2} + 0.2$      | V    |       |
| Input low level (DC)  | VIL(DC) | -0.2                 | $0.35 \cdot V_{DD2}$ | V    |       |

Notes:

1. Refer to LPDDR4 AC Over/Undershoot section.



## 5.4. Single Ended Output Slew Rate

Figure - Single Ended Output Slew Rate Definition

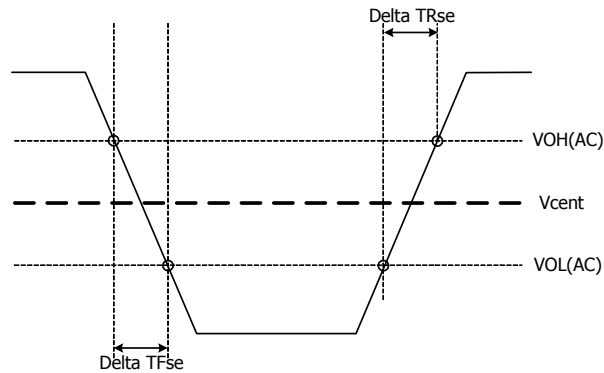
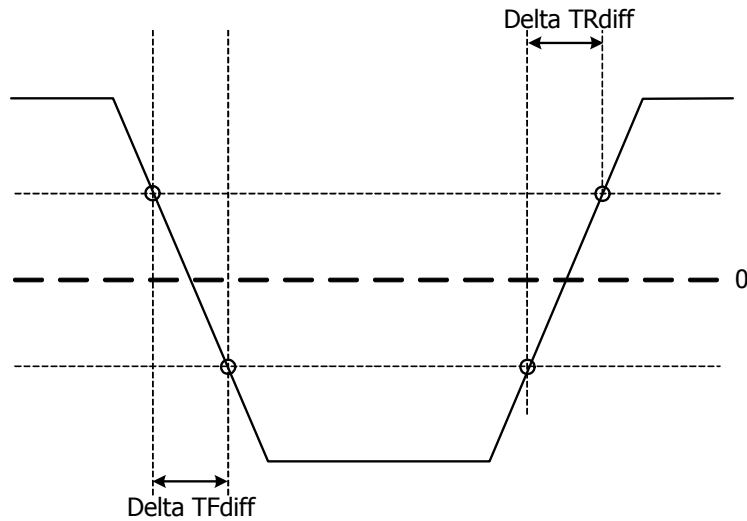


Table - Output Slew Rate (Single-ended)

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Symbol | Value        |              | Units |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------|--------------|-------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |        | Min (Note 1) | Max (Note 2) |       |
| Single-ended Output Slew Rate ( $VOH = VDDQ \cdot 0.5$ )                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | SRQse  | 3.0          | 9.0          | V/ns  |
| Output slew-rate matching ratio (Rise to Fall)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        | 0.8          | 1.2          |       |
| Description: SR: Slew Rate<br>Q: Query Output (like in DQ, which stands for Data-in, Query-Output)<br>se: Single-ended Signals<br><br>Notes:<br>1 Measured with output reference load.<br>2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.<br>3 The output slew rate for falling and rising edges is defined and measured between $VOL(AC) = 0.2 \cdot VOH(DC)$ and $VOH(AC) = 0.8 \cdot VOH(DC)$ .<br>4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching. |        |              |              |       |

## 5.5. Differential Output Slew Rate

**Figure - Differential Output Slew Rate Definition**



**Table - Differential Output Slew Rate**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Symbol  | Value        |              | Units |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------|--------------|-------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | Min (Note 1) | Max (Note 2) |       |
| Single-ended Output Slew Rate ( $V_{OH} = V_{DDQ} \cdot 0.5$ )                                                                                                                                                                                                                                                                                                                                                                                                           | SRQdiff | 6            | 18           | V/ns  |
| Description: SR: Slew Rate<br>Q: Query Output (like in DQ, which stands for Data-in, Query-Output)<br>diff: Differential Signals<br><br>Notes:<br>1 Measured with output reference load.<br>2 The output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC) = 0.2 \cdot V_{OH}(DC)$ and $V_{OH}(AC) = 0.8 \cdot V_{OH}(DC)$ .<br>3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching. |         |              |              |       |

## 5.6. Overshoot and Undershoot Specification for LVSTL

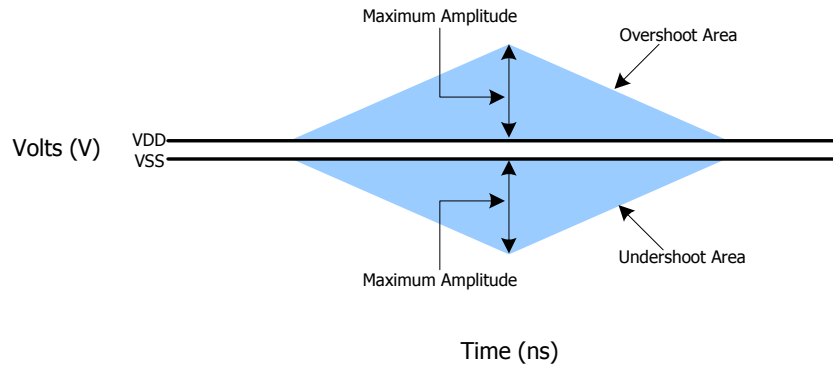
**Table - AC Overshoot / Undershoot Specification**

| Parameter                                          | 1600 to 3200 | 4266 | Units |
|----------------------------------------------------|--------------|------|-------|
| Maximum peak amplitude allowed for overshoot area  | 0.3V         | TBD  | V     |
| Maximum peak amplitude allowed for undershoot area | 0.3V         | TBD  | V     |
| Maximum overshoot area above VDD/VDDQ              | 0.1V-ns      | TBD  | V-ns  |
| Maximum undershoot area below VSS/VSSQ             | 0.1V-ns      | TBD  | V-ns  |

Notes:

1. VDD stands for VDD2 for CA[5:0], CK\_t, CK\_c, CS\_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS\_t and DQS\_c.
2. VSS stands for VSS for CA[5:0], CK\_t, CK\_c, CS\_n, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS\_t and DQS\_c.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

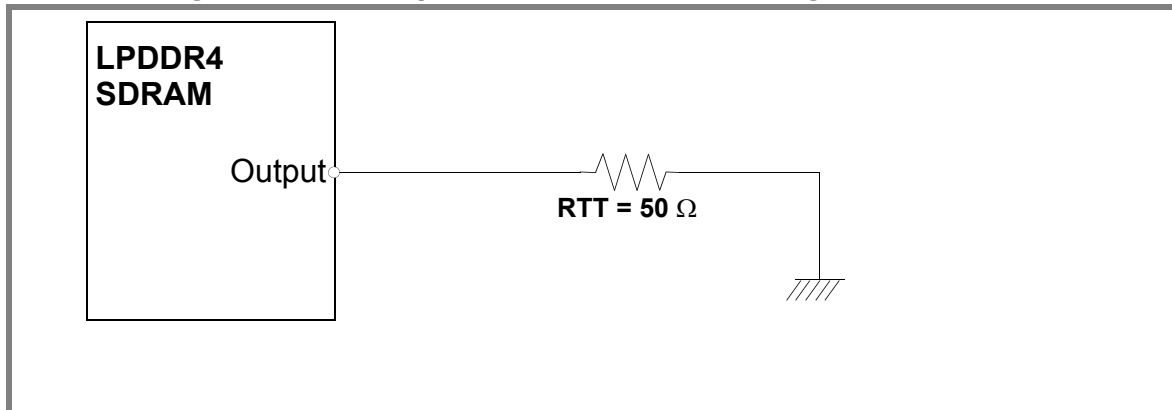
**Figure - AC Overshoot and Undershoot Definition**



### 5.7. LVSTL Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

**Figure - Driver Output Reference Load for Timing and Slew Rate**

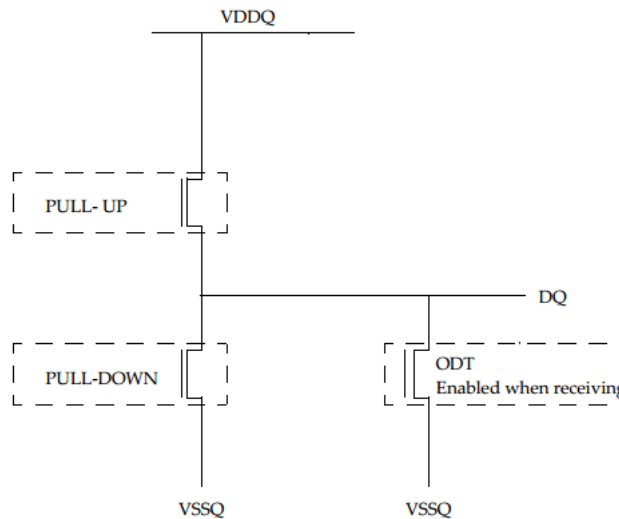


Note: 1. All output timing parameter values (like  $t_{DQSCk}$ ,  $t_{DQSQ}$ ,  $t_{QHS}$ ,  $t_{HZ}$ ,  $t_{RPRE}$  etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

### 5.8. LVSTL (Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in figure below.

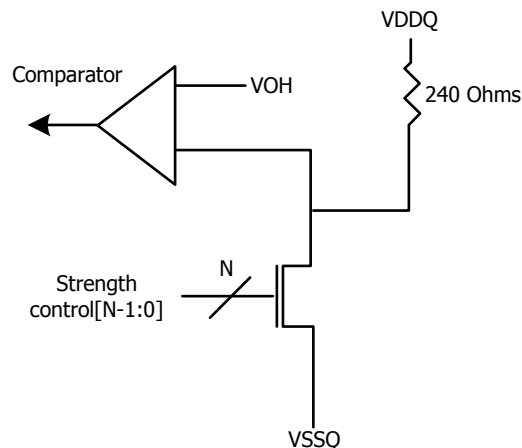
**Figure - LVSTL I/O Cell**



To ensure that the target impedance is achieved the LVSTL I/O cell is designed to be calibrated as following procedure.

- 1) First calibrate the pull-down device against a 240 Ohm resistor to VDDQ via the ZQ pin.
  - Set Strength Control to minimum setting
  - Increase drive strength until comparator detects data bit is less than VOH.
  - NMOS pull-down device is calibrated to 240 Ohms

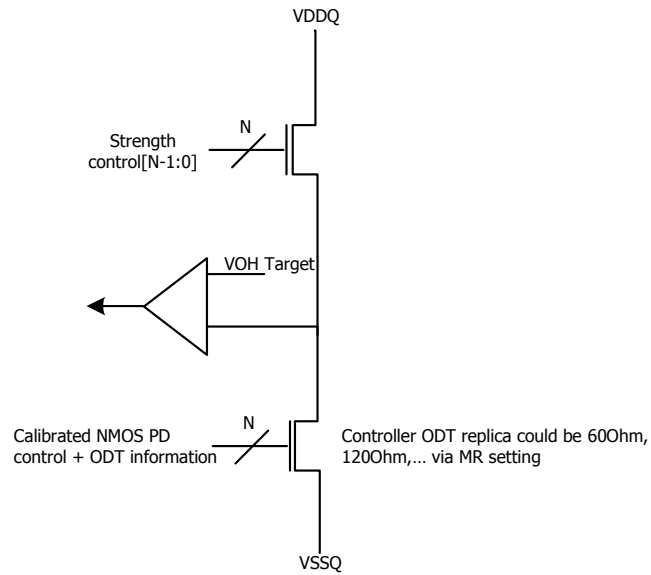
**Figure - Pull-down calibration**



- 2) Then calibrate the pull-up device against the calibrated pull-down device.
  - Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS)

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is greater than VOH target
- NMOS pull-up device is now calibrated to VOH target

**Figure - Pull-up calibration**



## 6. Input/Output Capacitance

**Table - Input/Output Capacitance**

| Parameter                                          | Symbol | Min/Max | 3733-533 | Unit | Note  |
|----------------------------------------------------|--------|---------|----------|------|-------|
| Input capacitance, CK_t and CK_c                   | CCK    | Min     | 0.5      | pF   | 1,2   |
|                                                    |        | Max     | 0.9      |      |       |
| Input capacitance delta, CK_t and CK_c             | CDCK   | Min     | 0.0      | pF   | 1,2,3 |
|                                                    |        | Max     | 0.09     |      |       |
| Input capacitance, all other input-only pins       | CI     | Min     | 0.5      | pF   | 1,2,4 |
|                                                    |        | Max     | 0.9      |      |       |
| Input capacitance delta, all other input-only pins | CDI    | Min     | -0.1     | pF   | 1,2,5 |
|                                                    |        | Max     | 0.1      |      |       |
| Input/output capacitance, DQ, DMI, DQS_t, DQS_c    | CIO    | Min     | 0.7      | pF   | 1,2,6 |
|                                                    |        | Max     | 1.3      |      |       |
| Input/output capacitance delta, DQS_t and DQS_c    | CDDQS  | Min     | 0.0      | pF   | 1,2,7 |
|                                                    |        | Max     | 0.1      |      |       |
| Input/output capacitance delta, DQ and DM          | CDIO   | Min     | -0.1     | pF   | 1,2,8 |
|                                                    |        | Max     | 0.1      |      |       |
| Input/Output Capacitance ZQ                        | CZQ    | Min     | 0.0      | pF   | 1,2   |
|                                                    |        | Max     | 5.0      |      |       |

**Notes**

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating).
3. Absolute value of CCK\_t . CCK\_c.
4. CI applies to CS\_n, CKE, CA0~CA5.
5.  $CDI = CI \cdot 0.5 \cdot (CCK\_t + CCK\_c)$
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS\_t and CDQS\_c.
8.  $CDIO = CIO \cdot 0.5 \cdot (CDQS\_t + CDQS\_c)$  in byte-lane.

## 7. IDD Specification Parameters and Test Conditions

### 7.1. IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW:  $V_{IN} \leq V_{IL(DC) \text{ MAX}}$

HIGH:  $V_{IN} \geq V_{IH(DC) \text{ MIN}}$

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See following tables for switching definition of signals.

**Table - Definition of switching for CA input signals**

| Switching for CA |      |      |      |      |      |      |      |      |
|------------------|------|------|------|------|------|------|------|------|
| CK_t edge        | R1   | R2   | R3   | R4   | R5   | R6   | R7   | R8   |
| CKE              | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH |
| CS               | LOW  | LOW  | LOW  | LOW  | LOW  | LOW  | LOW  | LOW  |
| CA0              | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH | HIGH | HIGH |
| CA1              | HIGH | HIGH | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH |
| CA2              | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH | HIGH | HIGH |
| CA3              | HIGH | HIGH | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH |
| CA4              | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH | HIGH | HIGH |
| CA5              | HIGH | HIGH | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH |

Notes:

1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

**Table - CA pattern for IDD4R**

| Clock Cycle Number | CKE  | CS   | Command  | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|----------|-----|-----|-----|-----|-----|-----|
| N                  | HIGH | HIGH | Read-1   | L   | H   | L   | L   | L   | L   |
| N+1                | HIGH | LOW  |          | L   | H   | L   | L   | L   | L   |
| N+2                | HIGH | HIGH | CAS-2    | L   | H   | L   | L   | H   | L   |
| N+3                | HIGH | LOW  |          | L   | L   | L   | L   | L   | L   |
| N+4                | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+5                | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+6                | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+7                | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+8                | HIGH | HIGH | Read-1   | L   | H   | L   | L   | L   | L   |
| N+9                | HIGH | LOW  |          | L   | H   | L   | L   | H   | L   |
| N+10               | HIGH | HIGH | CAS-2    | L   | H   | L   | L   | H   | H   |
| N+11               | HIGH | LOW  |          | H   | H   | H   | H   | H   | H   |
| N+12               | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+13               | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+14               | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+15               | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |

Notes:

1. BA[2:0] = 010, CA[9:4] = 000000 or 111111, Burst Order CA[3:2] = 00 or 11 (Same as LPDDR3 IDD4R Spec)
2. Difference from LPDDR3 Spec : CA pins are kept low with DES CMD to reduce ODT current.



**Table - CA pattern for IDD4W**

| Clock Cycle Number | CKE  | CS   | Command  | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|----------|-----|-----|-----|-----|-----|-----|
| N                  | HIGH | HIGH | Write-1  | L   | L   | H   | L   | L   | L   |
| N+1                | HIGH | LOW  |          | L   | H   | L   | L   | L   | L   |
| N+2                | HIGH | HIGH | CAS-2    | L   | H   | L   | L   | H   | L   |
| N+3                | HIGH | LOW  |          | L   | L   | L   | L   | L   | L   |
| N+4                | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+5                | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+6                | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+7                | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+8                | HIGH | HIGH | Write-1  | L   | L   | H   | L   | L   | L   |
| N+9                | HIGH | LOW  |          | L   | H   | L   | L   | H   | L   |
| N+10               | HIGH | HIGH | CAS-2    | L   | H   | L   | L   | H   | H   |
| N+11               | HIGH | LOW  |          | L   | L   | H   | H   | H   | H   |
| N+12               | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+13               | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+14               | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |
| N+15               | HIGH | LOW  | Deselect | L   | L   | L   | L   | L   | L   |

Notes:

1. BA[2:0] = 010, CA[9:4] = 000000 or 111111 (Same as LPDDR3 IDD4W Spec.)
2. Difference from LPDDR3 Spec:
  - 1-No burst ordering
  - 2-CA pins are kept low with DES CMD to reduce ODT current.

**Table - Data Pattern for IDD4W (DBI off)**

| DBI OFF case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL1          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4          | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6          | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL7          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL9          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL15         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|              |       |       |       |       |       |       |       |       |     |            |
| BL16         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL17         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |

| DBI OFF case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL19         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL21         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL22         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL23         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL24         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL25         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL27         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL29         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL30         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL31         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| No. of 1's   | 16    | 16    | 16    | 16    | 16    | 16    | 16    | 16    |     |            |

Notes:

1. Simplified pattern compared with last showing.
2. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

**Table - Data Pattern for IDD4R (DBI off)**

| DBI OFF case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL1          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4          | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6          | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL7          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL9          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL15         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|              |       |       |       |       |       |       |       |       |     |            |
| BL16         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL17         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL19         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL21         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |

| DBI OFF case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL22         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL23         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL24         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL25         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL27         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL29         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL30         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL31         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| No. of 1's   | 16    | 16    | 16    | 16    | 16    | 16    | 16    | 16    |     |            |

Notes:

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

**Table - Data Pattern for IDD4W (DBI on)**

| DBI ON case |       |       |       |       |       |       |       |       |     | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|             | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL1         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL7         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL9         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL15        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL16        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL17        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL19        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL21        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL22        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL23        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL24        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL25        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |

| DBI ON case |       |       |       |       |       |       |       |       |     | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|             | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL26        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL27        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL29        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL30        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL31        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| No. of 1's  | 8     | 8     | 8     | 8     | 8     | 8     | 16    | 16    | 8   |            |

Notes:

1. Green colored cells are DBI enabled burst.

**Table - Data Pattern for IDD4R (DBI on)**

| DBI OFF case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL1          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4          | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6          | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL7          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL9          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL15         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL16         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL17         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL19         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL21         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL22         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL23         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL24         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL25         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL27         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL29         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |

| DBI OFF case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL30         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL31         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| No. of 1's   | 8     | 8     | 8     | 8     | 8     | 8     | 16    | 16    | 8   |            |

Notes:

1. Green colored cells are DBI enabled burst.

## 7.2. IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range

**Table - LPDDR4 IDD Specification Parameters and Operating Conditions**

| Parameter/Condition                                                                                                                                                                                                        | Symbol              | Power Supply | 3733  | 4266  | Units | Notes |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|--------------|-------|-------|-------|-------|
| <b>Operating one bank active-precharge current:</b><br>tCK = tCKmin; tRC = tRCmin;<br>CKE is HIGH;<br>CS is LOW between valid commands;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled     | IDD0 <sub>1</sub>   | VDD1         | 24.20 | 24.20 | mA    |       |
|                                                                                                                                                                                                                            | IDD0 <sub>2</sub>   | VDD2         | 65.00 | 65.00 | mA    |       |
|                                                                                                                                                                                                                            | IDD0 <sub>Q</sub>   | VDDQ         | 2.00  | 2.00  | mA    | 3     |
| <b>Idle power-down standby current:</b><br>tCK = tCKmin;<br>CKE is LOW;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled                                | IDD2P <sub>1</sub>  | VDD1         | 1.95  | 1.95  | mA    |       |
|                                                                                                                                                                                                                            | IDD2P <sub>2</sub>  | VDD2         | 6.75  | 6.75  | mA    |       |
|                                                                                                                                                                                                                            | IDD2P <sub>Q</sub>  | VDDQ         | 0.80  | 0.80  | mA    | 3     |
| <b>Idle power-down standby current with clock stop:</b><br>CK_t = LOW, CK_c = HIGH;<br>CKE is LOW;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled         | IDD2PS <sub>1</sub> | VDD1         | 1.95  | 1.95  | mA    |       |
|                                                                                                                                                                                                                            | IDD2PS <sub>2</sub> | VDD2         | 6.75  | 6.75  | mA    |       |
|                                                                                                                                                                                                                            | IDD2PS <sub>Q</sub> | VDDQ         | 0.80  | 0.80  | mA    | 3     |
| <b>Idle non power-down standby current:</b><br>tCK = tCKmin;<br>CKE is HIGH;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                            | IDD2N <sub>1</sub>  | VDD1         | 1.95  | 1.95  | mA    |       |
|                                                                                                                                                                                                                            | IDD2N <sub>2</sub>  | VDD2         | 35.40 | 35.40 | mA    |       |
|                                                                                                                                                                                                                            | IDD2N <sub>Q</sub>  | VDDQ         | 2.00  | 2.00  | mA    | 3     |
| <b>Idle non power-down standby current with clock stopped:</b><br>CK_t = LOW, CK_c = HIGH;<br>CKE is HIGH;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | IDD2NS <sub>1</sub> | VDD1         | 1.95  | 1.95  | mA    |       |
|                                                                                                                                                                                                                            | IDD2NS <sub>2</sub> | VDD2         | 27.20 | 27.20 | mA    |       |
|                                                                                                                                                                                                                            | IDD2NS <sub>Q</sub> | VDDQ         | 2.00  | 2.00  | mA    | 3     |
| <b>Active power-down standby current:</b><br>tCK = tCKmin;<br>CKE is LOW;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                               | IDD3P <sub>1</sub>  | VDD1         | 9.00  | 9.00  | mA    |       |
|                                                                                                                                                                                                                            | IDD3P <sub>2</sub>  | VDD2         | 9.00  | 9.00  | mA    |       |
|                                                                                                                                                                                                                            | IDD3P <sub>Q</sub>  | VDDQ         | 0.80  | 0.80  | mA    | 3     |

| Parameter / Condition                                                                                                                                                                                                             | Symbol              | Power Supply | 3733   | 4266   | Units | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|--------------|--------|--------|-------|-------|
| <b>Active power-down standby current with clock stop:</b><br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled                  | IDD3PS <sub>1</sub> | VDD1         | 9.00   | 9.00   | mA    |       |
|                                                                                                                                                                                                                                   | IDD3PS <sub>2</sub> | VDD2         | 9.00   | 9.00   | mA    |       |
|                                                                                                                                                                                                                                   | IDD3PS <sub>Q</sub> | VDDQ         | 0.80   | 0.80   | mA    | 4     |
| <b>Active non-power-down standby current:</b><br>tCK = tCKmin;<br>CKE is HIGH;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                                 | IDD3N <sub>1</sub>  | VDD1         | 13.20  | 13.20  | mA    |       |
|                                                                                                                                                                                                                                   | IDD3N <sub>2</sub>  | VDD2         | 36.60  | 36.60  | mA    |       |
|                                                                                                                                                                                                                                   | IDD3N <sub>Q</sub>  | VDDQ         | 2.00   | 2.00   | mA    | 4     |
| <b>Active non-power-down standby current with clock stopped:</b><br>CK_t=LOW, CK_c=HIGH;<br>CKE is HIGH;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled          | IDD3NS <sub>1</sub> | VDD1         | 13.20  | 13.20  | mA    |       |
|                                                                                                                                                                                                                                   | IDD3NS <sub>2</sub> | VDD2         | 28.40  | 28.40  | mA    |       |
|                                                                                                                                                                                                                                   | IDD3NS <sub>Q</sub> | VDDQ         | 2.00   | 2.00   | mA    | 4     |
| <b>Operating burst READ current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 8; RL = RL(MIN);<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled | IDD4R <sub>1</sub>  | VDD1         | 25.00  | 26.60  | mA    |       |
|                                                                                                                                                                                                                                   | IDD4R <sub>2</sub>  | VDD2         | 380.00 | 420.00 | mA    |       |
|                                                                                                                                                                                                                                   | IDD4R <sub>Q</sub>  | VDDQ         | 171.00 | 172.00 | mA    | 5     |
| <b>Operating burst WRITE current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 8; WL = WLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled  | IDD4W <sub>1</sub>  | VDD1         | 23.00  | 27.00  | mA    |       |
|                                                                                                                                                                                                                                   | IDD4W <sub>2</sub>  | VDD2         | 359.35 | 398.55 | mA    |       |
|                                                                                                                                                                                                                                   | IDD4W <sub>Q</sub>  | VDDQ         | 2.00   | 2.00   | mA    | 4     |
| <b>All-bank REFRESH Burst current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tRFCabmin;<br>Burst refresh;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled               | IDD5 <sub>1</sub>   | VDD1         | 93.40  | 93.40  | mA    |       |
|                                                                                                                                                                                                                                   | IDD5 <sub>2</sub>   | VDD2         | 153.00 | 153.00 | mA    |       |
|                                                                                                                                                                                                                                   | IDD5 <sub>Q</sub>   | VDDQ         | 2.00   | 2.00   | mA    | 4     |
| <b>All-bank REFRESH Average current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled                                   | IDD5AB <sub>1</sub> | VDD1         | 8.00   | 8.00   | mA    |       |
|                                                                                                                                                                                                                                   | IDD5AB <sub>2</sub> | VDD2         | 48.00  | 48.00  | mA    |       |
|                                                                                                                                                                                                                                   | IDD5AB <sub>Q</sub> | VDDQ         | 2.00   | 2.00   | mA    | 4     |

| Parameter/Condition                                                                                                                                                                                              | Symbol              | Power Supply | 3733  | 4266  | Units | Notes      |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|--------------|-------|-------|-------|------------|
| <b>Per-bank REFRESH Average current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI/8;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled                | IDD5PB <sub>1</sub> | VDD1         | 8.00  | 8.00  | mA    |            |
|                                                                                                                                                                                                                  | IDD5PB <sub>2</sub> | VDD2         | 48.0  | 48.0  | mA    |            |
|                                                                                                                                                                                                                  | IDD5PB <sub>Q</sub> | VDDQ         | 2.00  | 2.00  | mA    | 4          |
| <b>Self refresh current (85°C):</b><br>CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled  | IDD6 <sub>1</sub>   | VDD1         | 7.60  | 7.60  | mA    | 6,7,8,10   |
|                                                                                                                                                                                                                  | IDD6 <sub>2</sub>   | VDD2         | 14.00 | 14.00 | mA    | 6,7,8,10   |
|                                                                                                                                                                                                                  | IDD6 <sub>Q</sub>   | VDDQ         | 0.80  | 0.80  | mA    | 4,6,7,8,10 |
| <b>Self refresh current (45°C):</b><br>CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled  | IDD6 <sub>1</sub>   | VDD1         | 1.10  | 1.10  | mA    | 6,7,8,10   |
|                                                                                                                                                                                                                  | IDD6 <sub>2</sub>   | VDD2         | 1.40  | 1.40  | mA    | 6,7,8,10   |
|                                                                                                                                                                                                                  | IDD6 <sub>Q</sub>   | VDDQ         | 0.10  | 0.10  | mA    | 4,6,7,8,10 |
| <b>Self refresh current (25°C):</b><br>CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled  | IDD6 <sub>1</sub>   | VDD1         | 0.60  | 0.60  | mA    | 6,7,8,10   |
|                                                                                                                                                                                                                  | IDD6 <sub>2</sub>   | VDD2         | 0.70  | 0.70  | mA    | 6,7,8,10   |
|                                                                                                                                                                                                                  | IDD6 <sub>Q</sub>   | VDDQ         | 0.10  | 0.10  | mA    | 4,6,7,8,10 |
| <b>Self refresh current (105°C):</b><br>CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | IDD6ET <sub>1</sub> | VDD1         | 19.70 | 19.70 | mA    | 7,8,11     |
|                                                                                                                                                                                                                  | IDD6ET <sub>2</sub> | VDD2         | 31.20 | 31.20 | mA    | 7,8,11     |
|                                                                                                                                                                                                                  | IDD6ET <sub>Q</sub> | VDDQ         | 0.10  | 0.10  | mA    | 4,7,8,11   |

Notes:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 ohm.
6. The 1x Self-Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
9. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
10. IDD6 85°C is guaranteed, IDD6 45°C is typical of the distribution of the arithmetic mean.
11. IDD6ET is a typical value, is sampled only, and is not tested.



## 8. Electrical Characteristics and AC Timings

### 8.1. AC Timing Parameters

Table - Core Parameters

| Parameter                                     | Symbol | min<br>max | Data Rate                                                                        |      |      |      |      |      |      |      | Unit     | Note |
|-----------------------------------------------|--------|------------|----------------------------------------------------------------------------------|------|------|------|------|------|------|------|----------|------|
|                                               |        |            | 533                                                                              | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 |          |      |
| ACTIVE to ACTIVE command period               | tRC    | min        | tRAS + tRPab (with all-bank precharge)<br>tRAS + tRPpb (with per-bank precharge) |      |      |      |      |      |      |      | ns       |      |
| Minimum Self-Refresh Time (Entry to Exit)     | tSR    | min        | max(15ns, 3nCK)                                                                  |      |      |      |      |      |      |      | ns       |      |
| Self Refresh exit to next valid command delay | tXSR   | min        | max(tRFCab + 7.5ns, 2nCK)                                                        |      |      |      |      |      |      |      | ns       |      |
| Exit power down to next valid command delay   | tXP    | min        | max(7.5ns, 5nCK)                                                                 |      |      |      |      |      |      |      | ns       |      |
| CAS to CAS delay                              | tCCD   | min        | 8                                                                                |      |      |      |      |      |      |      | tCK(avg) | 2    |
| CAS to CAS delay                              | tCCDMW | min        | 4 * tCCD                                                                         |      |      |      |      |      |      |      | tCK(avg) |      |
| Masked Write w/ECC                            |        |            |                                                                                  |      |      |      |      |      |      |      |          |      |
| Internal Read to Precharge command delay      | tRTP   | min        | max(7.5ns, 8nCK)                                                                 |      |      |      |      |      |      |      | ns       |      |
| RAS to CAS Delay                              | tRCD   | min        | max(18ns, 4nCK)                                                                  |      |      |      |      |      |      |      | ns       |      |
| Row Precharge Time (single bank)              | tRPpb  | min        | max(18ns, 4nCK)                                                                  |      |      |      |      |      |      |      | ns       |      |
| Row Precharge Time (all banks) - 8-bank       | tRPab  | min        | max(21ns, 4nCK)                                                                  |      |      |      |      |      |      |      | ns       |      |
| Row Active Time                               | tRAS   | min        | max(42ns, 3nCK)                                                                  |      |      |      |      |      |      |      | ns       |      |
|                                               |        | max        | min(9 * tREFI * Refresh Rate, 70.2)                                              |      |      |      |      |      |      |      | us       | 3    |
| Write Recovery Time                           | tWR    | min        | max{18ns, 4nCK}                                                                  |      |      |      |      |      |      |      | ns       |      |
| Write to Read Command Delay                   | tWTR   | min        | max(10ns, 8nCK)                                                                  |      |      |      |      |      |      |      | ns       |      |
| Active bank A to Active bank B                | tRRD   | min        | max(10ns, 4nck)                                                                  |      |      |      |      |      |      |      | ns       |      |
| Precharge to Precharge Delay                  | tPPD   | min        | 4                                                                                |      |      |      |      |      |      |      | tCK      |      |
| Four Bank Activate Window                     | tFAW   | min        | 40                                                                               |      |      |      |      |      |      |      | ns       |      |

Notes:

1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. The value is based on BL16. For BL32 need additional 8 tCK(avg) delay.
3. Refresh Rate is specified by MR4 OP[2:0].
4. Devices supporting 4267 Mbps specification shall support these timings at lower data rates.

Table - Clock timings

| Parameter                                                 | Symbol    | min<br>max | LPDDR4<br>1600             | LPDDR4<br>2400 | LPDDR4<br>3200 | LPDDR4<br>4200 | Unit     | Note |
|-----------------------------------------------------------|-----------|------------|----------------------------|----------------|----------------|----------------|----------|------|
| Clock Timing                                              |           |            |                            |                |                |                |          |      |
| Average Clock Period                                      | tCK(avg)  | min        | 1.25                       | 0.833          | 0.625          | 0.467          | ns       |      |
|                                                           |           | max        | 100                        | 100            | 100            | 100            |          |      |
| Average high pulse width                                  | tCH(avg)  | min        | 0.46                       | 0.46           | 0.46           | tbd            | tCK(avg) |      |
|                                                           |           | max        | 0.54                       | 0.54           | 0.54           | tbd            |          |      |
| Average low pulse width                                   | tCL(avg)  | min        | 0.46                       | 0.46           | 0.46           | tbd            | tCK(avg) |      |
|                                                           |           | max        | 0.54                       | 0.54           | 0.54           | tbd            |          |      |
| Absolute Clock Period                                     | tCK(abs)  | min        | tCK(avg)min + tJIT(per)min |                |                |                | ns       |      |
|                                                           |           | max        | -                          |                |                |                |          |      |
| Absolute clock HIGH pulse width                           | tCH(abs)  | min        | 0.43                       | 0.43           | 0.43           | tbd            | tCK(avg) |      |
|                                                           |           | max        | 0.57                       | 0.57           | 0.57           | tbd            |          |      |
| Absolute clock LOW pulse width                            | tCL(abs)  | min        | 0.43                       | 0.43           | 0.43           | tbd            | tCK(avg) |      |
|                                                           |           | max        | 0.57                       | 0.57           | 0.57           | tbd            |          |      |
| Clock Period Jitter                                       | tJIT(per) | min        | -70                        | -50            | -40            | tbd            | ps       |      |
|                                                           |           | max        | 70                         | 50             | 40             | tbd            |          |      |
| Maximum Clock Jitter between two consecutive clock cycles | tJIT(cc)  | min        | -                          |                |                |                | ps       |      |
|                                                           |           | max        | 140                        | 100            | 80             | tbd            |          |      |

**Table - ZQ Calibration timings**

| Parameter                       | Symbol   | min<br>max | DDR4<br>533     | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|---------------------------------|----------|------------|-----------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| ZQ Calibration Time             | tZQCAL   | max        | 1               |              |              |              |              |              |              |              | us   |      |
| ZQ Calibration Latch Quiet Time | tZQLAT   | max        | max(30ns, 8nCK) |              |              |              |              |              |              |              | ns   |      |
| Calibration Reset Time          | tZQRESET | max        | max(50ns, 3nCK) |              |              |              |              |              |              |              | ns   |      |

**Table - DQ Tx Voltage and Timings (Read Timing parameters)**

| Parameter                                                          | Symbol           | min<br>max | 1600/<br>1867                                                | 2133/<br>2400 | 3200 | 4266 | Unit     | Note  |
|--------------------------------------------------------------------|------------------|------------|--------------------------------------------------------------|---------------|------|------|----------|-------|
| Data Timing                                                        |                  |            |                                                              |               |      |      |          |       |
| DQS_t,DQS_c to DQ Skew                                             | tDQSQ            | max        | 0.18                                                         |               |      |      | UI       | 1     |
| DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)         | tQH              | min        | min(tQSH, tQSL)                                              |               |      |      | UI       | 1     |
| DQ output window time total, per pin (DBI-Disabled)                | tQW_total        | min        | 0.75                                                         | 0.73          | 0.7  | 0.7  | UI       | 1,4   |
| DQ output window time deterministic, per pin (DBI-Disabled)        | tQW_dj           | min        | tbd                                                          | tbd           | tbd  | tbd  | UI       | 1,4,3 |
| DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled) | tDQSQ_DBI        | max        | tbd                                                          | tbd           | tbd  | tbd  | UI       | 1     |
| DQ output hold time total from DQS_t, DQS_c (DBI-enabled)          | tQH_DBI          | min        | min(tQSH_DBI, tQSL_DBI)                                      |               |      |      | UI       | 1     |
| DQ output window time total, per pin (DBI-enabled)                 | tQW_total_DBI    | min        | tbd                                                          | tbd           | tbd  | tbd  | UI       | 1,4   |
| Read preamble                                                      | tRPRE            | min        | 1.8                                                          |               |      |      | tCK(avg) |       |
| Read postamble                                                     | tRPST            | min        | 0.4                                                          |               |      |      | tCK(avg) |       |
| Extended Read postamble                                            | tRPSTE           | min        | 1.4                                                          |               |      |      | tCK(avg) |       |
| DQS Low-impedance time from CK_t, CK_c                             | tLZ(DQS)         | min        | (RL x tCK) + tDQSCK(Min) - (tPRE(Max) x tCK) - 200ps         |               |      |      | ps       |       |
| DQS High-impedance time from CK_t, CK_c                            | tHZ(DQS)         | max        | (RL x tCK) + tDQSCK(Max) + (RPST(Max) x tCK) - 100ps         |               |      |      | ps       |       |
| DQ Low-impedance time from CK_t, CK_c                              | tLZ(DQ)          | min        | (RL x tCK) + tDQSCK(Min) - 200ps                             |               |      |      | ps       |       |
| DQ High-impedance time from CK_t, CK_c                             | tHZ(DQ)          | max        | (RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps |               |      |      | ps       |       |
| Data Strobe Timing                                                 |                  |            |                                                              |               |      |      |          |       |
| DQS output access time from CK/CK#                                 | tDQSCK           | min<br>max | 1.5<br>3.5                                                   |               |      |      | ns       | 8     |
| DQSCK Temperature Drift                                            | tDQSCK_temp      | max        | 4                                                            |               |      |      | ps/C     | 9     |
| DQSCK Volgate Drift                                                | tDQSCK_volt      | max        | 7                                                            |               |      |      | ps/mV    | 10    |
| CK to DQS Rank to Rank variation                                   | tDQSCK_rank2rank | max        | 1.0                                                          |               |      |      | ns       | 11,12 |
| DQS Output Low Pulse Width (DBI Disabled)                          | tQSL             | min        | tCL(abs)-0.05                                                |               |      |      | tCK(avg) | 4,5   |
| DQS Output High Pulse Width (DBI Disabled)                         | tQSH             | min        | tCH(abs)-0.05                                                |               |      |      | tCK(avg) | 4,6   |
| DQS Output Low Pulse Width (DBI Enabled)                           | tQSL_DBI         | min        | tCL(abs)-0.045                                               |               |      |      | tCK(avg) | 5,7   |
| DQS Output High Pulse Width (DBI Enabled)                          | tQSH_DBI         | min        | tCH(abs)-0.045                                               |               |      |      | tCK(avg) | 6,7   |

**Notes:**

- 1.DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are **tbd**.
- 2.The deterministic component of the total timing. Measurement method **tbd**.
- 3.This parameter will be characterized and guaranteed by design.
- 4.This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) - 0.04.
- 5.tQSL describes the instantaneous differential output low pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge
- 6.tQSH describes the instantaneous differential output high pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge

7. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs).
8. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
9. tDQSCK\_temp max delay variation as a function of Temperature.
10. tDQSCK\_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK\_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the  $\text{Max}\{\text{abs}\{\text{tDQSCKmin@V1}-\text{tDQSCKmax@V2}\}, \text{abs}\{\text{tDQSCKmax@V1}-\text{tDQSCKmin@V2}\}\} / \text{abs}\{\text{V1}-\text{V2}\}$ . For tester measurement VDDQ = VDD2 is assumed.
11. The same voltage and temperature are applied to tDQS2CK\_rank2rank.
12. tDQSCK\_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
13.  $\text{UI} = \text{tCK}(\text{avg}) / \text{min}/2$

**Table - DQ Rx Voltage and Timing Parameters (Write Timing Parameters)**

| Symbol            | Parameter                                                 | min<br>max | 1600/1867 <sup>A)</sup> | 2133/2400  | 3200       | 4266       | Unit     | Note           |
|-------------------|-----------------------------------------------------------|------------|-------------------------|------------|------------|------------|----------|----------------|
| VdIVW_total       | Rx Mask voltage p-p total                                 | max        | 140                     | 140        | 140        | 120        | mV       | 1,2,3,5        |
| VdIVW_dV          | Rx Mask voltage - deterministic                           | max        | tbd                     | tbd        | tbd        | tbd        | mV       | 1,5            |
| TdIVW_total       | Rx timing window total<br>(At VdIVW voltage levels)       | max        | 0.22                    | 0.22       | 0.25       | 0.25       | UI       | 1,2,4,5        |
| TdIVW_dj          | Rx deterministic timing                                   | max        | tbd                     | tbd        | tbd        | tbd        | UI       | 1,5            |
| TdIVW_1bit        | Rx timing window 1bit toggle<br>(At VdIVW voltage levels) | max        | tbd                     | tbd        | tbd        | tbd        | UI       | 1,2,4,5<br>,14 |
| VIHL_AC           | DQ AC input pulse amplitude p-p                           | min        | 180                     | 180        | 180        | 170        | mV       | 7,15           |
| TdIPW             | DQ input pulse width<br>(At Vcent_DQ)                     | min        | 0.45                    | 0.45       | 0.45       | 0.45       | UI       | 8              |
| TDQS2DQ           | DQ to DQS offset                                          | min<br>max | 200<br>800              | 200<br>800 | 200<br>800 | 200<br>800 | ps       | 9              |
| TDQDQ             | DQ to DQ offset                                           | max        | 30                      | 30         | 30         | 30         | ps       | 10             |
| TDQS2DQ_temp      | DQ to DQS offset temperature variation                    | max        | 0.6                     | 0.6        | 0.6        | 0.6        | ps/°C    | 11             |
| TDQS2DQ_volt      | DQ to DQS offset voltage variation                        | max        | 33                      | 33         | 33         | 33         | ps/50mV  | 12             |
| TDQS2DQ_rank2rank | DQ to DQS offset rank to rank                             | max        | 200                     | 200        | 200        | 200        | ps       | 17,18          |
| tDQSS             | Write command to 1st DQS latching<br>transition           | min<br>max | 0.75<br>1.25            |            |            |            | tCK(avg) |                |
| tDQSH             | DQS input high-level width                                | min        | 0.4                     |            |            |            | tCK(avg) |                |
| tDQSL             | DQS input low-level width                                 | min        | 0.4                     |            |            |            | tCK(avg) |                |
| tDSS              | DQS falling edge to CK setup time                         | min        | 0.2                     |            |            |            | tCK(avg) |                |
| tDSH              | DQS falling edge hold time from CK                        | min        | 0.2                     |            |            |            | tCK(avg) |                |
| tWPRE             | Write preamble                                            | min        | 1.8                     |            |            |            | tCK(avg) |                |
| tWPST             | 0.5 tCK Write postamble                                   | min        | 0.4                     |            |            |            | tCK(avg) |                |
| tWPSTE            | 1.5 tCK Write postamble                                   | min        | 1.4                     |            |            |            | tCK(avg) |                |
| SRIN_dIVW         | Input slew rate over<br>VdIVW_total                       | min<br>max | 1<br>7                  | 1<br>7     | 1<br>7     | 1<br>7     | V/ns     | 13             |

**Notes:**

1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >250KHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2. The design specification is a BER <tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent\_DQ(pin\_mid).
4. Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels.
5. Defined over the DQ internal Vref range. The Rx mask at the pin must be within the internal Vref DQ range irrespective of the input signal common mode.
6. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd
7. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent\_DQ(pin\_mid) such that VIHL\_AC/2 min must be met both above and below Vcent\_DQ.

8. DQ only minimum input pulse width defined at the Vcent\_DQ(pin\_mid).
9. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
10. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
11. TDQS2DQ max delay variation as a function of temperature.
12. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2.
13. Input slew rate over VdIVW Mask centered at Vcent\_DQ(pin\_mid).
14. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
15. VIH<sub>L</sub>\_AC does not have to be met when no transitions are occurring.
16. The same voltage and temperature are applied to tDQS2DQ\_rank2rank.
17. tDQS2DQ\_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

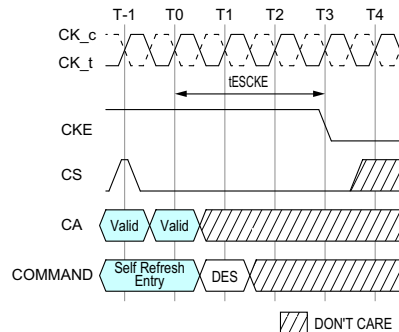
A. The following Rx voltage and timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. The timing parameters in UI can be converted to absolute time values where  $t_{ck}(avg)_{min}/2 = 625ps$  for DQ=1600. For example the  $TdIVW_{total}(ps) = 0.22 * 625ps = 137.5ps$ .

**Table - Self-Refresh Timing Parameters**

| Parameter                                        | Symbol | min<br>max | DDR4<br>533               | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|--------------------------------------------------|--------|------------|---------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| Delay from Self Refresh Entry to CKE Input Low   | tESCKE | min        | max(1.75ns, 3tCK)         |              |              |              |              |              |              |              | nCK  | 1    |
| Minimum Self-Refresh Time<br>(Entry to Exit)     | tSR    | min        | max(15ns, 3nCK)           |              |              |              |              |              |              |              | ns   | 1    |
| Self refresh exit to next valid command<br>delay | tXSR   | min        | max(trFCab + 7.5ns, 2nCK) |              |              |              |              |              |              |              | ns   | 1,2  |

Note

1. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 \* tCK) and 1.75ns has transpired. The case which 3tCK is applied to is shown below.



2. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are only allowed during this period.

**Table - Command Address Input Parameters**

| Symbol    | Parameter                         | min<br>max | DQ-1333 <sup>A)</sup> | DQ-1600/<br>1867 | DQ-3200 | DQ-4266 | Unit | Note    |
|-----------|-----------------------------------|------------|-----------------------|------------------|---------|---------|------|---------|
| VcIVW     | Rx Mask voltage p-p               | max        | 175                   | 175              | 155     | 145     | mV   | 1,2,4   |
| tcIVW     | Rx timing window                  | max        | 0.3                   | 0.3              | 0.3     | 0.3     | UI   | 1,2,3,4 |
| VIHL_AC   | CA AC input pulse amplitude pk-pk | min        | 210                   | 210              | 190     | 180     | mV   | 5,8     |
| TcIPW     | CA input pulse width              | min        | 0.55                  | 0.55             | 0.6     | 0.6     | UI   | 6       |
| SRIN_cIVW | Input slew rate over VcIVW        | min<br>max | 1<br>7                | 1<br>7           | 1<br>7  | 1<br>7  | V/ns | 7       |

Notes:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent\_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.

4. Defined over the CA internal Vref range. The Rx mask at the pin must be within the internal Vref CA range irrespective of the input signal common mode.
  5. CA only input pulse signal amplitude into the receiver must meet or exceed VIH<sub>L</sub> AC at any point over the total UI. No timing requirement above level. VIH<sub>L</sub> AC is the peak to peak voltage centered around Vcent\_CA(pin mid) such that VIH<sub>L</sub>\_AC/2 min must be met both above and below Vcent\_CA.
  6. CA only minimum input pulse width defined at the Vcent\_CA(pin mid).
  7. Input slew rate over VcIVW Mask centered at Vcent\_CA(pin mid).
  8. VIH<sub>L</sub>\_AC does not have to be met when no transitions are occurring.
  9. UI=tCK(avg)min/2
- A. The following Rx voltage and timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. The timing parameters in UI can be converted to absolute time values where tck(avg)min= 1.5ns for DQ=1333. For example the tClVW(ps) = 0.3\*1.5ns=450ps.

**Table - Boot Parameters**

| Parameter                                   | Symbol  | min<br>max | DDR4<br>533            | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|---------------------------------------------|---------|------------|------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| Clock Cycle Time                            | tCKb    | min<br>max | Note 1, 2<br>Note 1, 2 |              |              |              |              |              |              |              | ns   |      |
| Address & Control Input Setup Time          | tISb    | min        | 1150                   |              |              |              |              |              |              |              | ps   |      |
| Address & Control Input Hold Time           | tIHb    | min        | 1150                   |              |              |              |              |              |              |              | ps   |      |
| DQS Output Data Access Time from CK/CK#     | tDQSCKb | min<br>max | 2<br>10                |              |              |              |              |              |              |              | ns   |      |
| Data Strobe Edge to Output Data Edge tDQSQb | tDQSQb  | max        | 1.2                    |              |              |              |              |              |              |              | ns   |      |

**Notes**

1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent

**Table - Mode Register Parameters**

| Parameter                                                                 | Symbol | min<br>max | DDR4<br>533      | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|---------------------------------------------------------------------------|--------|------------|------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| Additional time after tXP has expired until the MRR command may be issued | tMRRi  | min        | tRCD + 3nCK      |              |              |              |              |              |              |              | ns   |      |
| MODE REGISTER Write command period                                        | tMRW   | min        | max(10ns, 10nCK) |              |              |              |              |              |              |              | ns   |      |
| MODE REGISTER Read command period                                         | tMRR   | min        | 8                |              |              |              |              |              |              |              | nCK  |      |
| Mode Register Write Set Command Delay                                     | tMRD   | min        | max(14ns, 10nCK) |              |              |              |              |              |              |              | ns   |      |

**Table - VRCG Enable/Disable Timing**

| Parameter                           | Symbol        | min<br>max | DDR4<br>533 | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|-------------------------------------|---------------|------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| VREF high current mode enable time  | tVRCG_Enable  | max        | 200         |              |              |              |              |              |              |              | ns   |      |
| VREF high current mode disable time | tVRCG_Disable | max        | 100         |              |              |              |              |              |              |              | ns   |      |

**Table - Command Bus Training Parameters**

| Parameter                                                | Symbol   | min<br>max | DDR4<br>533      | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|----------------------------------------------------------|----------|------------|------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| Clock and Command Valid after CKE Low                    | tCKELCK  | min        | max(7.5ns, 5nCK) |              |              |              |              |              |              |              | tCK  |      |
| Data Setup for Vref Training Mode                        | tDStrain | min        | 2                |              |              |              |              |              |              |              | ns   |      |
| Data Hold for Vref Training Mode                         | tDHtrain | min        | 2                |              |              |              |              |              |              |              | ns   |      |
| Asynchronous Data Read                                   | tADR     | max        | 20               |              |              |              |              |              |              |              | ns   |      |
| CA Bus Training Command to CA Bus Training Command Delay | tCACD    | min        | RU(tADR/tCK)     |              |              |              |              |              |              |              | tCK  | 2    |
| Valid Strobe Requirement before CKE Low                  | tDQSCKE  | min        | 10               |              |              |              |              |              |              |              | ns   | 1    |

| Parameter                                                   | Symbol      | min<br>max | DDR4<br>533       | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|-------------------------------------------------------------|-------------|------------|-------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| First CA Bus Training Command Following CKE Low             | tCAENT      | min        | 250               |              |              |              |              |              |              |              | ns   |      |
| Vref Step Time – multiple steps                             | tVref_long  | max        | 250               |              |              |              |              |              |              |              | ns   |      |
| Vref Step Time – one step                                   | tVref_short | max        | 80                |              |              |              |              |              |              |              | ns   |      |
| Valid Clock Requirement before CS High                      | tCKPRECS    | min        | 2*tCK + tXP       |              |              |              |              |              |              |              | -    |      |
| Valid Clock Requirement after CS High                       | tCKPSTCS    | min        | max (7.5ns, 5nCK) |              |              |              |              |              |              |              | -    |      |
| Minimum delay from CS to DQS toggle in command bus training | tCS_Vref    | min        | 2                 |              |              |              |              |              |              |              | tCK  |      |
| Minimum delay from CKE High to Strobe High Impedance        | tCKEHDQS    | min        | 10                |              |              |              |              |              |              |              | ns   |      |
| Clock and Command valid before CKE HIGH                     | tCKCKEH     | min        | 2                 |              |              |              |              |              |              |              | tCK  |      |
| CA Bus Training CKE High to DQ Tri-state                    | tMRZ        | min        | 1.5               |              |              |              |              |              |              |              | ns   |      |
| ODT turn-on latency from CKE                                | tCKELODton  | min        | 20                |              |              |              |              |              |              |              | ns   |      |
| ODT turn-off latency from CKE                               | tCKELODtoff | min        | 20                |              |              |              |              |              |              |              | ns   |      |

Notes:

1. DQS\_t has to retain a low level during tDQSCKE period, as well as DQS\_c has to retain a high level.
2. If tCADC is violated, the data for samples which violate tCADC will not be available, except for the last sample (where tCADC after this sample is met). Valid data for the last sample will be available after tADR.

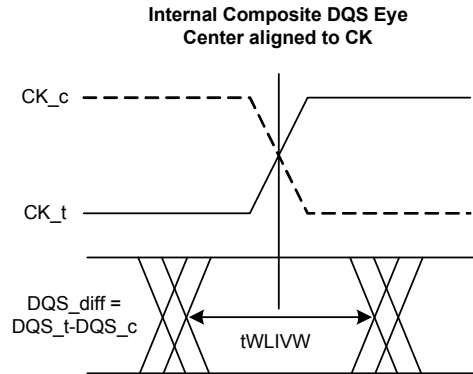
**Table - Write Leveling Parameters**

| Parameter                                                      | Symbol       | min<br>max | DDR4<br>533      | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|----------------------------------------------------------------|--------------|------------|------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| DQS_t/DQS_c delay after write leveling mode is programmed      | tWLDQSEN     | min        | 20               |              |              |              |              |              |              |              | tCK  |      |
| Write preamble for Write Leveling                              | tWLWPRE      | min        | 20               |              |              |              |              |              |              |              | tCK  |      |
| First DQS_t/DQS_c edge after write leveling mode is programmed | tWLMRD       | min        | 40               |              |              |              |              |              |              |              | tCK  |      |
| Write leveling output delay                                    | tWLO         | min        | 0                |              |              |              |              |              |              |              | ns   |      |
|                                                                |              | max        | 20               |              |              |              |              |              |              |              |      |      |
| Valid Clock Requirement before DQS Toggle                      | tCKPRDQS     | min        | max(7.5ns, 4nCK) |              |              |              |              |              |              |              |      |      |
| Valid Clock Requirement after DQS Toggle                       | tCKPSTDQS    | min        | max(7.5ns, 4nCK) |              |              |              |              |              |              |              |      |      |
| Write leveling hold time                                       | tWLH         | min        |                  |              | 150          | 100          |              | 75           |              | 50           | ps   | 1,2  |
| Write leveling setup time                                      | tWLS         | min        |                  |              | 150          | 100          |              | 75           |              | 50           | ps   | 1,2  |
| Write leveling invalid window                                  | tWLIVW_Total | min        |                  |              | 240          | 160          |              | 120          |              | 90           | ps   | 1,2  |

Notes:

1. In addition to the traditional setup and hold time specifications above, there is value in a invalid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
2. tWLIVW\_Total is defined in a similar manner to tDIVW\_Total, except that here it is a DQS invalid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling invalid window.

The DQS input mask for timing with respect to CK is shown in the following figure. The "total" mask (tDIVW\_total) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

**Figure - DQS\_t/DQS\_c and CK\_t/CK\_c at DRAM Latch**

**Table - Read Preamble Training Timings**

| Parameter                                | Symbol | min<br>max | DDR4<br>533     | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|------------------------------------------|--------|------------|-----------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| Delay from MRW command to DQS Driven out | tSDO   | max        | min(tMRD, 15ns) |              |              |              |              |              |              |              | tCK  | 1    |

**Table - MPC [Write FIFO] AC Timing**

| Parameter                                                                          | Symbol | min<br>max | DDR4<br>533 | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|------------------------------------------------------------------------------------|--------|------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| Additional time after tXP has expired until MPC [Write FIFO] command may be issued | tMPCWR | min        | tRCD + 3nCK |              |              |              |              |              |              |              |      |      |

**Table - DQS Interval Oscillator AC Timing**

| Parameter                                         | Symbol | min<br>max | Value           | Unit | Note |
|---------------------------------------------------|--------|------------|-----------------|------|------|
| Delay time from OSC stop to Mode Register Readout | tOSCO  | min        | max(40ns, 8nCK) | ns   |      |

**Table - Frequency Set Point Timing**

| Parameter                                                         | Symbol     | min<br>max | DDR4<br>533      | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|-------------------------------------------------------------------|------------|------------|------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| Frequency Set Point Switching Time                                | tFC_Short  | min        | 200              |              |              |              |              |              |              |              | ns   | 1    |
|                                                                   | tFC_Middle | min        | 200              |              |              |              |              |              |              |              | ns   | 1    |
|                                                                   | tFC_Long   | min        | 250              |              |              |              |              |              |              |              | ns   | 1    |
| Valid Clock Requirement after entering FSP change                 | tCKFSPE    | min        | max(7.5ns, 4nCK) |              |              |              |              |              |              |              |      |      |
| Valid Clock Requirement before 1st valid command after FSP change | tCKFSPX    | min        | max(7.5ns, 4nCK) |              |              |              |              |              |              |              |      |      |

Notes:

- Frequency Set Point Switching Time depends on value of Vref(ca) setting: MR12 OP[5:0] and Vref(ca) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table "tFC value mapping".  
Additionally change of Frequency Set Point may affect Vref(dq) setting. Setting time of Vref(dq) level is same as Vref(ca) level.

**Table - CA ODT setting timing**

| Parameter                | Symbol | Min/Max | LPDDR4-1600/1866/2133/2400/3200/4266 | Units | Note |
|--------------------------|--------|---------|--------------------------------------|-------|------|
| ODT CA Value Update Time | tODTUP | Min     | RU(tbd ns/tCK(avg))                  |       |      |

**Table - Power Down Timing**

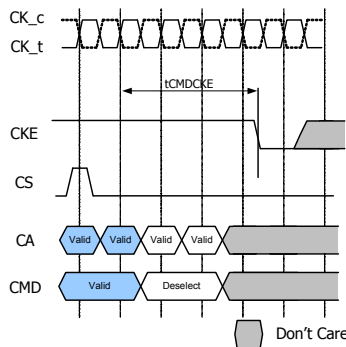
| Parameter                                                                                | Symbol   | min<br>max | DDR4<br>533       | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|------------------------------------------------------------------------------------------|----------|------------|-------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| CKE minimum pulse width<br>(HIGH and LOW pulse width)                                    | tCKE     | min        | Max(7.5ns, 4nCK)  |              |              |              |              |              |              |              | -    |      |
| Delay from valid command to CKE input LOW                                                | tCMDCKE  | min        | Max(1.75ns, 3nCK) |              |              |              |              |              |              |              | ns   | 1    |
| Valid Clock Requirement after CKE Input low                                              | tCKELCK  | min        | Max(5ns, 5nCK)    |              |              |              |              |              |              |              | ns   | 1    |
| Valid CS Requirement before CKE Input Low                                                | tCSCKE   | min        | 1.75              |              |              |              |              |              |              |              | ns   |      |
| Valid CS Requirement after CKE Input low                                                 | tCKELCS  | min        | Max(5ns, 5nCK)    |              |              |              |              |              |              |              | ns   |      |
| Valid Clock Requirement before CKE Input High                                            | tCKCKEH  | min        | Max(1.75ns, 3nCK) |              |              |              |              |              |              |              | ns   | 1    |
| Exit power- down to next valid command delay                                             | tXP      | min        | Max(7.5ns, 5nCK)  |              |              |              |              |              |              |              | ns   | 1    |
| Valid CS Requirement before CKE Input High                                               | tCSCKEH  | min        | 1.75              |              |              |              |              |              |              |              | ns   |      |
| Valid CS Requirement after CKE Input High                                                | tCKEHCS  | min        | Max(7.5ns, 5nCK)  |              |              |              |              |              |              |              | ns   |      |
| Valid Clock and CS Requirement after CKE Input low<br>after MRW Command                  | tMRWCKEL | min        | Max(14ns, 10nCK)  |              |              |              |              |              |              |              | ns   | 1    |
| Valid Clock and CS Requirement after CKE Input low<br>after ZQ Calibration Start Command | tZQCKE   | min        | Max(1.75ns, 3nCK) |              |              |              |              |              |              |              | ns   | 1    |

Notes:

1. Delay time has to satisfy both analog time(ns) and clock count(nCK).

For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 \*tCK) and 3.75ns has transpired.

The case which 3nCK is applied to is shown below.

**Figure - tCMDCKE Timing**

**Table - PPR Timing Parameters**

| Parameter                | Symbol    | LPDDR4 |     | Unit | Notes |
|--------------------------|-----------|--------|-----|------|-------|
|                          |           | Min    | Max |      |       |
| PPR Programming Time     | tPGM      | 1000   | -   | ms   |       |
| PPR Exit Time            | tPGM_Exit | 15     | -   | ns   |       |
| New Address Setting Time | tPGMPST   | 50     | -   | us   |       |



**Table - Temperature Derating for AC timing**

| Parameter                                       | Symbol  | min<br>max | DDR4<br>533  | DDR4<br>1066 | DDR4<br>1600 | DDR4<br>2133 | DDR4<br>2667 | DDR4<br>3200 | DDR4<br>3733 | DDR4<br>4267 | Unit | Note |
|-------------------------------------------------|---------|------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|------|------|
| DQS Output access time from CK_t/CK_c (derated) | tDQSCkD | max        | 3600         |              |              |              |              |              |              |              | ps   | 1    |
| RAS-to-CAS delay (derated)                      | tRCDd   | min        | tRCD + 1.875 |              |              |              |              |              |              |              | ns   | 1    |
| Activate-to-Activate command period (derated)   | tRCd    | min        | tRC + 3.75   |              |              |              |              |              |              |              | ns   | 1    |
| Row active time (derated)                       | tRASd   | min        | tRAS + 1.875 |              |              |              |              |              |              |              | ns   | 1    |
| Row precharge time (derated)                    | tRPd    | min        | tRP + 1.875  |              |              |              |              |              |              |              | ns   | 1    |
| Active bank A to Active bank B (derated)        | tRRDd   | min        | tRRD + 1.875 |              |              |              |              |              |              |              | ns   | 1    |

Notes:

1. Timing derating applies for operation at 85°C to 105°C

## 8.2. CA Rx voltage and timing

The command and address(CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

Figure - CA Receiver(Rx) mask

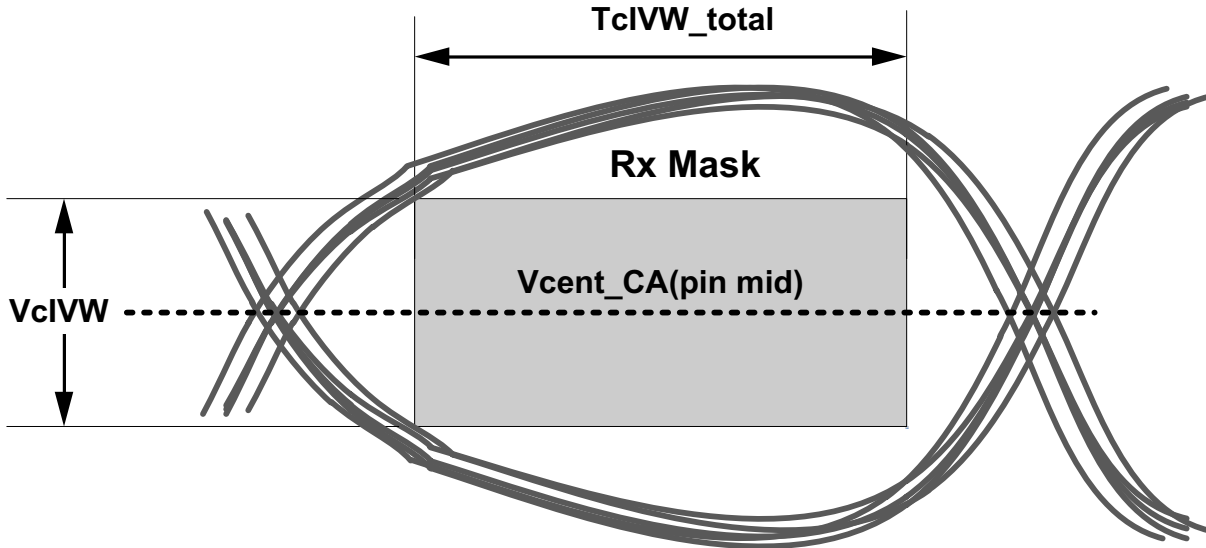
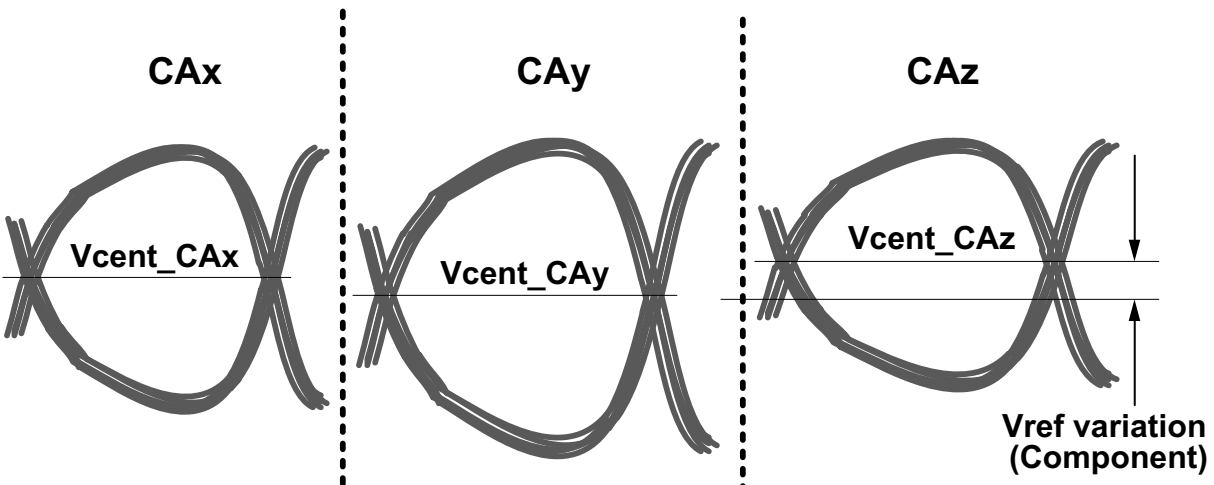


Figure - Across pin Vref CA voltage variation



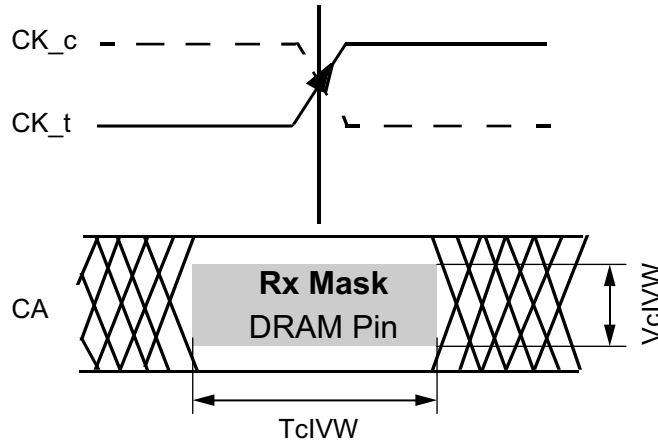
Vcent\_CA(pin avg) is defined as the midpoint between the largest Vcent\_CA voltage level and the smallest Vcent\_CA voltage level across all CA and CS pins for a given DRAM component. Each CA pin Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in the above figure. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level Vref will be set by the

system to account for Ron and ODT settings.

**Figure - CA Timing at the DRAM pins**

**CK\_t, CK\_c Data-in at DRAM Pin**

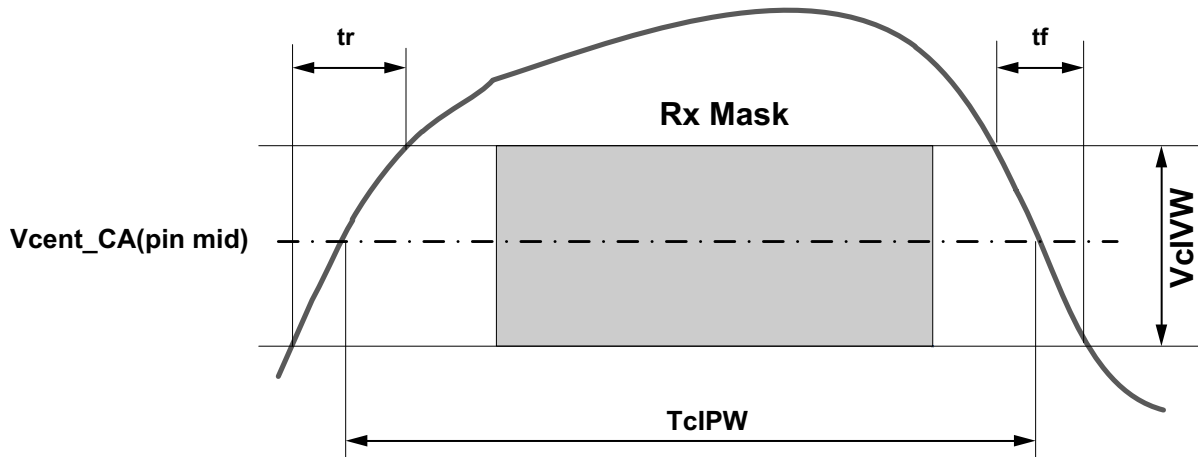
**Minimum CA Eye center aligned**



TcIVW for all CA signals is defined as centered on the CK\_t/CK\_c crossing at the DRAM pin.

All of the timing terms in figure 150 are measured from the CK\_t/CK\_c to the center(midpoint) of the TcIVW window taken at the VcIVW\_total voltage levels centered around Vcent\_CA(pin mid).

**Figure - CA TcIPW and SRIN\_cIVW definition (for each input pulse)**



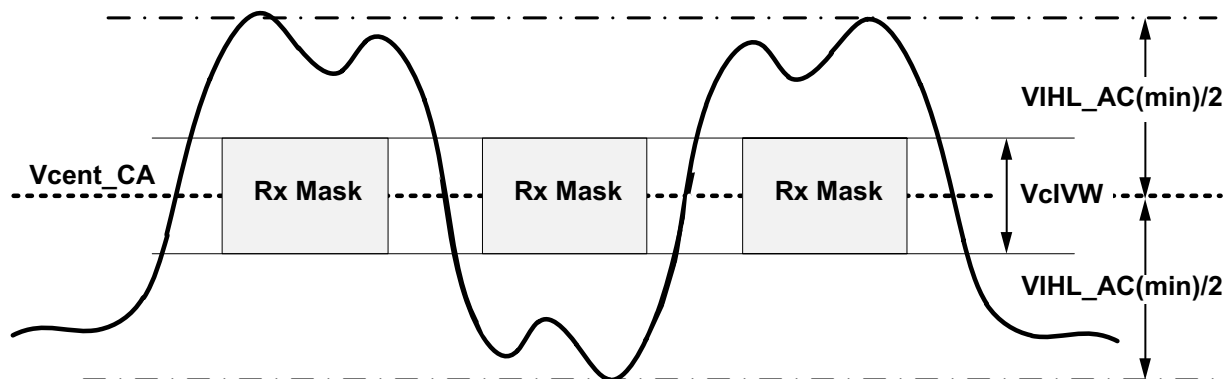
Note

1. SRIN\_cIVW=VcIVW\_Total/(tr or tf), signal must be monotonic within tr and tf range.

Notes:

1. SRIN\_cIVW=VcIVW/(tr or tf), signal must be monotonic within tr and tf range.

Figure - CA VIHIL\_AC definition (for each input pulse)



### 8.3. DRAM Data Timing

Figure - Read data timing definitions  $t_{QH}$  and  $t_{DQSQ}$  across on DQ signals per DQS group

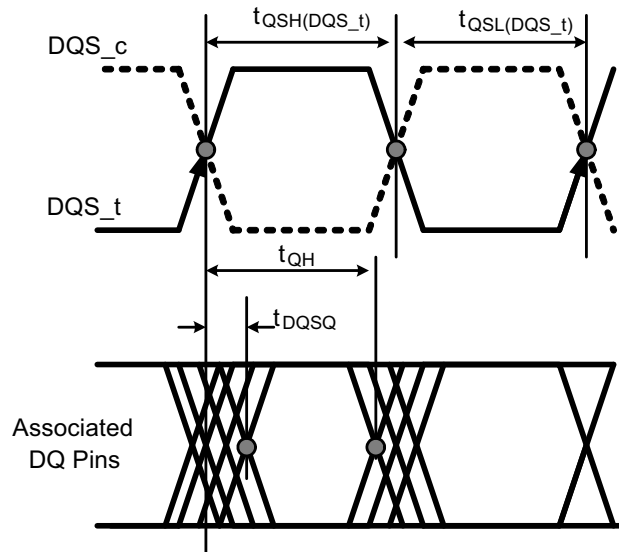
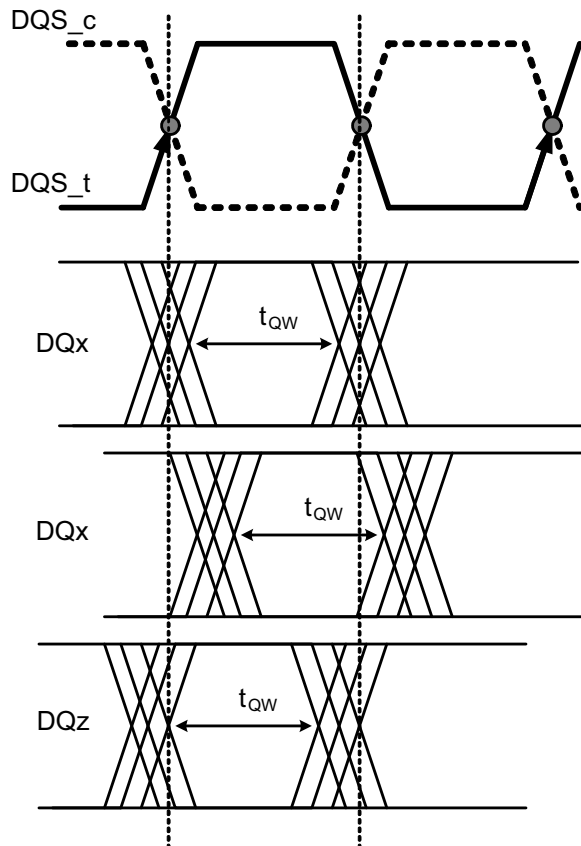
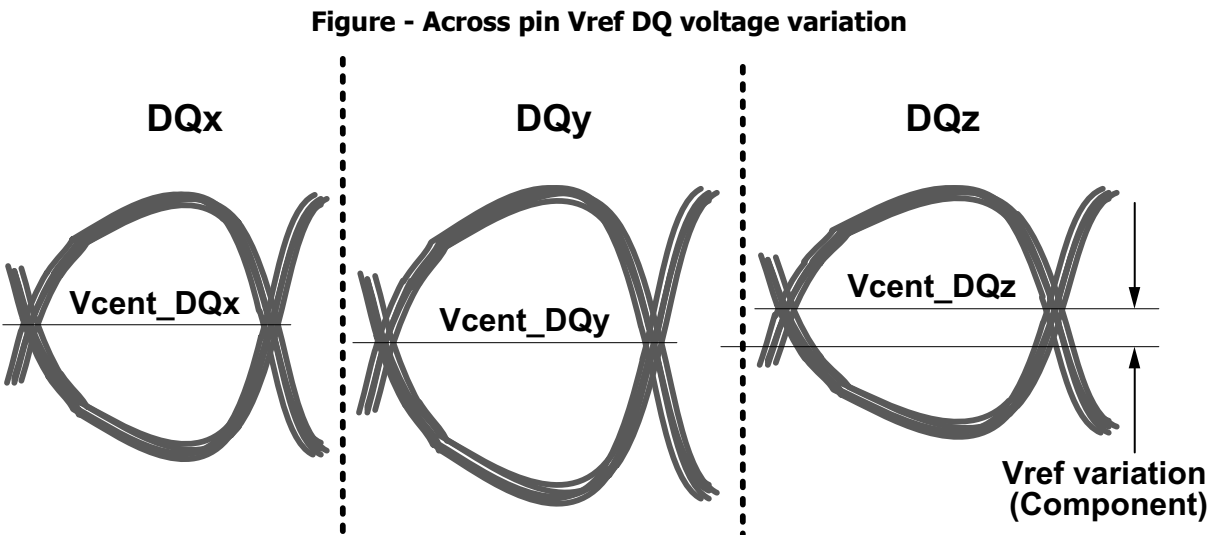
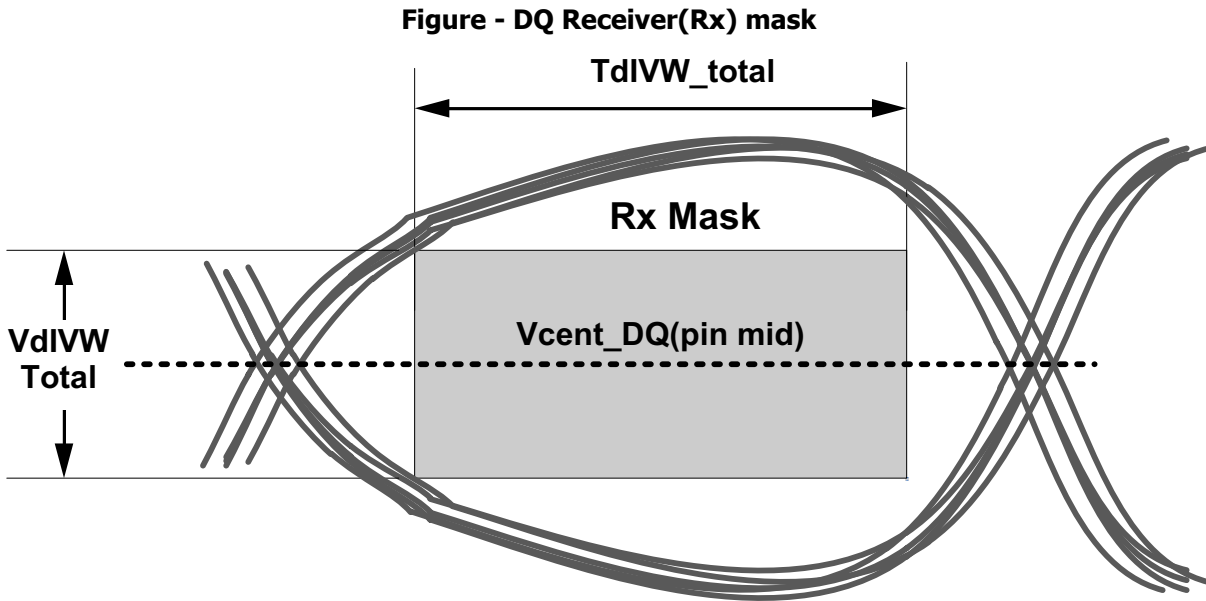


Figure - Read data timing  $t_{QW}$  valid window defined per DQ signal



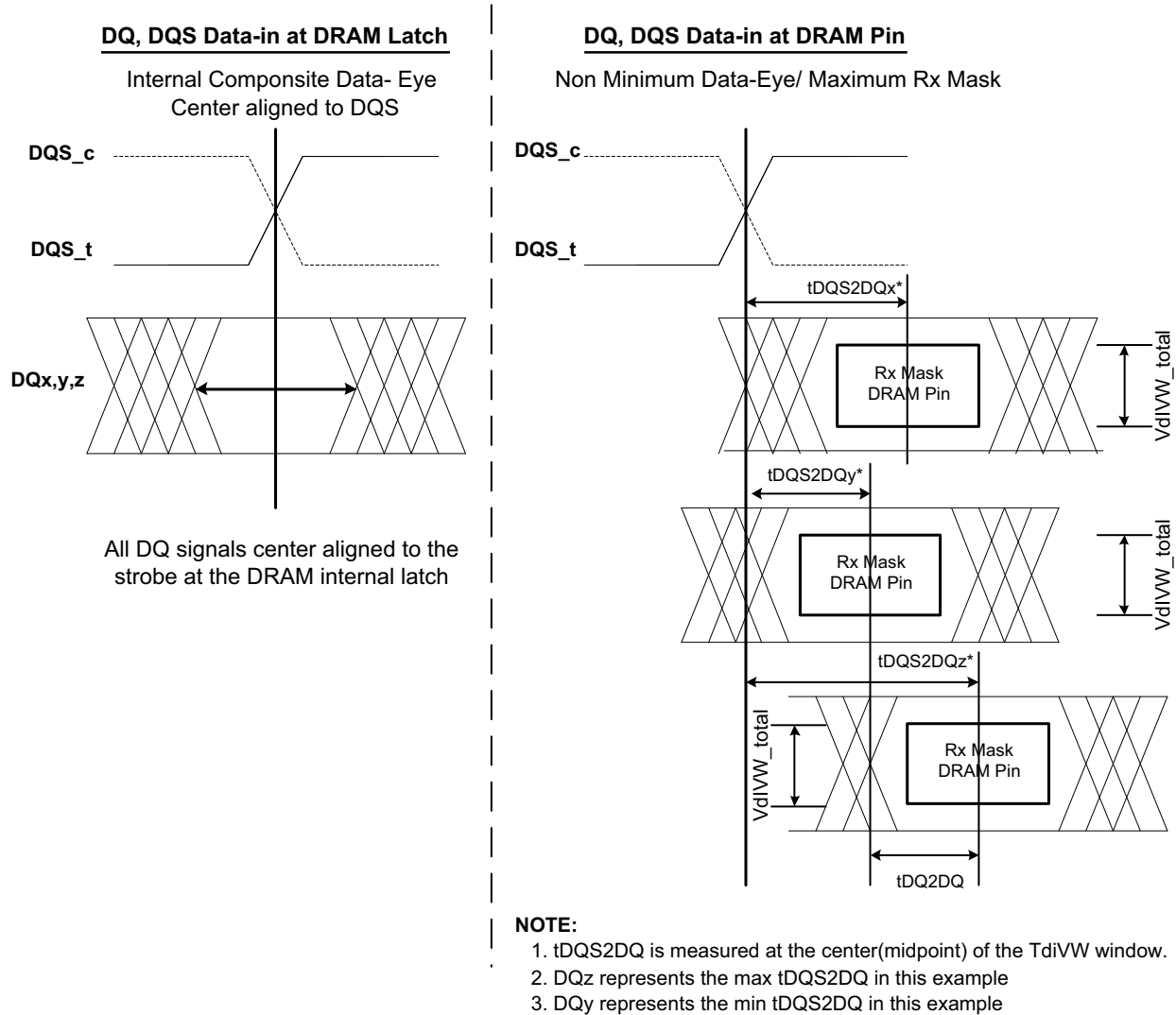
#### 8.4. DQ Rx Voltage and Timing Definition

The DQ input receiver mask for voltage and timing is shown in figure below, is applied per pin. The "total" mask ( $V_{dIVW\_total}$ ,  $T_{dIVW\_total}$ ) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD. The mask is a receiver property and it is not the valid data-eye.



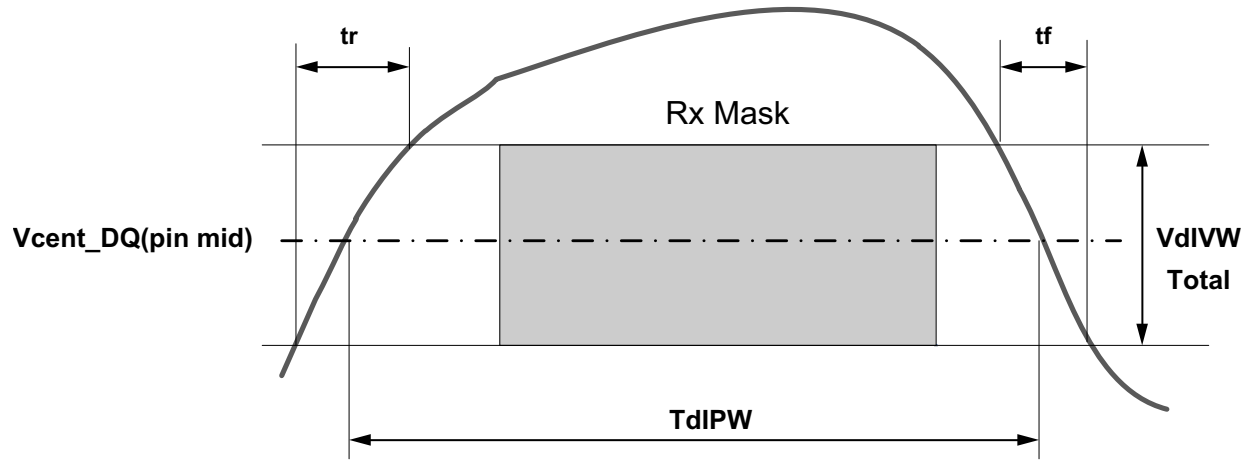
$V_{cent\_DQ(pin\_mid)}$  is defined as the midpoint between the largest  $V_{cent\_DQ}$  voltage level and the smallest  $V_{cent\_DQ}$  voltage level across all DQ pins for a given DRAM component. Each DQ  $V_{cent}$  is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in the above figure. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level VREF will be set by the system to account for Ron and ODT settings.

**Figure - DQ to DQS (tDQS2DQ and tDQDQ) Timings at the DRAM pins referenced from the internal latch**



All of the timing terms in DQ to DQS t are measured from the DQS\_t/DQS\_c to the center(midpoint) of the TdIVW window taken at the VdIVW\_total voltage levels centered around Vcent\_DQ(pin\_mid). In the above figure the timings at the pins are referenced with respect to all DQ signals center aligned to the DRAM internal latch. The data to data offset is defined as the difference between the min and max tDQS2DQ for a given component.

**Figure - DQ TdIPW and SRIN\_dIVW definition (for each input pulse)**



Note

1.  $SRIN\_dIVW = VdIVW_{Total} / (tr \text{ or } tf)$ , signal must be monotonic within  $tr$  and  $tf$  range.

Notes:

1.  $SRIN\_dIVW - VdIVW_{Total} / (tr \text{ or } tf)$ , signal must be monotonic within  $tr$  and  $tf$  range.

**Figure - DQ VIHL\_AC definition (for each input pulse)**

