V39(01M/02M/04M)SA
1M/2M/4M Bit SPI MRAM

Preliminary

1. Product Overview

V39(01M/02M/04M)SA is a family of 1M~4M bits SPI interface MRAM devices organized as 131,072~524,288 words of 8 bits. They are the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of pins. Unlike other serial memories, with the V39(01M/02M/04M)SA family both reads and writes can occur randomly in memory with no delay between writes. The HSxM3SC family provides highly reliable data storage over a wide range of temperatures.

The V39(01M/02M/04M)SA chip offers the following key features:

- pMTJ STT-MRAM technology
  - STT process
  - 1Mb~4Mb capacity
- SPI Interface
  - 54 MHz @SPI SDR READ/Write mode
  - Supports SPI Mode 0 and SPI Mode 3
- Operating Voltage
  - Standard voltage: single VCC 2.7-3.6V
- Operating Temperature
  - 40˚C to 85˚C or 40˚C to 105˚C
- Data Protection
  - Block memory write protection modes
- Power Consumption
  - Sleep current 10μA (typical)
  - Standby current 100μA (typical)
  - Operating current 6mA (typical @ SPI 54 MHz)
  - Read current 4mA(typical @SPI 54MHz)
- Reliability
  - Write endurance 1E12 or 1E10
  - Retention time > 10 years @ 85˚C
- Package
  - SOP8 150mil
  - SOP8 208mil
  - DFN8 5x6mm

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2. Pin Descriptions

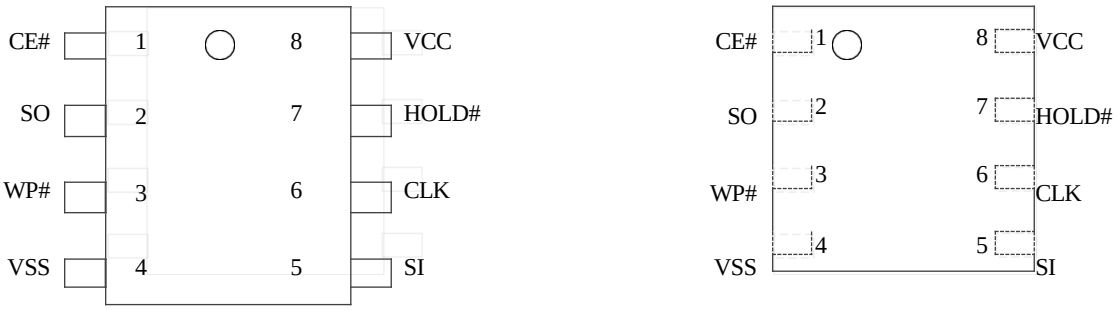


Figure 1 Package Pin Diagram

Pin Number	Pin Name	Interface type	Interface Description
1	CE#	Input	Chip Select Enable Pin
2	SO	Output	Serial Output
3	WP#	Input	Write Protection Pin
4	VSS	Reference	Ground
5	SI	Input	Serial Data Input Pin
6	CLK	Input	Serial Clock Pin
7	HOLD#	Input	Hold Pin
8	VCC	Supply	Power Supply

Table 1 Pin Descriptions

Pin Function Description:

(1) CE#: Chip select enable signal, valid at low level. When chip enable is high, the memory is powered down to minimize standby power, inputs are ignored and the serial output pin is Hi-Z.

(2) SO: Data output pin is driven during a read operation and remains Hi-Z at all other times. Data transitions on the data output occur on the falling edge of CLK.

(3) WP#: A low on the write protect input prevents write operations to the Status Register.

(4) VSS: Ground pin.

(5) SI: All data is input to the device through this pin. This pin is sampled on the rising edge of CLK and ignored at other times.

(6) CLK: CLK：Synchronizes the operation of the MRAM. The clock can operate up to 54MHz to shift commands, address, and data into the memory. Inputs are captured on the rising edge of clock. Data outputs from the MRAM occur on the falling edge of clock. The serial MRAM supports both SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). In Mode 0, the clock is normally low. In Mode 3, the clock is normally high.

(7) HOLD#: A low on the HOLD# pin interrupts a memory operation for another task.

When HOLD# is low, the current operation is suspended. The device will ignore transitions on the CE# and CLK when HOLD# is low. SO is Hi-Z when HOLD# is low. All transitions of HOLD# must occur while CE# is low.

(8) VCC：Power supply pin .

3. SR Register

The V39(01M/02M/04M)SA consists of the two status registers. Every status register consists of the 8 bits listed in Table 2. All bits in the status register are volatile and pre-set in the “0” state by power- up. RFU0, RFU1 and RFU2 mean reserved bits.

Symbol	Bit							
	7	6	5	4	3	2	1	0
SR#1	WP#EN	RFU0	TBSEL	BP2	BP1	BP0	WREN	LOAD_BUSY
SR#2	SRLK	RFU2	RFU1	DC4	DC3	DC2	DC1	DC0

Table 2 SR Register bit Assignmemts

3.1 SR#1 Register

As seen in Table 3, the WP#EN bit is used in conjunction with bit 1 (WREN) and the Write Protection pin (WP#) to provide hardware memory block protection. Bits BP0, BP1, BP2 and TBSEL define the memory block arrays that are protected as described in Table 4. The state of bits 7, 5, 4, 3 and 2 can be user modified. The state of bits 6, 1 and 0 cannot be user modified.

The WREN command is set the WREN bit. The WREN bit is reset to 0 by the following situation: Power-Up, Write Disable command.

When WREN is reset to 0, writes to all blocks and status register are protected. When WREN is set to 1, BP0, BP1, BP2 and TBSEL determine which memory blocks are protected. While WP#EN is reset to 0 and WREN is set to 1, status register bits BP0, BP1, BP2 and TBSEL can be modified. Once WP#EN is set to 1, WP# must be high to modify WP#EN, BP0, BP1, BP2 and TBSEL.

The memory enters hardware block protection when the WP# input is low and the WP#EN bit is set to 1. The memory leaves hardware block protection only when the WP# pin goes high. WhileWP# is low, the write protection blocks for the memory are determined by the status register bits BP0, BP1, BP2 and TBSEL and cannot be modified without taking the WP# signal high again.

If the WP# signal is high (independent of the status of WP#EN bit), the memory is in software protection mode. This means that block write protection is controlled solely by the status register BP0, BP1, BP2 and TBSEL block write protect bits and this information can be modified using the WRSR command.

WREN (SR#1)	WP#EN (SR#1)	WP# (Pin)	Status Registers	Protected Blocks	Unprotected Blocks
0	X	X	Protected	Protected	Protected
1	0	X	Writable	Protected	Writable
1	1	Low	Protected	Protected	Writable
1	1	High	Writable	Protected	Writable

Table 3 Write protection function

TBSEL = 0			
BP2	**BP1**	**BP0**	**4Mb (8 blocks)**
0	0	0	None Protected Area
0	0	1	1 block in Protected Area (0x70000 – 0x7FFFF)
0	1	0	2 blocks in Protected Area (0x60000 – 0x7FFFF)
0	1	1	3 blocks in Protected Area (0x50000 – 0x7FFFF)
1	0	0	4 blocks in Protected Area (0x40000 – 0x7FFFF)
1	0	1	5 blocks in Protected Area (0x30000 – 0x7FFFF)
1	1	0	6 blocks in Protected Area (0x20000 – 0x7FFFF)
1	1	1	7 blocks in Protected Area (0x10000 – 0x7FFFF)
TBSEL = 1			
BP2	**BP1**	**BP0**	**4Mb (8 blocks)**
0	0	0	None Protected Area
0	0	1	1 block in Protected Area (0x00000 – 0xFFFF)
0	1	0	2 blocks in Protected Area (0x00000 – 0x1FFFF)
0	1	1	3 blocks in Protected Area (0x00000 – 0x2FFFF)
1	0	0	4 blocks in Protected Area (0x00000 – 0x3FFFF)
1	0	1	5 blocks in Protected Area (0x00000 – 0x4FFFF)
1	1	0	6 blocks in Protected Area (0x00000 – 0x5FFFF)
1	1	1	7 blocks in Protected Area (0x00000 – 0x6FFFF)

Table 4 4Mb HS4M3SC Block Memory Write Protection

TBSEL = 0			
BP2	**BP1**	**BP0**	**2Mb (4 blocks)**
0	0	0	None Protected Area
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	1 block in Protected Area (0x30000 – 0x3FFFF)
1	1	0	2 blocks in Protected Area (0x20000 – 0x3FFFF)
1	1	1	3 blocks in Protected Area (0x10000 – 0x3FFFF)
TBSEL = 1			
BP2	**BP1**	**BP0**	**2Mb (4 blocks)**
0	0	0	None Protected Area
0	0	1	1 block in Protected Area (0x00000 – 0xFFFF)
0	1	0	2 blocks in Protected Area (0x00000 – 0x1FFFF)
0	1	1	3 blocks in Protected Area (0x00000 – 0x2FFFF)
1	0	0	4 blocks in Protected Area (0x00000 – 0x3FFFF)
1	0	1	
1	1	0	
1	1	1	

Table 5 2Mb HS4M3SC Block Memory Write Protection

TBSEL = 0			
BP2	**BP1**	**BP0**	**1Mb (2 blocks)**
0	0	0	None Protected Area
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	1 block in Protected Area (0x10000 – 0x1FFFF)
TBSEL = 1			
BP2	**BP1**	**BP0**	**1Mb (2 blocks)**
0	0	0	None Protected Area
0	0	1	1 block in Protected Area (0x00000 – 0xFFFF)
0	1	0	2 blocks in Protected Area (0x00000 – 0x1FFFF)
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 6 1Mb HS4M3SC Block Memory Write Protection

3.2 SR#2 Register

The state of bits 7, 4, 3, 2, 1 and 0 can be user modified. The state of bits 6 and 5 can be user modified but will affect memory normal operation.

The state of bits 4, 3, 2, 1 and 0 are used in memory array read latency (Dummy) selection.

When the state of bit 7 (SRLK) is set to 1, writes to TBSEL, BP2, BP1 and BP0 bits are protected.

DC4	DC3	DC2	DC1	DC0	Dummy Cycles	Max Read Frequency (MHz)	
0	0	0	0	0	0	50	Default
0	0	0	0	1	1	50	-
0	0	0	1	X	2~3	54	-
0	0	1	X	X	4~7	54	-
0	1	X	X	X	8~15	54	-
1	X	X	X	X	16~31	54	-

Table 7 Memory Array Read Latency Selection

4 Chip Functions

A typical SPI communications protocol consists of command, address and data components. Commands define the operation that must be executed. If the density of memory is 4Mb, the address range is 00000h – 7FFFFh, and the bit [18:0] of address is addressable. If the density of memory is 2Mb, the address range is 00000h – 3FFFFh, and the bit [17:0] of address is addressable. If the density of memory is 1Mb, the address range is 00000h – 1FFFFh, and the bit [16:0] of address is addressable. All command, address and data information is transferred sequentially. Instructions are structured as follows:

1. Each instruction begins with CE# going low (logic ‘0’) and ends with CE# returning high (logic ‘1’).
2. CLK marks the transfer of each bit.
3. The command can be stand alone or followed by address to select a memory location. The address is always 24-bits wide.
4. All commands, address and data are shifted with the most significant bit first.
5. Accept 16 kinds of command specified in opcode. Opcode is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If CE# is risen while inputting opcode, the command are not performed.

Instruction Name	Command(Opcode)						
	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7~
Write Status Register #1	WRSR 01h	S7-S0					
Read Status Register #1	RDSR 05h	S7-S0					
Write Status Register #2	WRSX 87h	S7-S0					
Read Status Register #2	RDSX 35h	S7-S0					
Write Memory Array	WRITE 02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	D7-D0
Read Memory Array	READ 03h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	D7-D0
Fast Read Memory Array	FSTRD 0Bh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	D7-D0
Write Enable	WREN 06h						
Write Disable	WRDI 04h						
Enter Sleep Mode	SLEEP B9h						
Exit Sleep Mode	WAKE ABh						
Read Unique ID	RUID 4Bh	ID87~ID0					
Read MANU ID	RMID 9Fh	ID7~ID0					
Read Device ID	RDID 90h	ID7~ID0					
Software Reset Enable	SRTE 66h						
Software Reset	SRST 99h						

Table 8 Chip Function Table

4.1 Control Instruation

Control instructions consist WREN, WRDI, SLEEP and WAKE.

The Write Enable (WREN) command sets the WREN bit in the status register #1 (bit 2). The WREN bit must be set prior to writing either bit in the status register or the memory. The WREN command is entered by driving CE# low, sending the command code, and then driving CE# high.

The Write Disable (WRDI) command resets the WREN bit in the status register #1 (bit 2) to 0.This prevents writes to status register or memory. The WRDI command is entered by driving CE# low, sending the command code, and then driving CE# high.

The Enter Sleep Mode (SLEEP) command turns off internal MRAM power regulators in order to reduce the overall chip power to 10μA typical. The SLEEP command is entered by driving CE# low, sending the command code, and then driving CE# high.

The Exit Sleep Mode (WAKE) command turns on internal MRAM power regulators to allow normal operation. The WAKE command is entered by driving CE# low, sending the command code, and then driving CE# high.

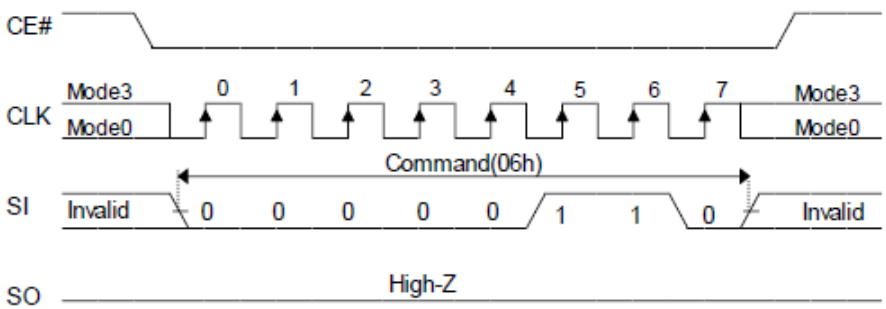


Figure 2 Enable (WREN) Timing

4.2 Reset Operation

If the Reset command is accepted, the device will return to its default power-on state and lose all the current volatile settings, such as Status Register bits.

The Reset command sequence as follow: CE# goes low -> Sending Software Reset Enable (SRTE) command -> CE# goes high -> CE# goes low -> Sending Software Reset (SRST) command -> CE# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST to reset. During this period, no command will be accepted.

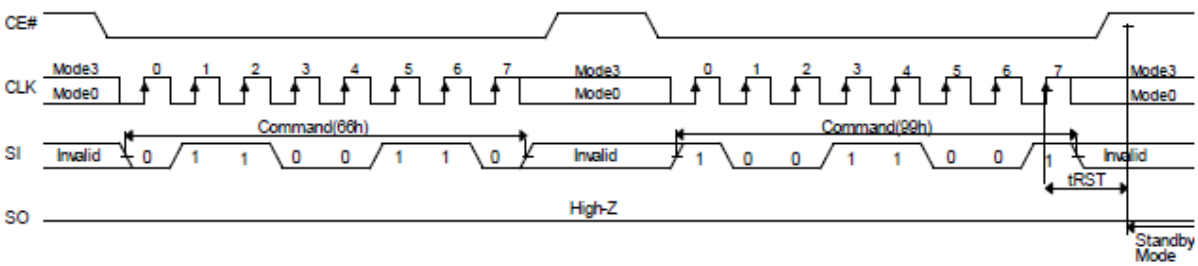


Figure 3 Software Reset Enable and Software Reset command Sequence Timing

4.3 Write SR Register Operation

The Write Status Register #1 (WRSR) command allows new values to be written to the Status Register #1. The Write Status Register #2 (WRSX) command allows new values to be written to the Status Register #2. The WRSR command and WRSX command are not executed unless the WREN bit has been set to 1 by executing a WREN command while pin WP# and the WP#EN bit correspond to values that make the Status Register #1 and #2 writable an seen in Table 3. Status Register bits are volatile upon power cycling.

The WREN bit is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. The bit 0 and bit 6 of the Status Register #1 are fixed to "0" and cannot be written. A SI value correspondent to bit 0 or bit 6 is ignored.

The WRSR command and WRSX command are entered by driving CE# low, sending the command code and status register write data byte, and then driving CE# high.

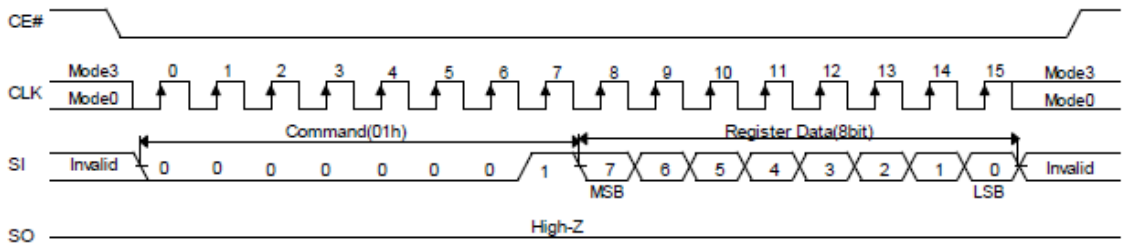


Figure 4 Write Status Register #1 (WRSR) Timing

4.4 Read SR Register Operation

The Read Status Register #1 (RDSR) command allows the Status Register #1 to be read.

The Read Status Register #2 (RDSX) command allows the Status Register #2 to be read.

The Status Register #1 can be read to check the status of WREN bit, WP#EN bit and block write protect bits.

The RDSR command and RDSX command are entered by driving CE# low, sending the command code, and then driving CE# high. After opcode of RDSR or RDSX is input to SI, 8-cycle clock is input to CLK. The SI value is invalid for this time. SO is output synchronously to a falling edge of CLK.

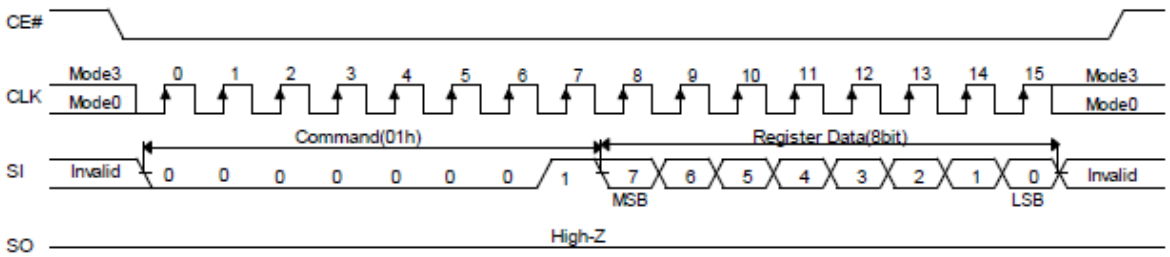


Figure 5. Read Status Register #1 (RDSR) Timing

4.5 Write Operations

The Write Memory Array (WRITE) command allows data bytes to be written starting at an address specified by the 24-bit address. The data bytes are written sequentially in memory until the write operation is terminated by bring CE# high. The entire memory can be written in a single command. The address counter will roll over to 0000H when the address reaches the top of memory.

MRAM can write data bytes continuously at its maximum rated clock speed without write delays or data polling. Back to back WRITE command to any random location in memory can be executed without write delay. MRAM is a random access memory rather than a page, sector, or block organized memory so it is ideal for both program and data storage.

The WRITE command is entered by driving CE# low, sending the command code, and then sequential write data bytes. Writes continue as long as the memory is clocked. The command is terminated by driving CE# high.

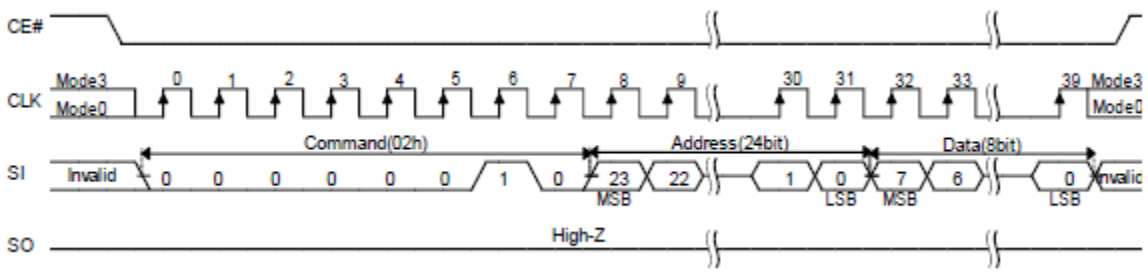


Figure 4 Write timing diagram

4.6 Normal Read Operation

The Read Memory Array (READ) command allows data bytes to be read starting at an address specified by the 24-bit address. The data bytes are read out sequentially from memory until the read operation is terminated by bring CE# high. The entire memory can be read in a single command. The address counter will roll over to 0000H when the address reaches the top of memory.

The READ command is entered by driving CE# low and sending the command code. The memory drives the read data bytes on the SO pin. SO is output synchronously to the falling edge of CLK. While reading, the SI value is invalid. Reads continue as long as the memory is clocked. The command is terminated by driving CE# high.

The Read Memory Array (READ) command can read data bytes continuously at its maximum rated clock speed (50MHz).

The Status Register #2 bit 4, 3, 2, 1, 0 must be reset to 0 prior to the Read Memory Array (READ) command. If a Read Memory Array (READ) command with the Status Register #2 bit 4, 3, 2, 1, 0 not be reset to 0, the output data will not be correct. The Status Register #2 bit 4, 3, 2, 1, 0 are reset to 0 by the following situation: Power-Up, Write Status Register #2 (WRSX) command.

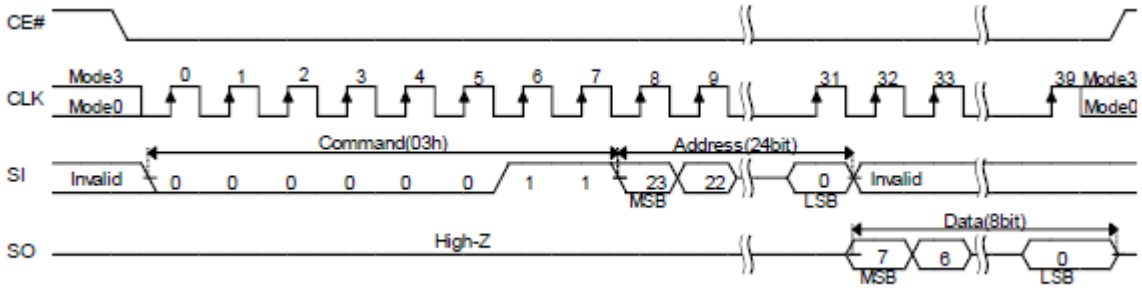


Figure 7 Read operation timing diagram

4.7 Fast Read Operation

The Fast Read Memory Array (FSTRD) command is for quickly reading data out. The Fast Read Memory Array (FSTRD) command reads MRAM memory cell array data. Arbitrary 24 bits address and opcode of FSTRD are input to SI followed by 0~31 bits dummy, each bit being latched- in during the rising edge of CLK. Then, 8-cycle clock is input to CLK. SO is output synchronously to the falling edge of CLK. While reading, the SI value is invalid. When CE# is risen, the FSTRD command is completed.

The entire memory array can be read from using a Fast Read Memory Array (FSTRD) command. After the starting address is entered, subsequent address are internally incremented as long as CE# is low and CLK continues to cycle. The first byte addressed can be at any location.

The Fast Read Memory Array (FSTRD) command consists latency cycles (dummy bits) to compensate for the memory array access time. The number of latency cycles (dummy bits) required depends on the operational frequency and is configurable - the Status Register #2 bit 4, 3, 2, 1 and 0. The latency cycles (dummy bits) are inserted after the address bits before the data comes out.

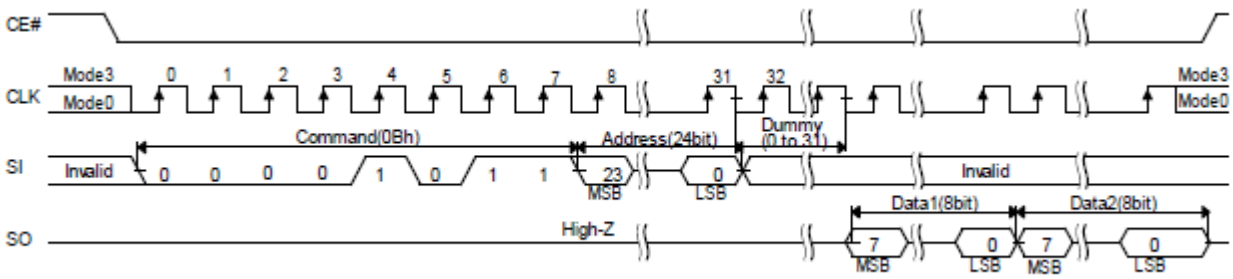


Figure 8 Fast Read operation timing diagram

4.8 Read Unique ID Operation

The Read Unique ID (RUID) command reads a unique ID which is defined in 88bits for each device. After performing the RUID opcode to SI, 88-cycle clock is input to CLK. The SI value is invalid for this time. SO is output synchronously to a falling edge of CLK. The Read Unique ID (RUID) command is terminated by driving CE# to the high at any time during data output. In the Read Unique ID (RUID) command, 88-bit Unique ID is output by continuously sending CLK clock, and SO holds the output state of the last bit until CE# is risen.

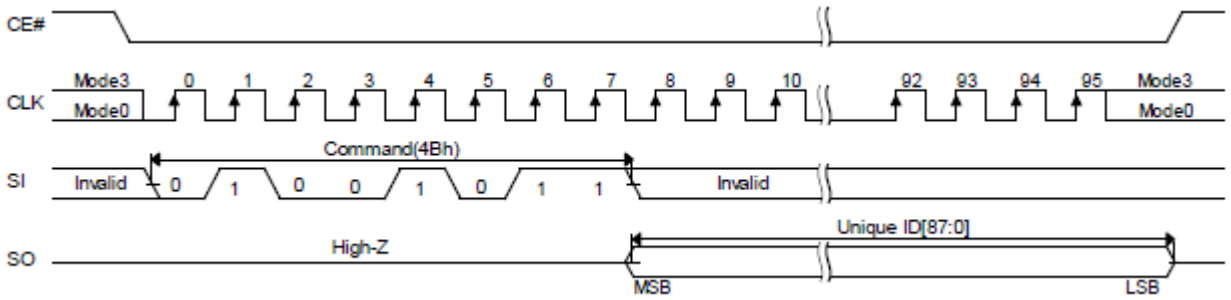


Figure 9 Read Unique ID operation timing diagram

4.9 Read Device ID Operation

The Read Device ID (RDID) command reads fixed Device ID. After performing the RDID opcode to SI, 8-cycle clock is input to CLK. The SI value is invalid for this time. SO is output synchronously to a falling edge of CLK. The output is in order of Product Grade ID (3bits)/Product Density ID (5bits). In the Read Device ID (RDID) command, 8-bit Device ID is output by continuously sending CLK clock, and SO holds the output state of the last bit until CE# is risen.

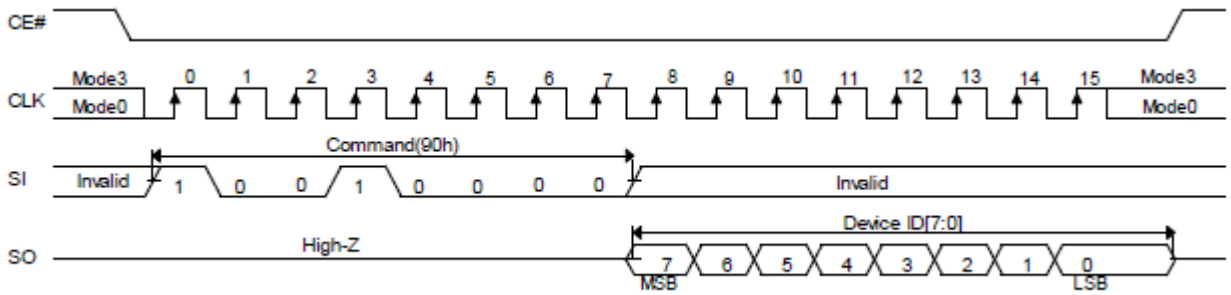


Figure 10 Read Device ID operation timing diagram

Device ID Value	Device ID Bit Assignments	
	7-5（3bits）	**4-0（5bits）**
	Product Grade ID	**Product Density ID**
29h	001（A）	01001（4Mb）
49h	010（B）	01001（4Mb）
69h	011（C）	01001（4Mb）
28h	001（A）	01000（2Mb）
48h	010（B）	01000（2Mb）
68h	011（C）	01000（2Mb）
27h	001（A）	00111（1Mb）
47h	010（B）	00111（1Mb）
67h	011（C）	00111（1Mb）

Table 9 Device ID

4.10 Read MANU ID Operation

The Read MANU ID (RMID) command reads fixed MANU ID. After performing the RMID opcode to SI, 8-cycle clock is input to CLK. The SI value is invalid for this time. SO is output synchronously to a falling edge of CLK. In the Read MANU ID (RMID) command, 8-bit MANU ID (26h) is output by continuously sending CLK clock, and SO holds the output state of the last bit until CE# is risen.

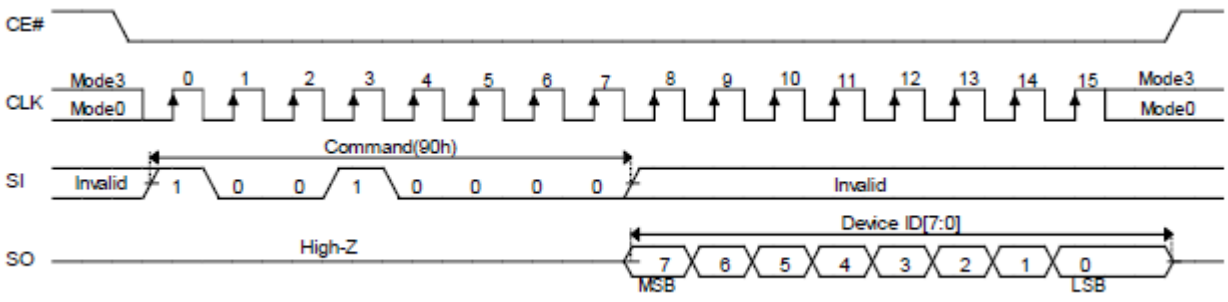


Figure 11 Read MANU ID timing diagram

4.11 Hold Operation

The HOLD# signal goes low to stop any serial communications with the device.

The operation of HOLD, need CE# keep low, and starts on falling edge of the HOLD# signal, with CLK signal being low (if CLK is not being low, HOLD operation will not start until CLK being low). The HOLD condition ends on rising edge of HOLD# signal with CLK being low (if CLK is not being low, HOLD operation will not end until CLK being low).

The SO is high impedance, both SI and CLK don't care during the HOLD operation, if CE# drives high during HOLD operation, it will reset the internal logic of the device. To restart communication with chip, the HOLD# pin must be at high and then CE# must be at low.

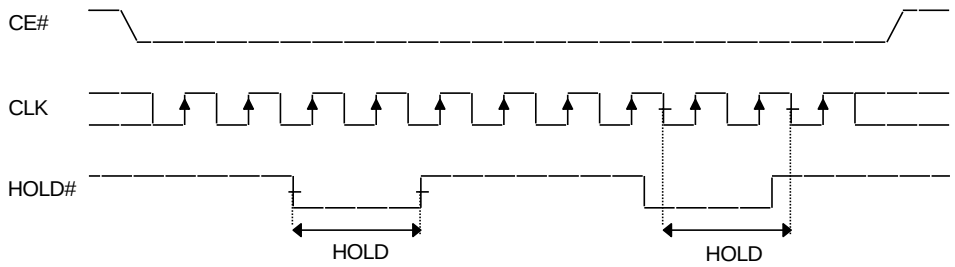


Figure 11. Hold timing operation

5 Device Mode

When CE# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so it can receive, decode and execute commands. But this mode is not the Sleep Mode. Executing the Enter Sleep Mode (SLEEP) command is the only way to put the device in the lowest consumption mode (the Sleep Mode).

Once the device has entered the Sleep Mode, all commands are ignored except the Exit Sleep Mode (WAKE) command, the Write Status Register #1 (WRSR) command and the Write Status Register #2 (WRSX) command. The Exit Sleep Mode (WAKE) command releases the device from this mode. The Write Status Register #1 (WRSR) command and the Write Status Register #2 (WRSX) command allow the Status Register #1 and the Status Register #2 of the device to be writeon SI.

The Sleep Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode.

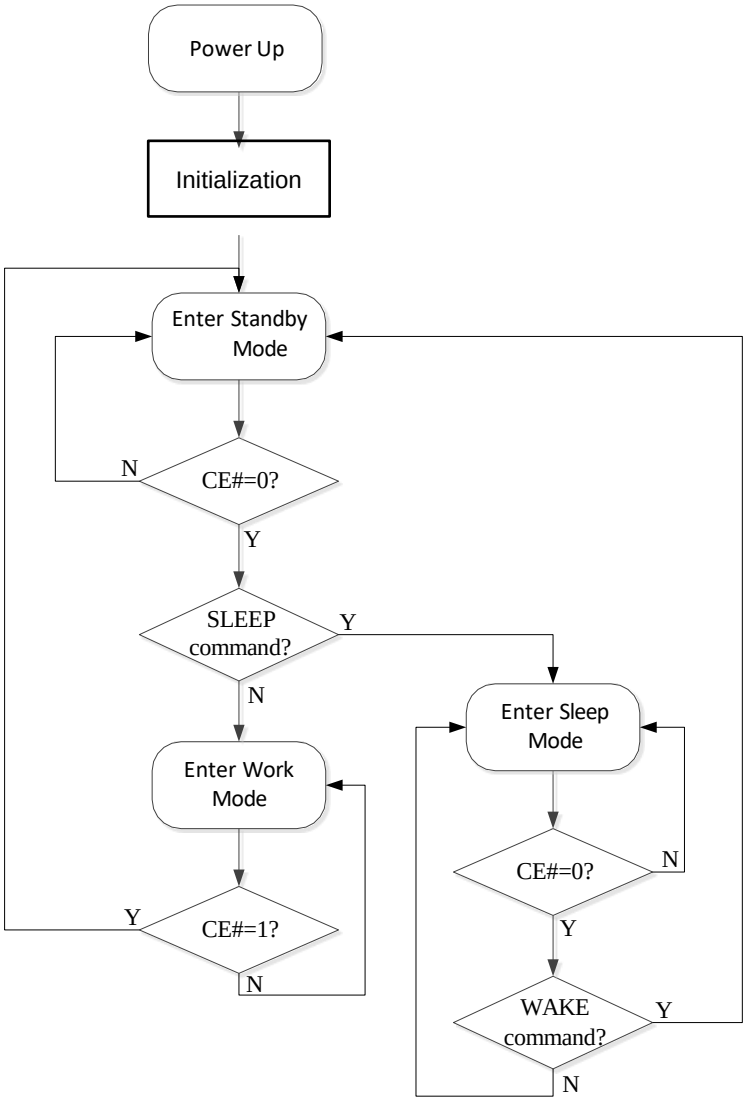


Figure 13 Device Modes Sequence

5.1 Enter Sleep Mode

The Enter Sleep Mode (SLEEP) command is entered by driving CE# low, followed by the command code on SI. CE# must be driven low for the entire duration of the sequence.

The Enter Sleep Mode (SLEEP) command sequence: CE# goes low -> sending Enter Sleep Mode (SLEEP) command -> CE# high. As soon as CE# is driven high, it requires a delay of tESLP before the supply current is reduced to ISLP and the Sleep Mode is entered. If power is removed when the device is in sleep mode, upon power restoration, the device enters normal standby mode. The only valid command following SLEEP mode entry is a WAKE command.

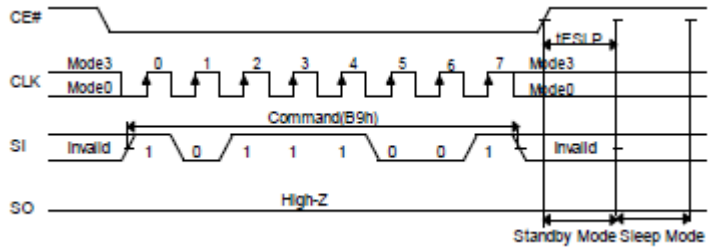


Figure 14 Enter Sleep Mode Timing

5.2 Exit Sleep Mode

To release the device from the Sleep Mode, the Exit Sleep Mode (WAKE) command is issued by driving the CE# pin low, shifting the instruction code “ABH” and driving CE# high as shown in Figure 15. The device returns to standby mode after tRSLP. The CE# pin must remain high until the tRSLP period is over. WAKE command must be executed after sleep mode entry and prior to any other command.

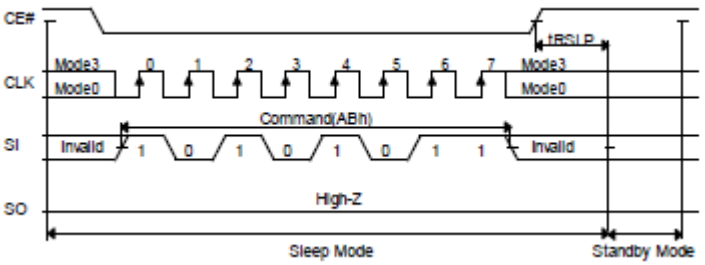


Figure 15 Exit Sleep Mode Timing

6 Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
VCC	Supply voltage		-0.5~4	V
V_{IN}	Voltage on any pin		-0.5~(VCC+0.5)	V
I_{OUT}	Output current per pin		±20	mA
T_{BIAS}	Temperature under bias	Industrial A Grade	-40~125	℃
		Industrial B Grade	-40~85	℃
		Industrial C Grade	-40~85	℃
T_{stg}	Storage Temperature		-55~150	℃
Hmax_write	Maximum magnetic field during write	Write	43000*	A/m
Hmax_read	Maximum magnetic field during read or standby	Read or Standby	46000*	A/m
Hmax_poweroff	Maximum magnetic field during power-off	Power-off	46000*	A/m

* The maximum magnetic field during write, read, and standby operations is measured when the magnetic field is applied perpendicular to the device's surface for a duration of 30 days. The device's diamagnetic performance is highly dependent on both the duration and direction of the magnetic field. For more detailed information on the device's diamagnetic characteristics, please refer to the Magnetic Field Environment Application Guide.

Table 10 Absolute Maximum Ratings

7 Electrical Characteristics

7.1 Operating Conditions

Symbol	Parameter		Min	Max	Unit
VCC	Power Supply voltage		2.7	3.6	V
T_A	Ambient temperature under bias	Industrial A	-40	125	℃
		Industrial B	-40	85	℃
		Industrial C	-40	85	℃

Table 11 Operating Conditions

7.2 DC Characteristics

Symbol	Parameter	Condition		Min	Typical	Max	Unit
$\|I_{LI}\|$	Input leakage current	0≦ CE# ＜VCC		-	-	140	µA
		CE# = VCC		-	-	1	µA
		WP#, HOLD#, CLK, SI = 0V~VCC		-	-	1	µA
$\|I_{LO}\|$	Output leakage current	SO = 0V~VCC		-	-	1	µA
I_{SLP}	Sleep current	CE# = VCC All inputs VSS or VCC		-	10	145	µA
I_{SBY}	Standby current	CLK = SI = CE# = VCC		-	100	5600	µA
I_{CC}	Operating current	Write	CLK = 1MHz	-	4	8	mA
			CLK = 40MHz	-	5	9	mA
			CLK = 54MHz	-	6	10	mA
		Read	CLK = 1MHz	-	2	6	mA
			CLK = 40MHz	-	3	7	mA
			CLK = 54MHz	-	4	8	mA
V_{IL}	Input low voltage	VCC = 2.7V~3.6V		-0.3	-	0.8	V
V_{IH}	Input high voltage	VCC = 2.7V~3.6V		VCC-0.4	-	VCC+0.3	V
V_{OL}	Output low voltage	I_{OL} = 3.1mA		-	-	0.2VCC	V
V_{OH}	Output high voltage	I_{OH} = -3.1mA		0.8VCC	-	-	V

Table 12 DC Characteristics

7.3 Pin Capacitance

Symbol	Parameter	Typical	Max
C_P	VCC/VSS power external capacitance	-	10μF+0.1nF
C_{IN}	Control input capacitance	-	8pF
C_{IO}	Input or output capacitance	-	12pF

Table 13 Pin Capacitance

7.4 AC Characteristics

Parameter	Value	Unit
Power supply voltage	2.7~3.6	V
Operation ambient temperature	-40~125（Industrial A） -40~85（Industrial B） -40~85（Industrial C）	℃
Input voltage magnitude	VCC - 0.4 ≤ V_{IH} ≤ VCC + 0.3 0 ≤ V_{IL} ≤ 0.8	V
Input rising time	2	ns
Input falling time	2	ns
Input judge level	VCC/2	V
Output judge level	VCC/2	V
Output Load	30	pF

Table 14 AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
f_{CLK}	CLK clock frequency for: READ(03h)	0	50	MHz
	CLK clock frequency for other command	0	54	MHz
t_{CH}/t_{CL}	CLK high/low time	9	-	ns
t_{CPH}	CE# high time	100	-	ns
t_{CSP}	CE# setup time	10	-	ns
t_{CHD}	CE# hold time	10	-	ns
t_{SP}	Data in setup time	2	-	ns
t_{HD}	Data in hold time	5	-	ns
t_{HZ}	Output disable time	-	6	ns
t_{ACLK}	Output data valid time for: READ(03h)	-	10	ns
	Output data valid time for other read operation	-	9	ns
t_{KOH}	Output hold time	4	-	ns
t_{RST}	Software reset time	500	-	µs
t_{ESLP}	Sleep mode entry time	-	10	µs
t_{RSLP}	Sleep mode exit time	550	-	µs
t_{SH}	HOLD# setup time	10	-	ns
t_{HH}	HOLD# hold time	10	-	ns
t_{HHZ}	HOLD# to output high impedance time	-	20	ns
t_{HLZ}	HOLD# to output low impedance time	-	20	ns

Table 14 AC Characteristics

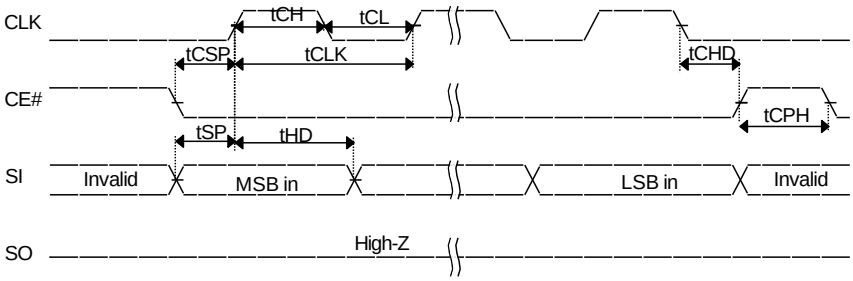


Figure 16 Serial Input Timing

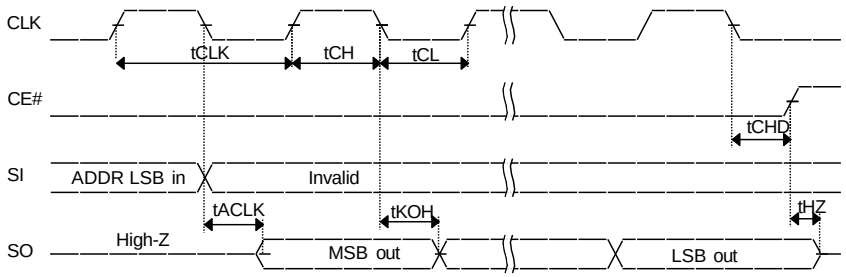


Figure 17 Serial Output Timing

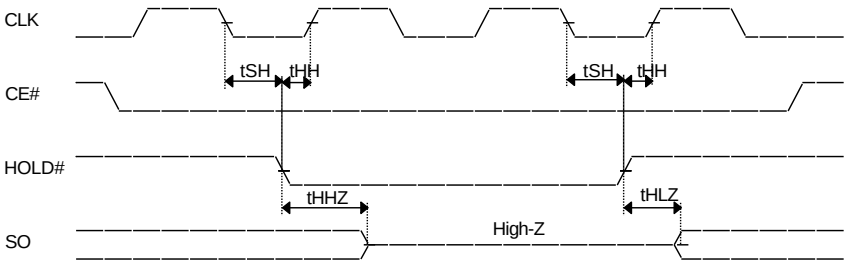


Figure 18 HOLD# Timing1

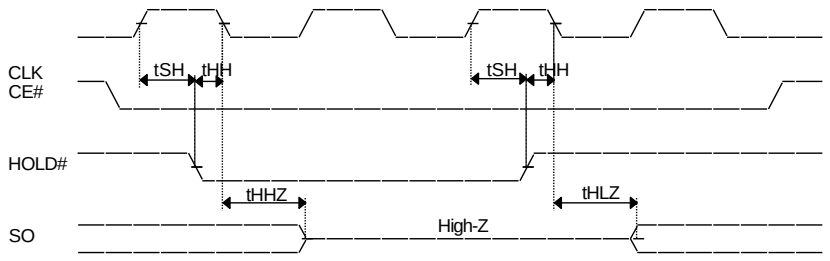


Figure 19 HOLD# Timing2

7.5 Power-Up Timing

The HSxM3SC is not accessible for a start-up time, tPU after power up. Users must wait this time from the time when VCC(min) is reached until the first CE# low to allow internal voltage references to become stable. The CE# signal should be pulled up to VCC so that the signal tracks the power supply during power-up sequence.

VCC(min) means VCC (minimum) and VCC(max) means VCC (maximum). Please refer to the Table 11.

Symbol	Parameter	Min	Max	Unit
V_{CI}	Write Inhibit Voltage	2.35	-	V
t_{PU}	Startup Time	500	-	µs

Table 16 16 Power-Up Timing

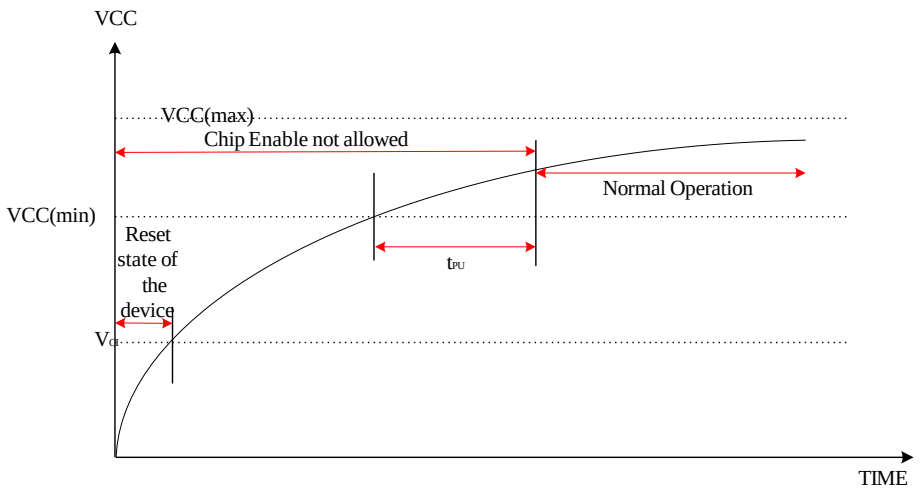
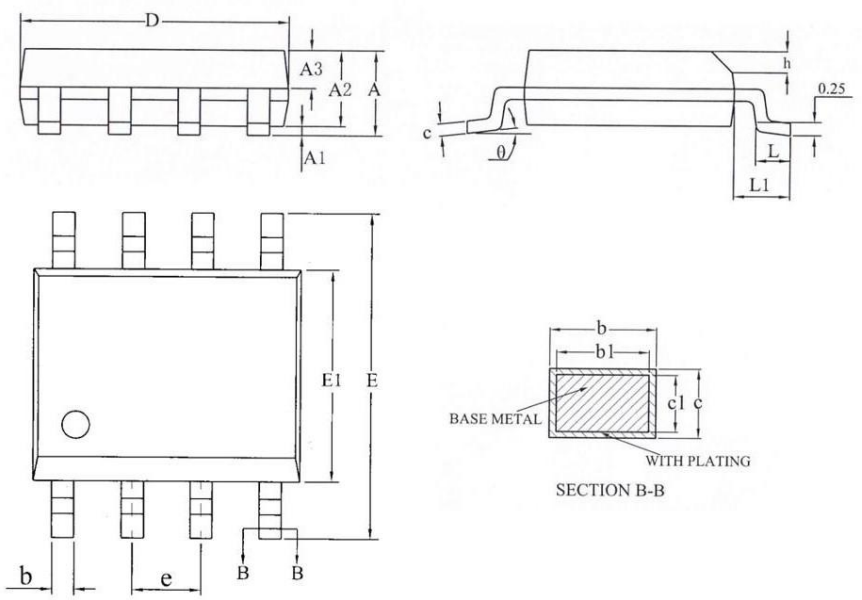


Figure 20 Power-Up Timing

8 Usage Instructions

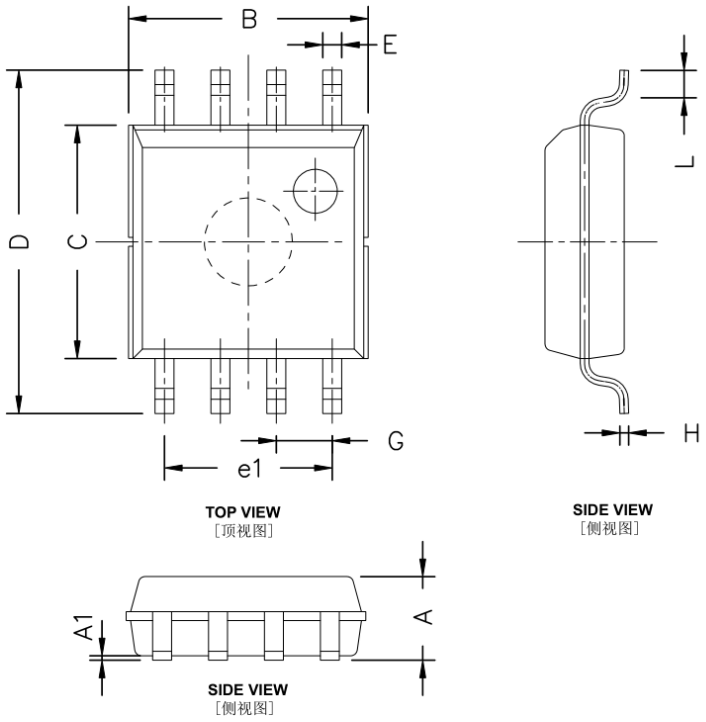
It is recommended that users program the chip after reflow soldering, because the chip cannot guarantee that the data written before reflow soldering will still be valid after reflow soldering.

9 Package Outline



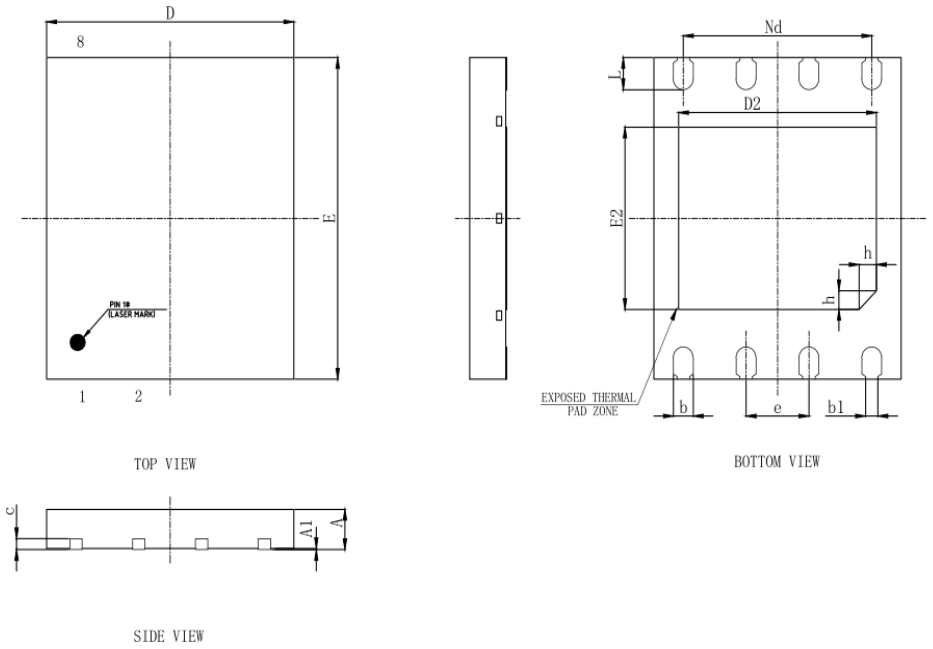
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 21 SOP8 150mil Package Outline



编号	尺寸（mm）		
	Min	TYP	Max
A	1.800	2.000	2.200
A1	0.050	0.150	0.250
B	5.100	5.400	5.700
C	5.000	5.300	5.600
D	7.400	7.800	8.200
G	1.270TYPE		
E	0.350	0.430	0.510
H	0.100	0.200	0.300
L	0.750TYPE		

Figure 22 SOP8 208mil Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.35	0.40	0.45
b1	0. 25REF		
c	0.18	0.203	0.25
D	4.90	5.00	5.10
Nd	3.81 BSC		
e	1.27 BSC		
E	5.90	6.00	6.10
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
L	0.55	0.60	0.65
h	0.30	0.35	0.40
L/F载体尺寸			

Figure 23 DFN8 (5mmx6mm) Package Outline

10. Product naming Rules

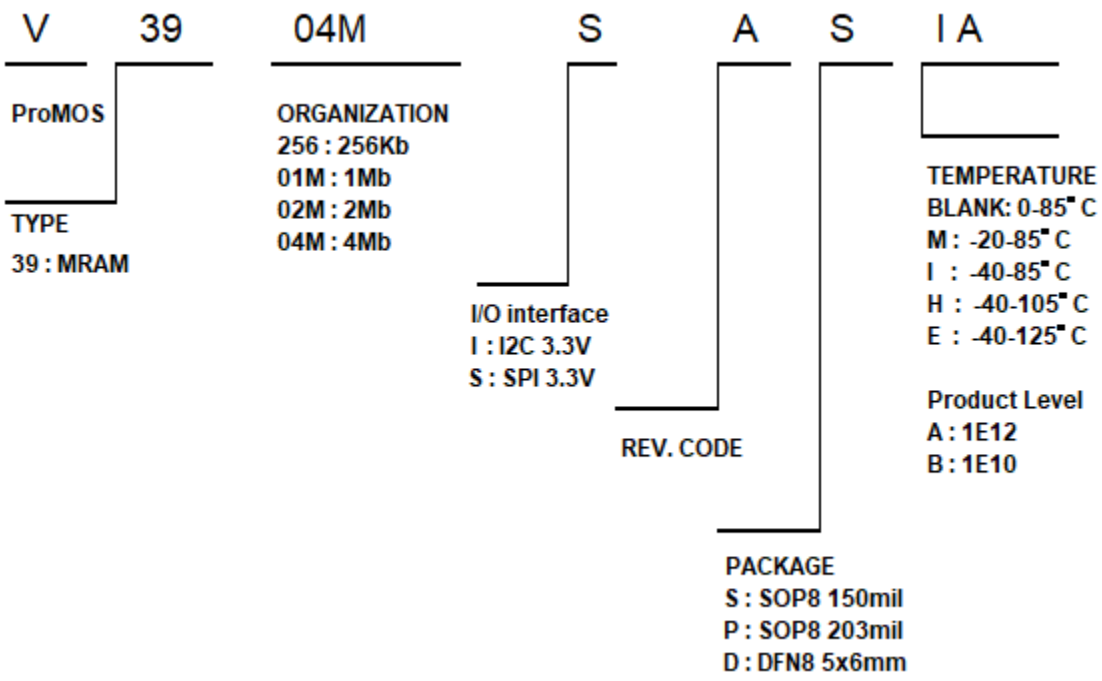


Figure 24 Naming rule description