V390416VAT
4M Bit Parallel STT-MRAM

Preliminary

The V390416VAT chip utilizes advanced pMTJ STT-MRAM technology and is a non-volatile MRAM device with an ASRAM interface. This device provides a parallel bus, offers read and write cycles up to 35ns, and boasts excellent reliability with over 10 years of data retention. The chip also features low-voltage write protection to prevent accidental data writes.

The V39C304161VAT35 chip offers the following key features:

- Capacity
  - · 4Mbit
- Asynchronous interface supporting 16/8-bit data addressing
  - · Read and write cycles up to 35ns
  - · 16-bit I/O with support for UBN/LBN switching
- Operating Voltage
  - · Standard voltage: Single VDD 3.3V
- Operating Temperature
  - · -40˚C to 125˚C
- Data Protection
  - · Data write protection is enabled when the voltage drops below 2.5V (typical)
- Power Consumption
  - · Static Power Consumption 1.7mA (typical)
  - · Dynamic Power Consumption Read Operation 20mA (typical)
  - · Dynamic Power Consumption Write Operation 35mA (typical)
- Reliability
  - · Maximum Erase/Write Endurance 1E12
  - · Retention ≥10 years @ 125˚C
- Package
  - · 44-Pin TSOP II

Table of Content

2. Logic Block Diagram

This chip implements an asynchronous data interface through five control signals: CEN, WEN, UBN, LBN, and OEN. The chip's logic block diagram is shown in Figure 1.

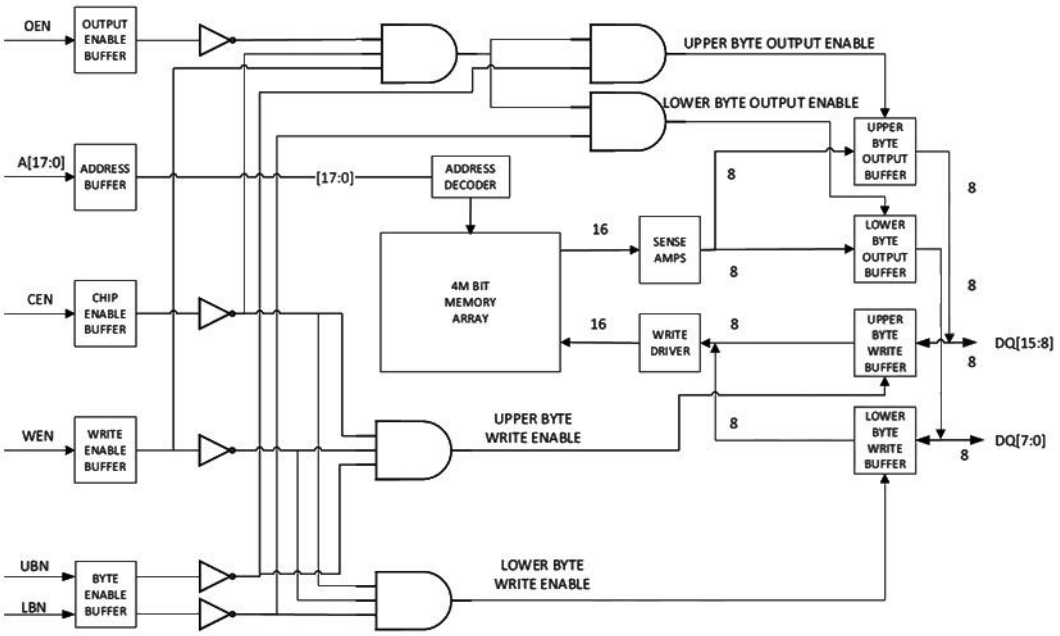


Figure 1 Chip block diagram

3. Packaging Information

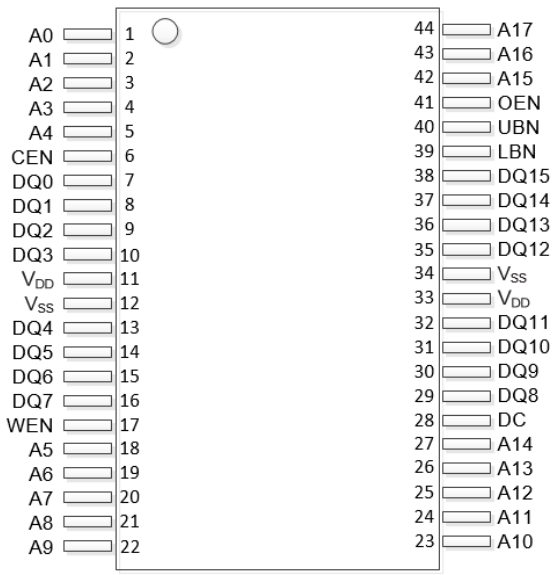


Figure 2 44-Pin TSOP II

4. Pin Descriptions

Interface	Interface Type	Interface Description
A	Input	Input Address Bit
CEN	Input	Chip Select Signal, Active Low
WEN	Input	Write Enable Signal, Active Low
OEN	Input	Output Data Enable Signal, Active Low
UBN	Input	High BYTE Enable Signal, Active Low
LBN	Input	Low BYTE Enable Signal, Active Low
DQ	Input / Output	Parallel Data Input/Output Pin
V_{DD}	-	Power Supply
V_{SS}	-	Ground

Table 1 Pin Descriptions

5. Operation Modes

CEN	OEN	WEN	UBN	LBN	Mode	VDD current	DQ[7:0]	DQ[15:8]
H	X	X	X	X	Unselected	I_{SB1}	Hi-Z	Hi-Z
L	H	H	X	X	Output Disable	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output Disable	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Low Byte read	I_{DDR}	Dout	Hi-Z
L	L	H	H	L	High Byte read	I_{DDR}	Hi-Z	Dout
L	L	H	L	L	16-bit read	I_{DDR}	Dout	Dout
L	X	L	L	H	Low Byte write	I_{DDW}	Din	Hi-Z
L	X	L	H	L	High Byte write	I_{DDW}	Hi-Z	Din
L	X	L	L	L	16-bit Write	I_{DDW}	Din	Din

Table 2 Operation Modes

Notes:
1. H = 1, L = 0, X = Don't Care state
2. Hi-Z = High Impedance state

6. Power-on/Power-off Characteristics

When V_{DD} is less than V_{WI}, the chip enters a write-protected state, preventing users from successfully writing data. After V_{DD} exceeds $V_{DD(min)}$, a 2ms power-up time (power stabilization time) is required before read and write operations can be performed. During power-up, the CEN and WEN signals should rise to V_{DD}-0.2V or V_{IH} (whichever is lower) along with V_{DD} and remain high during the power-up time. In most systems, the CEN and WEN pins can be pulled up with resistors to ensure they remain high even when the drive signals are in a high-impedance state at power-up. The CEN and WEN pins should remain high during a power-on reset and for a duration longer than the power-up time. If V_{DD} drops below V_{WI} due to power failure or voltage fluctuations, write operations are prohibited. When power is restored and V_{DD} exceeds $V_{DD(min)}$, the power-up time must be waited for.

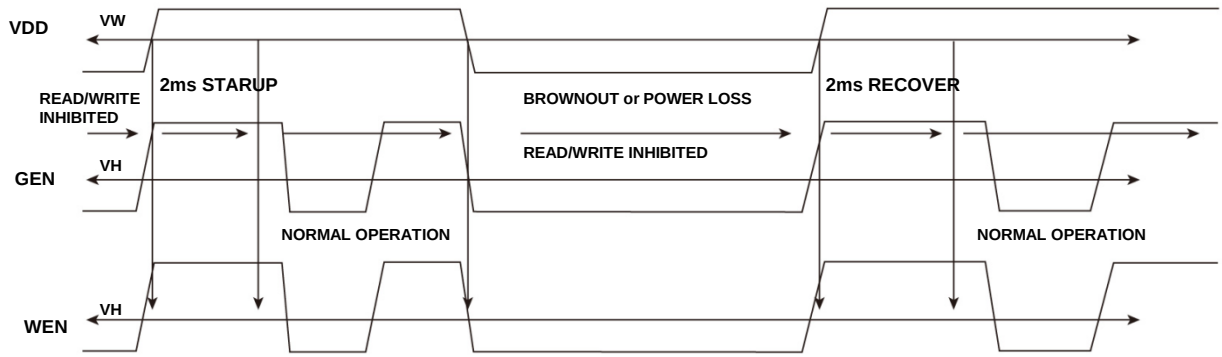


Figure 3 Power-on and Power-off timing diagram

7. Chip Functions

7.1 AC Characteristics Test Conditions

Parameter	Value	Unit
Reference level of Logic input timing measurement	1.5	V
Reference level of Logic output timing measurement	1.5	V
Logic input pulse level	0 or 3.0	V
Input rise/fall time	2	ns
Output load for Low-impedance and High-impedance	See Figure 4	
Output load for all other timing parameters	See Figure 5	

Table 3 AC characteristic test conditions

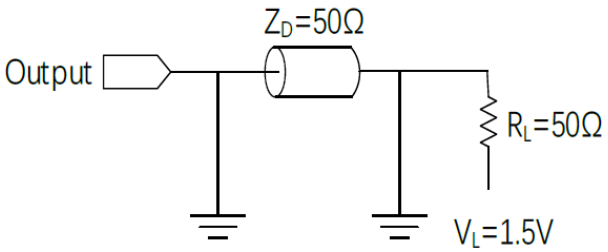


Figure 4 Output load test (for low impedance and high impedance parameters)

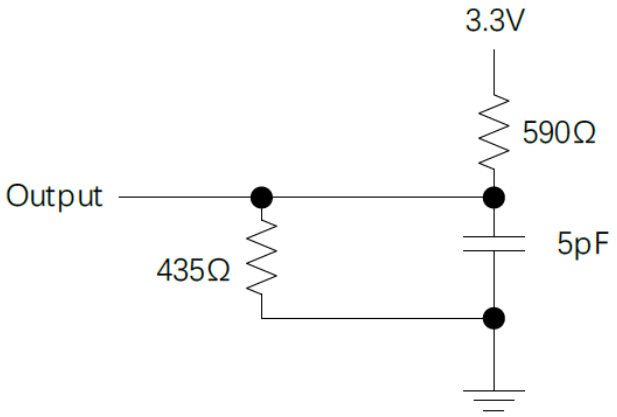


Figure 5 Output load test (for all others)

7.2 Write Mode

Symbol	Parameter	Min.	Max.	Unit
t_{AVAV}	Write cycle time (*2)	35	-	ns
t_{AVWL}	Address creation time	0	-	ns
t_{AVWH}	Address valid until write completes (OEN high)	18	-	ns
t_{AVWH}	Address valid until write completes (OEN low)	20	-	ns
t_{WLWH} t_{WLEH}	Write pulse width (OEN high)	15	-	ns
t_{WLWH} t_{WLEH}	Write pulse width (OEN low)	15	-	ns
t_{DVWH}	Data is valid until the write is completed	10	-	ns
t_{WHDX}	Data retention time	0	-	ns
t_{WLQZ}	WEN low to data Hi-Z (*3)	0	12	ns
t_{WHQX}	WEN high to output active (*3)	3	-	ns
t_{WHAX}	Write recovery time	12	-	ns

Table 4 Write cycle timing 1 (WEN control) (*1)

Note :

*1. All write operations occur during the overlap between CEN low and WEN low. Power supplies must be properly grounded and decoupled, and bus contention must be reduced or eliminated during read and write cycles. If OEN is pulled low during a write cycle, to reduce bus contention, OEN must be pulled low at the same time WEN is low or begins to go low, at least 2ns before WEN is pulled high. Pulling OEN low during WEN high will increase power consumption due to bus contention. The minimum time between CEN low in one cycle and CEN low in the next cycle must be equal to the minimum cycle allowed by the chip.

*2. All write cycle times are calculated from the arrival of the last address bit to the transition time of the first address bit.

*3. This parameter is a sample test, not a 100% device test. Signal transitions are measured within a ±200 mV range of the steady-state voltage. At any given voltage or temperature, tWLQZ (max) < tWHQX (min).The V39C304161VAT35 chip utilizes advanced pMTJ STT-MRAM technology and is a non-volatile MRAM device with an ASRAM interface. This device provides a parallel bus, offers read and write cycles up to 35ns, and boasts excellent reliability with over 10 years of data retention. The chip also features low-voltage write protection to prevent accidental data writes.

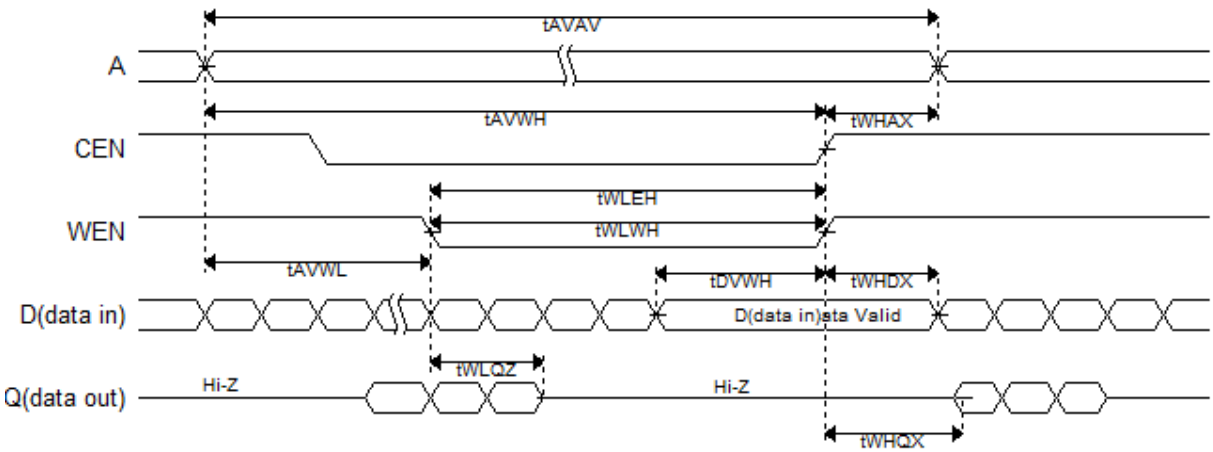


Figure 6 Write cycle timing 1 (WEN control)

Symbol	Parameter	Min.	Max.	Unit
t_{AVAV}	Write cycle time (*2)	35	-	ns
t_{AVEL}	Address creation time	0	-	ns
t_{AVEH}	Address valid until write completes (OEN high)	18	-	ns
t_{AVEH}	Address valid until write completes (OEN low)	20	-	ns
t_{ELEH} t_{ELWH}	Write pulse width (OEN high)	15	-	ns
t_{ELEH} t_{ELWH}	Write pulse width (OEN low) (*3)	15	-	ns
t_{DVEH}	Data is valid until the write is completed	10	-	ns
t_{EHDX}	Data retention time	0	-	ns
t_{EHAX}	Write recovery time	12	-	ns

Table 5 Write cycle timing 2 (CEN control) *1

Note :

*1. All write operations occur during the overlap between CEN low and WEN low. Power supplies must be properly grounded and decoupled, and bus contention must be reduced or eliminated during read and write cycles. If OEN is pulled low during a write cycle, to reduce bus contention, OEN must be pulled low at the same time WEN goes low or begins to go low, at least 2ns before WEN goes high. Pulling OEN low during WEN high will increase power consumption due to bus contention. The minimum time between CEN low in one cycle and CEN low in the next cycle must be equal to the minimum cycle time allowed by the chip.

*2. All write cycle times are calculated from the arrival of the last address bit to the transition time of the first address bit.

*3. If CEN goes low at the same time as WEN goes low or begins to go low, the outputs will remain in a high-impedance state. If CEN goes high before or at the same time as WEN goes high, the outputs will remain in a high-impedance state.

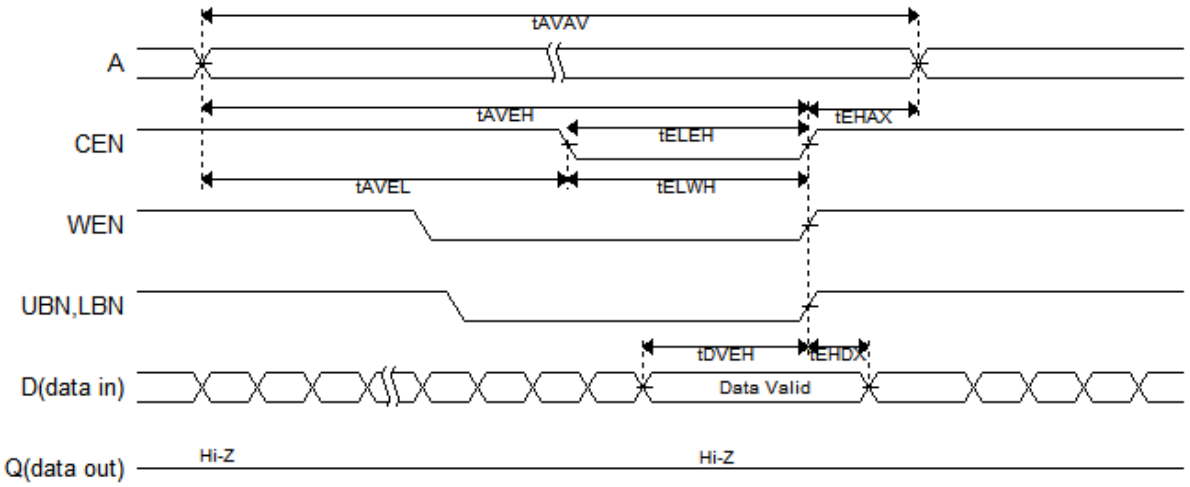


Figure 7 Write cycle timing 2 (CEN control)

Symbol	Parameter	Min.	Max.	Unit
tAVAV	Write cycle time (*2)	35	-	ns
tAVBL	Address creation time	0	-	ns
tAVBH	Address valid until write completes (OEN high)	18	-	ns
tAVBH	Address valid until write completes (OEN low)	20	-	ns
tBLEH tBLWH	Write pulse width (OEN high)	15	-	ns
tBLEH tBLWH	Write pulse width (OEN low)	15	-	ns
tDVBH	Data is valid until the write is completed	10	-	ns
tBHDX	Data retention time	0	-	ns
tBHAX	Write recovery time	12	-	ns

Table 6 Write cycle timing 3 (LBN/UBN control) (*1)

Note :

*1. All write operations must occur during the overlap between CEN low and WEN low. Power supplies must be properly grounded and decoupled, and bus contention must be reduced or eliminated during read and write cycles. If OEN is pulled low during a write cycle, to reduce bus contention, OEN must be pulled low at the same time WEN is low or begins to go low, at least 2ns before WEN goes high. Pulling OEN low during WEN high will increase power consumption due to bus contention. When both UBN and LBN are active, ensure that the skew between the two signals is less than 2ns. The minimum time between CEN low in one cycle and CEN low in the next cycle must be equal to the minimum cycle allowed by the chip.

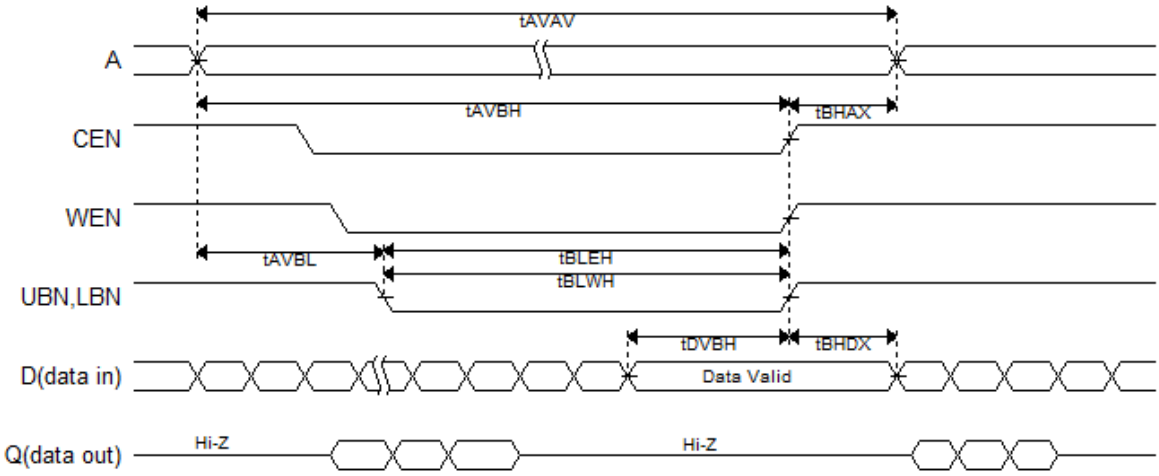


Figure 8 Write cycle timing 3 (LBN/UBN control)

7.3 Read Mode

Symbol	Parameter	Min.	Max.	Unit
t_{AVAV}	Read cycle time	35	-	ns
t_{AVQV}	Address access time	-	35	ns
t_{ELQV}	Enable access time (*2)	-	35	ns
t_{GLQV}	Output enable access time	-	15	ns
t_{BLQV}	Byte enable access time	-	15	ns
t_{AXQX}	Output hold after address change	3	-	ns
t_{ELQX}	Enable low level to output active (*3)	3	-	ns
t_{GLQV}	Output enable low to output active	0	-	ns
t_{BLQX}	Byte enable low to output active	0	-	ns
t_{EHQZ}	Enable high level to output Hi-Z (*3)	0	15	ns
t_{GHQZ}	Output enable high level to output Hi-Z (*3)	0	10	ns
t_{BHQZ}	Byte high level to output Hi-Z*3	0	10	ns

Table 7 Read cycle timing (*1)

Note :

*1. During a read cycle, WEN must be high. Power supplies must be properly grounded and decoupled, and bus contention must be reduced or eliminated during read and write cycles.

*2. The address is valid before CEN is low or goes low.

*3. This parameter is a sample test and not a 100% device test. Signal transitions are measured within a ±200 mV range based on steady-state voltage.

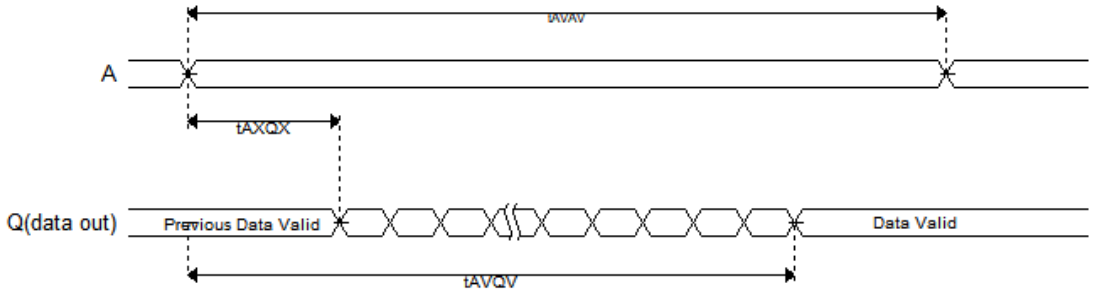


Figure 9 Read cycle timing 1

Note: The device is continuously selected (CEN ≤ V_{IL}, OEN ≤ V_{IL})

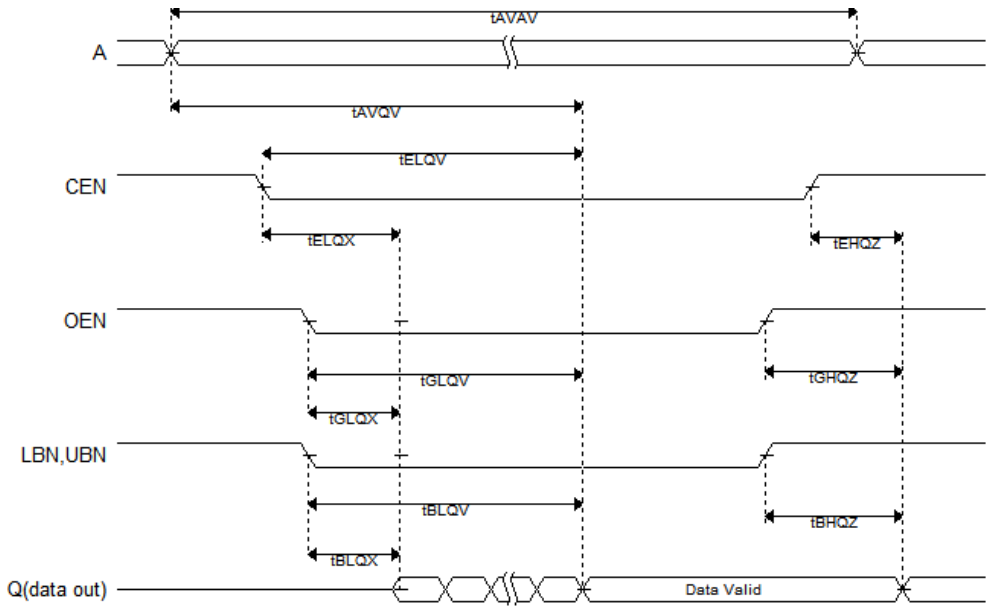


Figure 10 Read cycle timing 2

8. Absolute Operating Conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage (*1)	-0.5 to 4.0	V
V_{IN}	Any pin voltage (*1)	-0.5 to V_{DD}+ 0.5	V
I_{OUT}	Output current per pin	±20	mA
P_D	Package power consumption (*2)	0.6	W
T_{BIAS}	Bias temperature	-40 to 125	℃
Tstg	Storage temperature	-55 to 150	℃
T_{Lead}	Pin soldering temperature (up to 3 minutes)	260	℃
Hmax_write	Maximum magnetic field during writing (*3)	18000	A/m
Hmax_read	Maximum magnetic field during reading or standby (*3)	50000	A/m

Table 8 Extreme working conditions

Note :

*1. All voltages are referenced to V_{SS}.

*2. Power consumption depends on package characteristics and operating environment.

*3. Maximum magnetic field values during write, read, and standby are measured with the magnetic field perpendicular to the chip surface and for 30 days. Chip magnetic resistance is closely related to magnetic field duration and direction. Please refer to the Magnetic Field Environment Application Guide for more detailed chip magnetic resistance information.

9. Electrical Characteristics

9.1. Working Conditions

Symbol	Parameter	Min.	Typical	Max.	Unit
V_{DD}	Supply voltage (*1)	2.7	3.3	3.6	V
T_A	Temperature	-40	-	125	℃
V_{WT}	Write inhibit voltage	2.4	2.5	2.7	V

Table 9 Working conditions

Note :
*1. All voltages are referenced to V_{SS}.

9.2. Pin Capacitance

Symbol	Parameter	Typical	Max.	Unit
C_{Ina}	Address input capacitance	-	6	pF
C_{Inc}	Control input capacitance	-	6	pF
$C_{I/O}$	Input/output capacitors	-	8	pF

Table 10 Pin capacitance

Note : f=1.0MHz, dV=3.0V, TA=25℃. Sampling test, not full test.

9.3. DC Characteristics

Symbol	Parameter	Test condition	Min.	Typical	Max.	Unit
$\|I_{LI}\|$	Input leakage current	Vin = 0 Vin = V_{DD} (max)	-	-	±1	µA
$\|I_{LO}\|$	Output leakage current	Vout = 0 Vout = V_{DD} (max)	-	-	±1	µA
V_{IH}	Input high level	-	2.2	-	V_{DD}+0.3	V
V_{IL}	Input low level	-	-0.5	-	0.8	V
V_{OH}	Output high level	I_{OH} = -4 mA I_{OH} = -100 uA	2.4 V_{DD}-0.2			V
V_{OL}	Output low level	I_{OL} = +4 mA I_{OL} = +100 uA			0.4 V_{ss}+0.2	V
I_{DDR}	Read current (*1)	I_{OUT} = 0 mA V_{DD} = max	-	20	-	mA
I_{DDW}	Write current (*2)	V_{DD} = max	-	35	-	mA
I_{SB1}	Standby current	V_{DD} = max , CEN = V_{DD} , Other pins have fixed levels	-	1.7	-	mA

Table 11 DC characteristics

Note :

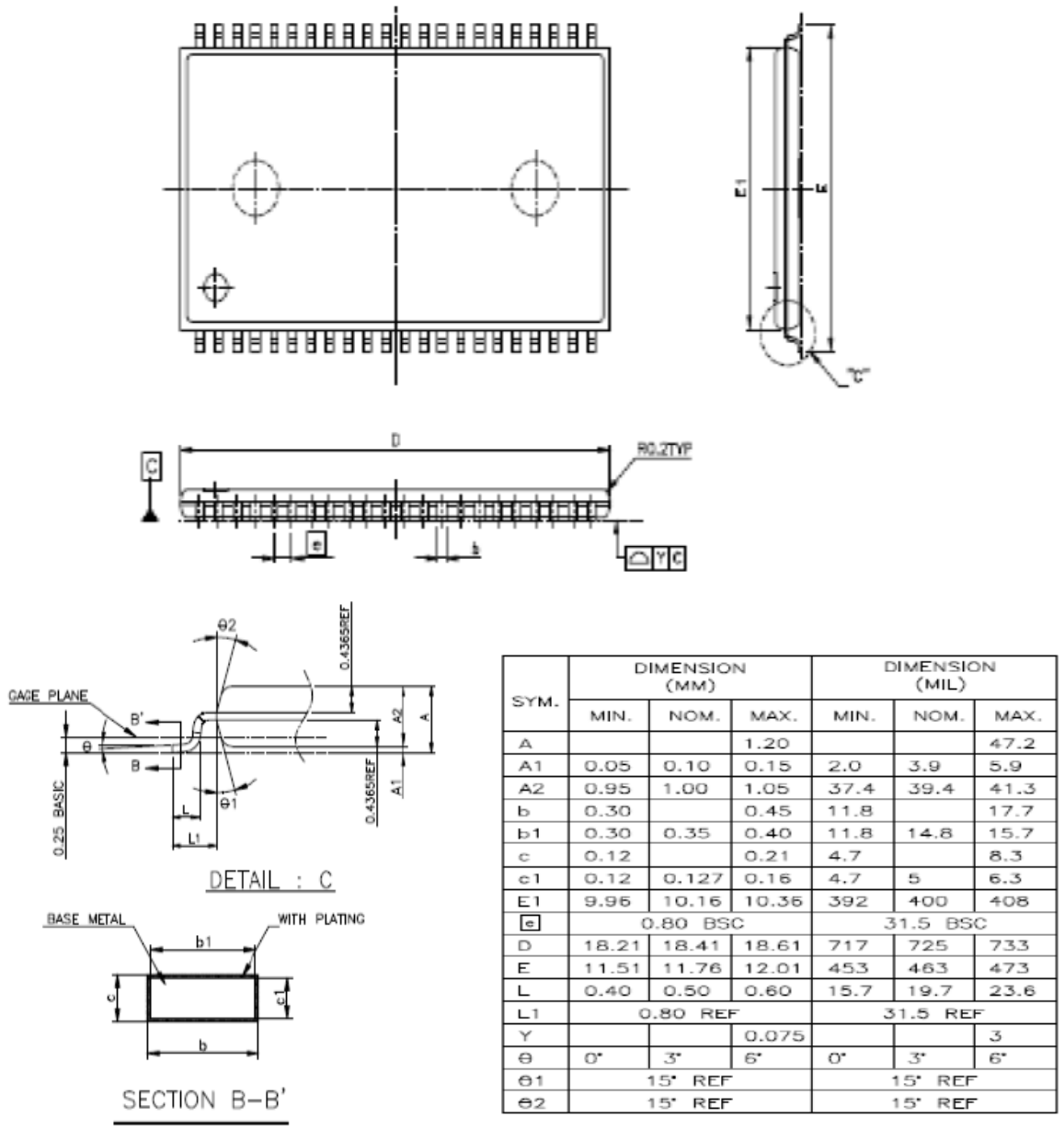
*1. Read power consumption is measured under the condition of the shortest read cycle 35ns.

*2. Write power consumption is measured under the conditions of the shortest write cycle of 35ns and the shortest write pulse width of 15ns. As the proportion of write pulse width to write cycle increases, write power consumption will increase.

10. Precautions for Use

It is recommended that users program the chip after reflow soldering, because the chip cannot guarantee that the data written before reflow soldering will still be valid after reflow soldering.

11. Package Outline



SYM.	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30		0.45	11.8		17.7
b1	0.30	0.35	0.40	11.8	14.8	15.7
c	0.12		0.21	4.7		8.3
c1	0.12	0.127	0.16	4.7	5	6.3
E1	9.96	10.16	10.36	392	400	408
e	0.80 BSC			31.5 BSC		
D	18.21	18.41	18.61	717	725	733
E	11.51	11.76	12.01	453	463	473
L	0.40	0.50	0.60	15.7	19.7	23.6
L1	0.80 REF			31.5 REF		
Y			0.075			3
θ	0°	3°	6°	0°	3°	6°
θ1	15° REF			15° REF		
θ2	15° REF			15° REF		

Figure 11 Package outline

11. Product Naming Rules

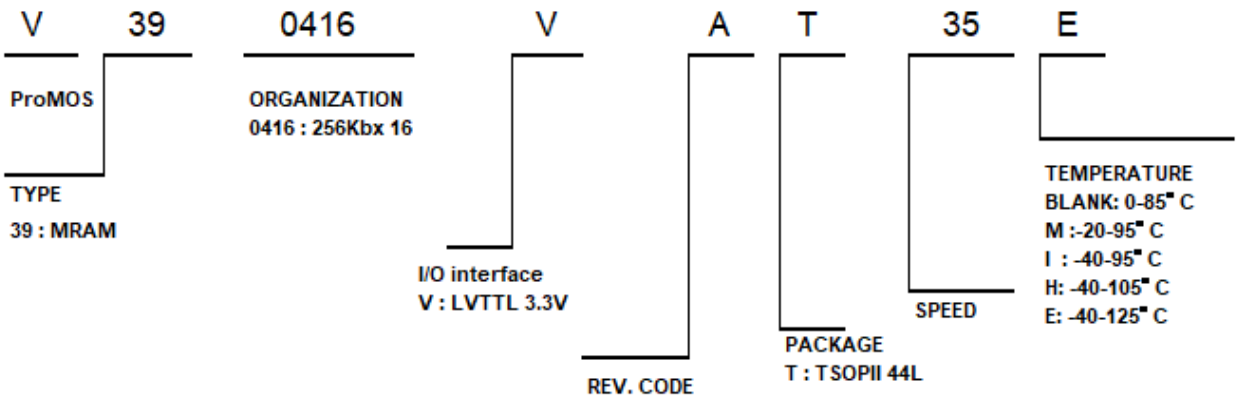


Figure 12 Naming rules description