V39256IAS
256K Bit Serial MRAM

Preliminary

1. Product Overview

The V39256IAS a 256Kb I2C interface non-volatile memory chip. Utilizing advanced pMTJ STT-MRAM technology, it achieves read and write speed up to 500kHz, offering exceptional reliability and over 20 years of data retention.

The HS256K3CD chip offers the following key features:

- pMTJ STT-MRAM technology
  - STT process
  - 256Kb capacity
- I2C Interface
  - Supports standard mode (100kHz) and fast mode (500kHz)
  - Schmitt triggers and noise suppression filters for SDA and SCL
  - Fast write time (100ns min)
- Operating Voltage
  - Standard voltage: single VCC 2.7-3.6V
- Operating Temperature
  - 40˚C to 85˚C
- Data Protection
  - Supports hardware write protection for the entire capacity, configurable via the WP flag Power consumption
- Power Consumption
  - Sleep current 2μA (typical)
  - Standby current 20μA (typical)
  - Operating current 400μA (typical write current @ 500kHz)
- Reliability
  - Write cycle 1E12
  - Retention time > 20 years @ 85˚C
- Package
  - SOP8

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2. Pin Descriptions

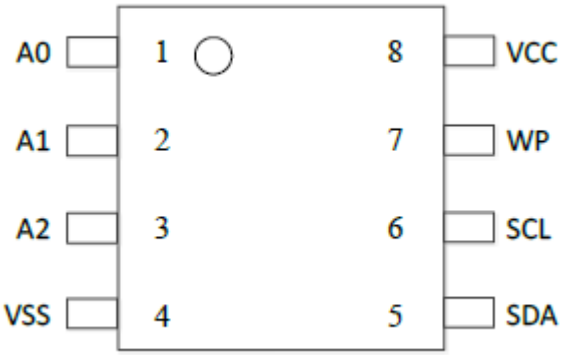


Figure 1 SOP8 Pin Diagram

Pin Number	Pin Name	Interface type	Interface Description
1	A0	Input	Address Pin
2	A1	Input	Address Pin
3	A2	Input	Connect to VSS or Floating
4	VSS	-	Ground
5	SDA	Input / Output	Serial Data Input / Output Pin
6	SCL	Input	Serial Clock Pin
7	WP	Input	Data Write Protection Pin
8	VCC	-	Power Supply

Table 1 Pin Descriptions

Pin Function Description:

(1) A0, A1: Address pins are used to identify each device. Connect A0 and A1 to the VCC pin or the VSS pin to define the device address. The chip will only work when the device address defined by A0 and A1 matches the device address word input by the SDA pin. The A0 and A1 pins have internal pull-down resistors. When in the floating state, they will be recognized as a low level by the chip. A maximum of 4 HS256K3CD chips can be mounted on the same data bus.

(2) A2: A2 must be connected to VSS or left floating. It is not allowed to connect to VCC. The A2 pin has an internal pull-down resistor. When in the floating state, it will be recognized as a low level by the chip.

(3) VSS: Ground pin.

(4) SDA: Serial data input/output pin, which can be connected to multiple devices. This pin is an open-drain output and requires a pull-up resistor to connect to the external circuit.

(5) SCL: Clock input pin for serial data input/output. Data is sampled on the rising edge of the clock and output on the falling edge. This pin is an open-drain output and requires a pull-up resistor to connect to an external circuit.

(6) WP: Write protection pin. When connected to VCC, write operations are prohibited at all capacity. When connected to VSS, write operations are allowed at all capacity. The WP pin only affects write operations and does not affect read operations. WP has an internal pull-down resistor and is recognized as a low level by the chip when left floating.

(7) VCC: Power supply pin.

3. Chip Functions

(1) The HS256K3CD supports the I2C bus and operates as a slave device.

(2) The I2C bus defines master and slave devices in communication. The master device is responsible for initiating data transmission and generating clock signals for data synchronization. After being addressed by the master device, the slave device responds and exchanges data with the master.

(3) Multiple devices can be connected to an I2C bus. Each device has a corresponding device address. Data can only be transferred from one device to the device with the corresponding address.

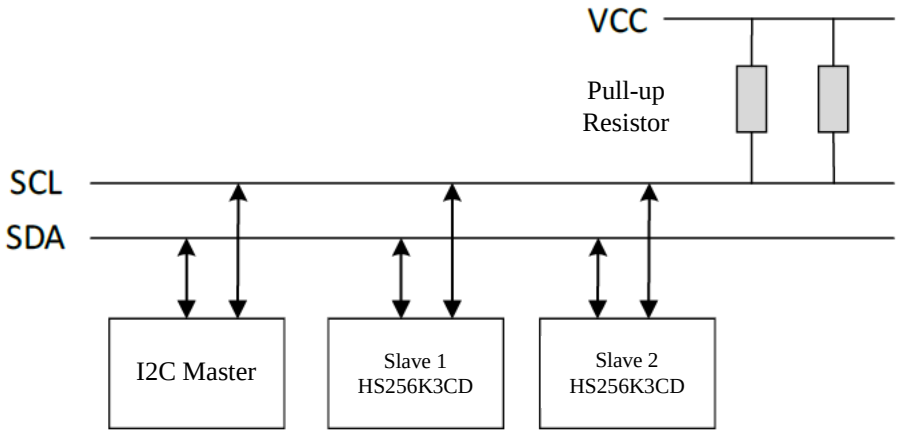


Figure 2 I2C Interface example

3.1 I2C Protocol

Starting condition (S) :

A start condition is indicated by a transition of SDA from high to low while SCL is high. All commands should be preceded by a start condition. A start condition can terminate an ongoing operation at any time.

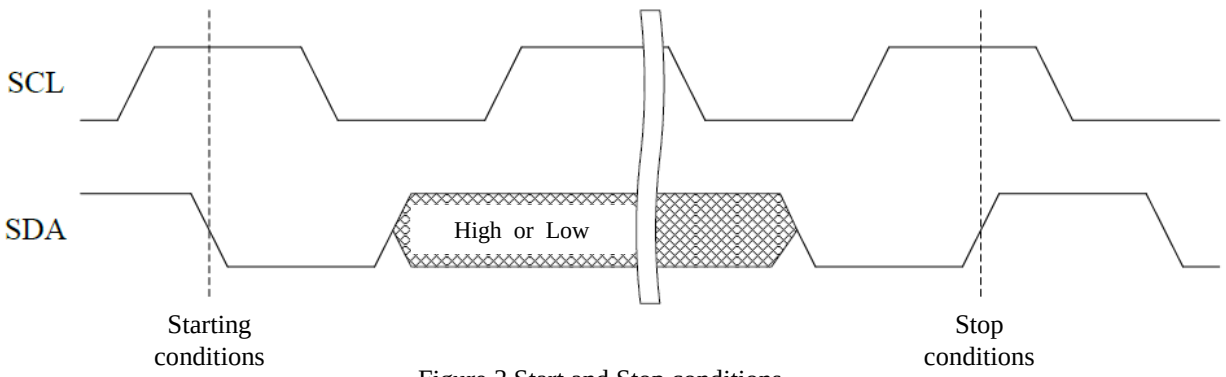


Figure 3 Start and Stop conditions

Stop condition (P) :

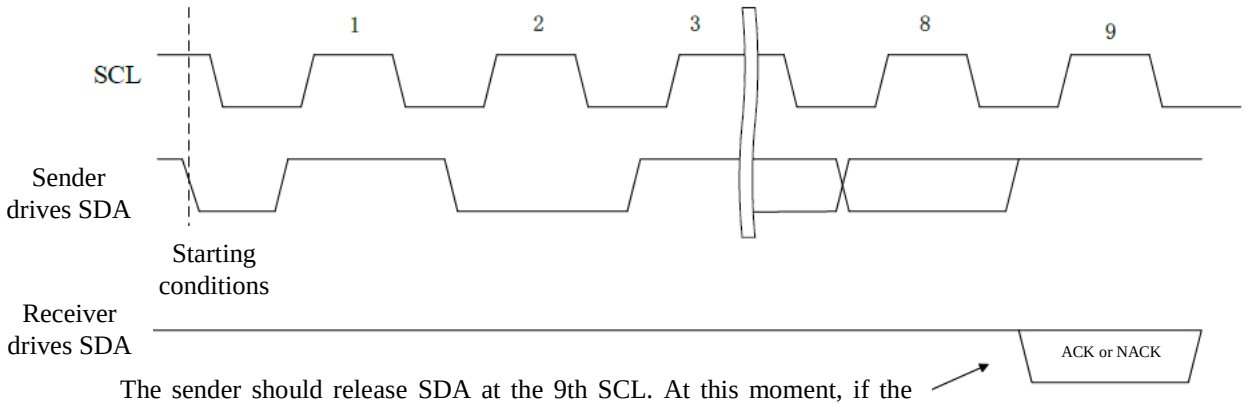
A SDA transition from low to high during SCL's high period indicates a stop condition. This condition terminates the current operation.

Data/Address Transfer :

In stop and start conditions, the SDA level transition occurs during SCL's high period. Data and address signals must transit during SCL's low period and remain stable during SCL's high period.

Acknowledgement (ACK) and non-acknowledgement (NACK) :

On the I2C bus, serial data, including memory addresses or information, is transmitted and received in groups of 8 bits. Each successful transmission or reception of an 8-bit data group results in an acknowledgement signal. After each 8-bit data transmission, the sender temporarily enters a high-impedance state during the ninth clock cycle to allow reception and detection of the acknowledgement signal. During this high-impedance release period, if the receiver pulls SDA low, an acknowledgement signal (ACK) is issued, indicating successful reception of the previous 8 bits of data. If the receiver pulls SDA high, a negative acknowledgement signal (NACK) is issued, indicating a failure to receive the previous 8 bits of data.



The sender should release SDA at the 9th SCL. At this moment, if the receiver successfully receives the previous 8 bits of data, it should pull down SDA and give an acknowledgement signal ACK, otherwise it gives a non-acknowledgement signal NACK.

Figure 4 Response timing diagram

3.2 Device Address Word

After the start condition, enter the 8-bit device address word, as shown in the figure below. Bits 7-4 are the device type code, which is 1010 for this chip. Bits 3-1 are the device address code, which is used to distinguish different devices mounted on the bus. Bit 0 is the read/write code (R/W). R/W=1 indicates a read operation, and R/W=0 indicates a write operation.

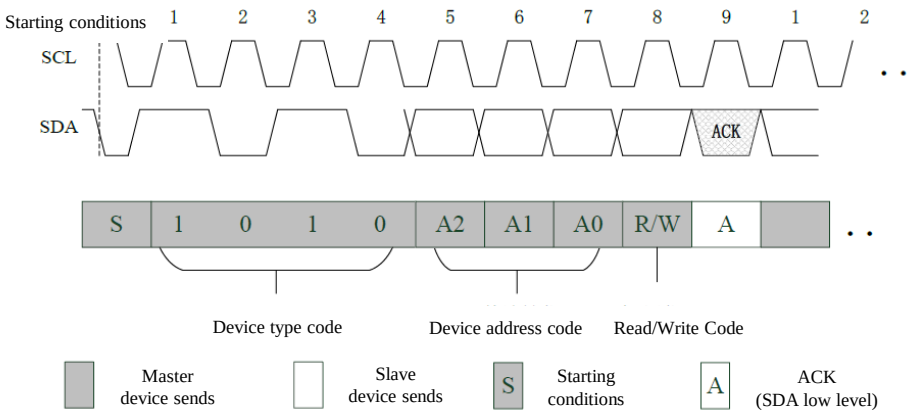


Figure 5 Device address word timing diagram

3.3 Write Operation

All write operations, including the single-byte write shown in Figure 6 and the multi-byte write shown in Figure 7, begin with a start condition, followed by the device address, and then the memory address to be accessed and the data to be written. The R/W bit in bit 0 of the device address must be set to 0 to indicate a write operation. The slave generates an acknowledgement (ACK) after successfully receiving 8 bits of data from the master, and a non-acknowledge (NACK) if reception fails. The master can write any number of bytes in a single write operation. After receiving an acknowledgment from the slave, the write operation ends with a stop condition (P). Data is written to the memory in ascending order, starting with the input memory address. The address counter rolls over to 0000h after reaching the last address, 7FFFh.

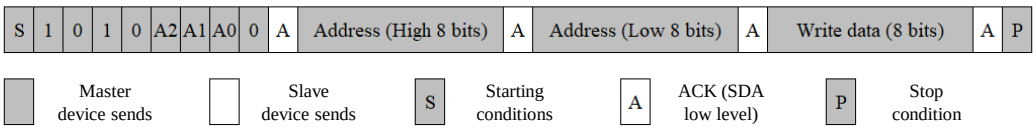


Figure 6 Single byte write diagram

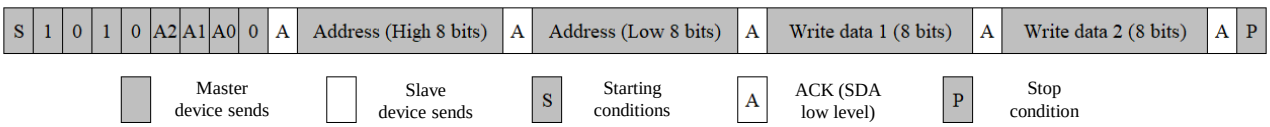


Figure 7 Schematic diagram of multi-byte writing
(taking 2 bytes as an example)

Unlike other non-volatile memory technologies, MRAM has no write latency. This is because the write and read cycles of the magnetic storage array are nearly identical and very short compared to the bus clock. For users, both write and read operations can be initiated immediately after the previous write operation completes, eliminating the need for a delay or post-write confirmation like EEPROM chips. If a confirmation poll is performed, the result is usually that the write is complete, allowing subsequent operations to proceed.

3.4 Read Operation

Read operations can be categorized into 3 types, such as Current Address Read, Random Address Read, and Sequential Read.

Current Address Read :

If a write or read operation successfully completes with a stop condition, assuming the last address accessed is n, and if the power is not turned off during this operation, the following command can be sent to read the data at address n+1. If n is the last address, 7FFFh, then n+1 will point to address 0000h. If the power is turned off and then on again during this operation, the current address n becomes undefined.

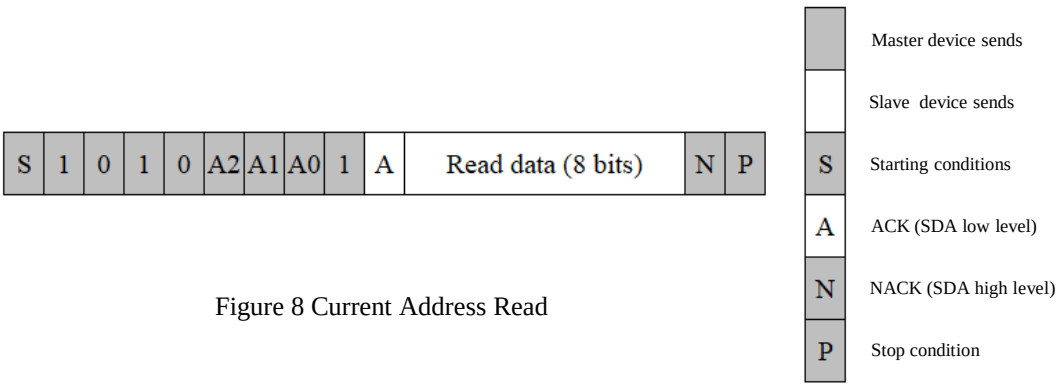


Figure 8 Current Address Read

Random Address Read :

Random Address Read provides a simple operation for reading from any address. As shown in the figure below, this instruction can be divided into two parts:

1. The first three bytes are identical to a write operation, with the R/W bit set to 0 to set the memory address to be accessed.
2. The remaining portion, starting with the second S, is identical to a current address read operation, with the R/W bit set to 1 to read the data at the specified address.

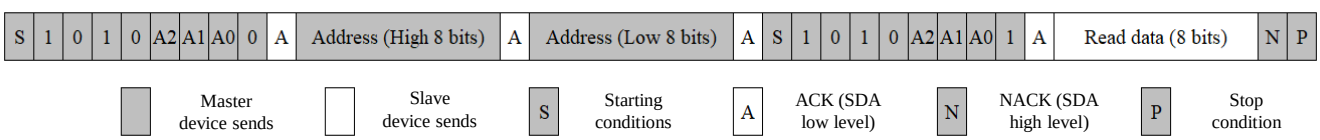


Figure 9 Random Address Read

Sequential Read :

By specifying the address in the same way as for random reads, data can be received continuously after the device address word (input R/W "1"). If the read exceeds the end of the address by 7FFFh, the read address automatically rolls over to 0000h and continues reading.

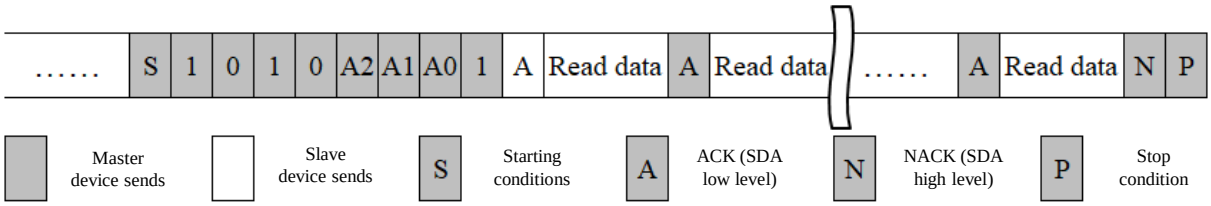


Figure 10 Sequential Read

3.5 Sleep Mode

Sleep mode is a low power mode that is entered and exited through the following instructions.

Entering Sleep Mode :

Entering Sleep mode operates as follows:

1. The master sends a start condition (S);
2. The master sends the command F8h;
3. The slave sends an ACK;
4. The host sends an 8-bit device address word, where the R/W bit (bit 0) can be either 0 or 1;
5. The slave sends an ACK;
6. The master sends another start condition (S);
7. The master sends the command 86h;
8. The slave sends an ACK;
9. The master sends a stop condition to ensure the device enters sleep mode.

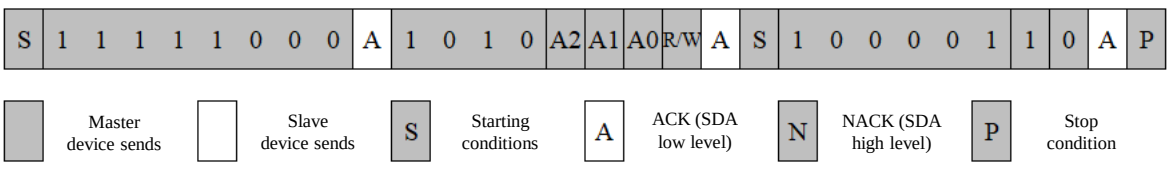


Figure 11 Entering Sleep Mode

Exit Sleep Mode Instructions :

During sleep mode, the chip monitors the status of the SDA and SCL pins in real time. Upon receiving the Exit Sleep Mode command and waiting for the tREC wake-up time, the chip exits sleep mode.

Exiting sleep mode operates as follows:

1. The host sends a start condition (S) followed by an 8-bit device address, where the R/W bit (bit 0) can be either 0 or 1;
2. On the ninth rising clock edge following the start condition, the recovery operation begins, gradually turning on the internal power supplies;
3. After the wake-up time (tREC) has passed and the power supply is stabilized, the chip exits sleep mode and returns to the standby state, where read and write access is possible.

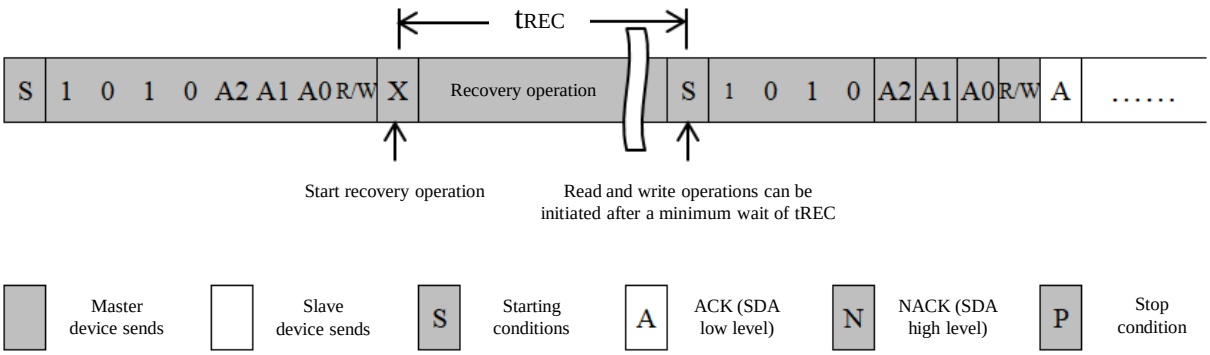


Figure 12 Exiting Sleep Mode

3.6 Device ID

Device ID consists of 3 bytes and is read-only information. It includes Manufacturer ID and Product ID. The bit distribution information is shown in the following table.

Device ID	
23 – 12 (12 bits)	11 – 0 (12 bits)
Manufacturer ID	Product ID

Table 2 Device ID bit allocation table

The Device ID can be accessed through the following instructions:

1. The host sends a start condition (S);
2. The host sends the command F8h;
3. The slave sends an ACK;
4. The host sends the 8-bit device address, where the R/W bit (bit 0) can be either 0 or 1;
5. The slave sends an ACK;
6. The host sends another start condition (S);
7. The host sends the command F9h;
8. The slave sends an ACK;
9. The host receives the Device ID byte and continues receiving by sending an ACK until the last byte is received. It terminates the Device ID read operation by sending a NACK;
10. The host ends the operation by sending a stop condition (P), and the slave returns to standby mode.

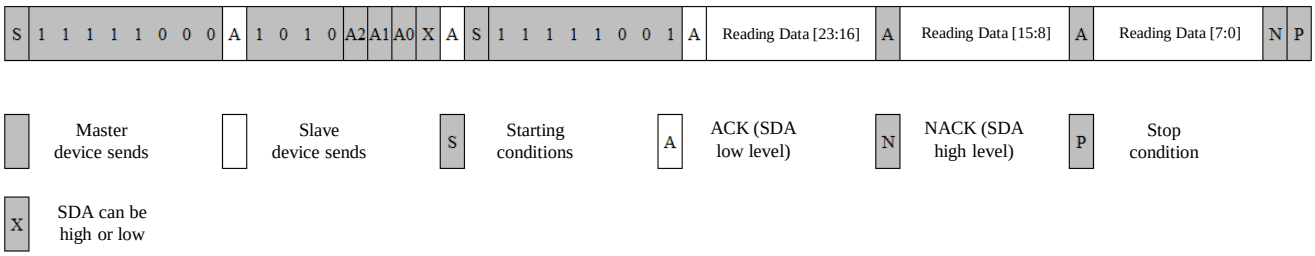


Figure 13 Reading the DEVICE ID

3.7 Serial Number

The Serial Number consists of 8 bytes and is read-only information that can be used to uniquely identify a PC board or system.

The serial number can be obtained using a similar operation to reading the device ID. The specific steps are as follows:

1. The host sends a start condition (S);
2. The host sends the command F8h;
3. The slave sends an ACK;
4. The host sends the 8-bit device address, where the R/W bit (bit 0) can be either 0 or 1;
5. The slave sends an ACK;
6. The host sends another start condition (S);
7. The host sends the command CDh to read the serial number.
8. The slave sends an ACK;
9. The host receives the serial number byte and sends an ACK to indicate continued reception. After the last byte is received, the host ends the serial number read operation by sending a NACK;
10. The host sends a stop condition (P) to terminate the operation, and the slave device returns to standby mode.

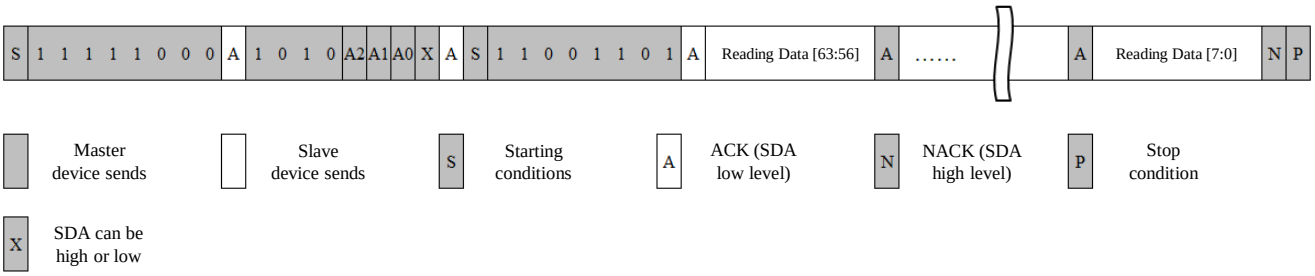


Figure 14 Reading the Serial Number

4. Absolute Operating Conditions

Symbol	Parameter	Test Condition	Limit Value	Unit
VCC	Power supply		0 to 3.6	V
Vin	Input voltage per pin		0 to 3.6	V
Iout	Output current per pin		±3	mA
Tbias	Temperature under bias		-40 to 85	℃
Tstg	Storage temperature		-55 o 125	℃
Tlead	Pin soldering temperature (less than 3 minutes)		260	℃
Hmax_write	Maximum magnetic field during writing (*1)	Write	4,000	A/m
Hmax_read	Maximum magnetic field during reading or standby (*1)	Read or Standby	12,000	A/m
Hmax_poweroff	Maximum magnetic field when power is off (*1)	Power-off	45,000	A/m

Table 3 Extreme working conditions

Note :

*1: The test conditions are room temperature and exposure to a vertical magnetic field for one month to measure the magnetic resistance.

5. Electrical Characteristics

This chapter introduces the chip's electrical characteristics. The AC and DC parameter values shown in the following table are derived based on the operating conditions shown in Table 4 and the measurement conditions noted in Table 5. When users query a parameter, ensure that the operating and measurement conditions match.

5.1 Operating Conditions

Symbol	Description	Min.	Max.	Unit
VCC	Power supply voltage	2.7	3.6	V
Tax	Temperature	-40	85	℃

Table 4 Operating Conditions

5.2 DC Characteristics

Symbol	Description	Test Conditions	Min.	Typical	Max.	Unit
$\|I_{LI}\|$	Input leakage current (*1)	V_{IN} = 0 V ~ VCC			1	µA
$\|I_{LO}\|$	Output leakage current (*2)	V_{OUT} = 0 V ~ VCC			1	µA
I_{SLP}	Sleep current	SCL、SDA = VCC A0、A1、A2、WP = 0 V		2	6	µA
I_{SBY}	Standby current	SCL、SDA = VCC ， A0、A1、A2、WP = 0 V or V_{CC} or Floating (*3)		20	35	µA
I_{CC}	Operation current	SCL=500KHz		400	600	µA
V_{IL}	Input low level	VCC = 2.7V ~3.6V	V_{SS}		VCC*2	V
V_{IH}	Input high level	VCC = 2.7V ~ 3.6V	VCC*0.8		VCC+0.3	V
V_{OL}	Output low level	I_{OL} = 3mA			VCC*2	V
R_{IN}	Input resistance (WP, A0, A1, A2)	V_{IN} = V_{IL} (Max)	50			kΩ
		V_{IN} = V_{IH} (Min)	1			MΩ

Table 5 DC Characteristics

Note:

*1. Applies to the SCL and SDA pins.

*2. Applies to the SDA pin.

*3. In addition to the pin level states shown in the table, the sleep mode test conditions must also ensure that the measurement time is after the stop condition and cannot be measured while the command is halfway through.

5.3 Pin Capacitance

Symbol	Parameter	Max.	Unit
C_{IN}	Input pin capacitance	15	pF
C_{IO}	I/O pin capacitance	15	pF

Table 6 Pin Capacitance

5.4 AC Characteristics

Symbol	Description	100kHz		500kHz		Unit
		Min.	Max.	Min.	Max.	
t_{CLK}	Clock cycle	10		2.5		µs
t_{HIGH}	Clock high time	4		0.6		µs
t_{LOW}	Clock low time	4.7		1.3		µs
t_R	SCL, SDA rise time		1000		300	ns
t_F	SCL, SDA fall time		300		300	ns
$t_{HD:STA}$	Hold time of the start condition	4		0.6		µs
$t_{SU:STA}$	Start condition setup time	4.7		0.6		µs
$t_{HD:DAT}$	Data input hold time	2		2		ns
$t_{SU:DAT}$	Data input setup time	250		100		ns
$t_{DH:DAT}$	Data output hold time	0		0		ns
$t_{SU:STO}$	Stop condition setup time	4		0.6		µs
t_{AA}	SCL low level to output data valid		3		0.9	µs
t_{BUF}	Precharge time (time between stop condition and start condition)	4.7		1.3		µs

Table 7 AC Characteristics

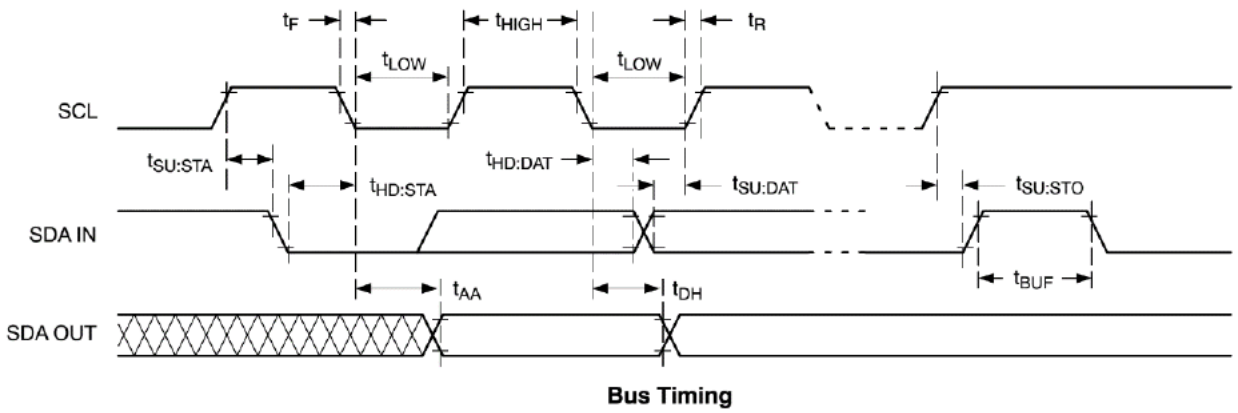


Figure 15 AC timing definition

5.5 Power-on / Power-off Characteristics

To protect data during initial power-up and power-up after power dropped, the chip does not support read or write operations when VCC is below VCC(min). VCC(min) refers to the minimum VCC value specified for normal chip operation, which is 2.7V in this chip. VCC(max) refers to the maximum VCC value specified for normal chip operation, which is 3.6V in this chip.

During initial power-up or power-up after power dropped, the chip must wait for tPU (power-up delay time) after the voltage reaches VCC(min) before it can begin normal operation. This time ensures that the internal chip voltage has stabilized. tPU is measured from the time VCC reaches VCC(min).

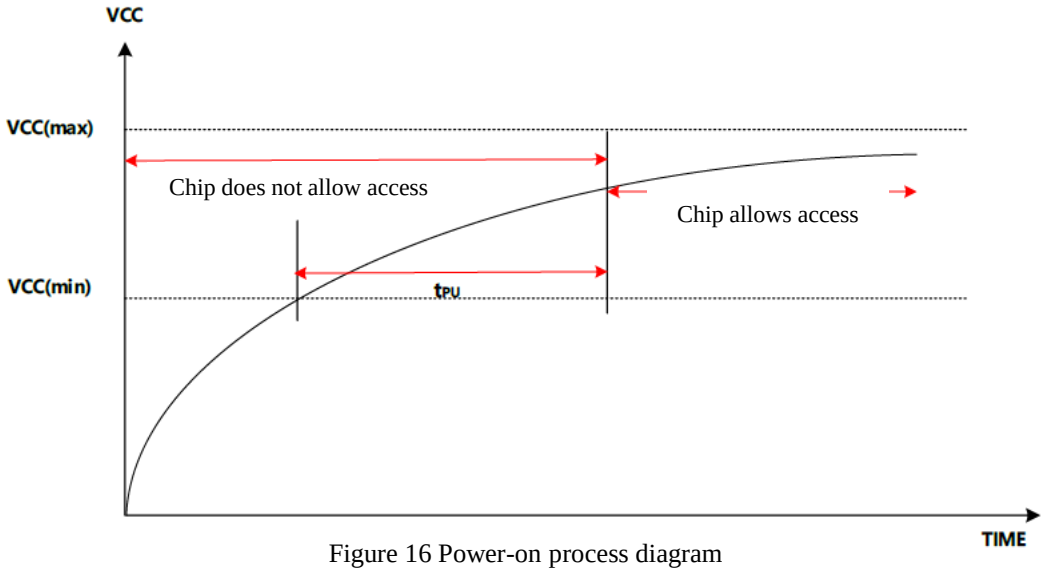


Figure 16 Power-on process diagram

During power-up, the following steps are required to properly initialize the chip:

1. Increase VCC (after tRVR);
2. When VCC is below VCC(min), it is recommended not to send commands to the chip;
3. During initial power-up or after a power-down then power-up, to wait tPU before accessing the chip;
4. After power-up, the chip is in standby mode.

When the chip is powered-off or has a power outage, follow the following steps to properly shut down the device:

1. Lower VCC to below VCC_RST;
2. When VCC is below VCC(min), do not send commands to the chip;
3. After a power-down, follow the power-up initialization procedure when VCC rises above VCC(min);
4. To stabilize the VCC level, it is recommended to add an appropriate decoupling capacitor to the VCC pin;
5. If VCC rises to VCC from a voltage between VCC(min) and VCC_RST, the chip is not guaranteed to function properly.

Symbol	Description	Min.	Typical	Max.	Unit
t_{PU}	Power-on delay time	100	-	-	µS
t_{RVR}	Rise time from VCC to VCC (min)	30	-	30000	µS
t_{RVF}	Fall time from VCC to V_{CC_RST}	20	-		µS
V_{CC_RST}	V_{CC} reset voltage	0	-	2	V
t_{PLOW}	V_{CC} low level time	50	-	-	mS
t_{REC}	Sleep wake-up time	16	-	-	µS

Table 8 Chip Power-on / Power-off parameters

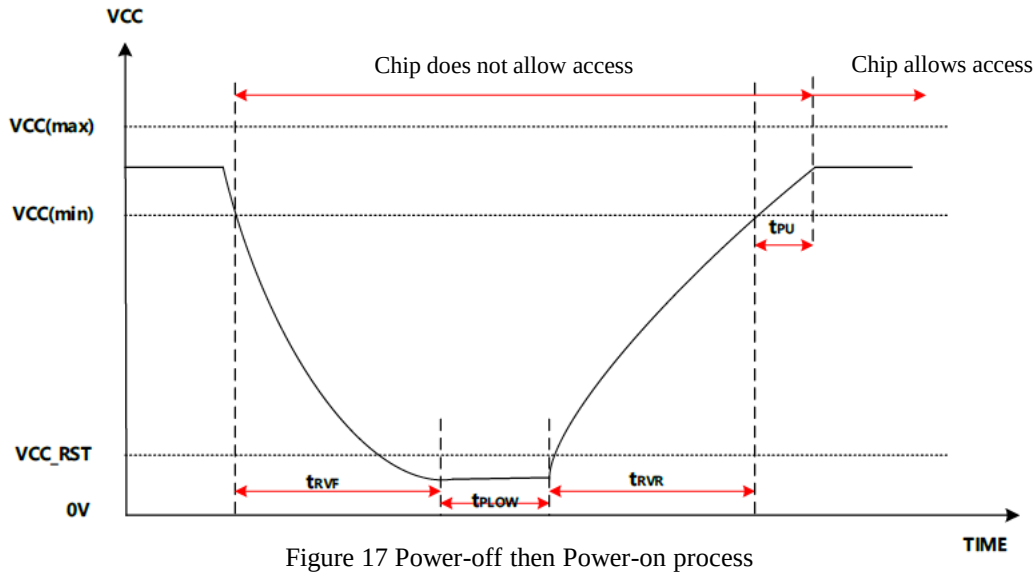
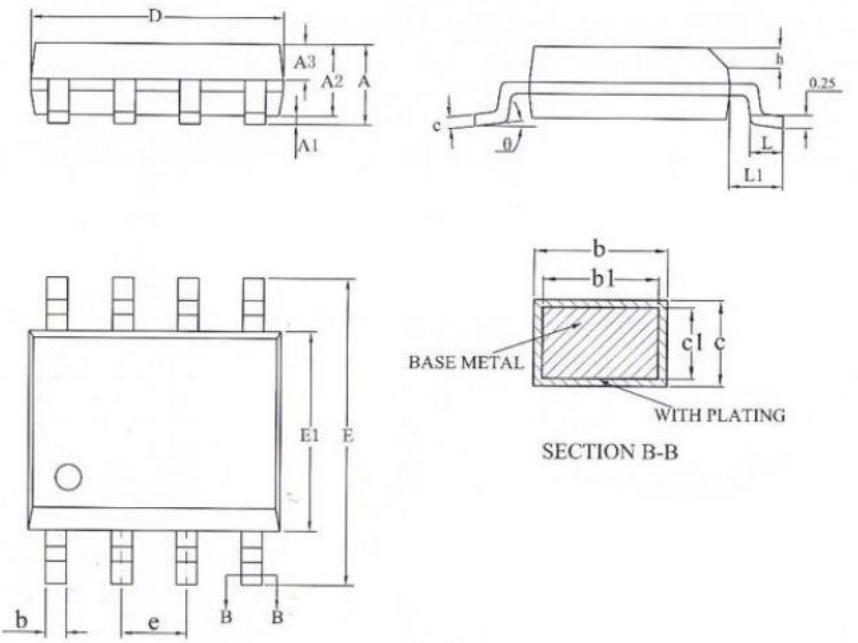


Figure 17 Power-off then Power-on process

6 Precautions for Use

It is recommended that users program the chip after reflow soldering, because the chip cannot guarantee that the data written before reflow soldering will still be valid after reflow soldering.

7 Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Table 8 Chip Power-on / Power-off parameters

8. Product naming Rules

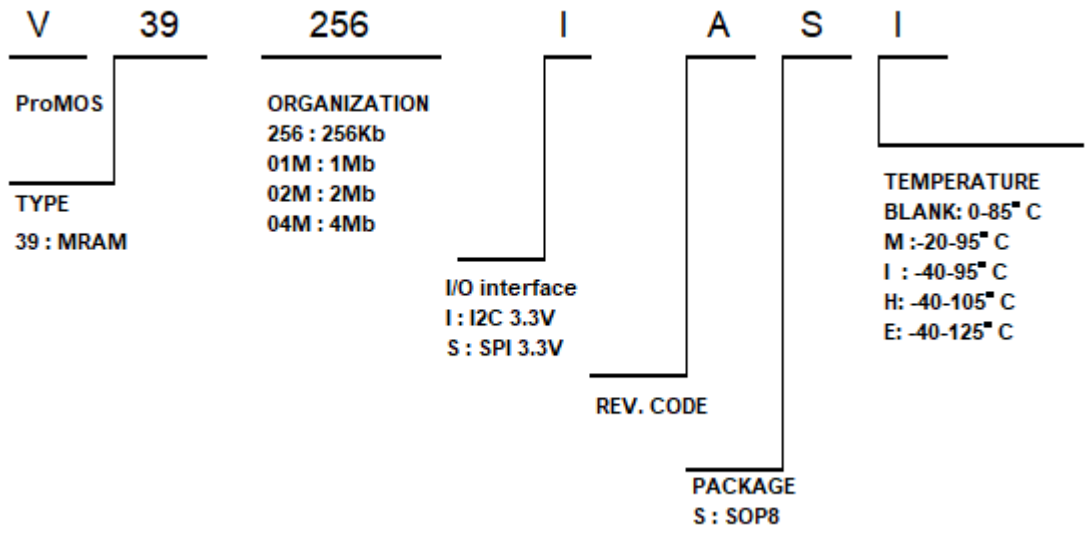


Figure 19 Naming rule description