V39256SAS
256K Bit Serial MRAM

Preliminary

1. Product Overview

The HS256K3SD is a 256Kb SPI (Serial Single Wire) interface non-volatile memory chip. Utilizing advanced pMTJ STT-MRAM technology, it supports single-wire SI and SO interfaces, enabling read and write speed up to 20MHz with zero write latency, excellent reliability, and over 10 years of data retention.

The HS256K3SD is an ideal solution for MCU external memory expansion. Its high throughput, low pin count, and small size make it an increasingly popular choice for embedded systems, network switches, automotive, and IoT applications.

The HS256K3CD chip offers the following key features:

- pMTJ STT-MRAM technology
  - STT process
  - 256Kb capacity
- SPI Interface
  - 10 MHz @ READ mode
  - 20 MHz @ Fast READ mode
  - 20 MHz @ Write mode, no write delay
  - Supports SPI Mode 0 and SPI Mode 3
- Operating Voltage
  - Standard voltage: single VCC 2.7-3.6V
- Operating Temperature
  - 40˚C to 85˚C
- Data Protection
  - Supports software write protection mode, configured via BP0 and BP1 in the SR0 register
- Power Consumption
  - Standby current 300μA (typical)
  - Operating current 3mA (typical @ 10 MHz)
- Reliability
  - Write endurance 1E12
  - Retention time > 10 years @ 85˚C
- Package
  - SOP8

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2. Pin Descriptions

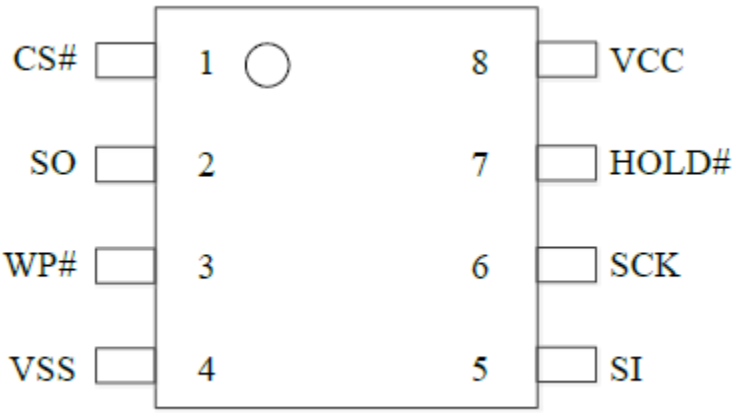


Figure 1 SOP8 Pin Diagram

Pin Number	Pin Name	Interface type	Interface Description
1	CS#	Input	Chip Select Enable Pin
2	SO	Output	Serial Output
3	WP#	Input	Write Protection Pin
4	VSS	-	Ground
5	SI	Input	Serial Data Input Pin
6	SCK	Input	Serial Clock Pin
7	HOLD#	Input	Hold Pin
8	VCC	-	Power Supply

Table 1 Pin Descriptions

Pin Function Description:

(1) CS#: Chip select enable signal, valid at low level; when CS# signal is invalid, the chip does not work.
(2) SO: Serial data output pin, valid during read operation, data output occurs at the falling edge of serial clock SCK. When HOLD# is at "low" level or CS# is at "high" level, SO is in high impedance state, and remains in output state at other times.
(3) WP#: This pin controls the write operation to the SR register, used in conjunction with WPEN, see Section 2.1 for details.
(4) VSS: Ground pin.
(5) SI: Serial input pin, sampled at the rising edge of serial clock SCK.
(6) SCK: Clock input pin, provides clock signal for serial data input and output. Data of SI pin is input synchronously with the rising edge of SCK, and data of SO pin is output synchronously with the rising edge of SCK. The chip supports SPI mode 0 (CPOL=0, CPHA=0) and SPI mode 3 (CPOL=1, CPHA=1). In mode 0, the clock is usually low when idle. In mode 3, the clock is usually high when idle.
(7) HOLD#: Hold pin. When low, it will interrupt the current communication of the chip. SO becomes high impedance state. SCK and SI are ignored. Pulling the Hold# low is only allowed to occur when CS# is low.
(8) VCC: Power supply pin.

3. SR Register

The HS256K3SD chip provides two SR registers, SR0 and SR1, which are stored in internal register units. SR0 and SR1 can be overwritten using register write instructions. The SR0 register status can be retrieved using read instructions, but the chip does not support SR1 register read instructions. The bit allocation table for SR0 and SR1 is shown in Table 2.

Register	Data Bit Definition							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SR0	WPEN	RFU0	RFU1	RFU2	BP1	BP0	WEL	RFU3
SR1	RFU4	RFU5	RFU6	RFU7	BYTE_EN	RFU8	RFU9	RFU10

Table 2 SR Register bit allocation table

3.1 SR0 Register

In the SR0 register, WPEN (Bit7), BP1 (Bit3), and BP0 (Bit2) are both readable and writable. RFU0 (Bit6), WEL (Bit1), and RFU3 (Bit0) are readable only. RFU1 (Bit5) and RFU2 (Bit4) are reserved bits and do not participate in chip control. The default value of the SR0 register after chip power-on initialization is 8'h01.

After a write enable command is issued, WEL (Bit1) changes to 1'b1; after a write disable command is issued, WEL (Bit1) changes to 1'b0.

The primary function of the SR0 register is to define the write protection mode. BP1 (Bit3) and BP0 (Bit2) define the protected area address range of the array, while the remaining address range is the unprotected area. The combination of WP#, WPEN (Bit7), and WEL (Bit1) defines how the write protection function is applied to the protected and unprotected areas and the SR register. Protected state: write operation is invalid; unprotected state: users can write normally.

BP1	BP0	Protected Area Address Range	
		32-bit addressing	8-bit addressing
0	0	No protected area	No protected area
0	1	0x1800 - 0x1FFF	0x6000 - 0x7FFF
1	0	0x1000 - 0x1FFF	0x4000 - 0x7FFF
0	1	0x0000 - 0x1FFF	0x0000 - 0x7FFF

Table 3 Address range of protected areas

WEL (SR0)	WPEN (SR0)	WPEN # (PIN)	Protected Areas	Non-protected Areas	SR Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Un-protected	Un-protected
1	1	0	Protected	Un-protected	Protected
1	1	1	Protected	Un-protected	Un-protected

Table 4 Write protection function

3.1 SR1 Register

All bits in the SR1 register are write-only. After chip power-up, the default value is 8'h00.

RFU4 (bit 7), RFU5 (bit 6), RFU6 (bit 5), RFU8 (bit 2), RFU9 (bit 1), and RFU10 (bit 0) are reserved bits that do not participate in chip control.

RFU7 (bit 4) is a writable reserved bit. To enable proper chip operation, the user must write 0 to bit 4.

BYTE_EN (bit 3) is a writable bit. When BYTE_EN = 1, the chip operates in 8-bit addressing mode. When BYTE_EN = 0, the chip operates in 32-bit addressing mode.

4 Chip Functions

According to the SPI protocol, the first 8 bits of input data are the command code, which defines the chip's operation. Depending on the command code, this may be followed by a 3-byte address, an idle clock cycle, and a data byte, or by a data byte directly.

The 24-bit (3-byte) address portion following the command code defines the address the chip will access. For a 256KB array, the effective address is 13 bits in 32-bit addressing mode and 15 bits in 8-bit addressing mode.

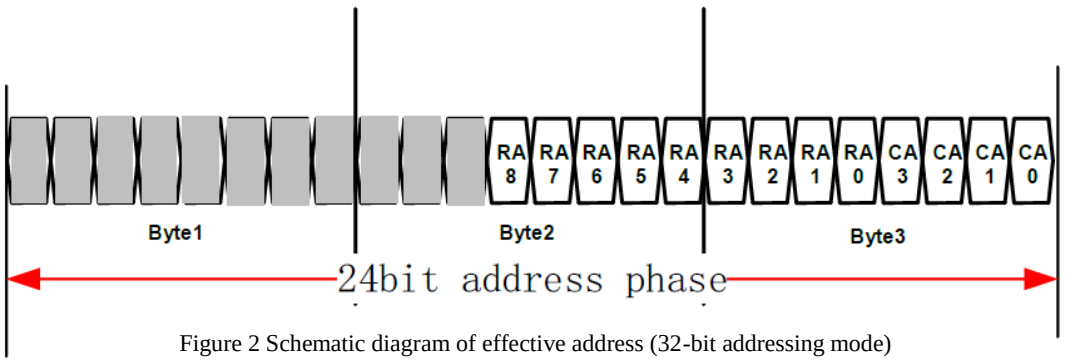


Figure 2 Schematic diagram of effective address (32-bit addressing mode)

Note :

1. All commands, addresses, and dummy bits in the HS256K3SD device are shifted in with the most significant bit first. Data bits are also shifted in or out with the most significant bit first.
2. To prevent partial access to the chip, the user must hold CS# active for a multiple of 8 clocks after CS# goes low.

Table 5 lists the functional operations supported by the chip.

Command	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7~
Write Enable	06h						
Write Disable	04h						
Normal read	03h	A23 - A0			D31-D0 (until CS# is pulled high)		
Fast Read	0Bh	A23 - A0			Dummy	D31-D0 (until CS# is pulled high)	
Write	02h	A23 - A0			D31-D 0 (until CS# is pulled high)		
SR0 Register Write	01h	S7 - S0					
SR0 Register Read	05h	S7 - S0					
SR1 Register Write	31h	S7 - S0					
Enter Sleep Mode	B9h						
Exit Sleep Mode	ABh						
Read MANU_ID	9Fh	ID7-ID0					
Read DEVICE_ID	90h	ID7-ID0					
Read UNIQUE_ID	4Bh	ID87~ID0					
Reset Enable	66h						
Reset	99h						

Table 5 Chip Function Table

4.1 Write Enable and Write Disable

The Write Enable command allows subsequent write commands, SR0 register write commands, and SR1 register write commands to take effect. The Write Disable command prevents subsequent write commands, SR0 register write commands, and SR1 register write commands from taking effect. After sending the Write Enable command, the Write Enable Latch bit (WEL) in the SR0 register is automatically set to 1. After sending the Write Disable command, the Write Enable Latch bit (WEL) in the SR0 register is automatically set to 0. The timing diagrams for the Write Enable and Write Disable commands are shown in Figures 3 and 4. First, pull CS# low, then send the 8-bit command code, and then pull CS# high to complete the command.

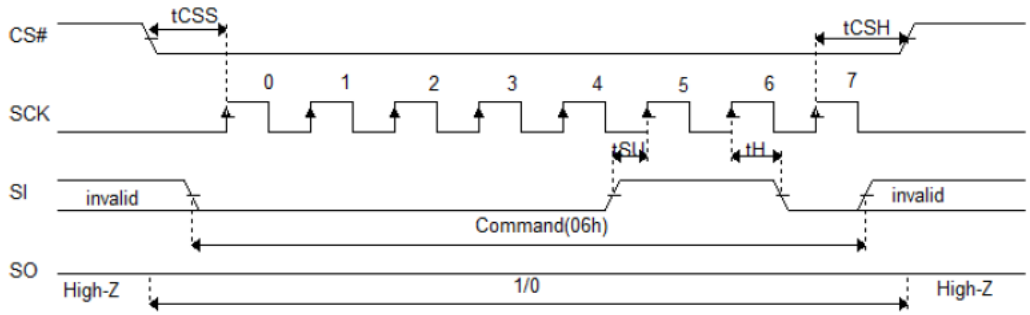


Figure 3 Write Enable timing diagram

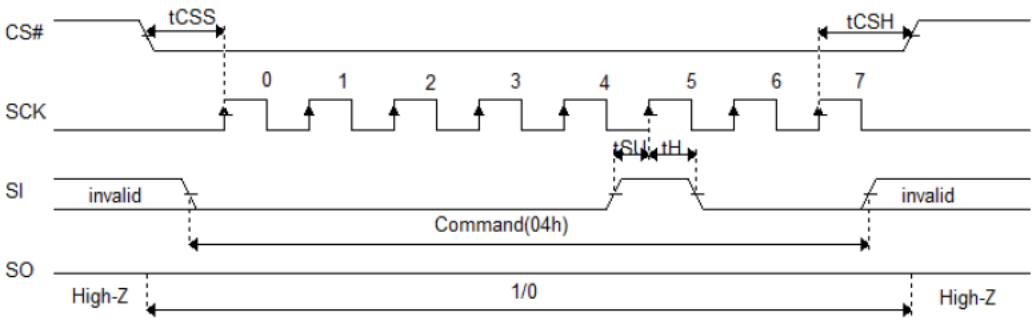


Figure 4 Write Disable timing diagram

4.2 Normal Read Operation

A standard read command allows data to be read starting at the location specified by a 24-bit address. If CS# remains low and SCK is continuously toggled, the user can continue to receive read data after the first data is received. The address automatically increments, and the chip reads out the data from subsequent addresses in sequence. When the address reaches the chip's maximum address, the next address rolls over to the chip's starting address, 00h, and the entire chip is read in an infinite loop until CS# is pulled high to terminate the read operation.

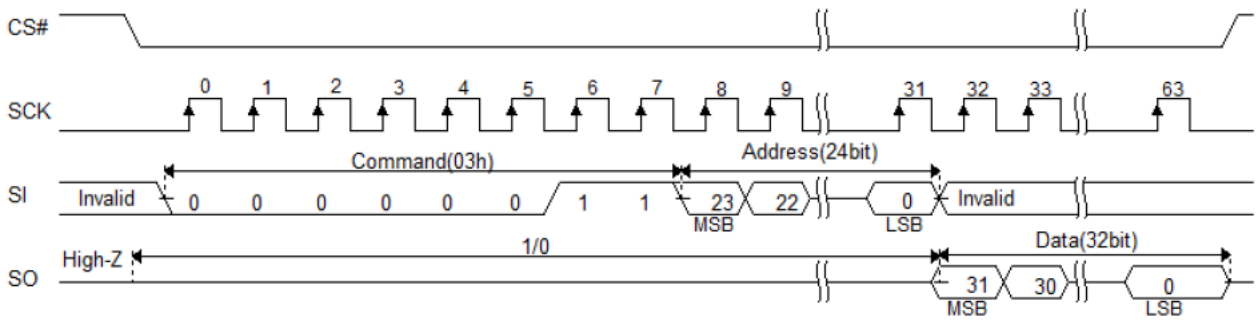


Figure 5 Read operation timing diagram

4.3 Fast Read Operation

The Fast Read command allows data to be read starting at the location specified by a 24 bit address. If CS# remains low and SCK is continuously toggled, the user can continue to receive read data after the first data is received. The address automatically increments, and the chip reads out the data from subsequent addresses in sequence. When the address reaches the chip's maximum address, the next address rolls over to the chip's starting address, 00h, in an infinite loop until CS# is pulled high to terminate the read operation.

The Fast Read command functions similarly to the Standard Read command, differing in that the Standard Read command supports access speeds up to 10 MHz, while the Fast Read command supports access speeds up to 20 MHz.

The Fast Read command timing is shown in Figure 6, where the dummy bit takes up 8 SCK bits.

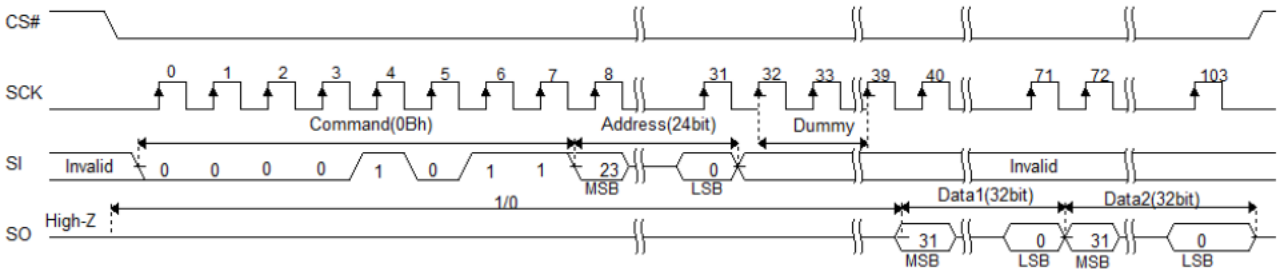


Figure 6 Fast Read operation timing diagram

4.4 Write Operation

The write command allows data to be written starting at the location specified by the 24 bit address. If CS# remains low and SCK is continuously toggling, the user can continue sending write data after the first data is sent. The chip will then write the data sequentially to the following addresses. When the address reaches the chip's maximum address, the next address will roll over to the chip's starting address, 00h, and write data to the entire chip in an infinite loop until CS# is pulled high to terminate the write operation. The data written earlier in the same address will be overwritten by the subsequent data written.

Before performing a write operation, ensure that the write is enabled (WEL = 1 in the SR0 register). The write operation timing is shown in Figure 7.

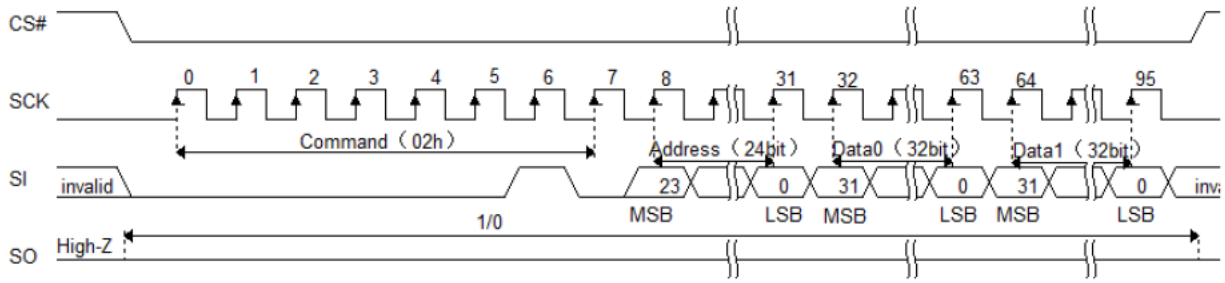


Figure 7 Write operation timing diagram

Note :
If the user sends a write command (02h) and write address after CS# goes low, at least one write data must be sent before pulling CS# high.

4.5 SR0 Register Read Operation

The SR0 register read instruction allows user to read the value of the SR0 register and obtain the status of WPEN, BP1, BP0 and WEL. The SR0 register read instruction timing is shown in Figure 8.

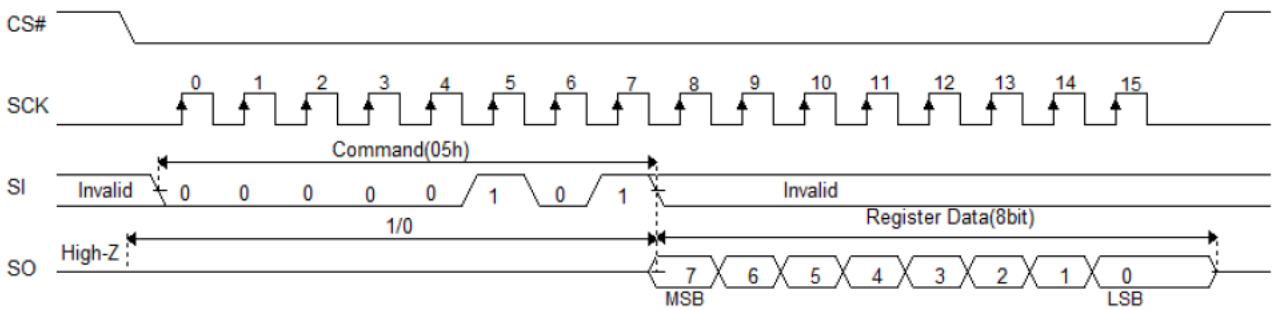


Figure 8 SR0 register read command timing diagram

4.6 Register Write Operation

The SR register write command allows new values to be written to the SR0 and SR1 registers. The command codes are 01h and 31h, respectively. The SR0 register write command timing and the SR1 register write command timing are shown in Figures 9 and 10. To execute the SR register write command, the write enable command must be executed first, WEL is set to 1, and the WP# pin and WPEN values are set as shown in Table 4 to enable the SR register to be written

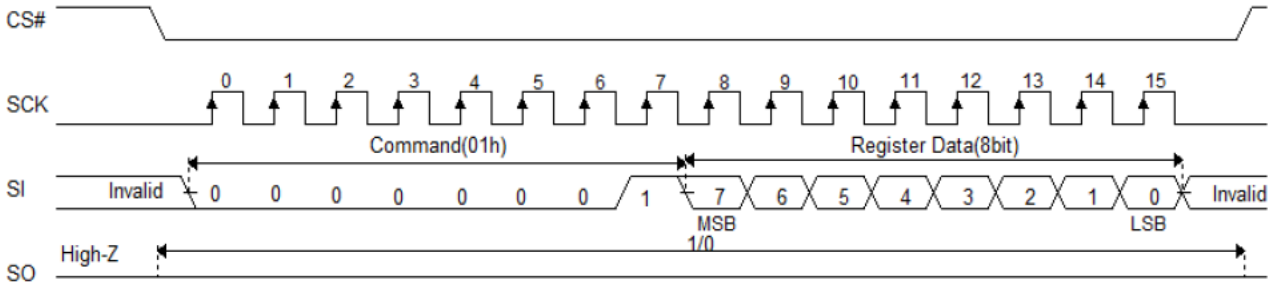


Figure 9 SR0 register write command timing diagram

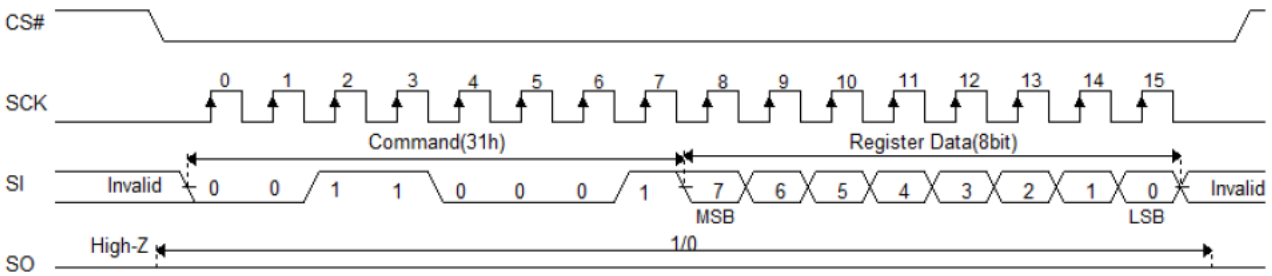


Figure 9 SR1 register write command timing diagram

4.7 Read ID Operation

This chip supports reading the MANU ID, DEVICE ID, and UNIQUE ID. Note that the read ID instruction is invalid in the following three situations: 1. In 8-bit addressing mode (i.e., when the SR1 register is 0x08); 2. After a reset operation (i.e., sending commands 66h, 99h); 3. After entering and exiting sleep mode (i.e., sending commands B9h, ABh). Therefore, it is recommended that users perform the read ID operation after power-on before performing other operations.

The MANU ID of this chip is 8 bits and can be read using the command (9Fh). After sending the 8-bit command code, the user receives the MANU ID. The MANU ID is 26h.

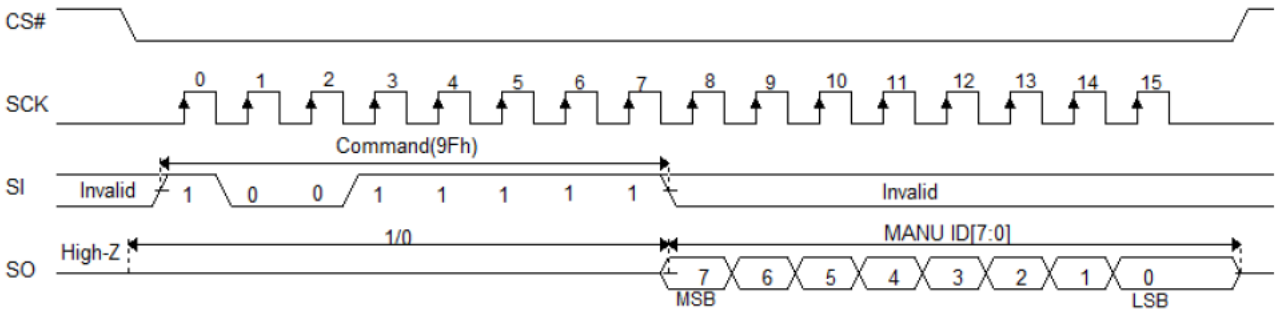


Figure 11 Read MANU ID command timing diagram

The DEVICE ID of this chip is 8 bits in total and can be read through the command (90h). After sending the 8-bit command code, the user can receive the DEVICE ID. The DEVICE ID is 29h.

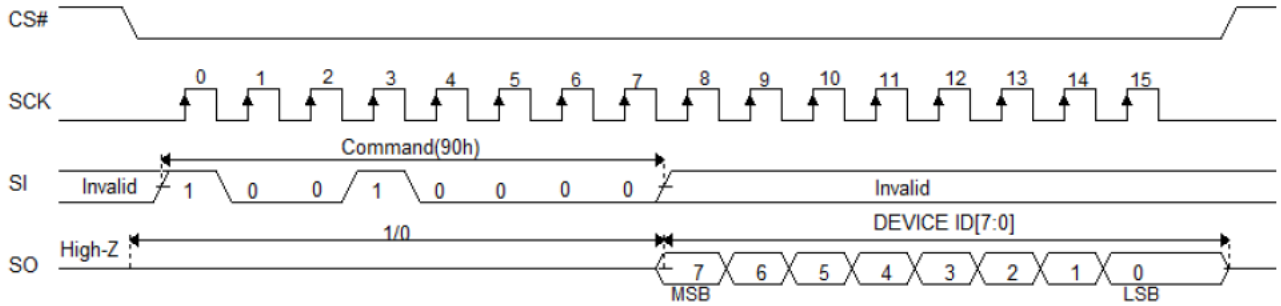


Figure 12 Read DEVICE ID command timing diagram

The UNIQUE ID of this chip is 88 bits in total and can be read through the command (4Bh). After sending the 8-bit command code, the user can receive the UNIQUE ID.

CMD	Byte1	Byte2	Byte3-Byte4	Byte5-Byte10	Byte11	Byte12
UNIQUE ID	4Bh	0h	7F7Fh	ID63-ID0		

Table 6 UNIQUE ID bit allocation table

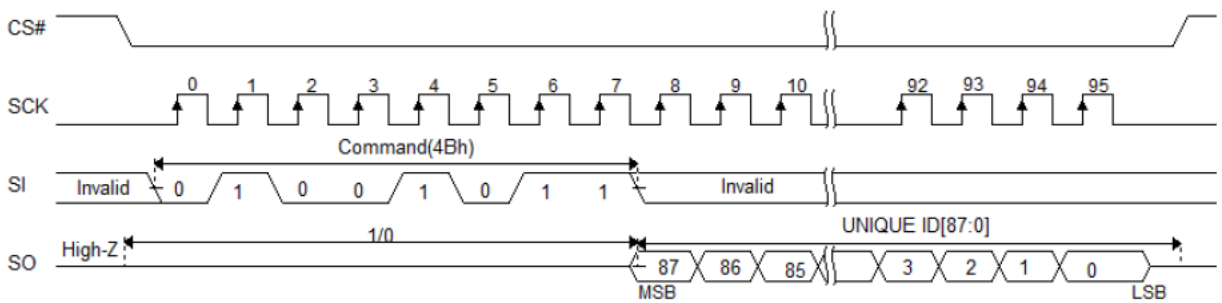


Figure 13 Read UNIQUE ID command timing diagram

4.8 Hold Function

The HOLD# pin is used to pause serial communication with the chip, implementing a hold function. When the chip is selected and serial communication is in progress, the HOLD# pin suspends serial communication between the chip and the user without requiring the user to reset the ongoing serial sequence. To suspend communication, the user simply pulls the HOLD# pin low while the SCK pin is low. To resume communication, the user simply pulls the HOLD# pin high while the SCK pin is low. While HOLD# is low, SCK is allowed to toggle. When communication between the chip and the user is suspended, the input value on the SI pin is ignored, and the SO pin is in a high-impedance state.

It should be noted that if the pin is pulled low while the CLK pin is low, then the HOLD# pin needs to be returned to a high level during the CLK pin is low; if the HOLD# pin is pulled low while the CLK pin is high, then the HOLD# pin needs to be returned to a high level during the CLK pin is high; if CS# is pulled high while HOLD# is low, the current operation will end.

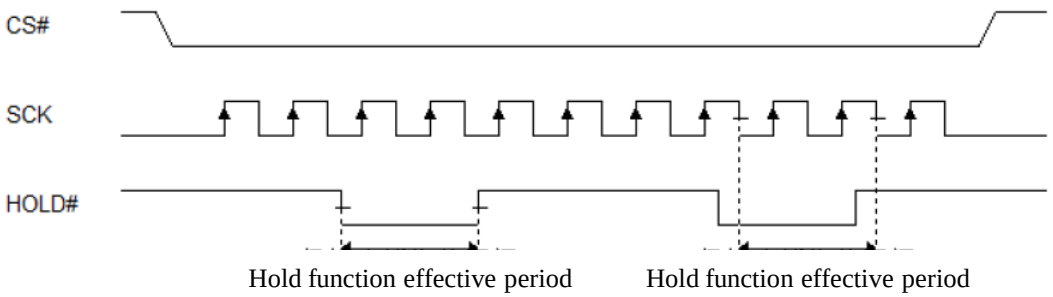


Figure 14 Hold function timing diagram

4.9 Reset Operation

The reset operation requires executing two command codes: the reset enable command and the reset command. After the user executes these two commands in sequence, the chip is reset and the values of all writable bits in the SR register are reset to the default value of 0. After a certain recovery time (tRST), the chip can be read and written normally.

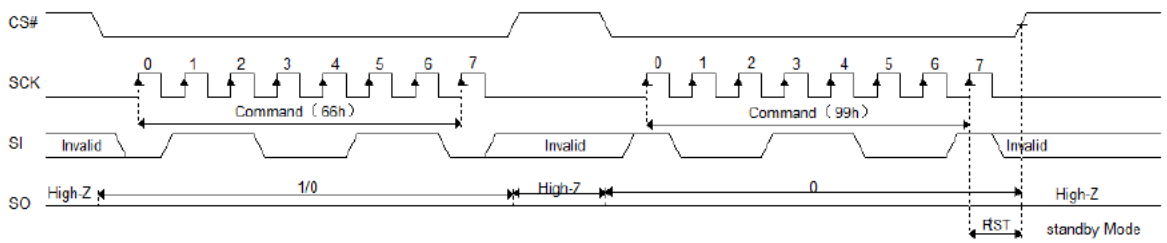


Figure 15 Reset Operation Timing

5 Chip Mode

This chip provides three modes: active, standby, and sleep mode. In active mode, read and write operations are primarily performed.

After power-on, when chip initialization is complete, the chip enters standby mode. The chip cannot receive command codes, the data on SI is invalid, and SO remains in the High-Z state. Then, when the user pulls CS# low and sends a command code other than B9h, the chip enters active mode, receiving the address and data on SI and reading or writing data at the specified address according to the command code. When the user pulls CS# low and sends a command code B9h, the chip enters sleep mode. In this case, the chip's internal power is turned off, disabling read and write operations. In active mode, pulling CS# high returns the chip to standby mode. In sleep mode, pulling CS# low and issuing the exit sleep command (ABh) causes the chip to wake up, re-enabling internal power and transitioning from sleep mode to standby mode.

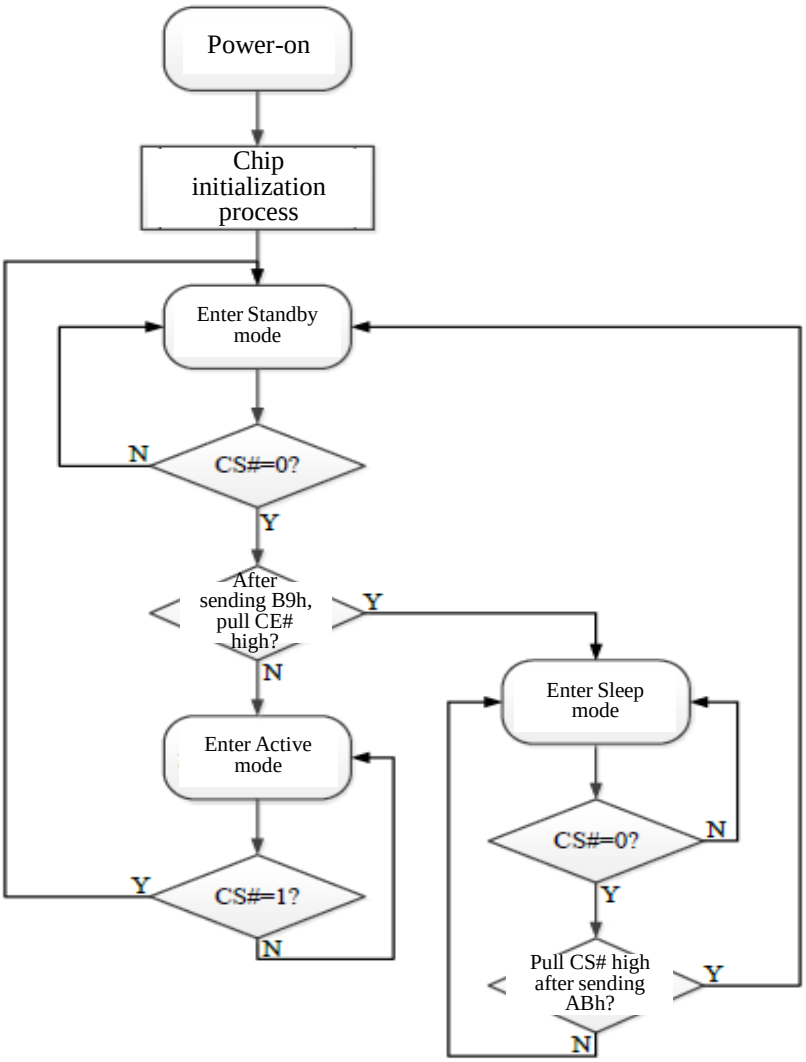


Figure 16 Chip mode switching

5.1 Entering Sleep Mode

Sleep mode is a low-power mode. When in this mode, the chip's internal power is turned off to conserve energy. The user can issue the "Enter Sleep Mode" command (B9h). After a certain time (TDP), the chip enters this mode. If power is lost during sleep mode, the chip returns to its normal standby state upon restoration of power.

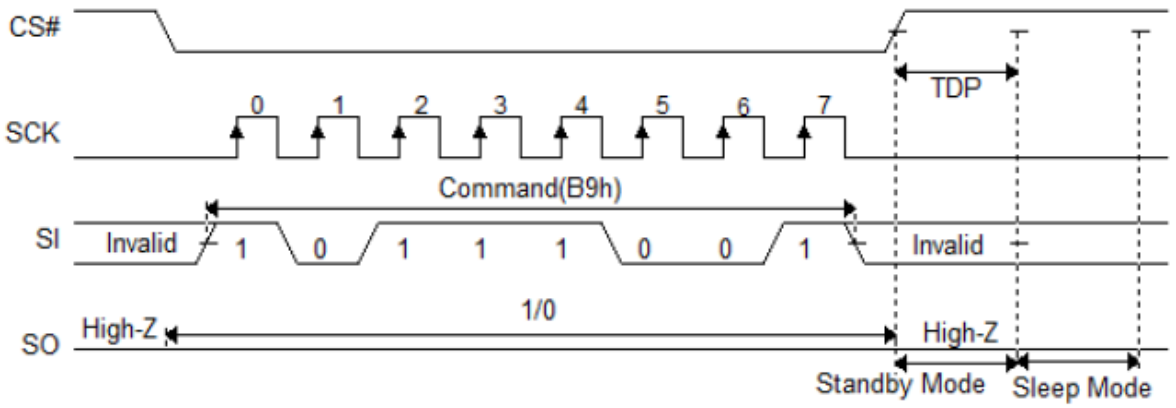


Figure 17 Timing of entering sleep mode

5.2 Exiting Sleep Mode

When the chip is in sleep mode, the user can issue the exit sleep mode command (ABh) to wake the chip. During the wake-up process, the internal power module will be turned back on. After the wake-up process is complete, the chip enters standby mode. The wake-up process requires a time of TRDP.

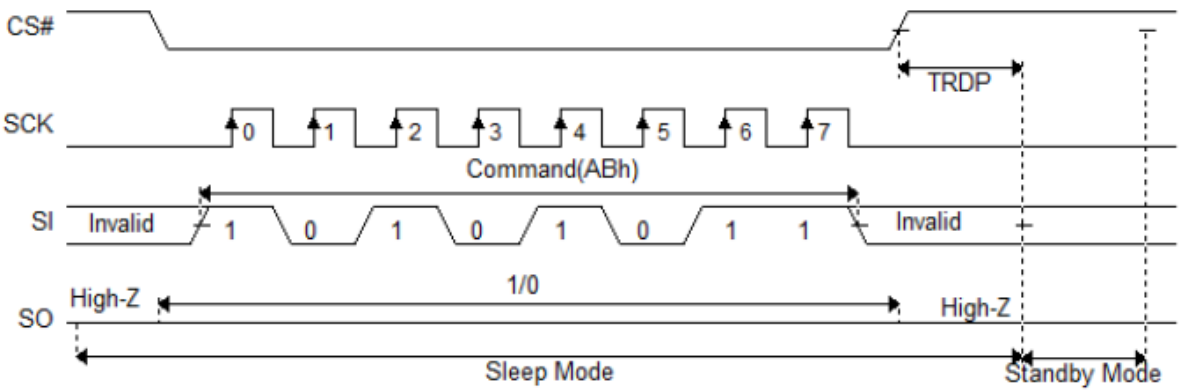


Figure 18 Timing of exiting sleep mode

6. Absolute Operating Conditions

Symbol	Parameter	Test Condition	Limit Value	Unit
VCC	Power supply		-0.3 to 4	V
Vin	Input voltage per pin		0 to 3.6	V
Iout	Output current per pin		±20	mA
Tbias	Temperature under bias		-40 to 85	℃
Tstg	Storage temperature		-55 o 125	℃
Tlead	Pin soldering temperature (less than 3 minutes)		260	℃
Hmax_write	Maximum magnetic field during writing (*1)	Write	12,000	A/m
Hmax_read	Maximum magnetic field during reading or standby (*1)	Read or Standby	12,000	A/m
Hmax_poweroff	Maximum magnetic field when power is off (*1)	Power-off	45,000	A/m

Table 7 Absolute Operating Conditions

Note :

*1: The test conditions are room temperature and exposure to a vertical magnetic field for one month to measure the magnetic resistance.

7 Electrical Characteristics

This chapter describes the chip's electrical characteristics. The AC and DC parameter values shown in the following table are derived based on the operating conditions shown in Table 8 and the measurement conditions noted in Table 9. When checking a parameter, ensure that the operating and measurement conditions match.

7.1 Operating Conditions

Symbol	Description	Min.	Typical	Max.	Unit
VCC	Power supply voltage	2.7	3.3	3.6	V
Tax	Temperature	-40		85	℃

Table 8 Operating Conditions

7.2 AC Characteristics

Symbol	Description	Min.	Typical	Max.	Unit
f_{SCK}	SCK clock frequency (normal read)			10	MHz
	SCK clock frequency (fast read)			20	
t_{WH}	Clock high time (except read operation)	15			ns
t_{WHR}	Clock high time (read operation)	20			ns
t_{WL}	Clock low time (except read operation)	15			ns
t_{WLR}	Clock low time (read operation)	20			ns
t_{CSS}	CS# setup time	3			ns
t_{CSH}	CS# hold time	10			ns
t_{SU}	Input data setup time on SCK rising edge	2			ns
t_{H}	Input data hold time on SCK rising edge	5			ns
t_{V}	SCK falling edge to data valid transition time	18		21	ns
t_{DIS}	CS# high to output data invalid time			6	ns
t_{OH}	Output data hold time on SCK falling edge	1.5			ns
t_{CS}	CS# high time (except write operation)	10			ns
t_{CSW}	CS# High Time (write Operation)	10			ns
t_{SH}	HOLD# setup time	10			ns
t_{HH}	HOLD #hold time	10			ns
t_{HHZ}	HOLD# low to output Hi-Z time	-	-	20	ns
t_{HLZ}	HOLD# high to output valid time	-	-	20	ns
t_{RST}	Reset recovery time (normal reading / writing)	600			µs
TDP	Time to enter sleep mode			3	µs
TRDP	Time to exit sleep mode			30	µs

Table 9 AC Characteristics

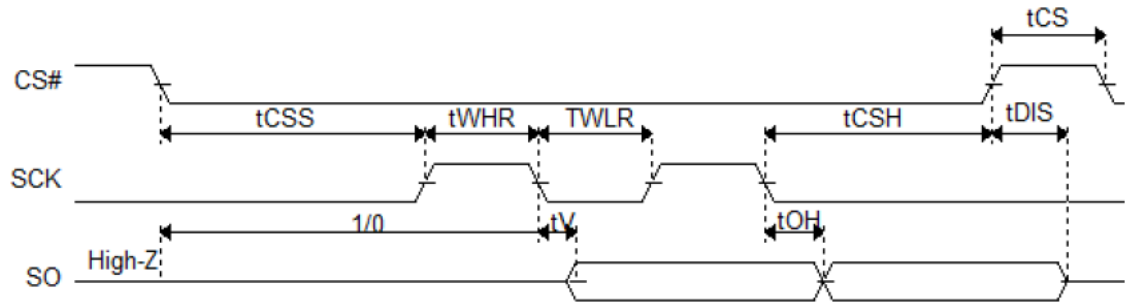


Figure 19 Normal read timing diagram

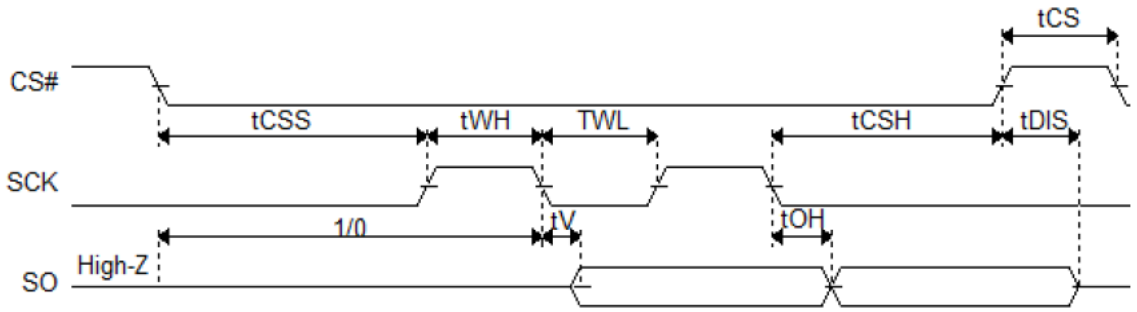


Figure 20 Fast read timing diagram

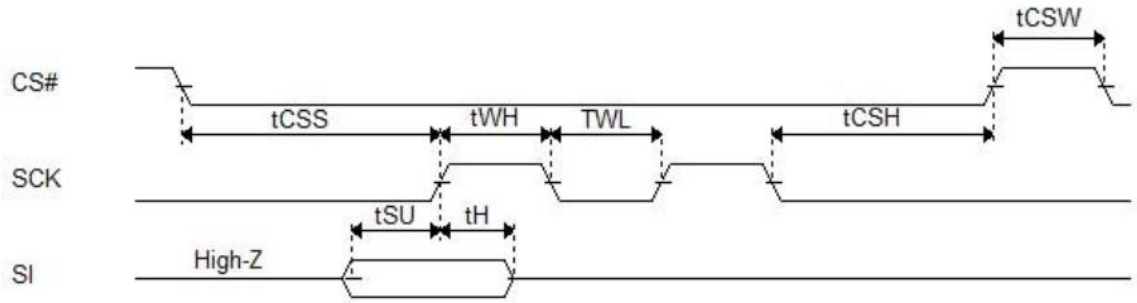


Figure 21 Input interface timing diagram

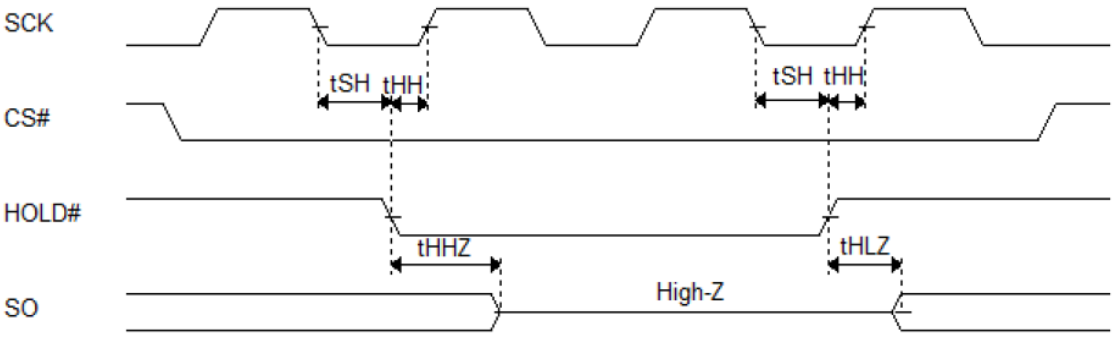


Figure 22 HOLD# interface timing diagram 1

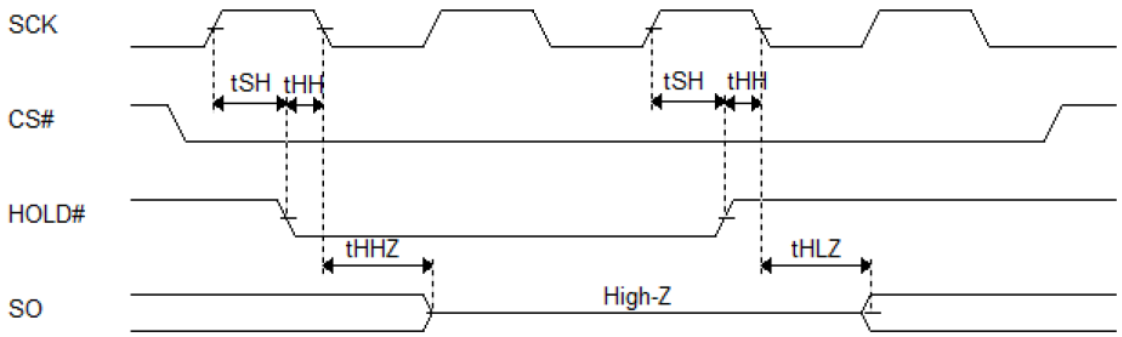


Figure 23 HOLD# interface timing diagram 2

7.3 DC Characteristics

Symbol	Description	Test Condition	Min.	Typical	Max.	Unit
I_{LI}	Input leakage current				±1	µA
I_{LO}	Output leakage current				±1	µA
I_{SBY}	Standby current	CS#=HOLD#=VCC, WP#=SCK=SI=VSS		300	500	µA
I_{SLP}	Sleep current	CS#=HOLD#=VCC, WP#=SCK=SI=VSS		2	4	µA
I_{CC1}	Write current	SPI@10MHz		3	5	mA
I_{CC2}	Read current	SPI@10MHz		3	5	mA
V_{IL}	Input low level		-0.3		0.2VCC	V
V_{IH}	Input high level		0.8VCC		VCC+0.3	V
V_{OL}	Output low level	IOL = 4mA			0.5	V
V_{OH}	Output high level	IOH = -4mA	VCC-0.6			V

Table 10 DC characteristics

7.4 Pin Capacitance

Symbol	Parameter	Max.	Unit
C_{IN}	Input pin capacitance	8	pF
C_{IO}	I/O pin capacitance	12	pF
C_{LOAD}	Load capacitance	32	pF

Table 11 Pin Capacitance

7.5 Power-on/Power-off Characteristics

To protect data during initial power-up and power-up after a power dropped, the chip can not complete read or write operations if VCC falls below the specified minimum voltage (VCC(min)). VCC(min) refers to the minimum specified VCC value for normal chip operation, which is 2.7V in this chip, and VCC(max) refers to the maximum specified VCC value for normal chip operation, which is 3.6V in this chip.

During initial power-up or power-up after power dropped, the chip must wait for tPU (power-up delay time) after the voltage reaches V_{CC}(min) before it can begin normal operation. This time ensures that the internal chip voltage has stabilized. tPU is measured from the time VCC reaches the specified minimum voltage (VCC(min)).

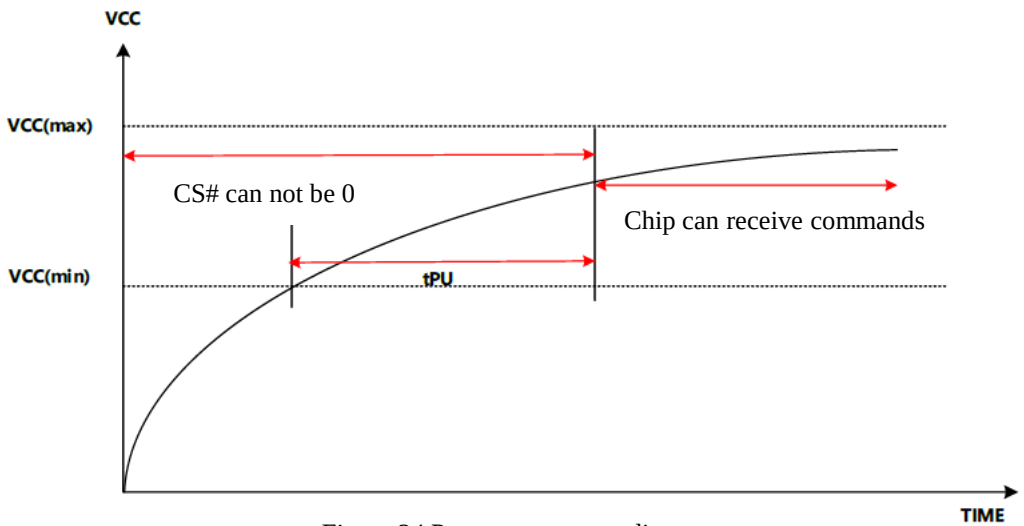


Figure 24 Power-on process diagram

During power-up, the following steps are required to properly initialize the chip:

1. Increase VCC (after t_{RVR});
2. During power-on, CS# must follow VCC (a 10KΩ pull-up resistor to VCC is recommended);
3. When VCC is below VCC(min), it is recommended not to send commands to the device;
4. During initial power-up or after a power-down and power-up, wait tPU before accessing the device;
5. After power-up, the device is in standby mode.

When the chip is powered-off or has a power outage, follow the following steps to properly shut down the device:

1. Lower VCC to below VCC_RST;
2. During power-off, CS# must follow VCC (a 10kΩ pull-up resistor to VCC is recommended);
3. When VCC is below VCC(min), device selection and command sending are not permitted;
4. After powering down and VCC rises above VCC(min), the power-on initialization procedure must be followed;
5. To stabilize the VCC level, it is recommended to add an appropriate decoupling capacitor to the VCC pin;
6. If VCC rises to VCC from a voltage between VCC(min) and VCC_RST, the chip is not guaranteed to function properly.

Symbol	Description	Min.	Typical	Max.	Unit
t_{PU}	Power-on delay time	100	-	-	μs
t_{RVR}	Rise time from VCC to VCC (min)	-	-	30	ms
t_{RVF}	Fall time from VCC to VCC_RST	20	-	-	μs
VCC_RST	VCC reset voltage	0	-	2	V
t_{PLOL}	VCC low level time	50	-	-	ms

Table 12 Chip power-on/power-off parameters

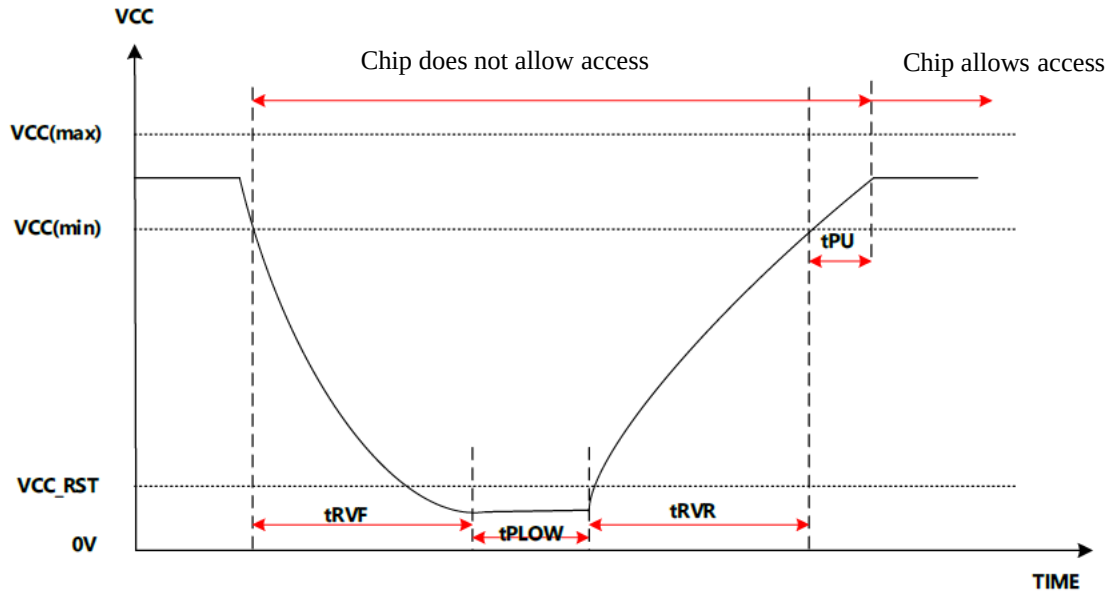
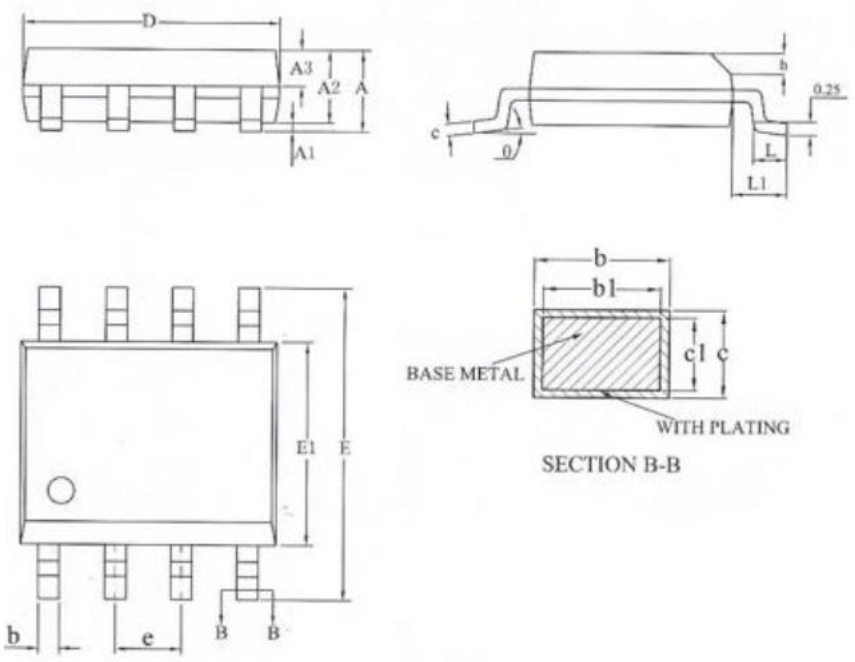


Figure 25 Power-off then Power-on process

8 Precautions for Use

It is recommended that users program the chip after reflow soldering, because the chip cannot guarantee that the data written before reflow soldering will still be valid after reflow soldering.

9 Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 26 Chip Package Outline

10. Product naming Rules

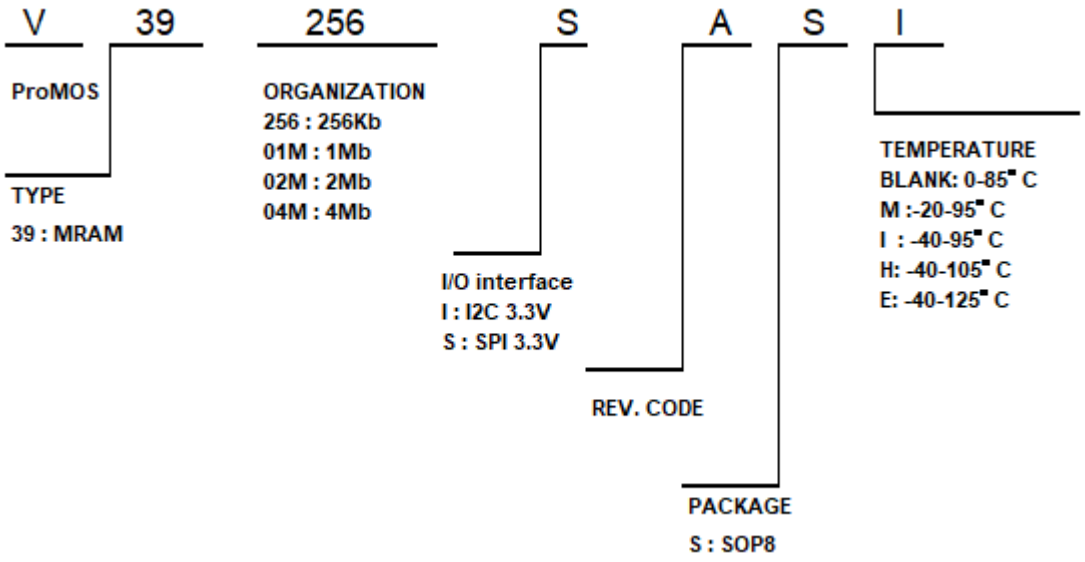


Figure 27 Naming rule description