SK hynix UFS Product Family
UFS 3.1 Compatible
1.1 Version.

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http://www.skhynix.com/en/index.jsp

Revision History

Revision No.	History	Draft Date	Remark
0.1	Preliminary version	Feb. 20, 2021	
1.0	Official Released Version	Aug. 30. 2021	
1.1	VDDIQ connection value change 1 -> 2.2uF Only support the Large Amplitude (LA) output level	Sep. 30. 2021	

Table of Contents

1. SK hynix UFS Introduction

1.1 General Description

SK hynix UFS product consists of NAND flash and UFS controller.
UFS has the built-in intelligent controller which manages interface protocols, wear leveling, bad block management, garbage collection, and ECC. The first UFS of SK hynix is compatible with JEDEC standard UFS3.1 specification and supports UniPro v1.8 and M-PHY v4.1 (Backward compatible with UniPro v1.61 and M-PHY v3.1)

1.2 Product Line-up

Density	Part Number	NAND Stack	PKG size (mm)	Package Type
128GB	HN8T05DEHKX073	512Gb x2	11.0 x 13.0 x 0.8	153FBGA
256GB	HN8T15DEHKX075	512Gb x4		
512GB	HN8T25DEHKX077	512Gb x8		
1TB	HN8T35DZHKX079	512Gb x16	11.0 x 13.0 x 1.0	

1.3 Key Features

- **UFS3.1 compatible**
  - backward compatibility with UFS3.0 & UFS2.2

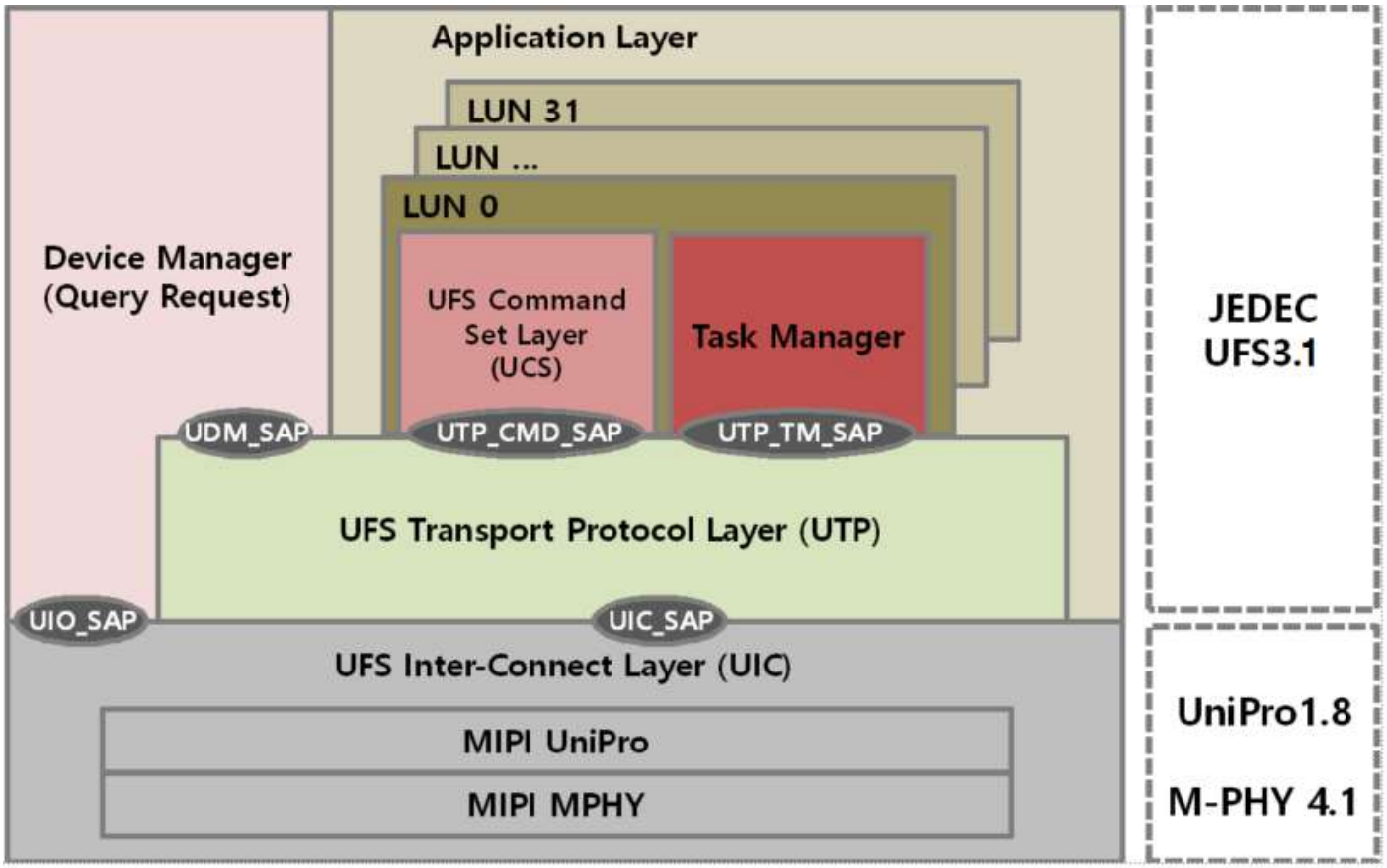
- **Operating Voltage Range**
  - V_{cc} (NAND) : 2.4V - 2.7V
  - V_{ccq} (CTRL) : 1.14V - 1.26V
  - V_{ccq2} (CTRL) : Not Used

- **Temperature**
  - Operation Temperature (-25℃ ~ +85℃)
  - Storage Temperature (-40℃ ~ +85℃)

- **Reference**
  - JEDEC UFS Specification V3.1
  - MIPI UniPro Specification V1.8
  - MIPI M-PHY Specification V4.1
  - JEDEC UFS HPB Extension v2.0

- **Supported Features**
  - Erase / Discard / Purge / Wipe
  - PWM G1~G4 / HS-G1~G4
  - 1L/2L
  - Command Queuing / Cache
  - Multi Region RPMB / BOOT LU
  - Power-on/HW/EndPoint/LU Reset
  - BKOP
  - High Priority LU
  - Reliable Write Operation
  - Write Protect, Secure Write Protect
  - Task Management operations
  - Secure Removal Type
  - Power Management operations
  - MAX 32 LU supported
  - Device Health Descriptor
  - Field Firmware Update
  - Host Performance Booster (HPB)
  - WriteBooster

1.4 UFS Architecture

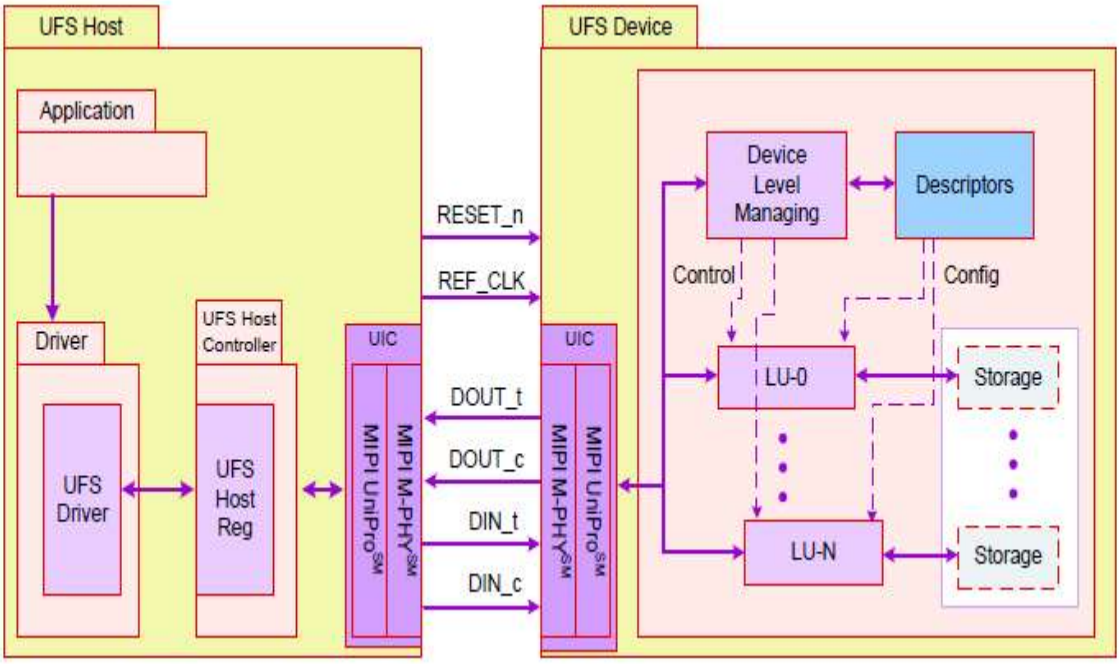


1.4.1 Reference Documents

1) JEDEC STANDARD Universal Flash Storage (UFS) Version 3.1 JESD220E
2) MIPI Alliance M-PHY Version 4.1
3) MIPI Alliance Unified Protocol (UniPro) Version 1.8
4) SAM, SCSI Architecture Model-5 (SAM-5), Revision 05, 19 May 2010
5) SPC, SCSI Primary Commands-4 (SPC-4), Revision 27, 11 Oct. 2010
6) SBC, SCSI Block Commands-3 (SBC-3) Revision 24, 05 Aug. 2010
7) JEDEC STANDARD Universal Flash Storage (UFS) Host Performance Booster(HPB) Version 2.0 JESD220D-3A

1.5 UFS System Model

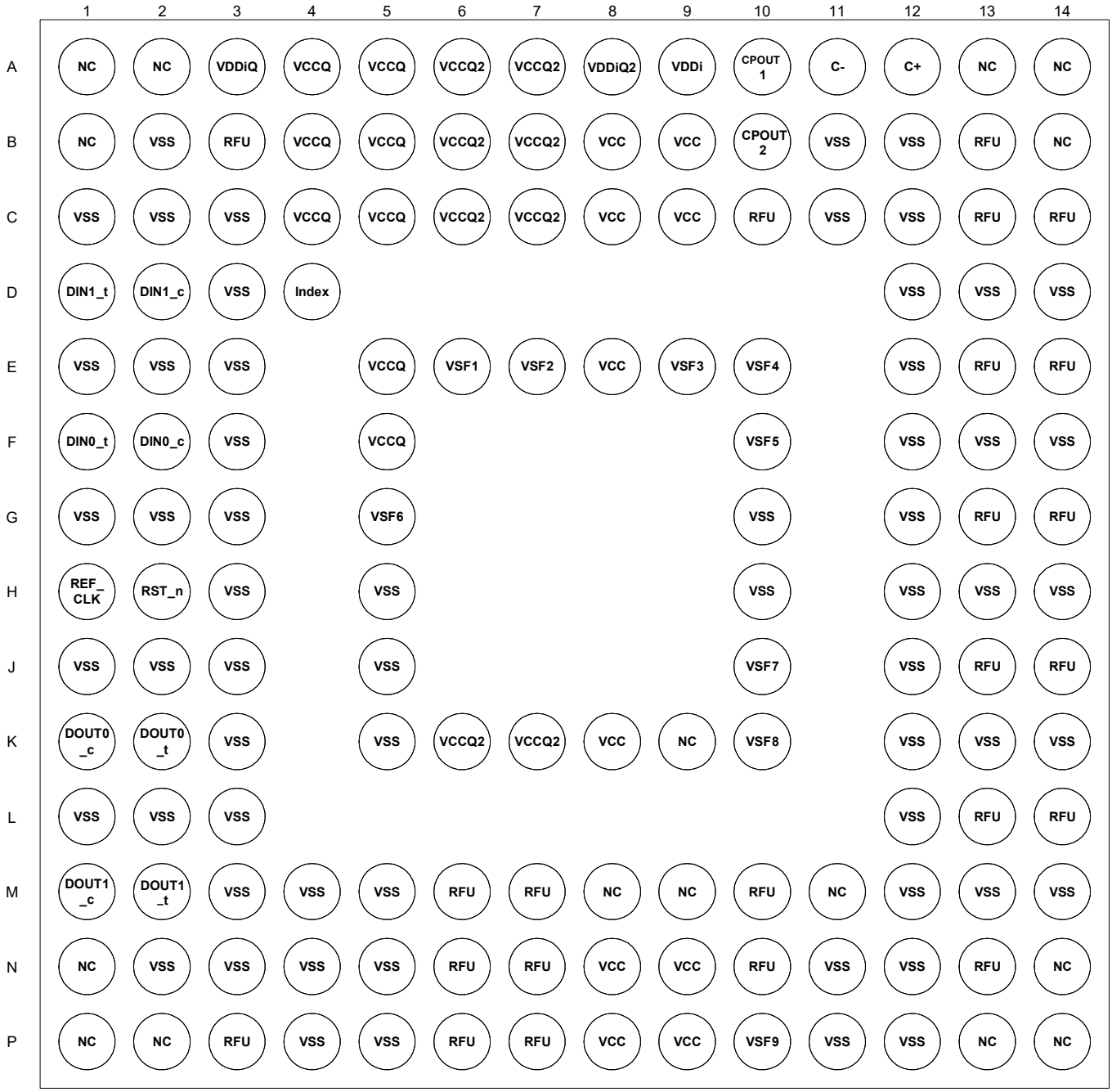
The Figure 1-1 shows an example of UFS system. It shows how an UFS host is connected to an UFS device, the position of UFS host controller and its related UFS HCI interface.



[Figure 1-1] UFS System Model

2. Package Configurations

2.1 Package Ball Map



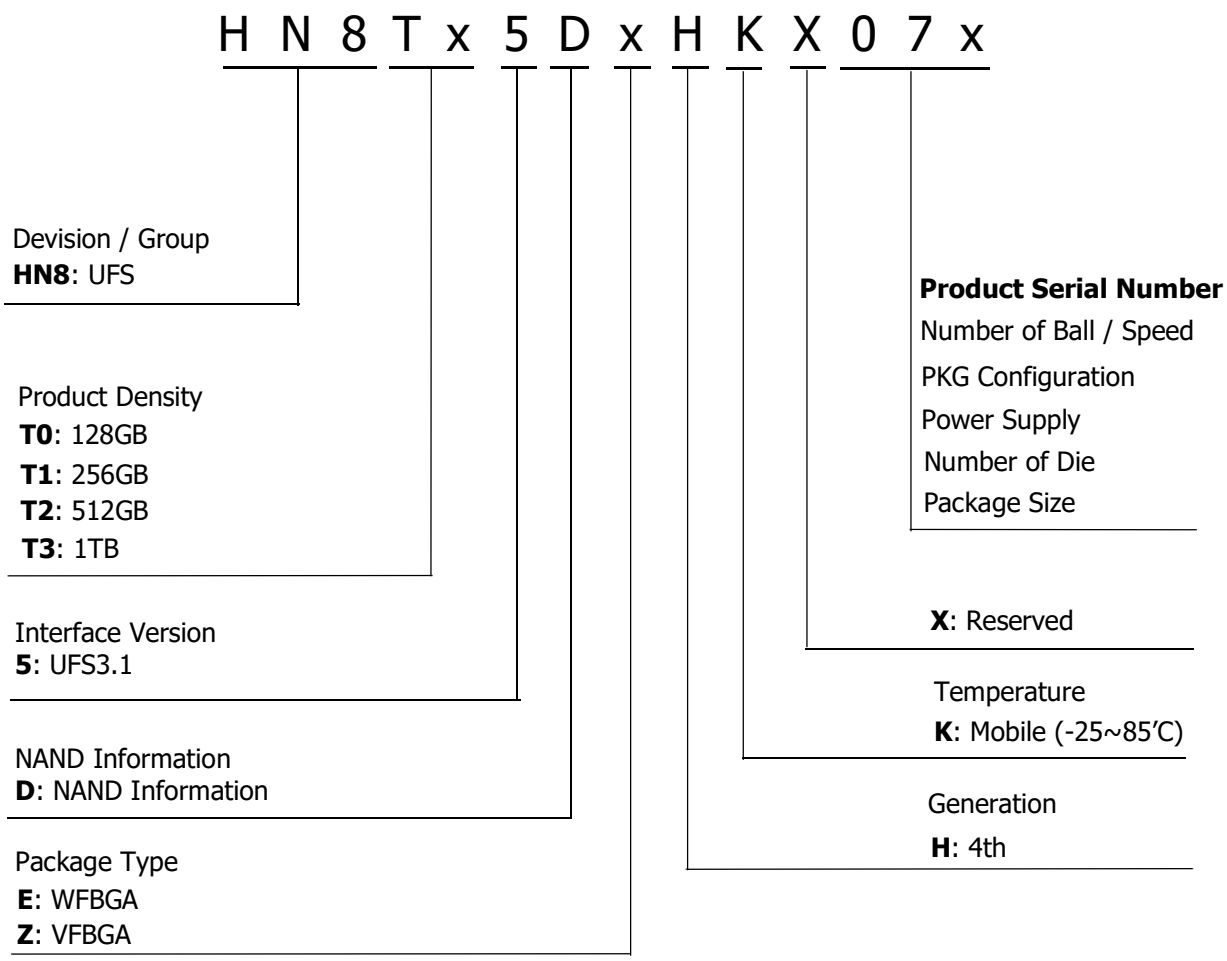
[Figure 2-1] 153 FBGA Ball Assignment

2.2 Pin Description

Name	Type	Pin No.	Description
V_{cc}	Supply	B8~9, C8~9, E8, K8, N8~9, P8~9	2.5V supply voltage for the memory devices
V_{ccq}	Supply	A4~5, B4~5, C4~5, E5, F5	1.2V supply voltage for the memory controller
V_{ccq2}	Supply	A6~7, B6~7, C6~7, K6~7	1.8V supply voltage for the memory controller Not used internally for SK hynix's UFS3.1
VDDi	Input	A9	Input terminal to provide bypass capacitor for internal regulator. No need to connect external capacitor.
VDDiQ	Input	A3	Input terminal to provide bypass capacitor for internal regulator. Connect 2.2µF capacitor from VDDiQ to ground.
VDDiQ2	Input	A8	Input terminal to provide bypass capacitor for internal regulator. No need to connect external capacitor.
Vss	Supply	B2, B11~12, C1~3, C11~12, D3, D12~14, E1~3, E12, F3, F12~14, G1~3, G10, G12, H3, H5, H10, H12~14, J1~3, J5, J12, K3, K5, K12~14, L1~3, L12, M3~5, M12~14, N2~5, N11~12, P4~5, P11~12	Supply voltage ground
RST_n	Input	H2	Input hardware reset signal. This is an active low signal.
REF_CLK	Input	H1	Input reference clock
DIN0_t DIN0_c	Input	F1 / F2	Downstream data lane 1. Differential input signals into UFS device from the host. DIN0_t is the positive node of the differential signal pair.
DIN1_t/ DIN1_c	Input	D1 / D2	Downstream data lane 2. Differential input signals into UFS device from the host.
DOUT0_t/ DOUT0_c	Output	K2 / K1	Upstream data lane 1. Differential output signals from the UFS device to the host. DOUT0_t is the positive node of the differential signal pair.
DOUT1_t/ DOUT1_c	Output	M2 / M1	Upstream data lane 2. Differential output signals from the UFS device to the host.
C+/C-	Input	A12 / A11	Optional charge pump capacitor terminal. Not used internally for SK hynix's UFS3.1
CPOUT1/ CPOUT2	Input	A10 / B10	Optional charge pump output capacitor terminal. Not used internally for SK hynix's UFS3.1
NC	Input		No connect
RFU	-		Reserved for Future Use
VSF	-	E6, E7, E9, E10, F10, G5, J10, K10, P10	Vendor Specific Function. SK hynix uses G5, E10, K10, P10 as VSF pin

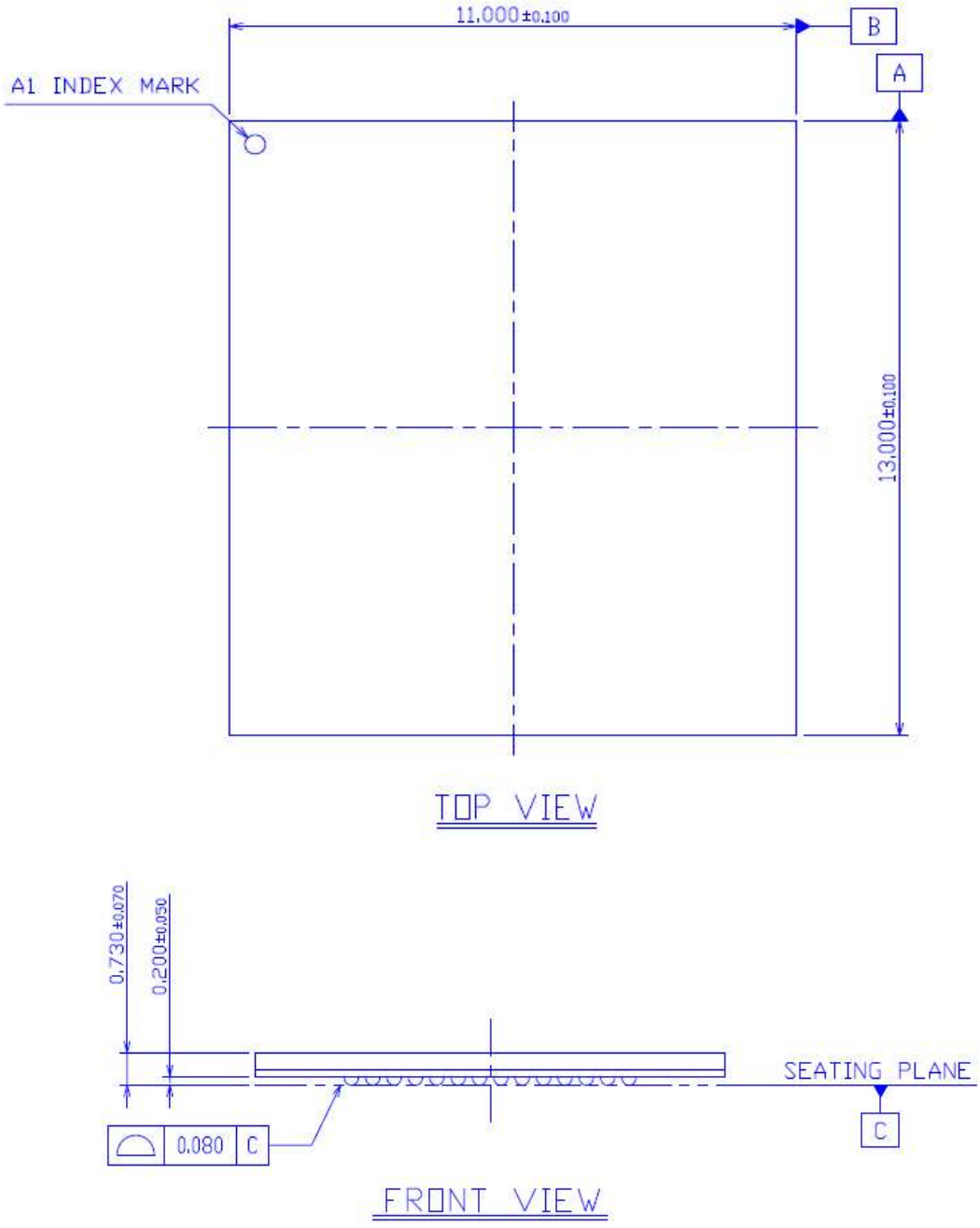
[Table 1] 153 FBGA Pin Description

2.3 Ordering Information

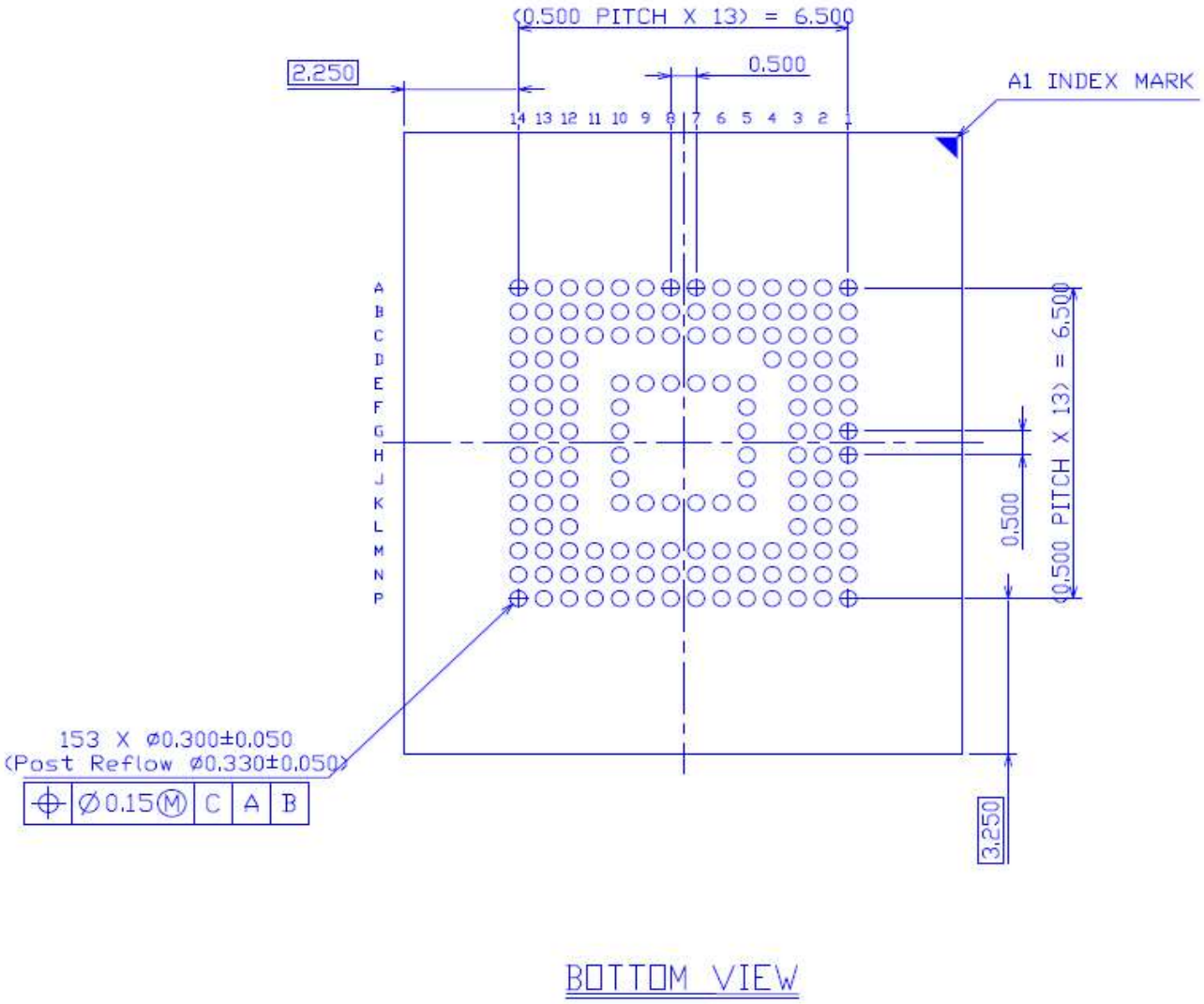


2.4 Package Mechanical Drawing

■ **11.0mm x 13.0mm x 0.8mm**

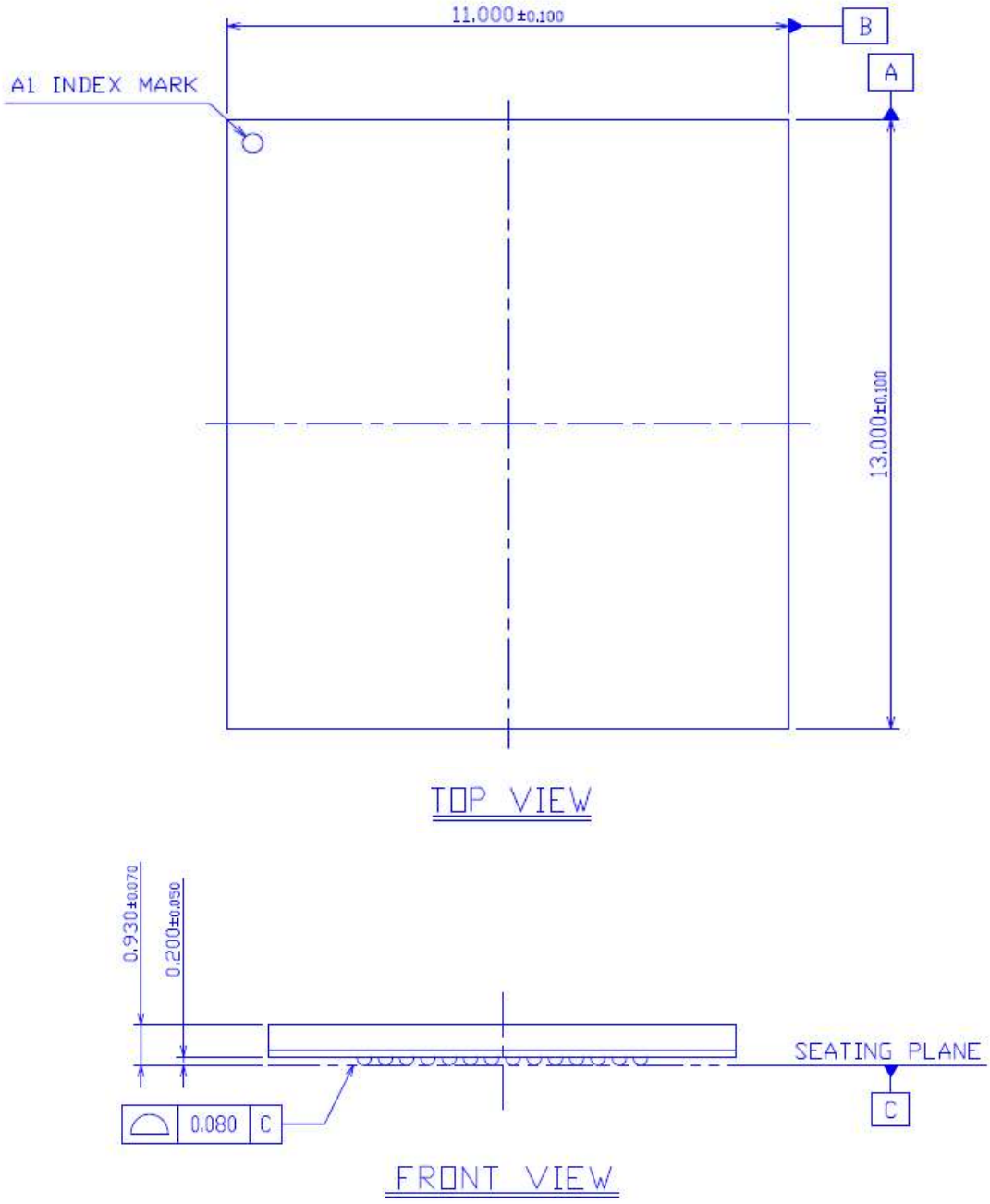


[Figure 2-2] Package Dimension Top and Side

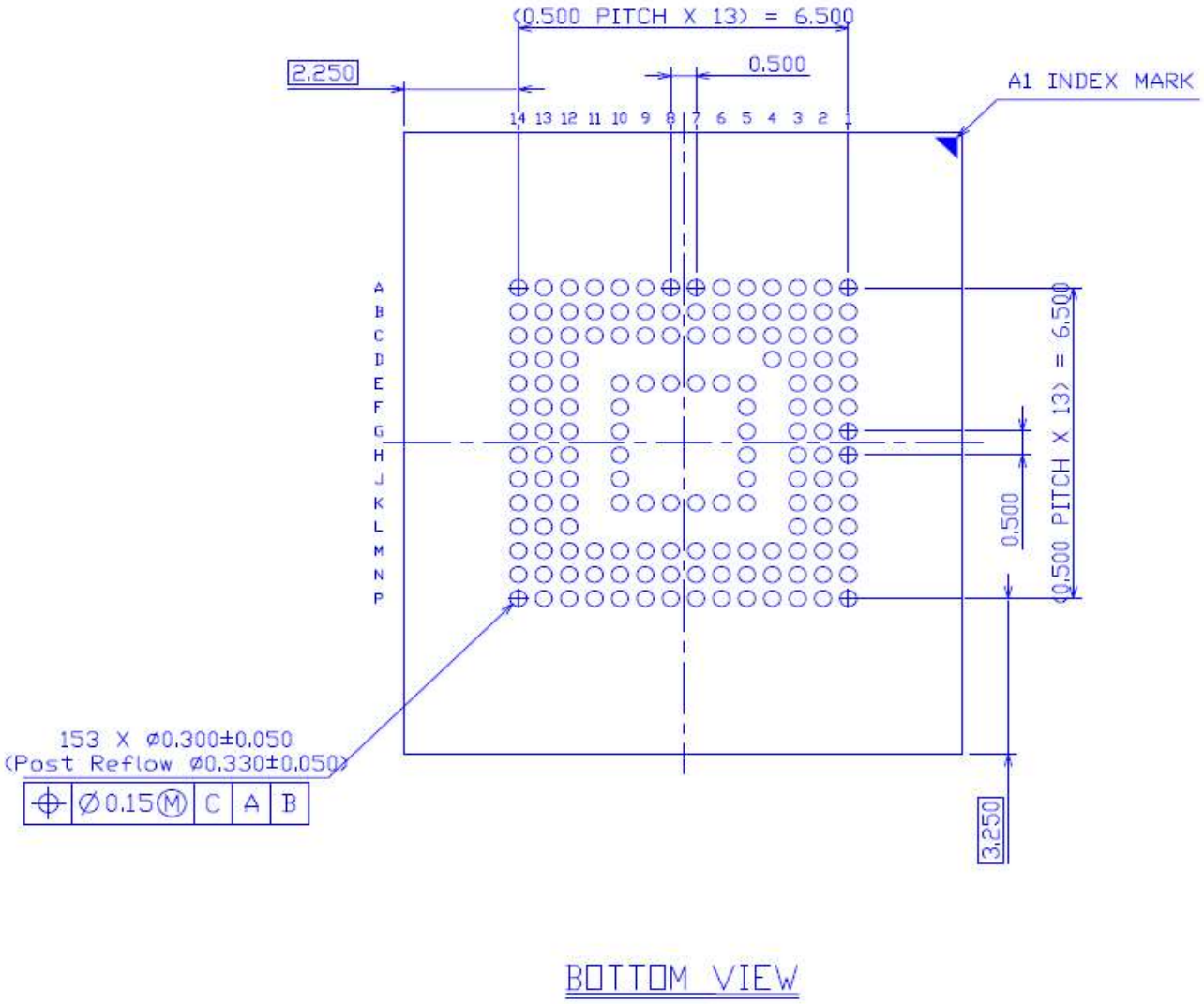


[Figure 2-3] Package Dimension Bottom

■ **11.0mm x 13.0mm x 1.0mm**

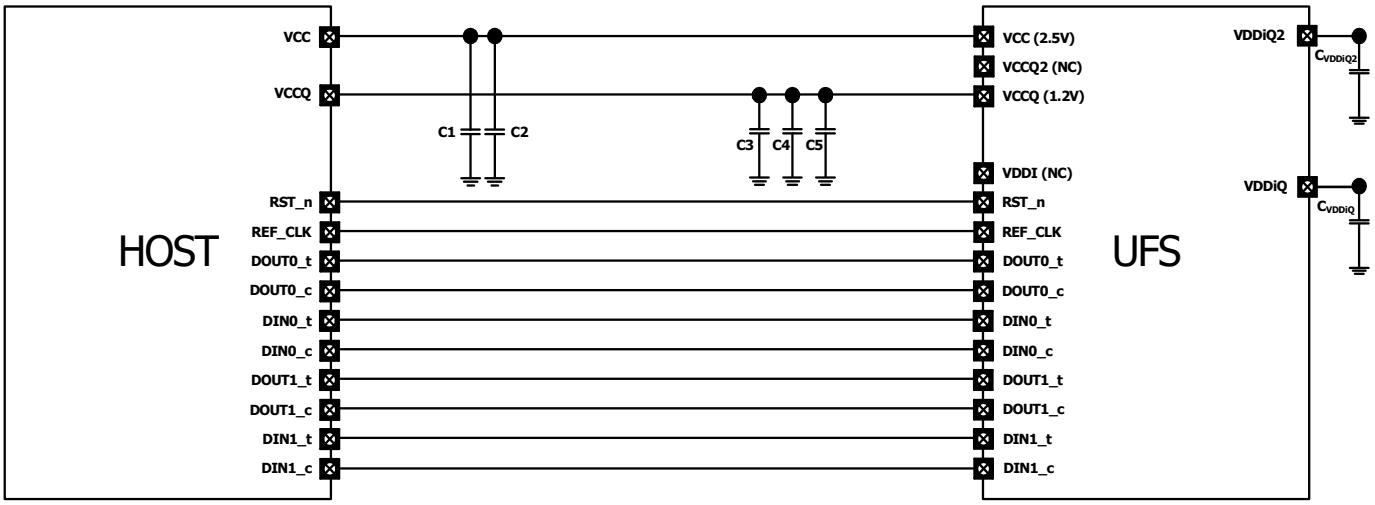


[Figure 2-4] Package Dimension Top and Side



[Figure 2-5] Package Dimension Bottom

2.5 Connection Guide



[Figure 2-6] Connection Guide Diagram

- If host does not support 2nd lane, then make 2nd signal line(DIN1_t, DIN1_C, DOUT1_t, DOUT1_C) floating.

[Unit : µF]

Parameter	Symbol	Min	Max	Recommend	Remark
V_{cc} (2.5V)	C_1	4.7	10	4.7	Capacitor should be connected with V_{cc} and Vss as close as possible
	C_2	0.1	1	0.1	
V_{ccq} (1.2V)	C_3	4.7	10	4.7	Capacitor should be connected with V_{ccq} and Vss as close as possible
	C_4 (Optional)	0	1	1	
	C_5	0.1	1	0.1	
VDDiQ	C_{VDDiQ}	1	4.7	2.2	Capacitor should be connected with V_{DDiQ} and V_{SS} as close as possible
VDDiQ2	C_{VDDiQ2} (Optional)	0	4.7	1	Capacitor should be connected with V_{DDiQ2} and V_{SS} as close as possible The connection of C_{VDDiQ2} capacitor that would be nice to have

[Table 2] Connection Guide Specification

3. UFS Characteristics

3.1 Performance

Density	Sequential (MB/s)		Test Condition
	Read	Write (Write-Booster On/Off)	
128GB	1,000	1,000/260	HS-G4B 1L Fast Mode
256GB	1,000	1,000/500	
512GB	1,000	1,000/500	
1TB	1,000	1,000/500	
128GB	1,800	1,000/260	HS-G4B 2L Fast Mode
256GB	2,000	1,600/500	
512GB	2,000	1,600/500	
1TB	2,000	1,600/500	

- Device level test without file system overhead.
- Queue depth 8
- Seq. Chunk size : 512KB
- Enabled feature : Cache on

3.2 Power

UFS Power Mode Management

UFS Power Mode	Unipro Power Mode	M-PHY Power Mode	V_{cc} Power	V_{ccq} Power
Active	FAST_STATE	HS-BURST	On	On
Idle	SLEEP_STATE	STALL	On	On
Hibernate	HIBERNATE_STATE	HIBERN8	On	On
Sleep	HIBERNATE_STATE	HIBERN8	Off[1)]	On
PowerDown	OFF_STATE	UNPOWERED	Off[1)]	Off[1)]
DeepSleep	OFF_STATE	UNPOWERED	Off[1)]	Off[1)]

- NOTE 1 Host may turn off the power for power consumption reduction.

3.2.1 Active Power Mode

Density	HS Gear4 x 1 lane		HS Gear4 x 2 lane	
	I_{CC}	I_{CCQ}	I_{CC}	I_{CCQ}
128GB	330mA	450mA	330mA	550mA
256GB	330mA	450mA	330mA	550mA
512GB	330mA	460mA	330mA	560mA
1TB	330mA	480mA	330mA	580mA

- V_{cc} = 2.5V, V_{ccq} = 1.2V, V_{ccq2} Not Used Internally
- HS-G4B 1L/2L Fast Mode, Not 100% tested
- The measurement for max RMS current is the average RMS current consumption over a period of 100ms.
- Room Temperature 25℃ Condition

3.2.2 Hibernate Power Mode

Density	HS Gear4 x 1 lane		HS Gear4 x 2 lane	
	I_{CC} (2.5v) 1)	I_{CCQ} (1.2v) 1)	I_{CC} (2.5v) 2)	I_{CCQ} (1.2v) 2)
128GB	30uA	340uA	30uA	340uA
256GB	60uA	360uA	60uA	360uA
512GB	120uA	400uA	120uA	400uA
1TB	240uA	480uA	240uA	480uA

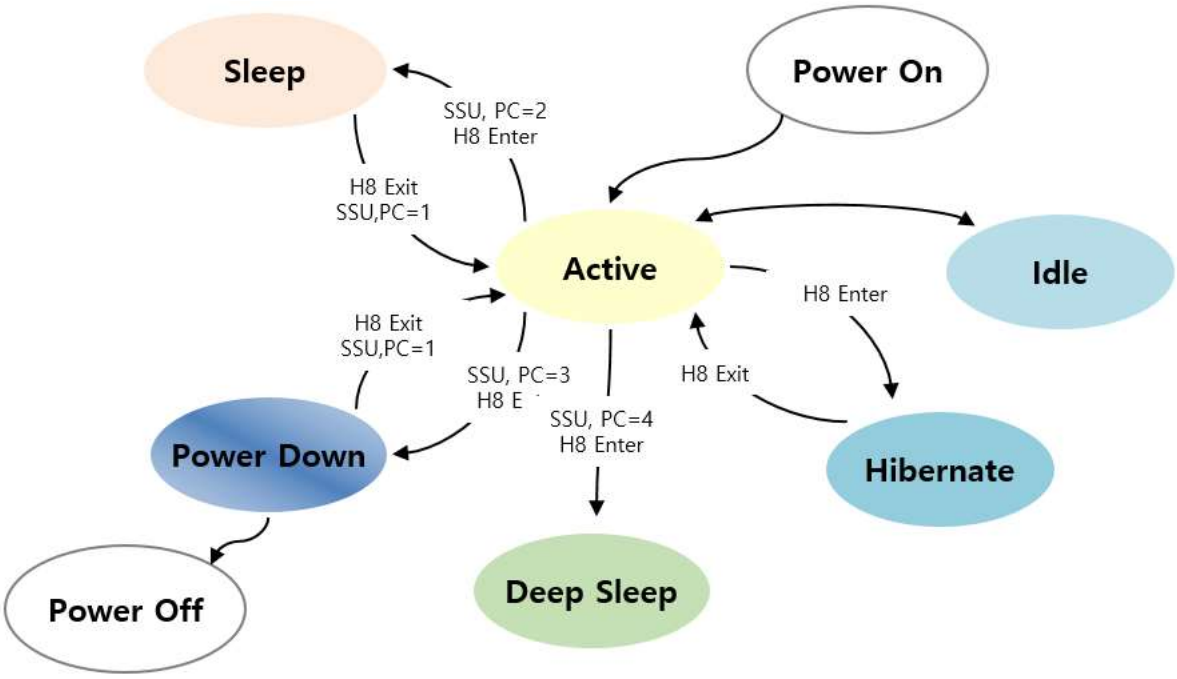
- Host shall issue "HIBERN8 Enter" to enter hibernate power mode. Room Temperature 25'C over a period of 100ms
- NOTE 1 Not 100% tested, Typical Value.
- NOTE 2 The measurement for max RMS current is the average RMS current consumption over a period 100ms

3.2.3 Sleep Power Mode

Density	HS Gear4 x 1 lane		HS Gear4 x 2 lane	
	I_{CC} (2.5v) 1)	I_{CCQ} (1.2v) 1)	I_{CC} (2.5v) 2)	I_{CCQ} (1.2v) 2)
128GB	0μA	340uA	0μA	340uA
256GB	0μA	360uA	0μA	360uA
512GB	0μA	400uA	0μA	400uA
1TB	0μA	480uA	0μA	480uA

- Host shall issue SSU(Sleep) and "HIBERN8 Enter" to enter Sleep, Room Temperature 25'C over a period of 100ms
- V_{cc} Off (V_{cc} = 0V)
- NOTE 1 Not 100% tested, Typical Value
- NOTE 2 The measurement for max RMS current is the average RMS current consumption over a period 100ms

3.2.4 UFS Power Mode Transition Diagram



[Figure 3-1] Power Mode State

- Host shall issue "Hibern8 enter" to enter hibernate power mode.
- In Sleep power mode, V_{cc} may be turned off to reduce power consumption.
- Both V_{cc} and V_{ccq} may be turned off at PowerDown mode.
- The only way to exit from DeepSleep Power mode is using a hardware reset or a power cycle

3.2.5 VCC Power Down Sequence

- Once Vcc drops under 2.0v, it shall be driven down Vcc to below 0.5v and stay low for at least 1ms before Vcc powered up

3.2.6 VCCQ Power Down Sequence

- Once Vccq drops under 1.1v, it shall be driven down Vccq to below 0.2v and stay low for at least 1ms before Vccq powered up

3.3 Temperature & Humidity

3.3.1 Temperature Condition

Density	Temperature	Remark
Operation Temperature[1)]	-25℃ ~ 85℃	-
Storage Temperature	-40℃ ~ 85℃	-

● NOTE 1 The operating temperature is the UFS case surface temperature on the center of top side of the case

3.3.2 Humidity Condition

Density	Humidity	Remark
Operation Humidity	0% RH ~ 95% RH (Non-Condensing)	-
Storage Humidity	0% RH ~ 95% RH (Non-Condensing)	-

3.4 Bandwidth

Bandwidth	Description	Remark
PWM-G1	3 ~ 9 Mbps	Mandatory
PWM-G2	6 ~ 18 Mbps	Mandatory
PWM-G3	12 ~ 36 Mbps	Mandatory
PWM-G4	24 ~ 72 Mbps	Mandatory
HS-G1	Rate A = 1,248 Mbps (19.2/38.4/26 MHz) Rate B = 1,459.2 Mbps (19.2/38.4 MHz) 1,456 Mbps (26 MHz)	Mandatory
HS-G2	Rate A = 2,496 Mbps (19.2/38.4/26 MHz) Rate B = 2,918.4 Mbps (19.2/38.4 MHz) 2,912 Mbps (26 MHz)	Mandatory
HS-G3	Rate A = 4,992 Mbps (19.2/38.4/26 MHz) Rate B = 5,836.8 Mbps (19.2/38.4MHz) 5,824 Mbps (26 MHz)	Mandatory
HS-G4	Rate A = 9,984 Mbps (19.2/38.4/26MHz) Rate B = 11,673.6 Mbps (19.2/38.4MHz) 11,648.0 Mbps (26MHz)	Mandatory

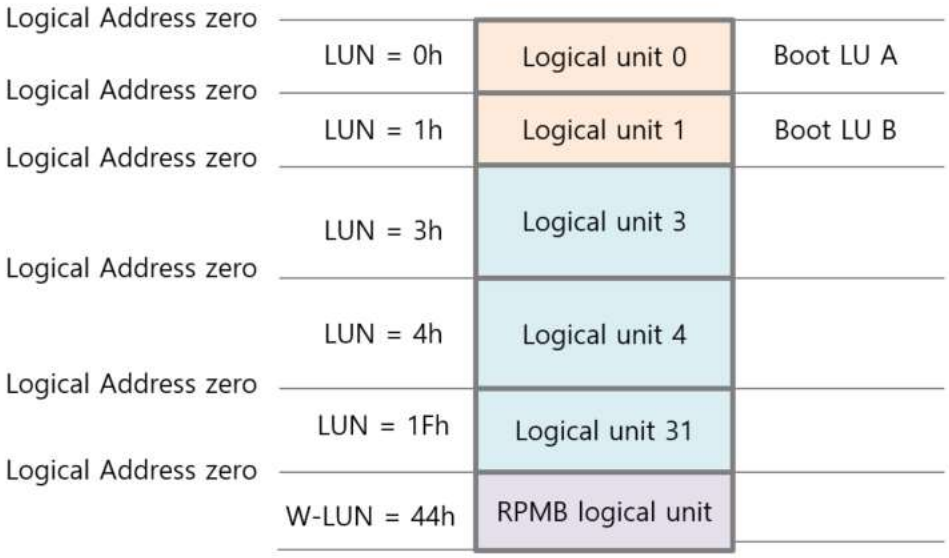
3.5 User Density Size

Capacity	User Density	Ratio	qTotalRawDeviceCapacity
128GB	119.16GB	93.1%	0x0EE64000
256GB	238.33GB	93.1%	0x1DCBC000
512GB	476.67GB	93.1%	0x3B96C000
1TB	953.34GB	93.1%	0x772D8000

- User Density and Ratio are the values before LU configuration
- RPMB Size is excluded in User density size.

3.6 Device LU Partitioning

UFS Device shall support up to 32 Logical Units and one RPMB LU. Two of 32 Logical Units can be configured as boot LU A & B.



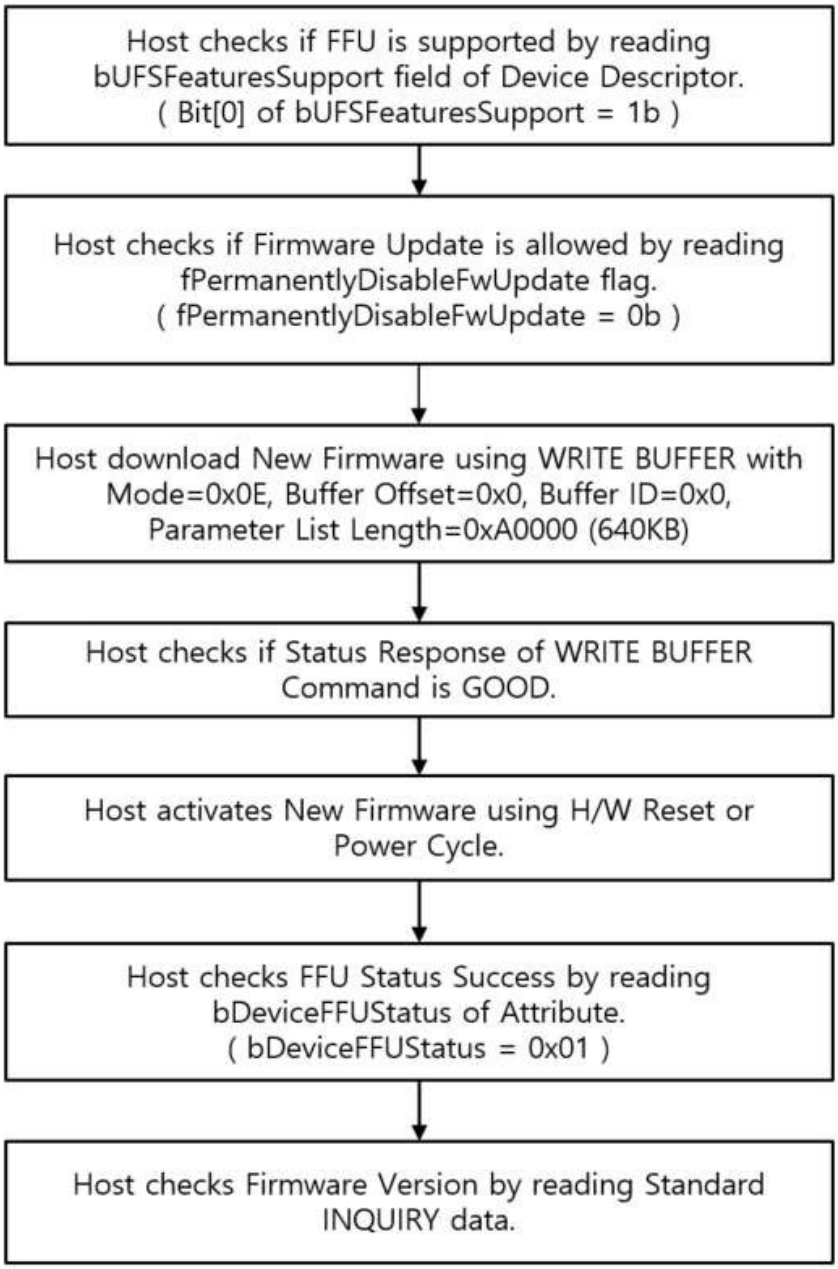
[Figure 3-2] Example of UFS Device Memory Organization

LUs	Supported Size
BOOT LU	4MB ~ 256MB
RPMB LU	16MB

4. UFS Feature Notes

4.1 Field Firmware Update (FFU)

SK hynix supports microcode download based Field Firmware Update using WRITE BUFFER command. For more details, see as the following chart like given below.



[Figure 4-1] FFU Flow Chart

4.1.1 WRITE BUFFER Command Parameters

WRITE BUFFER Command Parameters				
Byte	**Bit**	**Parameters**	**Value**	**Remark**
0	7:0	OPCODE	3Bh	
1	4:0	MODE	0Eh	Field Firmware Update
2	7:0	BUFFER ID	00h	Buffer 0 supported
3:5	7:0	BUFFER OFFSET	00h	Buffer 0 byte offset
6:8	7:0	PARAMETER LIST LENGTH	A0000h	F/W binary size in bytes (640KB)
9	7:0	CONTROL	00h	

4.1.2 FFU related parameters in Device Descriptor

FFU related Fields of Device Descriptor				
Offset	**Size**	**Name**	**MDV**	**Remark**
1Fh	1	bUFSFeaturesSupport	B1h	FFU feature supported TOO-HIGH/TOO-LOW_TEMPERATURE supported Host Performance Booster (HPB)
20h	1	bFFUTimeout	03h	Max FFU Timeout is 3 seconds.

4.1.3 FFU related parameters in Attributes

FFU related Attribute				
IDN	**Size**	**Name**	**Access Property**	**Remark**
14h	1	bDeviceFFUStatus	Read Only	Device FFU Status 00h: No information 01h: Successful microcode update 02h: Microcode corruption error 03h: Internal error 04h: Microcode version mismatch 05h-FEh: Reserved FFh: General Error

4.2 Supported VPD Pages

SK hynix supports VPD pages like below table.

EVPD	Page Code	VPD Page Name
0	00h	Standard INQUIRY Data
1	00h	Supported VPD Pages VPD page
1	80h	Unit Serial Number VPD page
1	83h	Device Identification VPD page
1	86h	Extended INQUIRY Data VPD page
1	87h	Mode Page Policy VPD page
1	B0h	Block Limits VPD Page
1	B1h	Block Device Characteristics VPD Page
1	B2h	Thin Provisioning VPD page

4.3 Mode Pages

SK hynix supports UFS supported pages.

Page Code		SUBPage Code	Page Name	Support
00h		-	Vendor specific	Not Support
01h ~ 1Fh (SCSI Specific)	0Ah	00h (Device specific STANDARD page)	CONTROL	Support
	01h		READ-WRITE ERROR RECOVERY	Support
	08h		CACHING	Support
	-	01h~DFh	Device Specific SUBPAGE	Not Support
	-	E0h~FEh	Vendor Specific SUBPAGE	Not Support
	-	FFh	ALL SUBPAGES	Not Support
20h ~ 3Eh (Vendor Specific)	-	00h	Vendor Specific STANDARD	Not Support
	-	01h~FEh	Vendor Specific SUBPAGE	Not Support
	-	FFh	ALL SUBPAGES	Not Support
3Fh (Return ALL pages)	3Fh	00h	ALL PAGES	Support
	3Fh	01h~FEh	Reserved	Reserved
	3Fh	FFh	ALL SUBPAGES	Not Support

5. UFS General Parameters

5.1 Power Supplies

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage (memory)	V_{cc}	2.4	2.7	V	
Supply Voltage (controller and IO)	V_{ccq}	1.14	1.26	V	
Supply Voltage (secondary for controller and IO)	V_{ccq2}	1.70	1.95	V	Not Used
Supply power-up for 2.5V	tPRUH		35	ms	
Supply power-up for 1.8V	tPRUL		25	ms	Not Used
Supply power-up for 1.2V	tPRUV		20	ms	

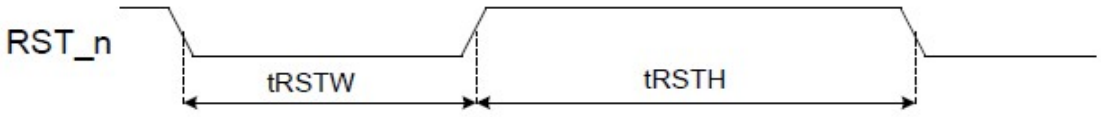
5.2 Reset Signal

5.2.1 Reset Signal Electrical Parameters

Parameter	Symbol	Min	Max	Unit	Remark
Input HIGH voltage	V_{IH}	0.65 * VCCQ	VCCQ + 0.3	V	
Input LOW voltage	V_{IL}	VSS - 0.3	0.35 * VCCQ	V	

5.2.2 Reset Timing Parameters

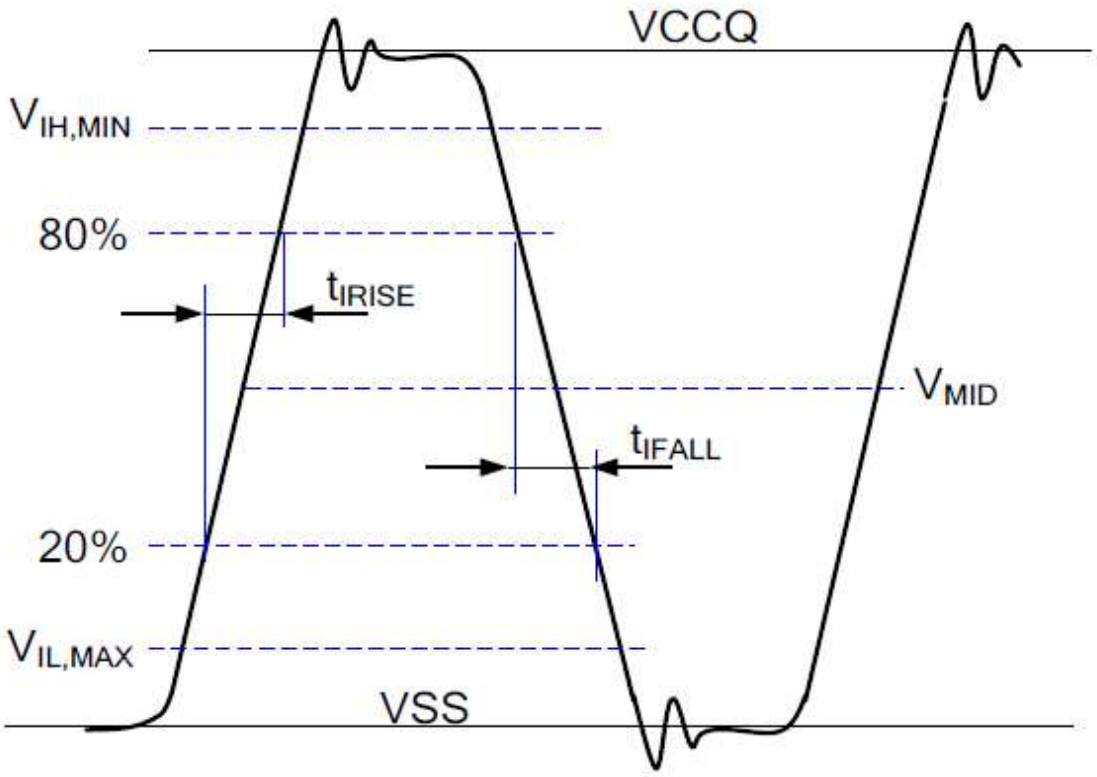
Symbol	Min	Max	Unit	Description
tRSTW	1	-	µs	RST_n Pulse Width
tRSTH	1	-	µs	RST_n High Period (Interval)
tRSTF	100	-	ns	RST_n Filter



[Figure 5-1] Reset Timing

5.3 Reference Clock

The M-PHY specification defines the reference clock optional for the State Machine Type I [MIPI M-PHY].



[Figure 5-2] Clock Input Levels, Rise Time, and Fall Time

Parameter	Symbol	Min	Max	Unit	Remark
Frequency	f_{ref}	19.2 **26 (Default)** 38.4		MHz	1
Frequency Error	f_{ERROR}	-150	+150	ppm	
Input High Voltage	V_{IH}	0.65*VCCQ	VCCQ+0.3	V	2
Input Low Voltage	V_{IL}	VSS-0.3	0.35*VCCQ	V	2
Input Clock Rise Time	t_{IRISE}	-	2	ns	3
Input Clock Fall Time	t_{IFALL}	-	2	ns	3
Duty Cycle	t_{DC}	45	55	%	4
Phase Noise	N	-	-66	dBC	5
Noise Floor Density (REFCLK Noise floor density from 50KHz to 10MHz)	$N_{Density}$	-	-140	dBC/Hz	6
Input Impedance	RL_{RX}	100		kΩ	7
	CL_{RX}	5		pF	
Input Leakage Current	I_{LKG}	-	10	μA	

- NOTE 1 HS-BURST rates A and B are achieved with integer multipliers of f_{ref}.
- NOTE 2 Figure 5-2 shows the input levels V_{IL}, MAX to V_{IH}, MIN.
- NOTE 3 Clock rise time and clock fall time shall be measured from 20% to 80% of the window defined by V_{IL}, MAX to V_{IH}, MIN
- NOTE 4 Clock duty cycle shall be measured at the Crossings of the REF_CLK signal with the midpoint VMID, defined as: VMID = (V_{IL},MAX + V_{IH},MIN) / 2
- NOTE 5 Integrated single side band phase noise from 50KHz to 10MHz. This parameter refers to the random jitter only.
- NOTE 6 White noise floor. This parameter refers to the random jitter only.
- NOTE 7 RL_{RX} and CL_{RX} include Rx package and Rx input impedance.

5.4 Bus Signal Levels

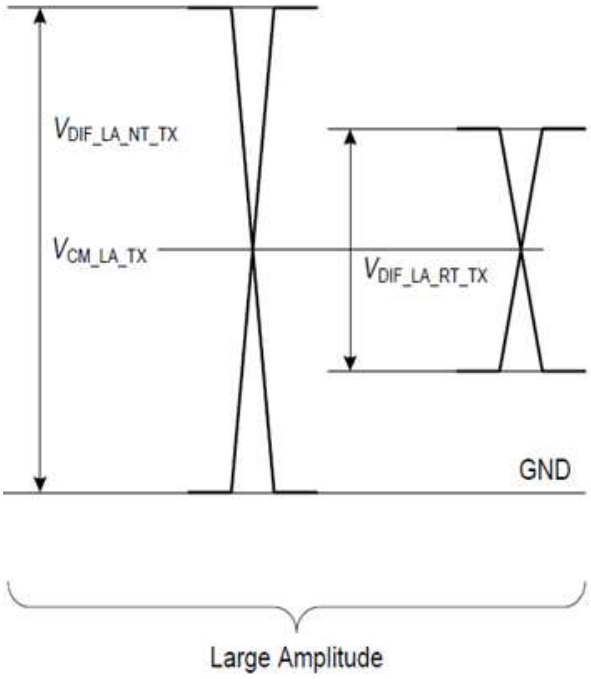
5.4.1 Output Level

SK hynix UFS supports the Large Amplitude (LA).
Every M-TX in every LINK will start communication with LA after power up or reset.

DOUT_t / DOUT_c pair should satisfy VCM_TX

$$V_{CM\_TX}(t) = \frac{V_{TXDP}(t) + V_{TXDN}(t)}{2}$$

V_{TXDP} / V_{TXDN} = Positive / Negative Signal Voltage



[Figure 5-3] M-TX Signal Levels

5.4.1.1 Common M-TX Parameters

Symbol	Min	Max	Unit	Description
$V_{DIF\_DC\_LA\_RT\_TX}$	160	300	mV	Large Amplitude differential TX DC voltage when the M-TX is terminated
$V_{DIF\_AC\_LA\_RT\_TX}$	140	310	mV	Large Amplitude differential TX AC voltage when the M-TX is terminated
$V_{DIF\_DC\_LA\_NT\_TX}$	320	600	mV	Large Amplitude differential TX DC voltage when the M-TX is NOT terminated
$V_{DIF\_AC\_LA\_NT\_TX}$	280	620	mV	Large Amplitude differential TX AC voltage when the M-TX is NOT terminated
$V_{CM\_LA\_TX}$	160	310	mV	Large Amplitude common-mode TX Voltage
R_{SE_TX}	40	60	Ω	Single-ended Output Resistance

5.4.2 Input Level

DIN_t / DIN_c pair should satisfy VCM_RX.

$$V_{CM\_RX}(t) = \frac{V_{RXDP}(t) + V_{RXDN}(t)}{2}$$

Symbol	Value		Unit	Description
	Min	Max		
M-RX Electrical				
$V_{DIF\_RT\_RX}$	60	310	mV	Differential RX voltage amplitude in terminated state. Defined for CJTPAT.
$V_{DIF\_NT\_RX}$	120	620	mV	Differential RX voltage amplitude when the M-RX is not terminated. Defined for CJTPAT
V_{CM_RX}	25	330	mV	RX common-mode voltage. Defined for CJTPAT
M-TX Resistance				
R_{DIF_RX}	80	110	Ω	Differential input resistance. Defined over V_{DIF_RX} Range.

6. Latency Time

Timing Parameter	Value	Remark
Read	MAX 100ms	
Write	MAX 200ms	
SYNC CACHE	MAX 300ms	
BKOP Termination Latency	MAX 40ms	bBackgroundOpsTermLat
Format (Wipe)	MAX 2 min	

- File system overhead is not considered
- Not 100% tested but tested with worst corner.

7. UPIU Transaction Codes

SK hynix UFS supports following UPIU transaction codes. Each command is used with corresponding UPIU. It is not allowed to use undefined codes. Refer to UFS specification for more detail information.

Initiator To Target	Transaction Code	Target to Initiator	Transaction Code
NOP Out	00 0000b	NOP In	10 0000b
Command	00 0001b	Response	10 0001b
Data Out	00 0010b	Data In	10 0010b
Task Management Request	00 0100b	Task Management Response	10 0100b
Reserved	01 0001b	Ready To Transfer	11 0001b
Query Request	01 0110b	Query Response	11 0110b
Reserved	01 1111b	Reject UPIU	11 1111b
Reserved	Others	Reserved	Others

7.1 UFS SCSI Command

Command name	Opcode	Command name	Opcode
FORMAT UNIT	04h	SECURITY PROTOCOL OUT	B5h
INQUIRY	12h	SEND DIAGNOSTIC	1Dh
MODE SELECT (10)	55h	START STOP UNIT	1Bh
MODE SENSE (10)	5Ah	SYNCHRONIZE CACHE (10)	35h
PRE-FETCH (10)	34h	SYNCHRONIZE CACHE (16)	91h
PRE-FETCH (16)	90h	TEST UNIT READY	00h
READ (6)	08h	UNMAP	42h
READ (10)	28h	VERIFY (10)	2Fh
READ (16)	88h	WRITE (6)	0Ah
READ BUFFER	3Ch	WRITE (10)	2Ah
READ CAPACITY (10)	25h	WRITE (16)	8Ah
READ CAPACITY (16)	9Eh	WRITE BUFFER	3Bh
REPORT LUNS	A0h	HPB READ	F8h
REQUEST SENSE	03h	HPB READ BUFFER	F9h
SECURITY PROTOCOL IN	A2h	HPB WRITE BUFFER	FAh

8. UFS Descriptors, Flags, Attributes

The UFS modules support following UFS descriptors defined in UFS specification. Refer to UFS specification for more detail information.

DESCRIPTOR TYPE	DESCRIPTOR IDN	DESCRIPTOR TYPE	DESCRIPTOR IDN
DEVICE	00h	RFU	06h
CONFIGURATION	01h	GEOMETRY	07h
UNIT	02h	POWER	08h
RFU	03h	DEVICE HEALTH	09h
INTERCONNECT	04h	RFU	0Ah~FFh
STRING	05h		

8.1 Device Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	59h	Size of this Descriptor
01h	1	bDescriptorIDN	00h	Device Descriptor Type Identifier
02h	1	bDevice	00h	00h: Device
03h	1	bDeviceClass	00h	00h: Mass Storage
04h	1	bDeviceSubClass	00h	00h: Embedded Bootable
05h	1	bProtocol	00h	00h: SCSI
06h	1	bNumberLU	User Conf.	Number of Logical Units (Default: 00h)
07h	1	bNumberWLU	04h	04h: 4 Well known logical units exist
08h	1	bBootEnable	User Conf.	00h: Boot feature disabled (Default) 01h: Bootable feature enabled
09h	1	bDescrAccessEn	User Conf.	00h: Device Descriptor access disabled (Default) 01h: Device Descriptor access enabled
0Ah	1	bInitPowerMode	User Conf.	00h: UFS-Sleep Mode 01h: Active Mode (Default)
0Bh	1	bHighPriorityLUN	User Conf.	00h-07h: Configured LUN has high priority 7Fh: All logical units have the same priority (Default)
0Ch	1	bSecureRemovalType	User Conf.	00h: Information removed by an erase of the physical memory (Default) 01h: Information removed by overwriting the addressed locations with a single character followed by an erase. 02h: Information removed by overwriting the addressed locations with a character, its complement, then a random character. 03h: Information removed using a vendor define mechanism.
0Dh	1	bSecurityLU	01h	01h: RPMB
0Eh	1	bBackgroundOpsTermLat	04h	bBackgroundOpsTermLat defines the maximum latency for the termination of ongoing background operations. The latency is expressed in units of 10ms.
0Fh	1	bInitActiveICCLevel	User Conf.	bInitActiveICCLevel defines the bActiveICCLevel value after power on or reset Valid range: 00h to 0Fh. (Default 00h)
10h	2	wSpecVersion	0310h	Specification version 3.1
12h	2	wManufactureDate	Device Specific	Manufacturing Date ex) 0121h = Jan. 2021

OFFSET	SIZE	NAME	VALUE	Description
14h	1	iManufacturerName	01h	Index to Manufacturer Name String
15h	1	iProductName	02h	Index to Product Name String
16h	1	iSerialNumber	03h	Index to Serial Number String
17h	1	iOemID	04h	Index to OEM ID String
18h	2	wManufacturerID	01ADh	Manufacturer ID
1Ah	1	bUD0BaseOffset	16h	Unit Descriptor 0 Base Offset
1Bh	1	bUDConfigPLength	1Ah	Unit Descr. Config. Param. Length Total size of the configurable Unit Descriptor parameters
1Ch	1	bDeviceRTTCap	02h	RTT Capability of device Maximum number of outstanding RTTs supported by device
1Dh	2	wPeriodicRTCUpdate	User Conf.	Frequency and method of Real-Time Clock update (Default 000h)
1Fh	1	bUFSFeatureSupport	B1h	UFS Features Support This field indicates which features are supported by the device. A feature is supported if the related bit is set to one. bit[0]: Field Firmware Update (FFU) bit[1]: Production State Awareness (PSA) bit[2]: Device Life Span bit[3]: Refresh Operation bit[4]: TOO_HIGH_TEMPERATURE bit[5]: TOO_LOW_TEMPERATURE bit[6]: Extended Temperature bit[7]: Host Performance Booster (HPB) Others: Reserved Bit 0 shall be set to one
20h	1	bFFUTimeout	03h	Field Firmware Update Timeout. The maximum time is expressed in units of seconds.
21h	1	bQueueDepth	20h	0: The device implements the per-LU queuing architecture.
22h	2	wDeviceVersion	Device Conf.	Device version 128GB: 4407h 256GB: 4507h 512GB: 4607h 1TB: 4707h
24h	1	bNumSecureWPArea	20h	Number of Secure Write Protect Areas
25h	4	dPSAMaxDataSize	00h	PSA Maximum Data Size
29h	1	bPSAStateTimeout	00h	PSA State Timeout
2Ah	1	iProductRevisionLevel	05h	Index to the string which contains the Product Revision Level
2Bh	5	Reserved		Reserved
30h	16	Reserved		Reserved for Unified Memory Extension standard

OFFSET	SIZE	NAME	VALUE	Description
40h	2	wHPBVersion	Device Conf.	HPB Specification Version Bit[15:8] = Major Version in BCD format Bit[07:4] = Minor Version in BCD format Bit[03:0] = Version suffix in BCD format ex) version 2.00 = 0200h
42h	1	bHPBControl	User Conf.	HPB Control Mode 00h: Host Control 01h: Device Control (Default)
4Fh	4	dExtendedUFSFeaturesSupport	1B1h	UFS Features Support This field indicates which features are supported by the device. A feature is supported if the related bit is set to one. bit[0]: Field Firmware Update (FFU) bit[1]: Production State Awareness (PSA) bit[2]: Device Life Span bit[3]: Refresh Operation bit[4]: TOO_HIGH_TEMPERATURE bit[5]: TOO_LOW_TEMPERATURE bit[6]: Extended Temperature bit[7]: Host Performance Booster (HPB) bit[8]: WriteBooster bit[9]: Performance Throttling Others: Reserved Bit 0 shall be set to one
53h	1	bWriteBoosterBufferPreserveUserSpcaeEn	User Conf.	Preserve User Space mode 00h: User space is reduced if WriteBooster Buffer is configured. The WriteBooster Buffer reduces the user space that can be configured at provisioning (default) 01h: User Space shall not be reduced if writebooster buffer is configured
54h	1	bWriteBoosterBufferType	User Conf.	WriteBooster Buffer Type 00: LU Dedicated Buffer Type (default) 01: Single Shared Buffer Type
55h	4	dNumSharedWriteBoosterBufferAllocUnits	User Conf.	The WriteBooster Buffer size for the shared WriteBooster Buffer Configuration. If this value is zero, then the shared WriteBooster is not configured for this device. (default 0)

8.2 Geometry Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	57h	Size of this Descriptor
01h	1	bDescriptorIDN	07h	Geometry Descriptor Type Identifier
02h	1	bMediaTechnology	00h	Reserved
03h	1	Resrved		Reserved
04h	8	qTotalRawDeviceCapacity	Device Conf.	Total Raw Device Capacity Total memory quantity available to the user to configure the device logical units (RPMB excluded). It is expressed in units of 512 Bytes. 128GB: 0EE64000h 256GB: 1DCBC000h 512GB: 3B96C000h 1TB : 772D8000h
0Ch	1	bMaxNumberLU	01h	32 Logical Units
0Dh	4	dSegmentSize	2000h	Segment Size It is expressed in units of 512 Bytes
11h	1	bAllocationUnitSize	01h	Allocation Unit Size Value expressed in number of Segments
12h	1	bMinAddrBlockSize	08h	Minimum addressable block size (4KB) Value expressed in unit of 512 Bytes
13h	1	bOptimalReadBlockSize	40h	Optimal read block size Value expressed in unit of 512 Bytes
14h	1	bOptimalWriteBlockSize	80h	Optimal write block size Value expressed in unit of 512 Bytes
15h	1	bMaxInBufferSize	40h	Max data-in buffer size (32KB) Value expressed in unit of 512 Bytes
16h	1	bMaxOutBufferSize	40h	Max data-out buffer size (32KB) Value expressed in unit of 512 Bytes
17h	1	bRPMB_ReadWriteSize	40h	Maximum number of RPMB frames (256 byte of data) allowed in Security Protocol In and Security Protocol Out.
18h	1	bDynamicCapacityResourcePolicy	00h	00h: Spare blocks resource management policy is per logical unit. The host should release amount of logical blocks from each logical unit as asked by the device.
19h	1	bDataOrdering	00h	00h: out-of-order data transfer is not supported by the device. 01h: out-of-order data transfer is supported by the device.
1Ah	1	bMaxContexIDNumber	0Fh	Maximum available number of contexts which are supported by the device.
1Bh	1	bSysDataTagUnitSize	00h	bSysDataUnitSize provides system data tag unit size, which can be calculated as in the following. (in bytes) Tag Unit Size = $2^{bSysDataTagUnitSize}$ x bMinAddrBlockSize x 512

OFFSET	SIZE	NAME	VALUE	Description
1Ch	1	bSysDataTagResSize	00h	This field is defined to inform the host about the maximum storage area size in bytes allocated by the device to handle system data by the tagging mechanism. System Data Tag Resource Size = $\text{Tag Unit Size} \times \text{floor}\left(\frac{\text{qTotalRawDeviceCapacity} \times 2^{\text{bSysDataTagResSize-1}}}{\text{Tag Unit Size}}\right)$ The range of valid bSysDataTagResSize values is from 0 to 6. Values in range of 7 to 0xFF are reserved. The formula covers a range from about 0.1% to 6.25% of the device capacity.
1Dh	1	bSupportedSecRTypes	09h	Supported Secure Removal Types Bit map which represents the supported Secure Removal types. Bit 0: Information removed by an erase of the physical memory Bit 1: Information removed by overwriting the addressed locations with a single character followed by an erase. Bit 2: Information removed by overwriting the addressed locations with a character, its complement, then a random character. Bit 3: Information removed using a vendor define mechanism. Others: Reserved A value of one means that the corresponding Secure Removal type is supported.
1Eh	2	wSupportedMemoryTypes	8079h	Bit 0: Normal memory type Bit 1: System code memory type Bit 2: Non-Persistent memory type Bit 3: Enhanced memory type 1 Bit 4: Enhanced memory type 2 Bit 5: Enhanced memory type 3 Bit 6: Enhanced memory type 4 Bit 15: RPMB memory type * SK hynix supports SLC type for all enhanced memory type. This device has no difference of each enhanced type.
20h	4	dSystemCodeMaxNAllocU	00h	System code memory type is not supported.
24h	2	wSystemCodeCapAdjFac	00h	System code memory type is not supported.
26h	4	dNonPersistMaxNAllocU	00h	Non-Persistent memory type is not supported.
2Ah	2	wNonPersistCapAdjFac	00h	Non-Persistent memory type is not supported.
2Ch	4	dEnhanced1MaxNAllocU	Device Conf.	Max Number of Allocation Units for the Enhanced memory type 1 128GB: 07732h 256GB: 0EE5Eh 512GB: 1DCB6h 1TB : 3B96Ch

OFFSET	SIZE	NAME	VALUE	Description
30h	2	wEnhanced1CapAdjFac	300h	Capacity Adjustment Factor for the Enhanced memory type 1 Factor used to adjust the memory capacity of this memory property from normal memory: Capacity Enhanced1 = CapacityNormalMem / CapAdjFac wEnhanced1CapAdjFac = INTEGER(256 × CapAdjFac)
32h	4	dEnhanced2MaxNAllocU	Device Conf	Max Number of Allocation Units for the Enhanced memory type 2 128GB: 07732h 256GB: 0EE5Eh 512GB: 1DCB6h 1TB : 3B96Ch
36h	2	wEnhanced2CapAdjFac	300h	Enhanced memory type 2 is supported.
38h	4	dEnhanced3MaxNAllocU	Device Conf	Max Number of Allocation Units for the Enhanced memory type 3 128GB: 07732h 256GB: 0EE5Eh 512GB: 1DCB6h 1TB : 3B96Ch
3Ch	2	wEnhanced3CapAdjFac	300h	Enhanced memory type 3 is supported.
3Eh	4	dEnhanced4MaxNAllocU	Device Conf	Max Number of Allocation Units for the Enhanced memory type 4 128GB: 07732h 256GB: 0EE5Eh 512GB: 1DCB6h 1TB : 3B96Ch
42h	2	wEnhanced4CapAdjFac	300h	Enhanced memory type 4 is supported.
44h	4	dOptimalLogicalBlockSize	03333003h	Optimal Logical Block Size Bit [3:0]: Normal memory type Bit [7:4]: System code memory type Bit [11:8]: Non-Persistent memory type Bit [15:12]: Enhanced memory type 1 Bit [19:16]: Enhanced memory type 2 Bit [23:20]: Enhanced memory type 3 Bit [27:24]: Enhanced memory type 4 Bit [31:28]: Reserved The optimal logical block size for each memory type can be calculated from the related dOptimalLogicalBlockSize field as indicated in the following: Optimal Logical Block Size = 2^ (dOptimalLogicalBlockSize field) x bMinAddrBlockSize x 512 byte

OFFSET	SIZE	NAME	VALUE	Description
48h	1	bHPBRegionSize	0Fh	HPB Region Size, which can be Calculated as in the following (in byte) HPB Region Size = 512B x 2^(bHPBRegionSize)
49h	1	bHPBNumberLU	20h	Maximum number of HPB LU supported by the device 00h: HPB is not supported by the device. 01h ~ 20h: Maximum number of HPB LU supported by the device Others : Reserved
4Ah	1	bHPBSubRegionSize	0Fh	HPB Sub-Region size, which can be calculated as in the following (in bytes) and shall be a multiple of Logical Block size HPB Sub-Region size = 512B x 2^bHPBSubRegion Size bHPBSubRegionSize shall not exceed bHPBRegionSize
4Bh	2	wDeviceMaxActiveHPBRegions	Device Conf.	Maximum number of Active HPB Regions that is supported by the device 128GB: 1DCDh 256GB: 3B98h 512GB: 4000h 1TB : 4000h
4Fh	4	dWriteBoosterBufferMaxNAllocUnits	Device Conf.	Maximum Total WriteBooster Buffer size which is supported by the entire device. The summation of the WriteBooster Buffer size for all LUs should be equal to or less than size value indicated by this descriptor 128GB: 1E00h 256GB: 3C00h 512GB: 7800h 1TB : F000h
53h	1	bDeviceMaxWriteBoosterLUs	02h	Number of maximum WriteBooster Buffer supported by the device Default 02h
54h	1	bWriteBoosterBufferCapAdjFac	03h	Capacity Adjustment Factor for the WriteBooster Buffer Memory Type This Value provides the LBA space reduction multiplication factor when WriteBooster Buffer is configured in user space reduction mode. Therefore, this parameter applies only if bWriteBoosterBuffer PreservedUserSpaceEn is 00h. 02h: MLC NAND 03h: TLC NAND
55h	1	bSupportedWriteBoosterBufferUserSpaceReductionTypes	01h	The supportability of user space reduction mode and preserve user space mode. 00h: WriteBooster Buffer can be configured only in user space reduction type 01h: WriteBooster Buffer can be configured only in preserve user space type (Default) 02h: Device can be configured in either user space reduction type or preserve user space type Others: Reserved
56h	1	bSupportedWriteBoosterBufferTypes	02h	The supportability of WriteBooster Buffer Type 00h: LU Based WriteBooster Buffer Configuration 01h: Single shared WriteBooster Buffer configuration 02h: Supporting both LU based WriteBooster Buffer and Single shared WriteBooster Buffer Configuration (Default) Others: Reserved

8.3 Unit Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	2Dh	Size of this Descriptor
01h	1	bDescriptorIDN	02h	UNIT Descriptor Type Identifier
02h	1	bUnitIndex	00h to 1Fh	Unit Index
03h	1	bLUEnable	User Conf.	Logical Unit Enable 00h: Logical Unit disabled (Default) 01h: Logical Unit enabled 02h: Logical Unit Enabled with HPB function Others: Reserved
04h	1	bBootLunID	User Conf.	Boot LUN ID 00h: Not bootable (Default) 01h: Boot LU A 02h: Boot LU B Others: Reserved
05h	1	bLUWriteProtect	User Conf.	Logical Unit Write Protect 00h: LU not write protected (Default) 01h: LU write protected when fPowerOnWPEn = 1 02h: LU permanently write protected when fPermanentWPEn = 1 Others: Reserved
06h	1	bLUQueueDepth	00h	Logical Unit Queue Depth Queue depth available in this LU. Queue depth of '0' means best effort by device to service the command task.
07h	1	bPSASensitive	00h	00h: LU is not sensitive to soldering. 01h: LU is sensitive to soldering. Others: Reserved
08h	1	bMemoryType	User Conf.	Memory Type bMemoryType defines logical unit memory type. 00h: Normal Memory (Default) 01h: System code memory type (Not supported) 02h: Non-Persistent memory type (Not supported) 03h: Enhanced memory type 1 04h: Enhanced memory type 2 05h: Enhanced memory type 3 06h: Enhanced memory type 4 Others: Reserved

OFFSET	SIZE	NAME	VALUE	Description
09h	1	bDataReliability	00h	Data Reliability bDataReliability defines the device behavior when a power failure occurs during a write operation to the logical unit 00h: the logical unit is not protected. Logical unit's entire data might be lost as a result of a power failure during a write operation (Default) 01h: logical unit is protected. Logical unit's data is protected against power failure. Others: Reserved
0Ah	1	bLogicalBlockSize	User Conf.	Logical Block Size (Default 0xC,4KB) The size of addressable logical blocks is equal the result of exponentiation with as base the number two and as exponent the bLogicalBlockSize value: $2^{bLogicalBlockSize}$(i.e., bLogicalBlockSize = 0Ch corresponds to 4 KByte Logical Block Size). Its minimum value is 0Ch, which corresponds to 4 Kbyte.
0Bh	8	qLogicalBlockCount	User Conf.	Logical Block Count (Default 00h) Total number of addressable Logical Blocks in the LU in Logical Block Size unit. qLogicalBlockCount can be configured setting the dNumAllocUnits parameter of the Configuration Descriptor.
13h	4	dEraseBlockSize	00h	Erase Block Size (4KB) in number of Logical Blocks. dEraseBlockSize value is updated automatically by the device after device configuration.
17h	1	bProvisioningType	User Conf.	Provisioning Type 00h: Thin Provisioning is disabled (default) 02h: Thin Provisioning is enabled and TPRZ = 0 03h: Thin Provisioning is enabled and TPRZ = 1 Others: Reserved
18h:1Fh	8	qPhyMemResourceCount	00h	Physical Memory Resource Count Total physical memory resource available in the logical unit. Value expressed in units of Logical Block Size.
20h	2	wContextCapabilities	User Conf.	Default 0000h Bit [3:0]: MaxContextID is the maximum amount of contexts that the LU supports simultaneously. The sum of all MaXContextID must not exceed bMaxContexIDNumber. Bit [6:4]: LARGE_UNIT_MAX_MULTIPLIER_M1 is the highest multiplier that can be configured for Large Unit contexts, minus one. Large Unit contexts may be configured to have a multiplier in the range: 1 ≤ multiplier ≤(LARGE_UNIT_MAX_MULTIPLIER_M1 + 1) This field is read only. Bit [15:7]: Reserved
22h	1	bLargeUnitGranularity_M1	00h	Large Unit is not supported.

OFFSET	SIZE	NAME	VALUE	Description
23h	2	wLUMaxActiveHPBRegions	User Conf.	Maximum Number of Active HPB Regions Maximum number of HPB Active Regions that is supported by the logical unit. Default value is 0000h
25h	2	wHPBPinnedRegionStartIdx	User Conf.	HPB Pinned Region Start Offset Default value is 0000h
27h	2	wNumHPBPinnedRegions	User Conf.	Number of HPB Pinned Regions Number of HPB pinned Regions assigned to the HPB logical unit. Value "0" means that there is no pinned Region for this LU.
29h	4	dLUNumWriteBoosterBufferAllocUnits	User Conf.	The WriteBooster Buffer size for the Logical Unit. If this value is '0', then the WriteBooster is not Supported for this LU

8.3.1 RPMB Unit Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	23h	Size of this Descriptor
01h	1	bDescriptorIDN	02h	RPMB Unit Descriptor Type Identifier
02h	1	bUnitIndex	C4h	Unit Index
03h	1	bLUEnable	01h	01h: Logical Unit enabled
04h	1	bBootLunID	00h	00h: Not bootable
05h	1	bLUWriteProtect	00h	00h: LU not write protected
06h	1	bLUQueueDepth	01h	Queue depth available in this LU.
07h	1	bPSASensitive	00h	
08h	1	bMemoryType	0Fh	0Fh: RPMB Memory Type
09h	1	bRPMBRegionEnable	01h	RPMB Region Enable Bit-0: Don't care. RPMB region 0 is always enabled independent of this bit value Bit-1: If set to 1, RPMB region 1 is enabled Bit-2: If set to 1, RPMB region 2 is enabled Bit-3: If set to 1, RPMB region 3 is enabled Bit-4 to Bit-7: Reserved
0Ah	1	bLogicalBlockSize	08h	The size of addressable logical blocks is equal the result of exponentiation with as base the number two and as exponent the bLogicalBlockSize value: $2^{bLogicalBlockSize}$ (i.e., bLogicalBlockSize = 08h corresponds to 256 Byte Logical Block Size)
0Bh	8	qLogicalBlockCount	00010000h	Total number of addressable Logical Blocks of the RPMB LU in Logical Block Size unit. For RPMB, Logical Block Count shall be a multiple of 512 (i.e., 128 KByte)
13h	1	bRPMBRegion0Size	80h	RPMB Region 0 Size RPMB Region 0 size is defined in 128KB unit (00h: 0KB, 01h: 128KB, ... , 80h: 16384KB) The MDV value multiplied by 512 shall match with the MDV value of LogicalBlockCount in the RPMB Unit Descriptor.
14h	1	bRPMBRegion1Size	00h	RPMB Region 1 Size RPMB Region 1 size is defined in 128KB unit (00h: 0KB, 01h: 128KB, ... , 80h: 16384KB)
15h	1	bRPMBRegion2Size	00h	RPMB Region 2 Size RPMB Region 2 size is defined in 128KB unit (00h: 0KB, 01h: 128KB, ... , 80h: 16384KB)
16h	1	bRPMBRegion3Size	00h	RPMB Region 3 Size RPMB Region 3 size is defined in 128KB unit (00h: 0KB, 01h: 128KB, ... , 80h: 16384KB)
17h	1	bProvisioningType	00h	00h: Thin Provisioning is disabled.
18h:1Fh	8	qPhyMemResourceCount	00010000h	Total physical memory resource available in the logical unit. Value expressed in units of bLogicalBlockSize.The dynamic device capacity feature does not apply to the RPMB well known logical unit. Therefore qPhyMemResourceCount value is always equal to qLogicalBlockCount value.
20h:22h	3	Reserved		Reserved

8.4 Power Parameters Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	62h	Size of this descriptor
01h	1	bDescriptorIDN	08h	Power Parameters Descriptor Type Identifier
02h	2	wActiveICCLevelsVCC(0)	8320h	2 byte maximum VCC current value for each of the 16 active current consumption levels starting with level 0
04h	2	wActiveICCLevelsVCC(1)		
06h	2	wActiveICCLevelsVCC(2)		
08h	2	wActiveICCLevelsVCC(3)		
0Ah	2	wActiveICCLevelsVCC(4)		
0Ch	2	wActiveICCLevelsVCC(5)		
0Eh	2	wActiveICCLevelsVCC(6)		
10h	2	wActiveICCLevelsVCC(7)		
12h	2	wActiveICCLevelsVCC(8)		
14h	2	wActiveICCLevelsVCC(9)		
16h	2	wActiveICCLevelsVCC(10)		
18h	2	wActiveICCLevelsVCC(11)		
1Ah	2	wActiveICCLevelsVCC(12)		
1Ch	2	wActiveICCLevelsVCC(13)		
1Eh	2	wActiveICCLevelsVCC(14)		
20h	2	wActiveICCLevelsVCC(15)		
22h	2	wActiveICCLevelsVCCQ(0)	8320h	2 byte maximum VCCQ current value for each of the 16 active current consumption levels starting with level 0
24h	2	wActiveICCLevelsVCCQ(1)		
26h	2	wActiveICCLevelsVCCQ(2)		
28h	2	wActiveICCLevelsVCCQ(3)		
2Ah	2	wActiveICCLevelsVCCQ(4)		
2Ch	2	wActiveICCLevelsVCCQ(5)		
2Eh	2	wActiveICCLevelsVCCQ(6)		
30h	2	wActiveICCLevelsVCCQ(7)		
32h	2	wActiveICCLevelsVCCQ(8)		
34h	2	wActiveICCLevelsVCCQ(9)		

OFFSET	SIZE	NAME	VALUE	Description
36h	2	wActiveICCLevelsVCCQ(10)	8320h	2 byte maximum VCCQ current value for each of the 16 active current consumption levels starting with level 0
38h	2	wActiveICCLevelsVCCQ(11)		
3Ah	2	wActiveICCLevelsVCCQ(12)		
3Ch	2	wActiveICCLevelsVCCQ(13)		
3Eh	2	wActiveICCLevelsVCCQ(14)		
40h	2	wActiveICCLevelsVCCQ(15)		
42h	2	wActiveICCLevelsVCCQ2(0)	00h	Not Used
44h	2	wActiveICCLevelsVCCQ2(1)		
46h	2	wActiveICCLevelsVCCQ2(2)		
48h	2	wActiveICCLevelsVCCQ2(3)		
4Ah	2	wActiveICCLevelsVCCQ2(4)		
4Ch	2	wActiveICCLevelsVCCQ2(5)		
4Eh	2	wActiveICCLevelsVCCQ2(6)		
50h	2	wActiveICCLevelsVCCQ2(7)		
52h	2	wActiveICCLevelsVCCQ2(8)		
54h	2	wActiveICCLevelsVCCQ2(9)		
56h	2	wActiveICCLevelsVCCQ2(10)		
58h	2	wActiveICCLevelsVCCQ2(11)		
5Ah	2	wActiveICCLevelsVCCQ2(12)		
5Ch	2	wActiveICCLevelsVCCQ2(13)		
5Eh	2	wActiveICCLevelsVCCQ2(14)		
60h	2	wActiveICCLevelsVCCQ2(15)		

8.5 Interconnect Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	06h	Size of this Descriptor
01h	1	bDescriptorIDN	04h	Interconnect Description Type Identifier
02h	2	bcdUniproVersion	0180h	MIPI UniPro version number in BCD format (i.e., version 1.8 = 0180h)
04h	2	bcdMphyVersion	0410h	MIPI M-PHY version number in BCD format (i.e., version 4.10 = 0410h)

8.6 Manufacturer Name String Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	12h	Size of this Descriptor
01h	1	bDescriptorIDN	05h	String Descriptor Type Identifier
02h	2	UC[0]	0053h	Unicode string character ("S")
04h	2	UC[1]	004Bh	Unicode string character ("K")
06h	2	UC[2]	0068h	Unicode string character ("h")
08h	2	UC[3]	0079h	Unicode string character ("y")
0Ah	2	UC[4]	006Eh	Unicode string character ("n")
0Ch	2	UC[5]	0069h	Unicode string character ("i”)
0Eh	2	UC[6]	0078h	Unicode string character ("x")
10h	2	UC[7]	0000h	NULL

8.7 Product Name String Descriptor

OFFSET	SIZE	NAME	128GB	256GB	512GB	1TB	Description
00h	1	bLength	22h	22h	22h	22h	Size of this Descriptor
01h	1	bDescriptorIDN	05h	05h	05h	05h	Type Identifier
02h	2	UC[0]	0048h	0048h	0048h	0048h	"H"
04h	2	UC[1]	004Eh	004Eh	004Eh	004Eh	"N"
06h	2	UC[2]	0038h	0038h	0038h	0038h	"8"
08h	2	UC[3]	0054h	0054h	0054h	0054h	"T"
0Ah	2	UC[4]	0030h	0031h	0032h	0033h	128GB: "0" 256GB: "1" 512GB: "2" 1TB : "3"
0Ch	2	UC[5]	0035h	0035h	0035h	0035h	"5"
0Eh	2	UC[6]	0044h	0044h	0044h	0044h	"D"
10h	2	UC[7]	0045h	0045h	0045h	005Ah	128GB: "E" 256GB: "E" 512GB: "E" 1TB : "Z"
12h	2	UC[8]	0048h	0048h	0048h	0048h	"H"
14h	2	UC[9]	004Bh	004Bh	004Bh	004Bh	"K"
16h	2	UC[10]	0058h	0058h	0058h	0058h	"X"
18h	2	UC[11]	0030h	0030h	0030h	0030h	"0"
1Ah	2	UC[12]	0037h	0037h	0037h	0037h	"7"
1Ch	2	UC[13]	0033h	0035h	0037h	0039h	128GB: "3" 256GB: "5" 512GB: "7" 1TB : "9"
1Eh	2	UC[14]	0000h	0000h	0000h	0000h	NULL
20h	2	UC[15]	0000h	0000h	0000h	0000h	NULL

8.8 OEM ID String Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	0Ah	Size of this Descriptor
01h	1	bDescriptorIDN	05h	String Description Type Identifier
02h	2	UC[0]	0030h	
04h	2	UC[1]	0031h	
06h	2	UC[2]	0041h	
08h	2	UC[3]	0044h	

8.9 Serial Number String Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	0Eh	Size of this Descriptor
01h	1	bDescriptorIDN	05h	String Descriptor Type Identifier
02h	2	UC[0]	-	Unique serial number hex code
04h	2	UC[1]	-	Unique serial number hex code
06h	2	UC[2]	-	Unique serial number hex code
08h	2	UC[3]	0000h	NULL
0Ah	2	UC[4]	0000h	NULL
0Ch	2	UC[5]	0000h	NULL

SK hynix supports 6 Bytes serial Number which is assigned by unique hex-code at each device. If some part of them (less than 6 bytes) are used, it couldn't be guaranteed uniqueness.

8.10 Product Revision Level String Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	0Ah	Size of this Descriptor
01h	1	bDescriptorIDN	05h	String Description Type Identifier
02h	2	UC[0]	0041h[1)]	"A"
04h	2	UC[1]	0030h[1)]	"0"
06h	2	UC[2]	0030h[1)]	"0"
08h	2	UC[3]	0031h[1)]	"1"

● NOTE 1 The value in product revision level string descriptor composed of the revision count of controller and the revision count of F/W patch. Above value is an example.

8.11 Device Health Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	2Dh	Size of this Descriptor
01h	1	bDescriptorIDN	09h	Device Health Descriptor Type Identifier
02h	1	bPreEOLInfo	Device Specific	Pre End of Life Information This field provides indication about device life time reflected by average reserved blocks. 00h: Not defined 01h: Normal 02h: Warning Consumed 80% of reserved blocks 03h: Critical Consumed 90% of reserved blocks Others: Reserved
03h	1	bDeviceLifeTimeEstA	Device Specific	This field provides an indication of the device life time based on the amount of performed program/erase cycles. The calculation method is vendor specific and referred as method A. 00h: information not available 01h: 0%~10% device life time used 02h: 10%~20% device life time used 03h: 20%~30% device life time used 04h: 30%~40% device life time used 05h: 40%~50% device life time used 06h: 50%~60% device life time used 07h: 60%~70% device life time used 08h: 70%~80% device life time used 09h: 80%~90% device life time used 0Ah: 90%~100% device life time used 0Bh: Exceeded its maximum estimated device life time Others: Reserved
04h	1	bDeviceLifeTimeEstB	Device Specific	This field provides an indication of the device life time based on the amount of performed program/erase cycles. The calculation method is vendor specific and referred as method B. 00h: Information not available 01h: 0%~10% device life time used 02h: 10%~20% device life time used 03h: 20%~30% device life time used 04h: 30%~40% device life time used 05h: 40%~50% device life time used 06h: 50%~60% device life time used 07h: 60%~70% device life time used 08h: 70%~80% device life time used 09h: 80%~90% device life time used 0Ah: 90%~100% device life time used 0Bh: Exceeded its maximum estimated device life time Others: Reserved

OFFSET	SIZE	NAME	VALUE	Description
05h	2	wFactoryBadBlockCount	Device Specific	Initial bad block count
07h	2	wRuntimeBadBlockCount	Device Specific	Run Time bad block count
09h	2	wMaxBlockEraseCount	Device Specific	Maximum NAND block erase count
0Bh	2	wMinBlockEraseCount	Device Specific	Minimum NAND block erase count
0Dh	2	wAveBlockEraseCount	Device Specific	Average NAND block erase count
0Fh	2	wReadReclaimCount	Device Specific	Count number of read reclaim operation
11h	4	dSPOCount	Device Specific	Count number of Sudden power off. If reach to 0xFFFFFFFF, it will not be increased further.
15h	4	dTotalWriteSize100M	Device Specific	Total write size, unit is 100MB
19h	4	dLVDCount	Device Specific	Low Voltage Detection of VCC, VCCQ power supply. Bit31~Bit16: LVD count of VCC(2.5V) Bit15~Bit0: LVD count of VCCQ(1.2V)
1Dh	2	wFFUCount	Device Specific	Success count of FFU to higher (not same) version firmware
1Fh	4	dTotalReadSize100M	Device Specific	Total read size, unit is 100MB
23h	1	bRemainReservedBlockCount	Device Specific	Count number of remain reserved block
24h	1	Reserved	-	-

OFFSET	SIZE	NAME	VALUE	Description
25h	4	dRefreshTotalCount	Device Specific	Total Refresh Count Indicate how many times the device complete refresh for the entire device. Incremented by 1 when dRefreshProgress reach 100000 (100.000%). - Not support feature
29h	4	dRefreshProgress	Device Specific	Refresh Progress Indicate the refresh progress in %. dRefreshProgress will indicate 0.000% ~ 100.000% in dec. dRefreshProgress = 100000 (dec) when it complete 100.000%. dRefreshProgress = 1000 (dec) when it complete 1.000%. When this value reach 100000 (100.000%) 1. Device stops refreshing even if it did not complete the number of units specified by bRefreshUnit 2. dRefreshProgress shall be reset to 0 3. dRefreshTotalCount shall be incremented by 1 When bRefreshMethod = 02h (Manual-Selective), even though some of physical blocks are not refreshed by device choice, dRefreshProgress should be incremented just as much as bRefreshUnit.

8.12 UFS Flags

IDN	NAME	TYPE	Default	Description
00h	Reserved			Reserved
01h	fDeviceInit	Read/ Set only	0	Device Initialization Host sets fDeviceInit flag to initiate device initialization after boot process is completed. Device resets flag when device initialization is completed. 0b: Device initialization completed or not started yet. 1b: Device initialization in progress.
02h	fPermanentWPEn	Read/ Write Once	0	Permanent Write Protection Enable fPermanentWPEn enables permanent write protection on all logical units configured as permanent protected; it cannot be toggled or cleared once it is set. 00h: Permanent write protection disabled. 01h: Permanent write protection enabled.
03h	fPowerOnWPEn	Read/ Power-on Reset	0	Power On Write Protection Enable fPowerOnWPEn enables the write protection on all logical units configured as power on write protected. If fPowerOnWPEn is equal to one and the device receives a Query Request to clear or toggle this flag, the Query Request shall fail and Response field shall be set to "F8h"(Parameter already written). The device shall set fPowerOnWPEn to zero in the event of power cycle or hardware reset. 0b: Power on write protection disabled. 1b: Power on write protection enabled.
04h	fBackgroundOpsEn	Read/ Volatile	1	Background Operations Enable 0b: Device is not permitted to run background operations. 1b: Device is permitted to run background operations.
05h	fDeviceLifeSpanModeEn	Read/ Volatile	0	Device Life Span Mode 0b: Device Life Span Mode is disabled. 1b: Device Life Span Mode is enabled.
06h	fPurgeEnable	Write Only/ Volatile	0	Purge Enable 0b: Purge operation is disabled. 1b: Purge operation is enabled. This flag shall only be set when the command queue of all logical units are empty and the bPurgeStatus is 00h (Idle). fPurgeEnable is automatically cleared by the UFS device when the operation completes or an error condition occurs. fPurgeEnable can be cleared by the host to interrupt an ongoing purge operation.
07h	fRefreshEnable	Write only/ Volatile	0	Refresh Enable 0b: Refresh operation is disabled. 1b: Refresh operation is enabled. This flag shall only be set when the command queue of all logical units are empty and the bRefreshStatus is 00h(idle) fRefreshEnable is automatically cleared by the UFS device when the operation completes or an error condition occurs. fRefreshEnable can be cleared by the host to interrupt an ongoing refresh operation.

IDN	NAME	TYPE	Default	Description
08h	fPhyResourceRemoval	Read/ Persistent	0	Physical Resource Removal The host sets this flag to one to indicate that the dynamic capacity operation shall commence upon device EndPointReset or hardware reset. The device shall reset this flag to zero after completion of dynamic capacity operation. The host cannot reset this flag.
09h	fBusyRTC	Read Only	0	Busy Real Time Clock 0b: Device is not executing internal operation related to RTC. 1b: Device is executing internal operation related to RTC. When this flag is set to one, it is recommended for the host to not send commands to the device.
0Ah	Reserved		0	Reserved
0Bh	fPermanentlyDisableFw Update	Read/ Write Once		Permanently Disable Firmware Update 0b: The UFS device firmware may be modified 1b: The UFS device shall permanently disallow future firmware updates to the UFS device
0Ch	Reserved	-	-	-
0Dh	Reserved	-	-	-
0Eh	fWriteBoosterEn	Read/ Volatile	0	writebooster Enable 0b: writebooster is not enabled 1b: writebooster is enabled
0Fh	fWriteBoosterBufferFlushEn	Read/ Volatile	0	Flush the data in writebooster Buffer to the user area of storage 0b: Flush operation is not performed 1b: Flush operation is performed
10h	fWriteBoosterBufferFlushDuringHibernate	Read/ Volatile	0	Flush writebooster Buffer during Hibernation state 0b: Device is not allowed to flush the writebooster buffer during Hibernation state of the device 1b: Device is allowed to flush the writebooster Buffer during Hibernation state of the device
11h	fHPBReset	Read / Set Only	0	HPB Reset Host set this flag as”1”to inform the device that host reset its HPB tables. After this flag is set all regions are inactive. Device reset flag as “0” when device inactivated all region information. 0b: HPB reset completed or not started yet 1b: HPB reset in progress
12h	fHPBEn	Read/ Persistent	0	HPB Enable 0h: HPB is not enabled 1h: HPB is enabled

8.13 UFS Attributes

IDN	NAME	TYPE	Size [Byte]	MDV	Description
00h	bBootLunEn	Read/ Persistent	1	00h	Boot LUN Enable 00h: Boot disabled 01h: Enabled boot from Boot LU A 02h: Enabled boot from Boot LU B All others: Reserved When bBootLunEn = 00h the boot feature is disabled, the device behaves as if bBootEnable would be equal to 0
01h	bMAX_DATA_SIZE_FOR_HPB_SINGLE_CMD	Read/ Read Only	1	Device Specific	Maximum HPB Data size for using single HPB command The size is calculated as (bMAX_DATA_SIZE_FOR_HPB_SINGLE_CMD + 1) * 4KB 00h: 4KB 01h: 8KB 02h: 12KB 03h: 16KB ... 07h: 32KB (Default) ... FEh: 1020KB FFh: 1024KB For example, if the value is 07h, only up to 32KB data should be issued with single HPB READ command, while bigger data is expected to be issued with HPB Read using HPB Read ID mode. If single HPB READ command is issued with bigger data size indicated by this attribute, the HPB READ command is handled as a normal READ command. If the HPB WRITE BUFFER command is issued with a small data size than indicated by this attribute, then the device can ignore the HPB entries delivered by the HPB WRITE BUFFER command, and respond with 'success' to indicated the command was received.
02h	bCurrentPowerMode	Read Only	1	11h	Current Power Mode 00h: Idle mode 10h: Pre-Active mode 11h: Active mode 20h: Pre-Sleep mode 22h: UFS-Sleep mode 30h: Pre-Power Down mode 33h: UFS-Power Down mode Others: Reserved

IDN	NAME	TYPE	Size [Byte]	MDV	Description
03h	bActiveICCLevel	Read/ Volatile	1	00h	bActiveICCLevel defines the maximum current consumption allowed during Active Mode. 00h: Lowest Active ICC level 0Fh: Highest Active ICC level Others: Reserved Valid range from 00h to 0Fh.
04h	bOutOfOrderDataEn	Read/ Write Once	1	00h	Out of Order Data transfer Enable 00h: Out-of-order data transfer is disabled. 01h: Out-of-order data transfer is enabled. Others: Reserved This bit shall have effect only when bDataOrdering = 01h.
05h	bBackgroundOpStatus	Read Only	1	00h	Background Operations Status Device health status for background operation 00h: Not required 01h: Required, not critical 02h: Required, performance impact 03h: Critical Others: Reserved
06h	bPurgeStatus	Read Only	1	00h	Purge Operation Status 00h: Idle (purge operation disabled) 01h: Purge operation in progress 02h: Purge operation stopped prematurely 03h: Purge operation completed successfully 04h: Purge operation failed due to logical unit queue not empty 05h: Purge operation general failure When the bPurgeStatus is equal to the values 02h, 03h, 04h or 05h, the bPurgeStatus is automatically cleared to 00h (Idle) the first time that it is read.
07h	bMaxDataInSize	Read/ Persistent	1	40h	Maximum Data In Size (32KB) Maximum data size in a DATA IN UPIU. Value expressed in number of 512 Byte units. bMaxDataInSize shall not exceed the bMaxInBufferSize parameter. bMaxDataInSize = bMaxInBufferSize when the UFS device is shipped.
08h	bMaxDataOutSize	Read/ Persistent	1	40h	Maximum Data-Out Size (32KB) Maximum data-size in a DATA-OUT UPIU. Value expressed in number of 512 Byte units. bMaxDataOutSize shall not exceed the bMaxOutBufferSize parameter. bMaxDataOutSize= bMaxOutBufferSize when the UFS device is shipped.

IDN	NAME	TYPE	Size [Byte]	MDV	Description
09h	dDynCapNeeded	Read Only	4	00h	Dynamic Capacity Needed The amount of physical memory needed to be removed from the physical memory resource pool of the particular logical unit, in units of bOptimalWriteBlockSize.
0Ah	bRefClkFreq	Read/ Persistent	1	01h	Reference Clock Frequency Value 0h:19.2MHz 1h: 26MHz 2h: 38.4MHz 3h: Obsolete Others: Reserved
0Bh	bConfigDescrLock	Read/ Write Once	1	00h	Configuration Descriptor Lock 0h: Configuration Descriptor not locked 1h: Configuration Descriptor locked Others: Reserved
0Ch	bMaxNumOfRTT	Read/ Persistent	1	02h	Maximum current number of outstanding RTTs in device that is allowed. bMaxNumOfRTT shall not exceed the bDeviceRTTCap parameter. This parameter can be written by the host only when all LU task queues are empty.
0Dh	wExceptionEventControl	Read/ Volatile	2	00h	Each bit, if set to '1' by the host, enables the assertion of the relevant exception event bit, allowing the device to raise the EVENT_ALERT bit in the Device Information field in the Response UPIU. Bit 0: DYNCAP_EVENT_EN Bit 1: SYSPOOL_EVENT_EN Bit 2: URGENT_BKOPS_EN Bit 3: TOO_HIGH_TEMP_EN Bit 4: TOO_LOW_TEMP_EN Bit 5: WRITEBOOSTER_FLUSH_NEEDED Bit 6: PERFORMANCE_THROTTLING 7-15: Reserved
0Eh	wExceptionEventStatus	Read Only	2	00h	Each bit represents an exception event. A bit will be set only if the relevant event has occurred (regardless of the wExceptionEventControl status). Bit 0: DYNCAP_NEEDED Bit 1: SYSPOOL_EXHAUSTED Bit 2: URGENT_BKOPS Bit 3: TOO_HIGH_TEMP Bit 4: TOO_LOW_TEMP Bit 5: WRITEBOOSTER_FLUSH_NEEDED Bit 6: PERFORMANCE_THROTTLING Bit 7-15: Reserved
0Fh	dSecondsPassed	Write Only/ Volatile	4	00h	Bit [31:0]: Seconds passed from TIME BASELINE (see wPeriodicRTCUpdate in Device Descriptor)

IDN	NAME	TYPE	Size [Byte]	MDV	Description
10h	wContextConf	Read/ Volatile	2	00h	INDEX specifies the LU number. SELECTOR specifies the Context ID within the LU. Valid range: 01h to 0Fh. Bit [15:8]: RFU Bit [7:6]: Reliability mode 00h: MODE0 (normal) 01h: MODE1 (non-Large Unit, reliable mode or Large Unit unit-by-unit mode) 02h: MODE2 (Large Unit, one-unit-tail mode) 03h: Reserved Bit [5:3]: Large Unit multiplier. If Large Unit context is set, this field defines the Large Unit size, else it is ignored Bit [2]: Large Unit context 00b: Context is not following Large Unit rules 01b: Context follows Large Unit rules Bit [1:0]: Activation and direction mode 00b: Context is closed and is no longer active. 01b: Context is configured and activated as a write-only context and according to the rest of the bits in this configuration register. 10b: Context is configured and activated as a read-only context and according to the rest of the bits in this configuration register. 11b: Context is configured and activated as a read/write context and according to the rest of the bits in this configuration register.
11h	Obsoleted	-	1	-	Obsoleted
12h	bHostActivateGCEn	Read/ Volatile	1	00h	Host Activate Garbage Collection Enable 00h: HOST_ACTIVATE_GC is OFF 01h: HOST_ACTIVATE_GC is ON When this attribute is set to one, device shall operate GC and bHostActivateGCEn is automatically cleared by the UFS device when the operation completes or a stop condition occurs. And Low Power mode is disabled.
13h	bHostActivateGCStatus	Read Only	1	00h	Host Activate Garbage Collection Status 00h: Not required 01h: HAGC is paused by Host Command 02h: Required / HAGC Operation Others: Reserved

IDN	NAME	TYPE	Size [Byte]	MDV	Description
14h	bDeviceFFUStatus	Read Only	1	00h	Device FFU Status 00h: No information 01h: Successful microcode update 02h: Microcode corruption error 03h: Internal error 04h: Microcode version mismatch 05h~FEh: Reserved 0FFh: General Error
15h	bPSAState	Read/ Persistent	1	00h	00h: 'Off'. PSA feature is off. 01h: 'Pre-soldering'. PSA feature is on, device is in the pre-soldering state. 02h: 'Loading Complete' PSA feature is on. The host will set to this value after the host finished writing data during pre-soldering state. 03h: 'Soldered'. PSA feature is no longer available. Set by the Device to indicate it is in post soldering state. This attributes unchangeable after it is in 'Soldered' state.
16h	dPSADataSize	Read/ Persistent	4	00h	The amount of data that the host plans to load to all logical units with bPSASensitive set to 1.
17h	bRefClkGatingWaitTime	Read Only	1	28h	Minimum time for which the reference clock is required by device during transition to LS-MODE or HIBERN8 state. The larger time requirement among the transition to LS-MODE and HIBERN8 states should be set for this attribute 00h: Undefined 01h: 1 micro second ... FFh: 255 micro second
18h	bDeviceCaseRoughTemperaure	Read Only	1	00h	Device's rough package case surface temperature. This value shall be valid when (TOO_HIGH_TEMPERATURE is supported and TOO_HIGH_TEMP_EN is enabled) or (TOO_LOW_TEMPERATURE is supported and TOO_LOW_TEMP_EN is enabled). 0 : Unknown Temperature 1~250 : (this value – 80) degrees in Celsius. (i.e -79 ºC ~ 170 ºC) Others: Reserved
19h	bDeviceTooHighTempBoundary	Read Only	1	A5h	High temperature boundary from which TOO_HIGH_TEMP in wExceptionEventStatus is turned on. 0 : Unknown 100~250: (this value – 80) degrees in celcius. (i.e 20 ºC ~ 170 ºC) Others: Reserved

IDN	NAME	TYPE	Size [Byte]	MDV	Description
1Ah	bDeviceTooLowTempBoundary	Read Only	1	37h	Low temperature boundary from which TOO_LOW_TEMP in wExceptionEventStatus is turned on. 0 : Unknown 1~80 : (this value – 80) degrees in celcius. (i.e -79 ºC ~ 0 ºC), Others: Reserved1Ch
1Bh	bThrottlingStatus	Read Only	1	00h	Each set bit represents an existing situation resulting in performance throttling Bit 0: Temperature, Others: reserved
1Ch	bWriteBoosterBufferFlushStatus	Read Only	1	00h	Flush Operation status of Writebooster Buffer 00h: IDLE. Device is not flushing the writebooster Buffer 01h: Flush Operation in progress 02h: Flush operation stopped prematurely by host's disabling flush enable flag or during hibernate flag 03h: Flush operation complete successfully 04h: Flush operation general failure others: reserved
1Dh	bAvailableWriteBoosterBufferSize	Read Only	1	00h	Available WriteBooster Buffer size this available buffer size is decreased by WriteBooster operation and increased by flush operation. Value expressed in units of 10% granularity 00h: 0% buffer remains 01h~09h: 10%~90% buffer remains 0Ah: 100% buffer remains Others: Reserved
1Eh	bWriteBoosterBufferLifeTimeEst	Read Only	1	00h	This field provides an indication of the writebooster Buffer lifetime based on the amount of performed program/erase cycle. In case of Preserve user space configuration for WriteBooster buffer, this lifetime will be reduced by writing on normal user level space, since Writebooster Buffer is shared with the user level space. 00h: Information not available, (writebooster Buffer is disabled) 01h: 0%~10% writebooster Buffer life time used 02h~09h 10%~90% writebooster Buffer life time used 0Ah: 90%~100% writebooster Buffer life time used 0Bh: Exceeded its maximum estimated WriteBooster Buffer life time Others: Reserved
1Fh	dCurrentWriteBoosterBufferSize	Read Only	4	00h	The current WriteBooster Buffer size. in the case of preserve user space mode, depending on available user space remained, the storage block for the writebooster Buffer may be used for the user space. Therefore, the Writebooster Buffer size can be less than initially configured WriteBooster Buffer size. Host can check the current WriteBooster Buffer size by checking this attribute. Value expressed in unit of Allocation Units. If this value is 0, then the current WriteBooster Buffer size is 0, in the csae of user space reduction mode, this value shall be same to the value of dLUNumWriteBoosterBufferAllocUnits or dNumSharedWiteBoosterBufferAllocUnits depending on buffer configuration mode

IDN	NAME	TYPE	Size [Byte]	MDV	Description
2Ch	bRefreshStatus	Read Only	1	00h	Refresh Operation Status 00h: Idle (refresh operation disabled) 01h: Refresh operation in progress 02h: Refresh operation stopped prematurely 03h: Refresh operation completed successfully 04h: Refresh operation failed due to logical unit queue not empty 05h: Refresh operation general failure. Others: Reserved When the bRefreshStatus is equal to the values 02h, 03h, 04h or 05h, the bRefreshStatus is automatically cleared to 00h (Idle) the first time that it is read.
2Dh	bRefreshFreq	Read/ Persistent	1	Device Specific	Refresh Frequency Host should make sure that dRefreshTotalCount will be incremented on this frequency. 00h: Not defined 01h: 1 month 02h: 2 month … FFh: 255 month
2Eh	bRefreshUnit	Read/ Persistent	1	Device Specific	Refresh Operation Unit This attribute may be set to adjust the minimum physical block numbers to be refreshed upon a single request (i.e. fRefreshEnable set to 1) 00h: Minimum refresh capability of Device 01h: 100.000% (i.e. entire device) Others: Reserved
2Fh	bRefreshMethod	Read/ Persistent	1	Device Specific	Refresh Method This parameter specifies the refresh operation method. 00h : Not defined 01h: Manual-Force The device is obliged to refresh the amount of physical blocks as requested by the host, regardless whether these blocks need refresh or not. The refresh command refreshes the amount of physical blocks given in bRefreshUnit. Refresh starts at the next physical block from where it stopped (or the first block if refresh was never triggered before). 02h: Manual-Selective The refresh command refreshes the amount of physical blocks given in bRefreshUnit. Refresh starts at the next physical block from where it stopped (or the first block if refresh was never triggered before). The device only refreshes the blocks that it considers to be in need of refresh. Regardless of the actually refreshed blocks, dRefreshProgress is increased by bRefreshUnit once the refresh command is completed. Others: Reserved

9. M-PHY & UniPro Attributes

9.1 M-TX Capability Attributes

MPHY capability attribute value in the table can be different from the value in the PACP_CAP_ind & PACP_CAP_EXT1_ind & PACP_CAP_EXT2_ind frame which is transmitted to the host during LinkStartUp. Some fields of PACP frame can be overwritten by FW.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	ESC_PA								EscParam_PA = PACP_BEGIN							
0	PACP_FunctionId = PACP_CAP_ind															
0	TSleepNoConfig					Reserved				Flags		MaxHS		MaxPWM		
0	TStallNoConfig								TSaveConfig							
0	VersionInfo															
0	Reserved															
0	Reserved															
0	Reserved															
0	CCITT CRC-16															

[Figure 9-1] PACP_CAP_ind

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	ESC_PA								EscParam_PA = PACP_BEGIN							
0	PACP_FunctionId = PACP_CAP_EXT1_ind															
0	THibern8								TMinActivate				Status			
0	TAdvHibern8								TAdvMinActivate				RxAdvGranularity			
0	MinRxTrailingClocks								RxPwmBurstClosureLength							
0	RxLsPrepareLength								RxPwmG6G7SyncLength							
0	RxHsG1PrepareLength								RxHsG1SyncLength							
0	RxHsG2PrepareLength								RxHsG2SyncLength							
0	RxHsG3PrepareLength								RxHsG3SyncLength							
0	Reserved															
0	Reserved															
0	CCITT CRC-16															

[Figure 9-2] PACP_CAP_EXT1_ind

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	ESC_PA								EscParam_PA = PACP_BEGIN							
0	PACP_FunctionID = PACP_CAP_EXT2_ind															
0	Reserved													MaxHS		
0	RxHsG4PrepareLength								RxHsG4SyncLength							
0	RxHsAdapRefresh								RxHsAdaptInitial							
0	Reserved															
0	Reserved															
0	Reserved															
0	Reserved															
0	Reserved															
0	Reserved															
0	Reserved															
0	Reserved															
0	Reserved															
0	Reserved															
0	CCITT CRC-16															

[Figure 9-3] PACP_CAP_EXT2_ind

Attributes Name	Attribute ID	Default value	Description
TX_HSMODE_Capability	0x01	01h	[0]: Specifies Support for HS-MODE. 0: False 1: True
TX_HSGEAR_Capability	0x02	04h	[2:0]: Specifies supported HS-GEARS 00 – Reserved 01 – HS-GEAR1 Only 10 – HS-GEAR1 to HS-GEAR2 11 – HS-GEAR1 to HS-GEAR3 100 – HS-GEAR1 to HS-GEAR4
TX_PWMG0_Capability	0x03	00h	PWM-G0 Capability [0]: Specifies Support for PWM-G0 0 – NO 1 – YES
TX_PWMGEAR_Capability	0x04	04h	[2:0]: Specifies supported PWM-GEARS other than PWM 000 – Reserved 001 – PWM-GEAR1 Only 010 – PWM-GEAR1 and PWM-GEAR2 011 – PWM-GEAR1 to PWM-GEAR3 100 – PWM-GEAR1 to PWM-GEAR4 101 – PWM-GEAR1 to PWM-GEAR5 110 – PWM-GEAR1 to PWM-GEAR6 111 – PWM-GEAR1 to PWM-GEAR7
TX_Amplitude_Capability	0x05	02h	[1:0]: Specifies supported signal amplitude levels 00 – Reserved 01 – SMALL AMPLITUDE Only 10 – LARGE AMPLITUDE Onlly 11 – LARGE and SMALL AMPLITUDE
TX_ExternalSYNC_Capability	0x06	00h	[0]: Specifies support for external SYNC pattern. 0 – FALSE 1 – TRUE
TX_HS_Unterminated_ LINE_Drive_Capability	0x07	00h	[0]: Specifies whether or not M-TX supports driving an unterminated LINE in HS-MODE. 0 – NO 1 – YES
TX_LS_Terminated_ LINE_Drive_Capability	0x08	00h	Specifies whether or not M-TX supports driving an Terminated LINE in LS-MODE. 0 – NO 1 – YES

Attributes Name	Attribute ID	Default value	Description
TX_Min_SLEEP_NoConfig_ Time_Capability	0x09	0Fh	[3:0]: Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed. Legal values are 0001 to 1111 (1 to 15)
TX_Min_STALL_NoConfig_Time _Capability	0x0A	FFh	[7:0]: Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed. Legal values are 8'h01 to 8'hFF (1 to 255)
TX_Min_SAVE_Config_ Time_Capability	0x0B	FAh	[7:0] Specifies minimum reconfiguration time (in 40ns steps). This applies to SLEEP and STALL states Legal values are 01h to FAh (1 to 250) which gives a Maximum time of 10000ns.
TX_REF_CLOCK_ SHARED_Capability	0x0C	01h	[0]: Specifies support for shared reference clock. 0 – NO 1 – YES
TX_PHY_MajorMinor_ Release_Capability	0x0D	41h	Specifies the major and minor numbers of the M-PHY Version supported by the TX portion of M-PHY Version [3:0]: Minor Version number. Fixed to 0x1 [7:4]: Major Version Number. Fixed to 0x4 The above values indicate that the M-PHY Version of the M-PHY Specification.
TX_PHY_Editorial_ Release_Capability	0x0E	01h	Specifies the sequence number of the M-Phy version [7:0]: This value is fixed to 0x01.
TX_Hibern8Time_ Capability	0x0F	01h	[7:0]: Specifies the minimum time (in 100 us steps) in HIBERN8 State. Legal values are 01h to 80h (1 to 128) which gives a range of 100us to 12.8ms.
TX_Advanced_ Granularity_Capability	0x10	00h	Support and degree of fine granularity steps for a reduced time in HIBERN8 state. If a finer granularity is specified, all coarser granularities shall be supported. [0]: supports fine granularity steps 0 – NO (100 µs step) 1 – YES [2:1]: step size 00 – 4 µs 01 – 8 µs 10 – 16 µs 11 – 32 µs

Attributes Name	Attribute ID	Default value	Description
TX_Advanced_ Hibern8time_Capability	0x11	01h	Specifies minimum time in HIBERN8 state when advanced granularity is supported in steps defined by TX_Advanced_Granularity_Capability. Existence depends on: TX_Advanced_Granularity_Capability [7:0] : 1 to 128
TX_HS_Equalizer_ Setting_Capability	0x12	03h	Support for transmit path de-emphasis for HS-MODE Existence depends on: TX_HSMODE_Capability [0] 0: De-emphasis of 3.5dB not supported, 1: De-emphasis of 3.5dB supported, [1] 0: De-emphasis of 6dB not supported, 1: De-emphasis of 6dB supported

9.2 M-RX Capability Attributes

Attributes Name	Attribute ID	Default value	PACP_CAP value	Description
RX_HSMODE_Capability	0x81	01h	01h	[0]: Specifies Support for HS-MODE. 0: False 1: True
RX_HSGEAR_Capability	0x82	04h	04h	[2:0]: Specifies supported HS-GEARS 00 – Reserved 01 – HS-GEAR1 Only 10 – HS-GEAR1 to HS-GEAR2 11 – HS-GEAR1 to HS-GEAR3 100 – HS-GEAR1 to HS-GEAR4
RX_PWMG0_Capability	0x83	00h	00h	[0]: Specifies Support for PWM-G0 0 – NO 1 – YES
RX_PWMGEAR_Capability	0x84	04h	04h	[2:0]: Specifies supported PWM-GEARS other than PWM-G0 000 – Reserved 001 – PWM-GEAR1 Only 010 – PWM-GEAR1 to PWM-GEAR2 011 – PWM-GEAR1 to PWM-GEAR3 100 – PWM-GEAR1 to PWM-GEAR4 101 – PWM-GEAR1 to PWM-GEAR5 110 – PWM-GEAR1 to PWM-GEAR6 111 – PWM-GEAR1 to PWM-GEAR7
RX_HS_Unterminated_Capability	0x85	00h	00h	[0]: Specifies support for disconnection of resistive termination in HS-MODE. 0 – NO 1 – YES
RX_LS_Terminated_Capability	0x86	00h	00h	[0]: Specifies support for enabling resistive termination in LSMode. 0 – NO 1 – YES
RX_Min_SLEEP_NoConfig_ Time_Capability	0x87	0Fh	0Fh	[3:0]: Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed. Legal values are 0x01 to 0x0F (1 to 15)

Attributes Name	Attribute ID	Default value	PACP_CAP value	Description
RX_Min_STALL_NoConfig_ Time_Capability	0x88	FFh	FFh	[7:0]: Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed. Legal values are 0x01 to 0xFF (1 to 255)
RX_Min_SAVE_Config_ Time_Capability	0x89	FAh	FAh	Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states. [7:0]: Specifies minimum reconfiguration time (in 40ns steps). This applies to SLEEP and STALL states Legal values are 01h to FAh (1 to 250) which gives a maximum time of 10000ns.
RX_REF_CLOCK_ SHARED_Capability	0x8A	01h	01h	[0]: Specifies support for shared reference clock 0 – NO 1 – YES
RX_HS_G1_SYNC_ LENGTH_Capability	0x8B	48h	4Ah	HSG1 Synchronization pattern length in SI [5:0]: Sync Length 1 to 15 for FINE 0 to 15 for COARSE [7:6]: SYNC Range 00: FINE 01: COARSE
RX_HS_G1_PREPARE_ LENGTH_Capability	0x8C	0Fh	0Fh	[3:0]: HS GEAR1 PREPARE Length Multiplier for M-RX (0 to 15)
RX_LS_PREPARE_LENGTH_ Capability	0x8D	0Ah	0Ah	[3:0]: PWM-Burst or SYS-Burst PREPARE Length Multiplier for M-RX (0 to 15)
RX_PWM_Burst_Closure_ Length_Capability	0x8E	1Fh	1Fh	Specifies minimum burst closure time (in SI) necessary to guarantee complete data processing inside M-RX
RX_Min_ActivateTime_ Capability	0x8F	01h	03h	[3:0]: Specifies minimum activate time needed in 100us steps (1 to 9)

Attributes Name	Attribute ID	Default value	PACP_CAP value	Description
RX_PHY_MajorMinor_ Release_Capability	0x90	41h	41h	Specifies the major and minor numbers of the M-PHY [3:0]: Minor Version Number. Fixed to 0x1 [7:4]: Major Version Number. Fixed to 0x4 Version of the M-PHY Specification.
RX_PHY_Editorial_ Release_Capability	0x91	01h	01h	Specifies the sequence number of the M-PHY version [7:0]: This value is fixed to 0x01.
RX_Hibern8Time_ Capability	0x92	01h	01h	[7:0]: Specifies the minimum time (in 100us steps) in HIBERN8 State. Legal values are 0x01 to 0x80 (1 to 128) which gives a range of 100us to 12.8ms. Even though RX_Hibern8Time_Capability is 0x1, it sends THibern8 in PACP_CAP_EXT1_ind
RX_PWM_G6_G7_SYNC_ LENGTH_Capability	0x93	00h	00h	Synchronization pattern length, in SI, for PWM-G6 and PWM-G7 in LS-MODE . Existence depends on: RX_PWMGEAR_Capability [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE Does not support PWMG6/G7
RX_HS_G2_SYNC_ LENGTH_Capability	0x94	48h	4Ah	High Speed GEAR 2 Synchronization pattern length in SI. Existence depends on: RX_HSGEAR_Capability [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE
RX_HS_G3_SYNC_ LENGTH_Capability	0x95	48h	4Fh	High Speed GEAR 3 Synchronization pattern length in SI. Existence depends on: RX_HSGEAR_Capability [5:0]: Sync Length 1 to 15 for FINE 0 to 15 for COARSE [7:6]: SYNC Range 00: FINE 01: COARSE
RX_HS_G2_PREPARE_ LENGTH_Capability	0x96	0Fh	0Fh	HS-G2 PREPARE length multiplier for M-RX. Existence depends on: RX_HSGEAR_Capability [3:0]: 0 to 15 [7:4]: Reserved

Attributes Name	Attribute ID	Default value	PACP_CAP value	Description
RX_HS_G3_PREPARE_ LENGTH_Capability	0x97	0Fh	0Fh	HS-G3 PREPARE length multiplier for M-RX. Existence depends on: RX_HSGEAR_Capability [3:0]: 0 to 15 [7:4]: Reserved
RX_Advanced_ Granularity_Capability	0x98	00h	00h	Support and degree of fine granularity steps for THIBERN8 and TACTIVATE. [0] Supports fine granularity steps 0 : No (100 µs step) 1 : Yes [2:1] Step size 00 : 4 µs 01 : 8 µs 10 : 16 µs 11 : 32 µs Even though RX_Advanced_Granularity_Capability is 0x1, it sends RxAdvGranularity in PACP_CAP_EXT1 _ind
RX_Advanced_ Hibern8Time_Capability	0x99	01h	01h	Specifies minimum time in HIBERN8 state when advanced granularity is supported in steps defined by RX_advanced_Granularity_Capability. Existence depends on: RX_Advanced_Granularity_Capability Range : 1 to 128 Even though RX_Advanced_Hibern8Time_Capability is 0x4, it sends TAdvHibern8 in PACP_CAP_EXT1_ind with 0x7
RX_Advanced_Min_ ActivateTime_Capability	0x9A	01h	01h	Specifies minimum activate time when advanced granularity is supported in steps defined by RX_Advanced_Granularity_Capability. Existence depends on: RX_Advanced_Granularity_Capability Range : 1 to 14 Even though RX_Advanced_Min_ActivateTime_Capability is 0x7, it sends TAdvMinActivate in PACP_CAP_EXT1_ind with 0x7

Attributes Name	Attribute ID	Default value	PACP_CAP value	Description
RX_HS_G4_SYNC_LENGTH_Capability	0x9B	48h	4Fh	High Speed GEAR 4 Synchronization pattern length in SI. *Existence depends on:* RX_HSGEAR_Capability [5:0]: Sync Length 1 to 15 for FINE 0 to 15 for COARSE [7:6]: SYNC Range 00: FINE 01: COARSE
RX_HS_G4_PREPARE_LENGTH_Capability	0x9C	0Fh	0Fh	HS-G4 PREPARE length multiplier for M-RX. *Existence depends on: RX_HSGEAR_Capability* [3:0]: 0 to 15 [7:4]: Reserved
RX_HS_Equalizer_Setting_Capability	0x9D	01h	01h	Support for receiver path channel equalization for HS-MODE. *Existence depends on: RX_HSMODE_Capability* B0 = 0: No equalization B0 = 1: Yes equalization
RX_HS_ADAPT_REFRESH_Capability	0x9E	91h	8Fh	REFRESH is used for RX adaptation refresh. High Speed adaptation pattern length of M-RX. *Existence depends on: RX_HS_Equalizer_Setting_Capability*
RX_HS_ADAPT_INITIAL_Capability	0x9F	91h	8Fh	INITIAL is used for initial RX adaptation. High Speed adaptation pattern length of M-RX. *Existence depends on: RX_HS_Equalizer_Setting_Capability* [6:0]: ADAPT_length 0 to 127 for FINE, 0 to 17 for COARSE [7]: ADAPT_type FINE=0, COARSE=1

9.3 M-TX Configuration Attributes

Attributes Name	Attribute ID	Default value	Description
TX_MODE	0x21	01h	[1:0]: M-TX operating mode. 01: LS_MODE 10: HS_MODE (default: LS_MODE)
TX_HSRATE_Series	0x22	01h	[1:0]: HS mode RATE series value of M-TX. 01: RATE-A 10: RATE-B (default: RATE-A)
TX_HSGEAR	0x23	01h	[1:0]: HS-GEAR value of M-TX. 01: HS-GEAR1 10: HS-GEAR2 11: HS-GEAR3 100: HS-GEAR4 (default: HS-GEAR1)
TX_PWMGEAR	0x24	01h	[2:0]: PWM-GEAR value of M-TX. 000: PWM-GEAR0 001: PWM-GEAR1 010: PWM-GEAR2 011: PWM-GEAR3 100: PWM-GEAR4 101: PWM-GEAR5 110: PWM-GEAR6 111: PWM-GEAR7 (default: PWM-GEAR1)
TX_Amplitude	0x25	02h	[0]: Controls the Drive Strength of the AFE Outputs on Transmit. 01: SMALL_AMPLITUDE 10: LARGE_AMPLITUDE (default: LARGE_AMPLITUDE) Other vendor specific MPHY attributes should be programmed to changed TX amplitude, Please contact SKH to change TX Amplitude.
TX_HS_SlewRate	0x26	00h	HS Slew Rate [7:0]: Controls the Slew Rate of M-TX. Does not support for this version. Instead of Slew Rate control, limited slew rate adopted for EMI reduction.
TX_SYNC_Source	0x27	00h	[0]: Source of Synchronization Pattern at M-TX. 0: INTERNAL_SYNC 1: EXTERNAL_SYNC

Attributes Name	Attribute ID	Default value	Description
TX_HS_SYNC_LENGTH	0x28	4Fh	HS mode Synchronization Pattern Length. [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE (default: COARSE, 15)
TX_HS_PREPARE_LENGTH	0x29	0Fh	[3:0]: HS PREPARE Length Multiplier for M-TX. (0 to 15) (default: 15)
TX_LS_PREPARE_LENGTH	0x2A	0Ah	[3:0]: PWM-Burst or SYS-Burst PREPARE Length Multiplier for M-TX. (0 to 15) (default: 10)
TX_HIBERN8_Control	0x2B	01h	[0]: M-TX HIBERN8 state control. 0: EXIT 1: ENTER Note: After LINE-RESET condition, the value is reset to EXIT state. (default: ENTER)
TX_LCC_Enable	0x2C	00h	[0]: Enables the Transmission of LCC at the end of Burst. 0: Disable 1: Read only [7:1]: Reserved (default: Disable)
TX_PWM_BURST_Closure_ Extension	0x2D	20h	[7:0]: BURST CLOSURE sequence duration in SI. (0 to 255) (default: 32)
TX_BYPASS_8B10B_Enable	0x2E	00h	[0]: Bypass 8b10b Encoding operation at M-TX. 0: FALSE 1: TRUE [7:1]: Reserved (default: FALSE)
TX_DRIVER_POLARITY	0x2F	00h	Output Driver Polarity [0]: Output Driver Polarity 0: NORMAL 1: INVERTED [7:1]: Reserved (default: NORMAL)
TX_HS_Unterminated_ LINE_Drive_Enable	0x30	00h	[0]: Enables/Disables the unterminated LINE in HS-MODE. 0: NO 1: YES [7:1]: Reserved (default: NO)

Attributes Name	Attribute ID	Default value	Description
TX_LS_Terminated_ LINE_Drive_Enable	0x31	00h	[0]: Enables/Disables the terminated LINE in LS-MODE. 0: NO 1: YES [7:1]: Reserved (default: NO)
TX_LCC_Sequencer	0x32	00h	LCC Sequencer bits [0]: LCC READ-CAPABILITY 0: Not Requested 1: Requested [1]: LCC READ-MFG-INFO 0: Not Requested 1: Requested [2]: LCC READ-VEND-INFO 0: Not Requested 1: Requested [6:3]: Reserved [7]: LCC WRITE-ATTRIBUTE 0: Not Requested 1: Requested (default: No READ or WRITE operation Requested)
TX_Min_ActivateTime	0x33	0Fh	[3:0]: Specifies minimum activate time needed in 100us steps (1 to 15) [7:4]: Reserved (default: 15)
TX_PWM_G6_G7_SYNC_ LENGTH	0x34	4Fh	PWM G6/G7 mode Synchronization Pattern Length. [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE (default: COARSE, 15) Does not support PWMG6/G7.
TX_Advanced_ Granularity_Step	0x35	00h	Support and degree of fine granularity steps for TACTIVATE Reset Value: 0 [0]: Supports advanced granularity 0: NO 1: YES [2:1] step size 00 = 4 µs 01 = 8 µs 10 = 16 µs 11 = 32 µs Others : Reserved

Attributes Name	Attribute ID	Default value	Description
TX_Advanced_Granularity	0x36	01h	Specifies minimum activate time when advanced granularity is supported in steps defined by TX_Advanced_Granularity_Step. [3:0]: 1 to 15 Others: Reserved Advanced granularity is not supported
TX_HS_Equalizer_Setting	0x37	00h	HS Transmit path de-emphasis value selection. Existence depends on: TX_HSMODE_Capability AND TX_HS_Equalizer_Setting_Capability Value depends on: TX_HS_Equalizer_Setting_Capability Required Values: Support for de-emphasis of 3.5 dB or 6 dB Reset Value: 0 for local RESET. LINE-RESET shall not reset the value of this attribute.
TX_MIN_SLEEP_NOCONFIG_TIME	0x38	0Fh	This amount of time(in SI) ensures remote MRX has transitioned to termination disable entering SLEEP. Set greater than or equal to remote RX_MIN_SLEEP_NOCONFIG_TIME_CAPABILITY. Default value is 0Fh, but this value is overwritten '00h' by FW.
TX_MIN_STALL_NOCONFIG_TIME	0x39	FFh	This amount of time(in SI) ensures remote MRX has transitioned to termination disable entering STALL. Set greater than or equal to remote RX_MIN_STALL_NOCONFIG_TIME_CAPABILITY.
TX_HS_ADAPT_LENGTH	0x3A	91h	High Speed adaptation pattern length of M-TX. *Existence depends on: TX_HSMODE_Capability* *Required Values: FINE, COARSE, 0 to 127* *Reset Values: COARSE, 17* [6:0]: ADAPT_length 0 to 127 for FINE 0 to 17 for COARSE [7]: ADAPT_type FINE = 0, COARSE = 1

9.4 M-RX Configuration Attributes

Attributes Name	Attribute ID	Default value	Description
RX_MODE	0xA1	01h	[1:0]: Operating mode. 01: LS_MODE 10: HS_MODE (default: LS_MODE)
RX_HSRATE_Series	0xA2	01h	[1:0]: HS mode rate series value. 01: RATE-A 10: RATE-B (default: RATE-A)
RX_HSGEAR	0xA3	01h	[1:0]: Current HS-Gear. 01: HS-GEAR1 10: HS-GEAR2 11: HS-GEAR3 (default: HS-GEAR1)
RX_PWMGEAR	0xA4	01h	[2:0]: Current PWM-GEAR. 000: PWM-GEAR0 001: PWM-GEAR1 010: PWM-GEAR2 011: PWM-GEAR3 100: PWM-GEAR4 101: PWM-GEAR5 110: PWM-GEAR6 111: PWM-GEAR7 (default: PWM-GEAR1)
RX_LS_Terminated_Enable	0xA5	00h	[0]: Enables/Disables the resistive termination of Receive in LS-MODE. 0: OFF 1: ON (default: OFF)
RX_HS_Unerminated_Enable	0xA6	00h	[0]: Enables/Disables the resistive termination of Receive in HS-MODE. 0: OFF 1: ON (default: OFF)
RX_Enter_HIBERN8	0xA7	01h	[0]: M-RX Entry to HIBERN8 State control. 0: NO 1: YES Note: After LINE-RESET condition, the value is reset to NO state. (default: YES)
RX_BYPASS_8B10B_Enable	0xA8	00h	[0]: Bypass 8b10b decoding at the M-RX. 0: FALSE 1: TRUE (default: FALSE)
RX_Termination_Force_Enable	0xA9	00h	Force connection of differential termination resistance, RDIF_RX, to enabled state, for RX S-Parameter test purposes. 0: NO 1: YES

Attributes Name	Attribute ID	Default value	Description
RX_ADAPT_Control	0xAA	01h	M-RX ADAPT sub-state control and ADAPT_type. *Req'd Values: ADAPT Control: ADAPT, SYNC* ADAPT Type: REFRESH, INITIAL *Reset Value:* INITIAL, SYNC [0]: ADAPT_control ADAPT = 0, SYNC = 1 [1]: ADAPT_type INITIAL = 0, REFRESH = 1
RX_RECEIVER_POLARITY	0xAB	00h	M-RX receiver polarity. *Req'd Values:* NORMAL, INVERTED *Reset Value:* NORMAL for local RESET. LINE-RESET shall not reset the value of this attribute. NORMAL = 0, INVERTED = 1

9.5 M-TX & M-RX Status Attributes

Attributes Name	Attribute ID	Default value	Description
TX_FSM_State	0x41	01h	[3:0]: Current State of M-TX 000: DISABLED 001: HIBERN8 010: SLEEP 011: STALL 100: LS-BUSRT 101: HS-BURST 110: LINE-CFG 111: LINE-RESET
RX_FSM_State	0xC1	01h	[3:0]: Current State of M-RX. 000: DISABLED 001: HIBERN8 010: SLEEP 011: STALL 100: LS-BUSRT 101: HS-BURST 110: LINE-CFG 111: LINE-RESET

9.6 UniPro L1.5 Attributes

Attributes Name	Attribute ID	Default value	Description
PA_PHY_Type	0x1500	01h	PHY Type
PA_AvailTxDataLanes	0x1520	02h	Available TX Data Lanes
PA_AvailRxDataLanes	0x1540	02h	Available RX Data Lanes
PA_MinRxTrailingClocks	0x1543	84h	Minimum number of PHY byte clock cycles without data to receive before a mode change from FAST_STATE or SLOW_STATE to SLEEP_STATE, or before a pause in data transmission while in FAST_STATE or SLOW_STATE.
PA_TxHsG1SyncLength	0x1552	4Fh	Start of Burst: High Speed Synchronization pattern Length in HS-G1, follows [MIPI02] Spec definition for TX_HS_SYNC_LENGTH
PA_TxHsG1PrepareLength	0x1553	0Fh	Start of Burst: Minimum Prepare time in HS-G1, follows [MIPI02] Spec definition for TX_HS_PREPARE_LENGTH
PA_TxHsG2SyncLength	0x1554	4Fh	Start of Burst: High Speed Synchronization pattern Length in HS-G2, follows [MIPI02] Spec definition for TX_HS_SYNC_LENGTH
PA_TxHsG2PrepareLength	0x1555	0Fh	Start of Burst: Minimum Prepare time in HS-G2, follows [MIPI02] Spec definition for TX_HS_PREPARE_LENGTH
PA_TxHsG3SyncLength	0x1556	4Fh	Start of Burst: High Speed Synchronization pattern Length in HS-G3, follows [MIPI02] Spec definition for TX_HS_SYNC_LENGTH
PA_TxHsG3PrepareLength	0x1557	0Fh	Start of Burst: Minimum Prepare time in HS-G3, follows [MIPI02] Spec definition for TX_HS_PREPARE_LENGTH
PA_TxMk2Extension	0x155A	00h	Peer supports MK2 signaling (inbound direction)
PA_PeerScrambling	0x155B	00h	Peer supports scrambling
PA_TxSkip	0x155C	00h	Peer indicates requirement for skip symbol insertion (Set during link startup)
PA_TxSkipPeriod	0x155D	FAh	A skip symbol <MK4,MK4> shall be inserted at least every interval with a number of PA_PDUs equal to PA_TxSkipPeriod. The value 250 should correspond to +/-2000ppm difference between local and remote.
PA_LocalTxLccEnable	0x155E	00h	Local MPHY Line Configuration Enable.
PA_PeerTxLccEnable	0x155F	00h	Peer M-PHY Line Configuration Enable, updated on reception of PACP_CAP_EXT1_ind frame.

Attributes Name	Attribute ID	Default value	Description
PA_ActiveTxDataLanes	0x1560	01h	Active TX Data Lanes
PA_ConnectedTxDataLanes	0x1561	00h	Number of TX Data Lanes connected
PA_TxTrailingClocks	0x1564	FFh	Number of PHY byte clock cycles forced without data before a mode change from FAST_STATE or SLOW_STATE to SLEEP_STATE.
PA_TxPWRStatus	0x1567	03h	TX power state status 000 : Off state 001 : Fast state 010 : Slow state 011 : Hibernate state 100 : Sleep state
PA_TxGear	0x1568	01h	TX Gear in PWM or HS Mode 001 : PWM_G1 or HS_G1 010 : PWM_G2 or HS_G2 011 : PWM_G3 or HS_G3 100 : PWM_G4 101 : PWM_G5 110 : PWM_G6 111 : PWM_G7
PA_TxTermination	0x1569	00h	FALSE - 0 TRUE - 1
PA_HSSeries	0x156A	01h	TX and RX Frequency Series in High Speed Mode A-1 B-2
PA_PWRMode	0x1571	55h	TX/RX power mode TX[b3:b0] RX[b7:b4] 0000 : Off mode 0001 : Fast mode 0010 : Slow mode 0100 : Fast auto mode 0101 : Slow auto mode 1111 : UNCHANGED.

Attributes Name	Attribute ID	Default value	Description
PA_ActiveRxDataLanes	0x1580	01h	Active RX Data Lanes 1 - one lane active 2 - two lanes active 3 - three lanes active 4 - four lanes active
PA_ConnectedRxDataLanes	0x1581	00h	Number of RX Data Lanes connected 0 - not connected 1 - 1 lane 2 - 2 lanes 3 - 3 lanes 4 - 4 lanes Updated at linkstartup
PA_RxPWRStatus	0x1582	03h	RX power state status 000 : Off state 001 : Fast state 010 : Slow state 011 : Hibernate state 100 : Sleep state
PA_RxGear	0x1583	01h	RX Gear in PWM or HS Mode 001 : PWM_G1 or HS_G1 010 : PWM_G2 or HS_G2 011 : PWM_G3 or HS_G3 100 : PWM_G4 101 : PWM_G5 110 : PWM_G6 111 : PWM_G7
PA_RxTermination	0x1584	00h	RX Termination
PA_Scrambling	0x1585	00h	Scrambling Request.
PA_MaxRxPWMGear	0x1586	01h	Maximum RX Low Speed Gears (PWM) 001 : PWM_G1 010 : PWM_G2 011 : PWM_G3 100 : PWM_G4 101 : PWM_G5 110 : PWM_G6 111 : PWM_G7
PA_MaxRxHSGear	0x1587	00h	Maximum RX High Speed Gears (HS), 0 means no HS available 00 : NO_HS 01 : HS_G1 10 : HS_G2 11 : HS_G3 100 : HS_G4

Attributes Name	Attribute ID	Default value	Description
PA_PACPReqTimeout	0x1590	3Fh	Expiration value of the PACP_REQUEST_TIMER when the PA Layer is waiting for a cnf Message The actual duration of the timeout period shall be the value set in the Attribute ±10%
PA_PACPReqEoBTimeout	0x1591	0Fh	Expiration value of the PACP_REQUEST_TIMER when the PA Layer is waiting for the end of burst. The actual duration of the timeout period shall be the value set in the Attribute ±10%
PA_RemoteVerInfo	0x15A0	00h	Peer Device version information. Available after a successful Link StartUp Sequence.
PA_LogicalLaneMap	0x15A1	00h	Logical to Physical Lane mapping. Shall be updated after LinkStartUp
PA_SleepNoConfigTime	0x15A2	0Fh	Minimum time to wait between bursts in PWM mode when no new configuration was performed.
PA_StallNoConfigTime	0x15A3	FFh	Minimum time to wait between bursts in HS mode when no new configuration was performed.
PA_SaveConfigTime	0x15A4	FAh	Minimum time to wait between bursts when a new Configuration was performed.
PA_ RxHSUnterminationCapability	0x15A5	00h	Specifies whether or not the inbound Link supports unterminated line in HS mode 0 - FALSE 1 - TRUE

Attributes Name	Attribute ID	Default value	Description
PA_ RxLSTerminationCapability	0x15A6	00h	Specifies whether or not the inbound Link supports terminated line in PWM mode.
PA_Hibern8Time	0x15A7	80h	Minimum time to wait in HIBERN8 before allowing a M-TX to exit HIBERN8.
PA_TActivate	0x15A8	10h	Time to wait in SAVE before activating a burst in order to wake up OMC and remote M-RX.
PA_LocalVerInfo	0x15A9	05h	Local version info. Delivered during Link Startup Sequence to the peer Device and stored in PA_RemoteVerInfo in the peer Device.
PA_Granularity	0x15AA	06h	Granularity for PA_TActivate and PA_Hibern8Time
PA_MK2ExtensionGuardBand	0x15AB	00h	MK2 extension time. The unit is PA_Granularity.
PA_PWRModeUserData [0 to 11]	0x15B0 to 0x15BB	00h	Data to be sent within PACP_PWR_req and delivered to the remote DME.
PA_PACPFrameCount	0x15C0	00h	Number of valid PACP frames received.
PA_PACPErrorCount	0x15C1	00h	Number of erroneous PACP frames received.
PA_PHYTestControl	0x15C2	00h	PHY Test Feature control register. b0: ContBurst b1: CfgReady b2: LineReset b3: TestPattern Transmit b4: TestPattern Select

Attributes Name	Attribute ID	Default value	Description
PA_TxHsG4SyncLength	0x15D0	4Fh	Start of Burst: High Speed Synchronization pattern Length in HS-G4. Follows [MIPI02] definition for TX_HS_SYNC_LENGTH
PA_TxHsG4PrepareLength	0x15D1	0Fh	Start of Burst: Minimum Prepare time in HS-G4. Follows [MIPI02] definition for TX_HS_PREPARE_LENGTH
PA_PeerRxHsAdaptRefresh	0x15D2	00h	Start of Burst: High Speed adaption pattern Length Follows [MIPI02] definition for TX_HS_ADAPT_LENGTH when M-PHY is configured for ADAPT state.
PA_PeerRxHsAdaptInitial	0x15D3	00h	Start of Burst: High Speed adaption pattern Length Follows [MIPI02] definition for TX_HS_ADAPT_LENGTH when M-PHY is configured for ADAPT state.
PA_TxHsAdaptType	0x15D4	03h	Adapt Type selector 00 = REFRESH 01 = INITIAL 10 = Reserved 11 = No ADAPT
PA_AdaptAfterLRSTInPA_INIT	0x15D5	02h	Adapt Type selector This value is used in PACP_PWR_req which is transmitted in SlowAuto_Mode as part of PA_INIT 00 = REFRESH 01 = INITIAL 10 = Previous ADAPT value 11 = No ADAPT

9.7 UniPro L2 Attributes

Attributes Name	Attribute ID	Default value	Description
DL_TxPreemptionCap	0x2000	01h	Preemption capability on transmit side for both Traffic Classes.
DL_TC0TxMaxSDUSize	0x2001	90h	TC0 Transmitter Maximum SDU Size
DL_TC0RxInitCreditVal	0x2002	7Ch	TC0 Receiver Initial Credit Value (initial register A value)
DL_TC1TxMaxSDUSize	0x2003	90h	TC1 Transmitter Maximum SDU Size
DL_TC1RxInitCreditVal	0x2004	00h	TC1 Receiver Initial Credit Value (initial register A value)
DL_TC0TxBufferSize	0x2005	76h	TC0 Transmitter Buffer Size
DL_TC1TxBufferSize	0x2006	00h	TC1 Transmitter Buffer Size
DL_TC0TXFCThreshold	0x2040	09h	Threshold for triggering an AFC0 Frame with CReq bit set to '1' to request flow control update from remote end. This Attribute is retained during hibernate.
DL_FC0ProtectionTimeOutVal	0x2041	1FFFh	Expiration value of the FC0_PROTECTION_TIMER The actual duration of the timeout period shall be the value set in the Attribute ±10%. A value of zero means "OFF" This Attribute is retained during hibernate.
DL_TC0ReplayTimeOutVal	0x2042	FFFFh	Expiration value of the TC0_REPLAY_TIMER The actual duration of the timeout period shall be the value set in the Attribute ±10%. A value of zero means "OFF" This Attribute is retained during hibernate.
DL_AFC0ReqTimeOutVal	0x2043	7FFFh	Expiration value of the AFC0_REQUEST_TIMER The actual duration of the timeout period shall be the value set in the Attribute ±10%. A value of zero means "OFF" This Attribute is retained during hibernate.
DL_AFC0CreditThreshold	0x2044	00h	Threshold for AFC0 triggering based on available TC0 credits at receiver. This Attribute is retained during hibernate.
DL_TC0OutAckThreshold	0x2045	00h	Number of outstanding acknowledgments for TC0
DL_PeerTC0Present	0x2046	00h	Peer Device supports TC0
DL_PeerTC0RxInitCreditVal	0x2047	00h	Peer TC0 Receiver Initial Credit Value (initial register A value)
DL_PeerTC1Present	0x2066	00h	Peer Device supports TC1
DL_PeerTC1RxInitCreditVal	0x2067	00h	Peer TC1 Receiver Initial Credit Value (initial register A value)

9.8 UniPro L3 Attributes

Attributes Name	Attribute ID	Default value	Description
N_DeviceID	0x3000	01h	Local Device ID
N_DevieID_valid	0x3001	01h	N_Device ID attribute is valid. 1 - True 0 - False
N_TC0TxMaxSDUSize	0x3020	0111h	Maximum Transmit payload size per packet for TC0
N_TC1TxMaxSDUSize	0x3021	0111h	Maximum Transmit payload size per packet for TC1

9.9 UniPro L4 Attributes

Attributes Name	Attribute ID	Default value	Description
T_NumCports	0x4000	01h	No. of available cports
T_NumTestFeatures	0x4001	01h	No. of available Test Feature instances
T_ConnectionState	0x4020	01h	State of the connection
T_PeerDeviceID	0x4021	00h	Device id of the peer cport
T_PeerCportID	0x4022	00h	CPortID of the peer cport
T_TrafficClass	0x4023	00h	Traffic Class of current connection
T_CPortFlags	0x4025	06h	E2E_FC off, CSD off, CSV off
T_TxTokenValue	0x4026	20h	Value of E2E FC Token transmitted
T_RxTokenValue	0x4027	20h	Value of E2E FC Token received
T_LocalBufferSpace	0x4028	00h	Amount of local buffer space
T_PeerBufferSpace	0x4029	00h	Conservative value of amount of buffer space at the peer cport
T_CreditsToSend	0x402A	00h	Amount of space in the local buffer that has not been communicated to remote destination port yet
T_CportMode	0x402B	01h	Cport mode .. 1 - Application 2 - Test mode
T_TC0TxMaxSDUSize	0x4060	0110h	Maximum Transmit payload size per segment for TC0

9.10 UniPro DME DDB L1 Attributes

Attributes Name	Attribute ID	Default value	Description
DME_DDBL1_Revision	0x5000	10h	The revision of the DDB Specification supported by this Device encoded as major-version * 0x10 + minor-version. The value shall be 0x10. (DDB v1.0).
DME_DDBL1_Level	0x5001	01h	Eight bit field indicating the DDB support: b0: DDB Level 1 support. Shall be 0b1. b1: DDB Level 2 get support. Shall be 0b1 if, and only if, the GET-DDB-LEVEL2 Service is supported. If b1 is set to '1', then b0 shall also be set to '1'. b2: DDB Level 2 set support. Shall be 0b1 if, and only if, the SET-DDB-LEVEL2 Service is supported. If b2 is set to '1', both b0 and b1 shall also be set to '1'. b[7:3]: Reserved. Shall be 0b00000.
DME_DDBL1_DeviceClass	0x5002	02h	The Device Class ID of the DME User as specified by the MIPI Alliance. If the Device does not conform to a specified device class, the value shall be zero
DME_DDBL1_ManufacturerID	0x5003	024Ah	Manufacturer ID of the DME User as specified by the MIPI Alliance.
DME_DDBL1_ProductID	0x5004	0A00h	The Manufacturer's internal product ID of the DME User.
DME_DDBL1_Length	0x5005	00h	The length of any DDB Level 2 data. For Devices supporting only DDB Level 1, the value shall be zero.

9.11 UniPro TstSrc/TstDst Attributes

Attributes Name	Attribute ID	Default value	Description
T_TstCPortID	0x4080	00h	The ID of the CPort-under-test
T_TstSrcOn	0x4081	00h	Message generation state
T_TstSrcPattern	0x4082	00h	Pattern used for Message generation
T_TstSrcIncrement	0x4083	01h	The increment value between two consecutive bytes
T_TstSrcMessageSize	0x4084	0100h	The size of each generated Message
T_TstSrcMessageCount	0x4085	0100h	The number of Messages generated (Nonzero: finite Message stream, zero: infinite Message stream).
T_TstSrcInterMessageGap	0x4086	00h	If non-zero, the gap time between two Messages The actual duration of the timeout period shall be the value set in the attribute ±10%. This value multiplied by SYS1CLK 1us Register (0x0FC) gives the no. of clocks Required
T_TstDstOn	0x40A1	00h	The state of TstDst
T_TstDstErrorDetectionEnable	0x40A2	00h	Enable analyzing incoming Messages
T_TstDstPattern	0x40A3	00h	The expected pattern in the incoming Messages
T_TstDstIncrement	0x40A4	01h	The expected increment value between two consecutive bytes
T_TstDstMessageCount	0x40A5	00h	Number of received Messages
T_TstDstMessageOffset	0x40A6	00h	Offset of error from start of Message
T_TstDstMessageSize	0x40A7	0100h	The expected size of incoming Message
T_TstDstFCCredits	0x40A8	0100h	The amount of credits passed to the flow control Service Primitive
T_TstDstInterFCTokenGap	0x40A9	00h	The interval in microseconds for which requesting T_CO_FLOWCONTROL. req is skipped. The actual duration of the timeout period shall be the value set in the attribute ±10%. This value multiplied bySYS1CLK 1us Register(0x0FC) gives the no. of clocks required
T_TstDstInitialFCCredits	0x40AA	0100h	The initial number of credits passed by the TstDst to T_CO_FLOWCONTROL.req after enabling the TstDst
T_TstDstErrorCode	0x40AB	00h	Error code that generated the TstDst disconnection 0 - NO_ERROR 1 - FRAGMENT_CORRUPT 2 - INVALID_MSG_SIZE 3 - UNEXPECTED_BYTE_VALUE